11AA02E48/11AA02E64

2K UNI/O® Serial EEPROMs with EUI-48™ or EUI-64™ Node Identity

DEVICE SELECTION TABLE

Part Number	Density (bits)	Vcc Range	Page Size (Bytes)	Temp. Ranges	Packages	Node Address
11AA02E48	2K	1.8-5.5V	16	I	SN, TT	EUI-48™
11AA02E64	2K	1.8-5.5V	16	I	SN, TT	EUI-64™

Features:

- Pre-programmed Globally Unique, 48-bit or 64-bit Node Address
- Compatible with EUI-48™ and EUI-64™
- Single I/O, UNI/O® Serial Interface Bus
- Low-Power CMOS Technology
  - 1 mA active current, typical
  - 1 µA standby current (max.)
- 256 x 8 Bit Organization
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kbps Max. Bit Rate – Equivalent to 100 kHz Clock Frequency
- Self-Timed Write Cycle (including Auto-Erase)
- Page-Write Buffer for up to 16 Bytes
- STATUS Register for Added Control:
  - Write enable latch bit
  - Write-In-Progress bit
- Block Write Protection
  - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection
  - Power-on/off data protection circuitry
  - Write enable latch
- High Reliability
  - Endurance: 1,000,000 erase/write cycles
  - Data retention: > 200 years
  - ESD protection: > 4,000V
- 3-lead SOT-23 and 8-lead SOIC Packages
- Pb-Free and RoHS Compliant
- Available Temperature Ranges:
  - Industrial (I): -40°C to +85°C

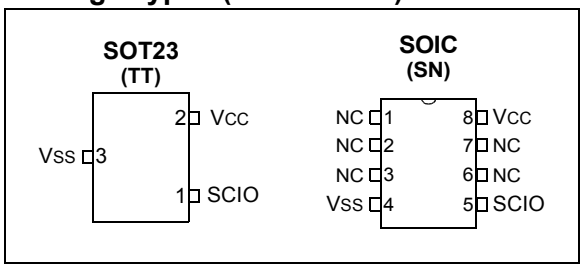
Description:

The Microchip Technology Inc. 11AA02E48/11AA02E64 (11AA02EXX*) device is a 2 Kbit Serial Electrically Erasable PROM. The device is organized in blocks of x8-bit memory and support the patented** single I/O UNI/O® serial bus. By using Manchester encoding techniques, the clock and data are combined into a single, serial bit stream (SCIO), where the clock signal is extracted by the receiver to correctly decode the timing and value of each bit.

Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1 uA and 1 mA, respectively.

The 11AA02EXX is available in standard 8-lead SOIC and 3-lead SOT-23 packages.

Package Types (not to scale)



Pin Function Table

Name	Function
SCIO	Serial Clock, Data Input/Output
VSS	Ground
VCC	Supply Voltage

* 11AA02EXX is used in this document as a generic part number for the 11AA02E48 and 11AA02E64 devices.

** Microchip's UNI/O® Bus products are covered by the following patents issued in the U.S.A.: 7,376,020 and 7,788,430.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

SCIO w.r.t. VSS..... -0.6V to VCC+1.0V

Storage temperature .....-65°C to 150°C

Ambient temperature under bias.....-40°C to 85°C

ESD protection on all pins.....4 kV

† NOTICE**:** Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Electrical Characteristics:** Industrial (I): VCC = 2.5V to 5.5V TA = -40°C to +85°C VCC = 1.8V to 2.5V TA = -20°C to +85°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D1	VIH	High-level Input Voltage	0.7*VCC	VCC+1	V	
D2	VIL	Low-level Input Voltage	-0.3 -0.3	0.3*VCC 0.2*VCC	V V	VCC ≥ 2.5V VCC < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger inputs (SCIO)	0.05*Vcc	—	V	VCC ≥ 2.5V (**Note 1**)
D4	VOH	High-level Output Voltage	VCC -0.5 VCC -0.5	— —	V V	IOH = -300 µA, VCC = 5.5V IOH = -200 µA, Vcc = 2.5V
D5	VOL	Low-level Output Voltage	— —	0.4 0.4	V V	IoI = 300 µA, VCC = 5.5V IoI = 200 µA, Vcc = 2.5V
D6	IO	Output Current Limit (**Note 2**)	— —	±4 ±3	mA mA	VCC = 5.5V (**Note 1**) Vcc = 2.5V (**Note 1**)
D7	ILI	Input Leakage Current (SCIO)	—	±1	µA	VIN = VSS or VCC
D8	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, FCLK = 1 MHz, VCC = 5.0V (**Note 1**)
D9	ICC Read	Read Operating Current	— —	3 1	mA mA	VCC=5.5V, FBUS=100 kHz, CB=100 pF VCC=2.5V, FBUS=100 kHz, CB=100 pF
D10	ICC Write	Write Operating Current	— —	5 3	mA mA	VCC = 5.5V VCC = 2.5V
D11	Iccs	Standby Current	—	1	µA	VCC = 5.5V, TA = 85°C
D12	ICCI	Idle Mode Current	—	50	µA	VCC = 5.5V

Note 1: This parameter is periodically sampled and not 100% tested.

2: The SCIO output driver impedance will vary to ensure IO is not exceeded.

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TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = 2.5V to 5.5V TA = -40°C to +85°C; VCC = 1.8V to 2.5V TA = -20°C to +85°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	FBUS	Serial Bus Frequency	10	100	kHz	—
2	TE	Bit Period	10	100	µs	—
3	TIJIT	Input Edge Jitter Tolerance	—	±0.06	UI	**(Note 3)**
4	FDRIFT	Serial Bus Frequency Drift Rate Tolerance	—	±0.50	% per byte	—
5	FDEV	Serial Bus Frequency Drift Limit	—	±5	% per command	—
6	TOJIT	Output Edge Jitter	—	±0.25	UI	**(Note 3)**
7	TR	SCIO Input Rise Time **(Note 1)**	—	100	ns	—
8	TF	SCIO Input Fall Time **(Note 1)**	—	100	ns	—
9	TSTBY	Standby Pulse Time	600	—	µs	—
10	TSS	Start Header Setup Time	10	—	µs	—
11	THDR	Start Header Low Pulse Time	5	—	µs	—
12	TSP	Input Filter Spike Suppression (SCIO)	—	50	ns	**(Note 1)**
13	TWC	Write Cycle Time (byte or page) Write Cycle Time (byte or page)	— —	5 10	ms ms	Write, WRSR commands ERAL, SETAL commands
14	—	Endurance (per page)	1M	—	cycles	25°C, VCC = 5.5V **(Note 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained on Microchip's web site: www.microchip.com.

3: A Unit Interval (UI) is equal to 1-bit period (TE) at the current bus frequency.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
VLO = 0.2V	
VHI = VCC - 0.2V	
CL = 100 pF	
Timing Measurement Reference Level	
Input	0.5 VCC
Output	0.5 VCC

FIGURE 1-1: BUS TIMING – START HEADER

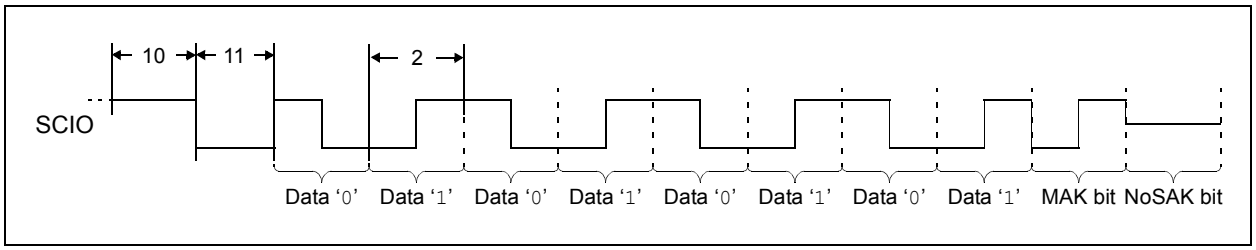


FIGURE 1-2: BUS TIMING – DATA

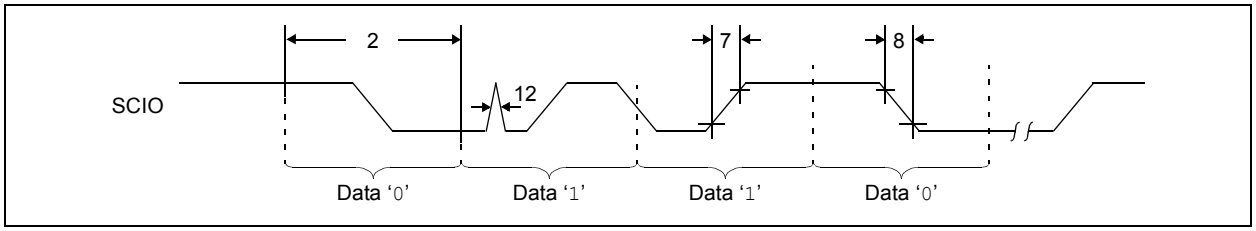


FIGURE 1-3: BUS TIMING – STANDBY PULSE

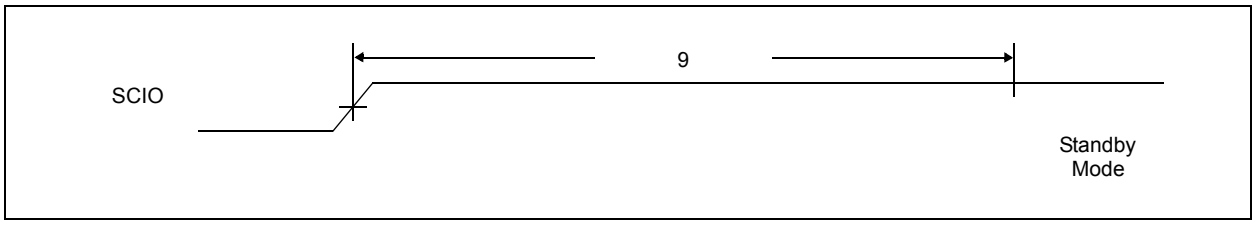
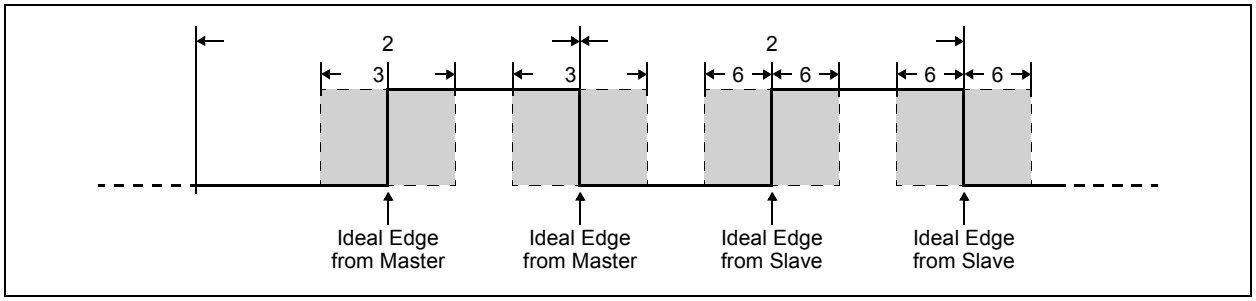


FIGURE 1-4: BUS TIMING – JITTER



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2.0 FUNCTIONAL DESCRIPTION

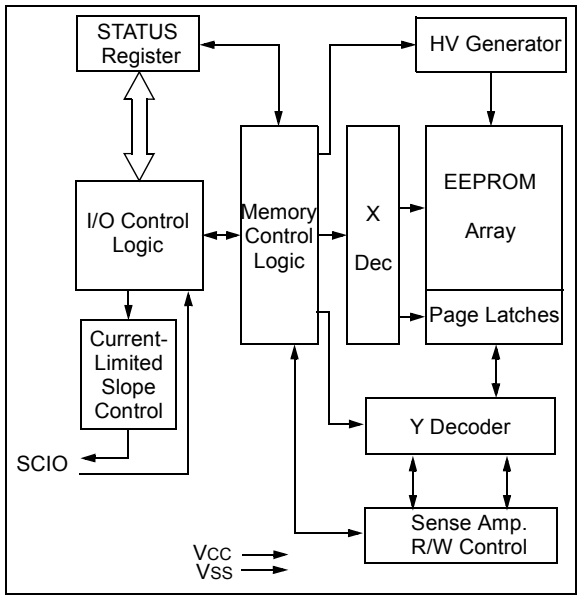
2.1 Principles of Operation

The 11AA02EXX family of serial EEPROMs support the UNI/O® protocol. They can be interfaced with microcontrollers, including Microchip's PIC® microcontrollers, ASICs, or any other device with an available discrete I/O line that can be configured properly to match the UNI/O protocol.

The 11AA02EXX devices contain an 8-bit instruction register. The devices are accessed via the SCIO pin.

Data is embedded into the I/O stream through Manchester encoding. The bus is controlled by a master device which determines the clock period, controls the bus access and initiates all operations, while the 11AA02EXX works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is active.

FIGURE 2-1: BLOCK DIAGRAM



3.0 BUS CHARACTERISTICS

3.1 Standby Pulse

When the master has control of SCIO, a standby pulse can be generated by holding SCIO high for TSTBY. At this time, the 11AA02EXX will reset and return to Standby mode. Subsequently, a high-to-low transition on SCIO (the first low pulse of the header) will return the device to the active state.

Once a command is terminated satisfactorily (i.e., via a NoMAK/SAK combination during the Acknowledge sequence), performing a standby pulse is not required to begin a new command as long as the device to be selected is the same device selected during the previous command. However, a period of TSS must be observed after the end of the command and before the beginning of the start header. After TSS, the start header (including THDR low pulse) can be transmitted in order to begin the new command.

If a command is terminated in any manner other than a NoMAK/SAK combination, then the master must perform a standby pulse before beginning a new command, regardless of which device is to be selected.

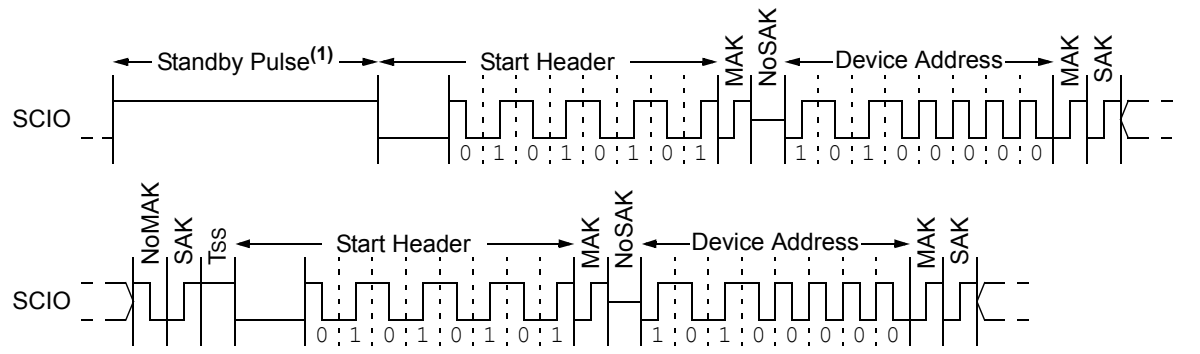
Note:	After a POR/BOR event occurs, a low-to-high transition on SCIO must be generated before proceeding with communication, including a standby pulse.

An example of two consecutive commands is shown in Figure 3-1. Note that the device address is the same for both commands, indicating that the same device is being selected both times.

A standby pulse cannot be generated while the slave has control of SCIO. In this situation, the master must wait for the slave to finish transmitting and to release SCIO before the pulse can be generated.

If, at any point during a command an error is detected by the master, a standby pulse should be generated and the command should be performed again.

FIGURE 3-1: CONSECUTIVE COMMANDS EXAMPLE



Note 1: After a POR/BOR event, a low-to-high transition on SCIO is required to occur before the first standby pulse.

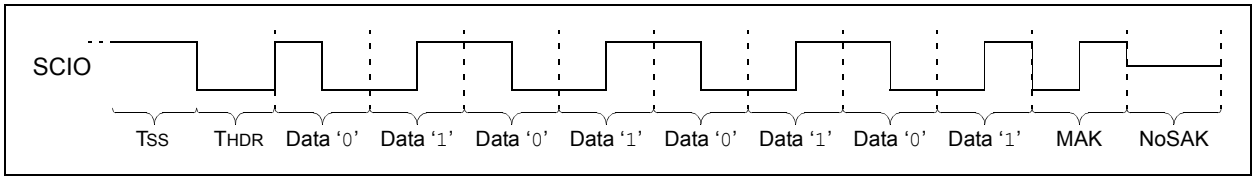
3.2 Start Data Transfer

All operations must be preceded by a start header. The start header consists of holding SCIO low for a period of THDR, followed by transmitting an 8-bit '01010101' code. This code is used to synchronize the slave's internal clock period with the master's clock period, so accurate timing is very important.

When a standby pulse is not required (i.e., between successive commands to the same device), a period of TSS must be observed after the end of the command and before the beginning of the start header.

Figure 3-2 shows the waveform for the start header, including the required Acknowledge sequence at the end of the byte.

FIGURE 3-2: START HEADER



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3.3 Acknowledge

An Acknowledge routine occurs after each byte is transmitted, including the start header. This routine consists of two bits. The first bit is transmitted by the master, and the second bit is transmitted by the slave.

Note:	A MAK must always be transmitted following the start header.

The Master Acknowledge, or MAK, is signified by transmitting a '1', and informs the slave that the current operation is to be continued. Conversely, a Not Acknowledge, or NoMAK, is signified by transmitting a '0', and is used to end the current operation (and initiate the write cycle for write operations).

Note:	When a NoMAK is used to end a WRITE or WRSR instruction, the write cycle is not initiated if no bytes of data have been received.

The slave Acknowledge, or SAK, is also signified by transmitting a '1', and confirms proper communication. However, unlike the NoMAK, the NoSAK is signified by the lack of a middle edge during the bit period.

Note:	In order to guard against bus contention, a NoSAK will occur after the start header.

A NoSAK will occur for the following events:

- Following the start header
- Following the device address, if no slave on the bus matches the transmitted address
- Following the command byte, if the command is invalid, including Read, CRRD, Write, WRSR, SETAL, and ERAL during a write cycle.
- If the slave becomes out of sync with the master
- If a command is terminated prematurely by using a NoMAK, with the exception of immediately after the device address.

See Figure 3.3 and Figure 3-4 for details.

If a NoSAK is received from the slave after any byte (except the start header), an error has occurred. The master should then perform a standby pulse and begin the desired command again.

FIGURE 3-3: ACKNOWLEDGE ROUTINE

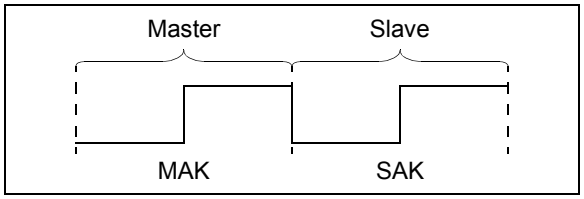
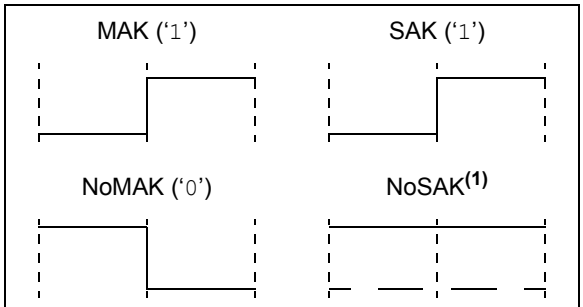


FIGURE 3-4: ACKNOWLEDGE BITS

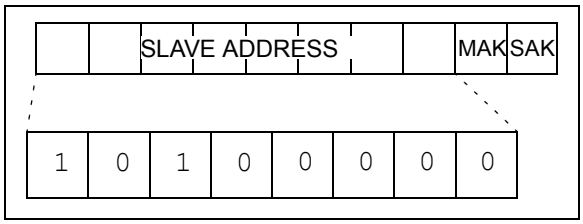


Note 1: A NoSAK is defined as any sequence that is not a valid SAK.

3.4 Device Addressing

A device address byte is the first byte received from the master device following the start header. The device address byte consists of a four-bit family code, for the 11AA02EXX this is set as '1010'. The last four bits of the device address byte are the device code, which is hardwired to '0000'.

FIGURE 3-5: DEVICE ADDRESS BYTE ALLOCATION



3.5 Bus Conflict Protection

To help guard against high current conditions arising from bus conflicts, the 11AA02EXX features a current-limited output driver. The I_{OL} and I_{OH} specifications describe the maximum current that can be sunk or sourced, respectively, by the SCIO pin. The 11AA02EXX will vary the output driver impedance to ensure that the maximum current level is not exceeded.

3.6 Device Standby

The 11AA02EXX features a low-power Standby mode during which the device is waiting to begin a new command. A high-to-low transition on SCIO will exit low-power mode and prepare the device for receiving the start header.

Standby mode will be entered upon the following conditions:

- A NoMAK followed by a SAK (i.e., valid termination of a command)
- Reception of a standby pulse

Note:	In the case of the WRITE, WRSR, SETAL, or ERAL commands, the write cycle is initiated upon receipt of the NoMAK, assuming all other write requirements have been met.

3.7 Device Idle

The 11AA02EXX features an Idle mode during which all serial data is ignored until a standby pulse occurs. Idle mode will be entered upon the following conditions:

- Invalid device address
- Invalid command byte, including Read, CRRD, Write, WRSR, SETAL and ERAL during a write cycle.
- Missed edge transition
- Reception of a MAK following a WREN, WRDI, SETAL, or ERAL command byte
- Reception of a MAK following the data byte of a WRSR command

An invalid start header will indirectly cause the device to enter Idle mode. Whether or not the start header is invalid cannot be detected by the slave, but will prevent the slave from synchronizing properly with the master. If the slave is not synchronized with the master, an edge transition will be missed, thus causing the device to enter Idle mode.

3.8 Synchronization

At the beginning of every command, the 11AA02EXX utilizes the start header to determine the master's bus clock period. This period is then used as a reference for all subsequent communication within that command.

The 11AA02EXX features re-synchronization circuitry which will monitor the position of the middle data edge during each MAK bit and subsequently adjust the internal time reference in order to remain synchronized with the master.

There are two variables which can cause the 11AA02EXX to lose synchronization. The first is frequency drift, defined as a change in the bit period, T_E. The second is edge jitter, which is a single occurrence change in the position of an edge within a bit period, while the bit period itself remains constant.

3.8.1 FREQUENCY DRIFT

Within a system, there is a possibility that frequencies can drift due to changes in voltage, temperature, etc. The re-synchronization circuitry provides some tolerance for such frequency drift. The tolerance range is specified by two parameters, F_{DRIFT} and F_{DEV}. F_{DRIFT} specifies the maximum tolerable change in bus frequency per byte. F_{DEV} specifies the overall limit in frequency deviation within an operation (i.e., from the end of the start header until communication is terminated for that operation). The start header at the beginning of the next operation will reset the re-synchronization circuitry and allow for another F_{DEV} amount of frequency drift.

3.8.2 EDGE JITTER

Ensuring that edge transitions from the master always occur exactly in the middle or end of the bit period is not always possible. Therefore, the re-synchronization circuitry is designed to provide some tolerance for edge jitter.

The 11AA02EXX adjusts its phase every MAK bit, so T_{IJIT} specifies the maximum allowable peak-to-peak jitter relative to the previous MAK bit. Since the position of the previous MAK bit would be difficult to measure by the master, the minimum and maximum jitter values for a system should be considered the worst-case. These values will be based on the execution time for different branch paths in software, jitter due to thermal noise, etc.

The difference between the minimum and maximum values, as a percentage of the bit period, should be calculated and then compared against T_{IJIT} to determine jitter compliance.

Note:	Because the 11AA02EXX only re-synchronizes during the MAK bit, the overall ability to remain synchronized depends on a combination of frequency drift and edge jitter (i.e., if the MAK bit edge is experiencing the maximum allowable edge jitter, then there is no room for frequency drift). Conversely, if the frequency has drifted to the maximum amount tolerable within a byte, then no edge jitter can be present.

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4.0 DEVICE COMMANDS

After the device address byte, a command byte must be sent by the master to indicate the type of operation to be performed. The code for each instruction is listed in Table 4-1.

TABLE 4-1: INSTRUCTION SET

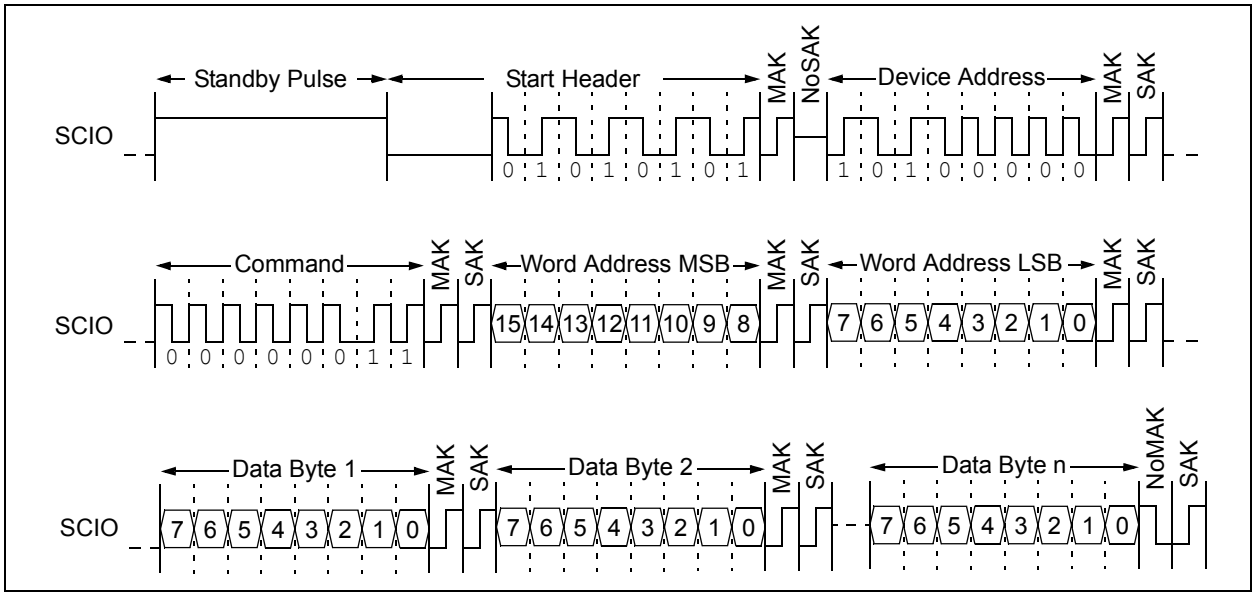
Instruction Name	Instruction Code	Hex Code	Description
READ	0000 0011	0x03	Read data from memory array beginning at specified address
CRRD	0000 0110	0x06	Read data from current location in memory array
WRITE	0110 1100	0x6C	Write data to memory array beginning at specified address
WREN	1001 0110	0x96	Set the write enable latch (enable write operations)
WRDI	1001 0001	0x91	Reset the write enable latch (disable write operations)
RDSR	0000 0101	0x05	Read STATUS register
WRSR	0110 1110	0x6E	Write STATUS register
ERAL	0110 1101	0x6D	Write '0x00' to entire array
SETAL	0110 0111	0x67	Write '0xFF' to entire array

4.1 Read Instruction

The Read command allows the master to access any memory location in a random manner. After the READ instruction has been sent to the slave, the two bytes of the Word Address are transmitted, with an Acknowledge sequence being performed after each byte. Then, the slave sends the first data byte to the master. If more data is to be read, the master sends a MAK, indicating that the slave should output the next data byte. This continues until the master sends a NoMAK, which ends the operation.

To provide sequential reads in this manner, the 11AA02EXX contains an internal Address Pointer which is incremented by one after the transmission of each byte. This Address Pointer allows the entire memory contents to be serially read during one operation. When the highest address is reached, the Address Pointer rolls over to address '0x00' if the master chooses to continue the operation by providing a MAK.

FIGURE 4-1: READ COMMAND SEQUENCE



4.2 Current Address Read (CRRD) Instruction

The internal address counter featured on the 11AA02EXX maintains the address of the last memory array location accessed. The CRRD instruction allows the master to read data back beginning from this current location. Consequently, no word address is provided upon issuing this command.

Note that, except for the initial word address, the READ and CRRD instructions are identical, including the ability to continue requesting data through the use of MAKs in order to sequentially read from the array.

As with the READ instruction, the CRRD instruction is terminated by transmitting a NoMAK.

Table 4-2 lists the events upon which the internal address counter is modified.

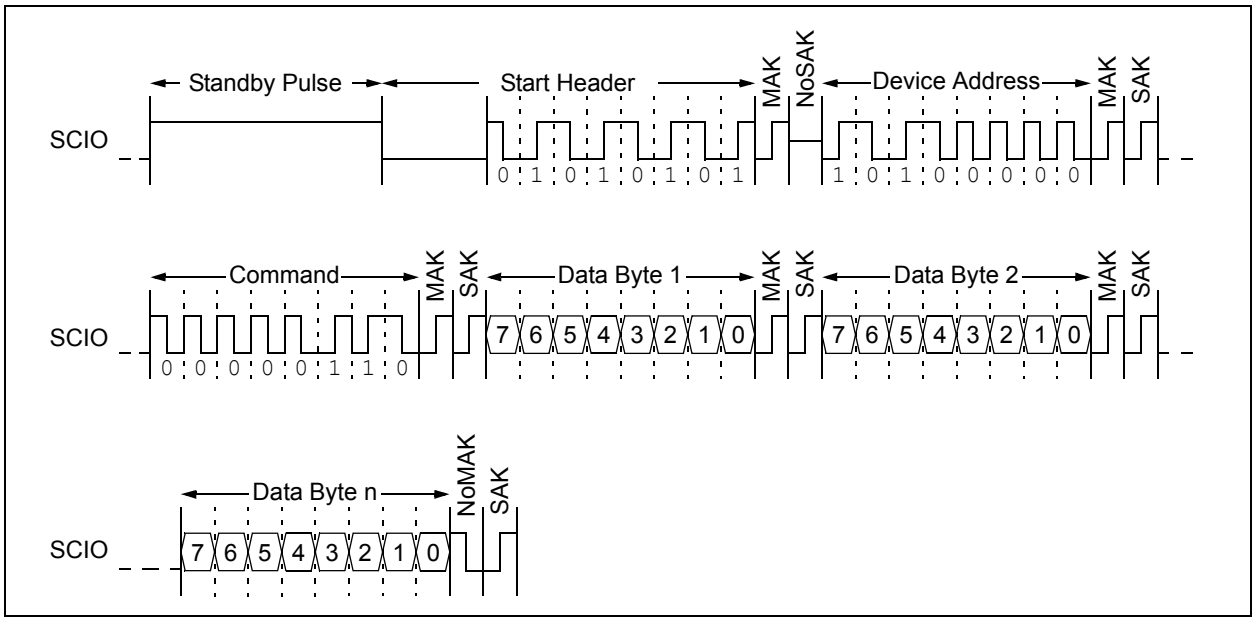
TABLE 4-2: INTERNAL ADDRESS COUNTER

Command	Event	Action
—	Power-on Reset	Counter is undefined
READ or WRITE	MAK edge following each Address byte	Counter is updated with newly received value
READ, WRITE, or CRRD	MAK/NoMAK edge following each data byte	Counter is incremented by 1

Note: If, following each data byte in a READ, WRITE, or CRRD instruction, neither a MAK nor a NoMAK edge is received (i.e., if a standby pulse occurs instead), the internal address counter will not be incremented.

Note: During a Write command, once the last data byte for a page has been loaded, the internal Address Pointer will rollover to the beginning of the selected page.

FIGURE 4-2: CRRD COMMAND SEQUENCE



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4.3 Write Instruction

Prior to any attempt to write data to the 11AA02EXX, the write enable latch must be set by issuing the WREN instruction (see **Section 4.4 "Write Enable (WREN) and Write Disable (WRDI) Instructions"**).

Once the write enable latch is set, the user may proceed with issuing a WRITE instruction (including the header and device address bytes) followed by the MSB and LSB of the Word Address. Once the last Acknowledge sequence has been performed, the master transmits the data byte to be written.

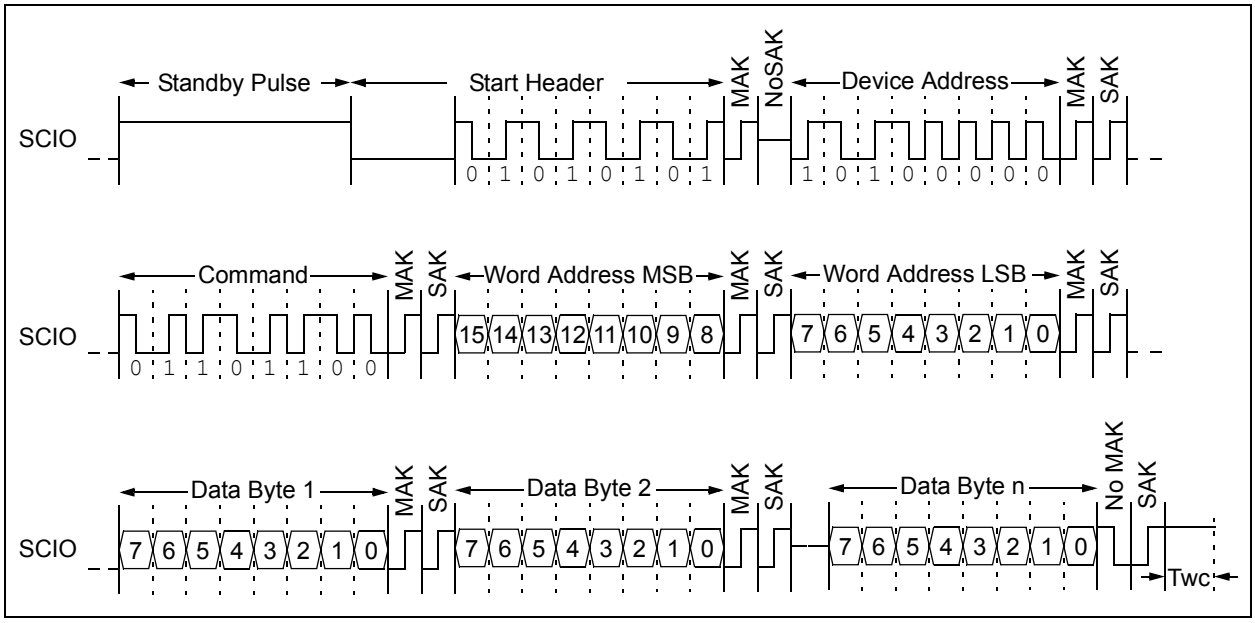
The 11AA02EXX features a 16-byte page buffer, meaning that up to 16 bytes can be written at one time. To utilize this feature, the master can transmit up to 16 data bytes to the 11AA02EXX, which are temporarily stored in the page buffer. After each data byte, the master sends a MAK, indicating whether or not another data byte is to follow. A NoMAK indicates that no more data is to follow, and as such will initiate the internal write cycle.

Note:	If a NoMAK is generated before any data has been provided, or if a standby pulse occurs before the NoMAK is generated, the 11AA02EXX will be reset, and the write cycle will not be initiated.

Upon receipt of each word, the four lower-order Address Pointer bits are internally incremented by one. The higher-order bits of the word address remain constant. If the master should transmit data past the end of the page, the address counter will roll over to the beginning of the page, where further received data will be written.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page size (16 bytes) and end at addresses that are integer multiples of the page size minus 1. As an example, the page that begins at address 0x30 ends at address 0x3F. If a page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 4-3: WRITE COMMAND SEQUENCE



4.4 Write Enable (WREN) and Write Disable (WRDI) Instructions

The 11AA02EXX contains a write enable latch. See Table 6-1 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI instruction will reset the latch.

Note:	The WREN and WRDI instructions must be terminated with a NoMAK following the command byte. If a NoMAK is not received at this point, the command will be considered invalid, and the device will go into Idle mode without responding with a SAK or executing the command.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- ERAL instruction successfully executed
- SETAL instruction successfully executed

FIGURE 4-4: WRITE ENABLE COMMAND SEQUENCE

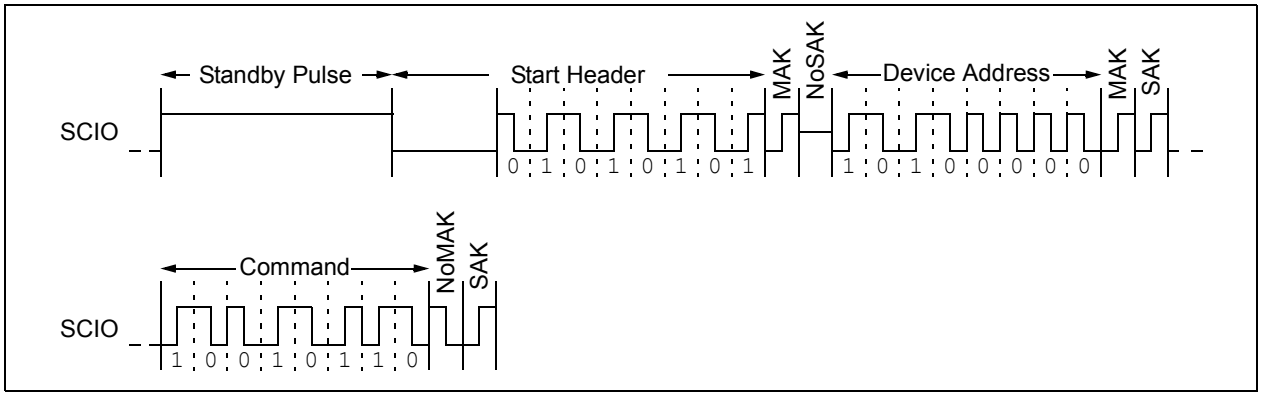
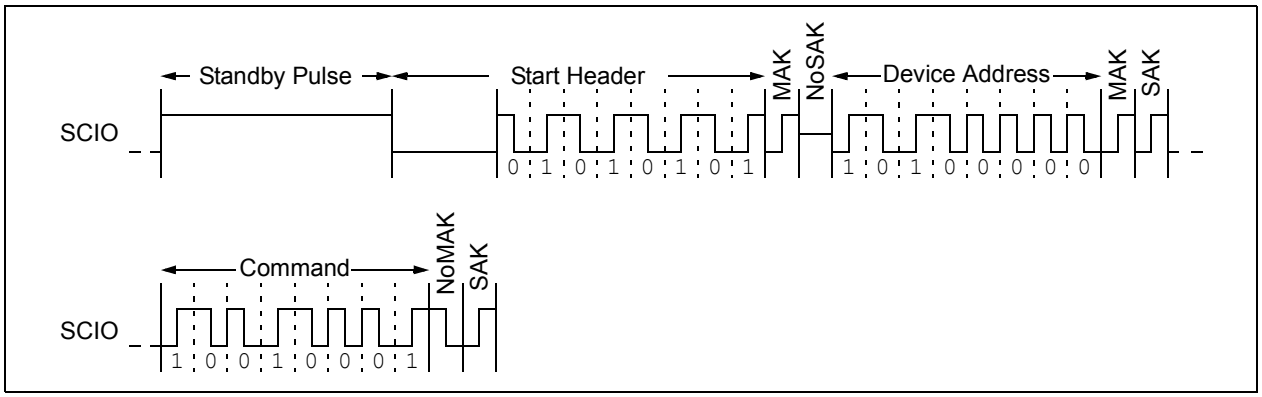


FIGURE 4-5: WRITE DISABLE COMMAND SEQUENCE



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4.5 Read Status Register (RDSR) Instruction

The RDSR instruction provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

Note: Bits 4-7 are don't cares, and will read as '0'.

The **Write-In-Process (WIP)** bit indicates whether the 11AA02EXX is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. This bit is set and cleared using the WREN and WRDI instructions, respectively. This bit is read-only for any other instruction.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user through the WRSR instruction. These bits are nonvolatile.

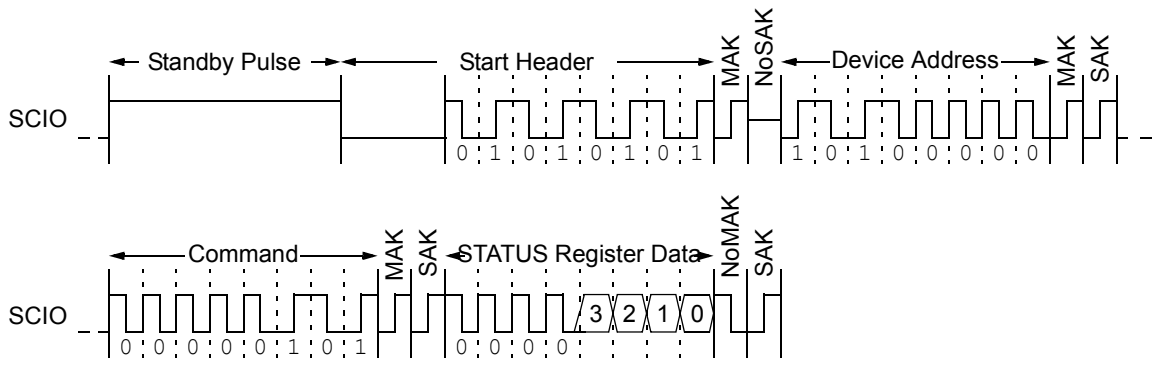
Note: If Read Status Register command is initiated while the 11AA02EXX is currently executing an internal write cycle on the STATUS register, the new Block Protection bit values will be read during the entire command.

The WIP and WEL bits will update dynamically (asynchronous to issuing the RDSR instruction). Furthermore, after the STATUS register data is received, the master can provide a MAK during the Acknowledge sequence to request that the data be transmitted again. This allows the master to continuously monitor the WIP and WEL bits without the need to issue another full command.

Once the master is finished, it provides a NoMAK to end the operation.

Note: The current drawn for a Read Status Register command during a write cycle is a combination of the ICC Read and ICC Write operating currents.

FIGURE 4-6: READ STATUS REGISTER COMMAND SEQUENCE



Note: The STATUS register data can continuously be read, or polled, by transmitting a MAK in place of the NoMAK.

4.6 Write Status Register (WRSR) Instruction

The WRSR instruction allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two, or all four of the segments of the array. The partitioning is controlled as illustrated in Table 4-3.

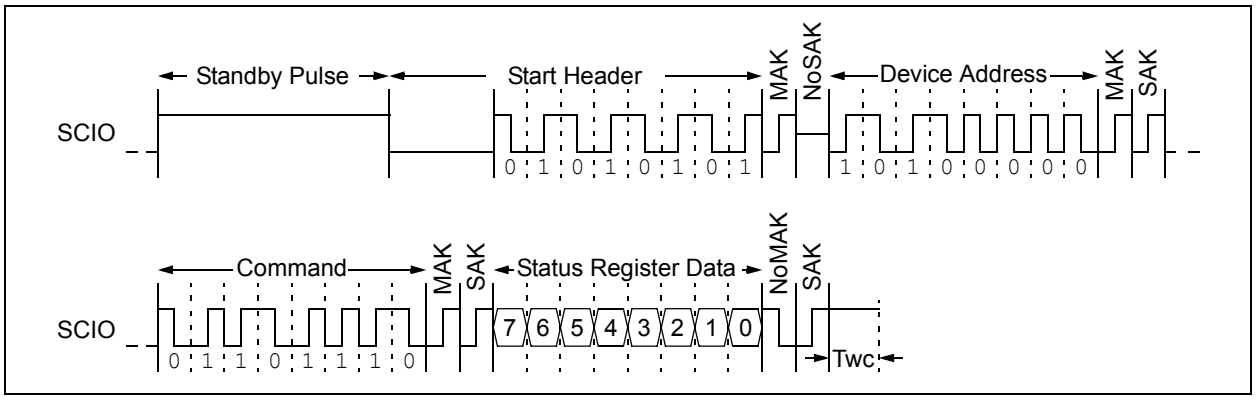
After transmitting the STATUS register data, the master must transmit a NoMAK during the Acknowledge sequence in order to initiate the internal write cycle.

Note: The WRSR instruction must be terminated with a NoMAK following the data byte. If a NoMAK is not received at this point, the command will be considered invalid, and the device will go into Idle mode without responding with a SAK or executing the command.

TABLE 4-3: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	none
0	1	upper 1/4 (C0h-FFh)
1	0	upper 1/2 (80h-FFh)
1	1	all (00h-FFh)

FIGURE 4-7: WRITE STATUS REGISTER COMMAND SEQUENCE



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4.7 Erase All (ERAL) Instruction

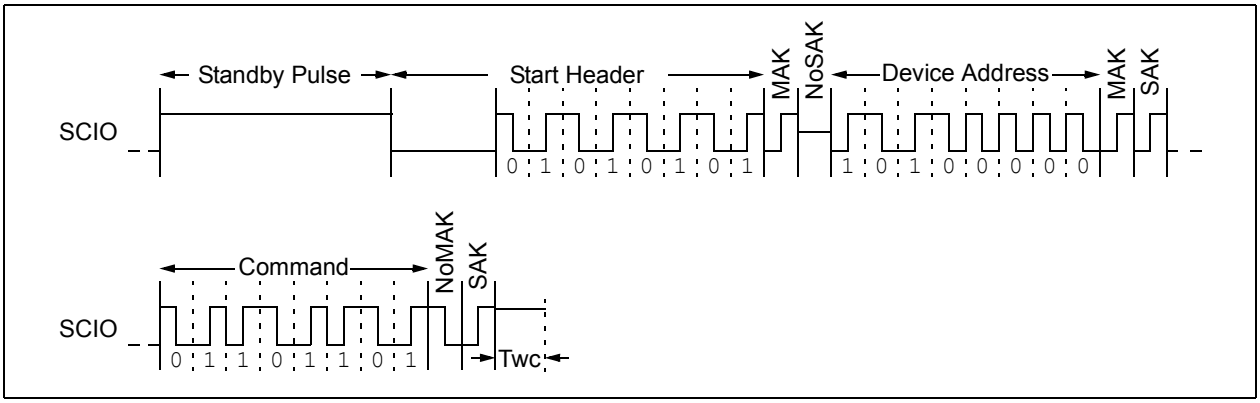
The ERAL instruction allows the user to write '0x00' to the entire memory array with one command. Note that the write enable latch (WEL) must first be set by issuing the WREN instruction.

Once the write enable latch is set, the user may proceed with issuing a ERAL instruction (including the header and device address bytes). Immediately after the NoMAK bit has been transmitted by the master, the internal write cycle is initiated, during which time all words of the memory array are written to '0x00'.

The ERAL instruction is ignored if either of the Block Protect bits (BP0, BP1) are not 0, meaning 1/4, 1/2, or all of the array is protected.

Note:	The ERAL instruction must be terminated with a NoMAK following the command byte. If a NoMAK is not received at this point, the command will be considered invalid, and the device will go into Idle mode without responding with a SAK or executing the command.

FIGURE 4-8: ERASE ALL COMMAND SEQUENCE



4.8 Set All (SETAL) Instruction

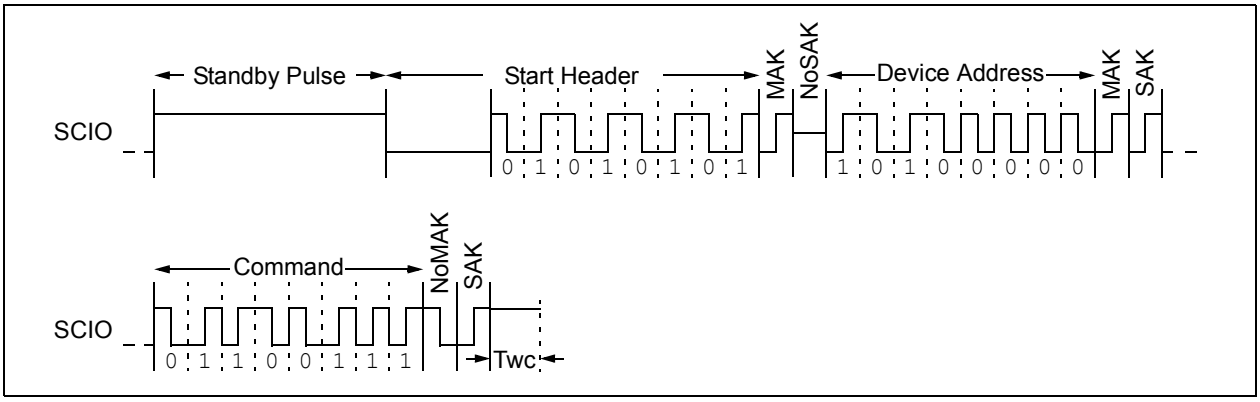
The SETAL instruction allows the user to write '0xFF' to the entire memory array with one command. Note that the write enable latch (WEL) must first be set by issuing the WREN instruction.

Once the write enable latch is set, the user may proceed with issuing a SETAL instruction (including the header and device address bytes). Immediately after the NoMAK bit has been transmitted by the master, the internal write cycle is initiated, during which time all words of the memory array are written to '0xFF'.

The SETAL instruction is ignored if either of the Block Protect bits (BP0, BP1) are not '0', meaning 1/4, 1/2, or all of the array is protected.

Note:	The SETAL instruction must be terminated with a NoMAK following the command byte. If a NoMAK is not received at this point, the command will be considered invalid, and the device will go into Idle mode without responding with a SAK or executing the command.

FIGURE 4-9: SET ALL COMMAND SEQUENCE



5.0 DATA PROTECTION

The following protection has been implemented to prevent inadvertent writes to the array:

- The Write Enable Latch (WEL) is reset on power-up
- A Write Enable (WREN) instruction must be issued to set the write enable latch
- After a write, ERAL, SETAL, or WRSR command, the write enable latch is reset
- Commands to access the array or write to the status register are ignored during an internal write cycle and programming is not affected

6.0 POWER-ON STATE

The 11AA02EXX powers on in the following state:

- The device is in low-power Shutdown mode, requiring a low-to-high transition on SCIO to enter Idle mode
- The Write Enable Latch (WEL) is reset
- The internal Address Pointer is undefined
- A low-to-high transition, standby pulse and subsequent high-to-low transition on SCIO (the first low pulse of the header) are required to enter the active state

TABLE 6-1: WRITE PROTECT FUNCTIONALITY MATRIX

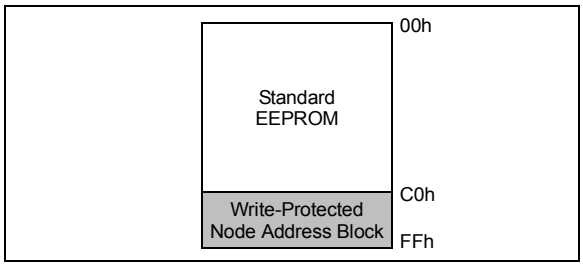
WEL	Protected Blocks	Unprotected Blocks	Status Register
0	Protected	Protected	Protected
1	Protected	Writable	Writable

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7.0 PRE-PROGRAMMED EUI-48™ OR EUI-64™ NODE ADDRESS

The 11AA02EXX is programmed at the factory with a globally unique node address stored in the upper 1/4 of the array and write-protected through the STATUS register. The remaining 1,536 bits are available for application use.

FIGURE 7-1: MEMORY ORGANIZATION



7.1 Factory-Programmed Write Protection

In order to help guard against accidental corruption of the node address, the BP1 and BP0 bits of the STATUS register are programmed at the factory to '0' and '1', respectively, as shown in the following table:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP
—	—	—	—	0	1	—	—

This protects the upper 1/4 of the array (0xC0 to 0xFF) from write operations. This array block can be utilized for writing by clearing the BP bits with a Write Status Register (WRSR) instruction. Note that if this is performed, care must be taken to prevent overwriting the node address value.

7.2 EUI-48™ Node Address (11AA02E48)

The 6-byte EUI-48™ node address value of the 11AA02E48 is stored in array locations 0xFA through 0xFF, as shown in Figure 7-2. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. Currently, Microchip's OUIs are 0x0004A3 and 0x001EC0, though this will change as addresses are exhausted. The remaining three bytes are the Extension Identifier, and are generated by Microchip to ensure a globally-unique, 48-bit value.

7.2.1 EUI-64™ SUPPORT USING THE 11AA02E48

The pre-programmed EUI-48 node address of the 11AA02E48 can easily be encapsulated at the application level to form a globally unique, 64-bit node address for systems utilizing the EUI-64 standard. This is done by adding 0xFFFE between the OUI and the Extension Identifier, as shown below.

Note: As an alternative, the 11AA02E64 features an EUI-64 node address that can be used in EUI-64 applications directly without the need for encapsulation, thereby simplifying system software. See **Section 7.3 "EUI-64™ Node Address (11AA02E64)"** for details.

FIGURE 7-2: EUI-48 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE (11AA02E48)

Description	24-bit Organizationally Unique Identifier			24-bit Extension Identifier		
Data	00h	04h	A3h	12h	34h	56h
Array Address	FAh					FFh

Corresponding EUI-48™ Node Address: 00-04-A3-12-34-56

Corresponding EUI-64™ Node Address After Encapsulation: 00-04-A3-FF-FE-12-34-56

7.3 EUI-64™ Node Address (11AA02E64)

The 8-byte EUI-64™ node address value of the 11AA02E64 is stored in array locations 0xF8 through 0xFF, as shown in Figure 7-3. The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. Currently, Microchip's OUIs are 0x0004A3 and 0x001EC0, though this will change as addresses are exhausted. The remaining five bytes are the Extension Identifier, and are generated by Microchip to ensure a globally-unique, 64-bit value.

Note:	In conformance with IEEE guidelines, Microchip will not use the values 0xFFFE and 0xFFFF for the first two bytes of the EUI-64 Extension Identifier. These two values are specifically reserved to allow applications to encapsulate EUI-48 addresses into EUI-64 addresses.

FIGURE 7-3: EUI-64 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE (11AA02E64)

Description	24-bit Organizationally Unique Identifier			40-bit Extension Identifier				
Data	00h	04h	A3h	12h	34h	56h	78h	90h
Array Address	F8h							FFh

Corresponding EUI-64™ Node Address: 00-04-A3-12-34-56-78-90

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8.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 8-1.

TABLE 8-1: PIN FUNCTION TABLE

Name	3-pin SOT-23	8-pin SOIC	Description
SCIO	1	5	Serial Clock, Data Input/Output
VCC	2	8	Supply Voltage
VSS	3	4	Ground
NC	—	1,2,3,6,7	No Internal Connection

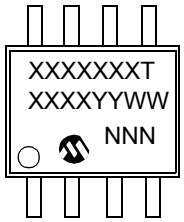
8.1 Serial Clock, Data Input/Output (SCIO)

SCIO is a bidirectional pin used to transfer commands and addresses into, as well as data into and out of, the device. The serial clock is embedded into the data stream through Manchester encoding. Each bit is represented by a signal transition at the middle of the bit period.

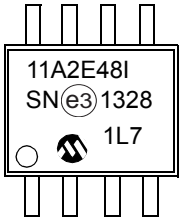
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

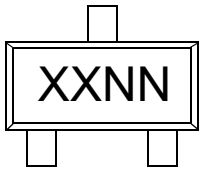
8-Lead SOIC



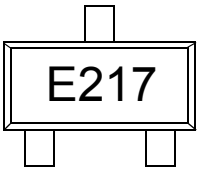
Example:



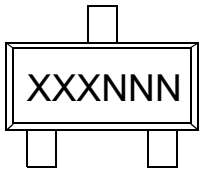
3-Lead SOT-23 (11AA02E48)



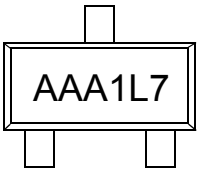
Example:



3-Lead SOT-23 (11AA02E64)



Example:



Part Number	1st Line Marking Code	
	SOT-23	SOIC
	I Temp.	I Temp.
11AA02E48	E2NN	11A2E48T
11AA02E64	AAANNN	11A2E64T

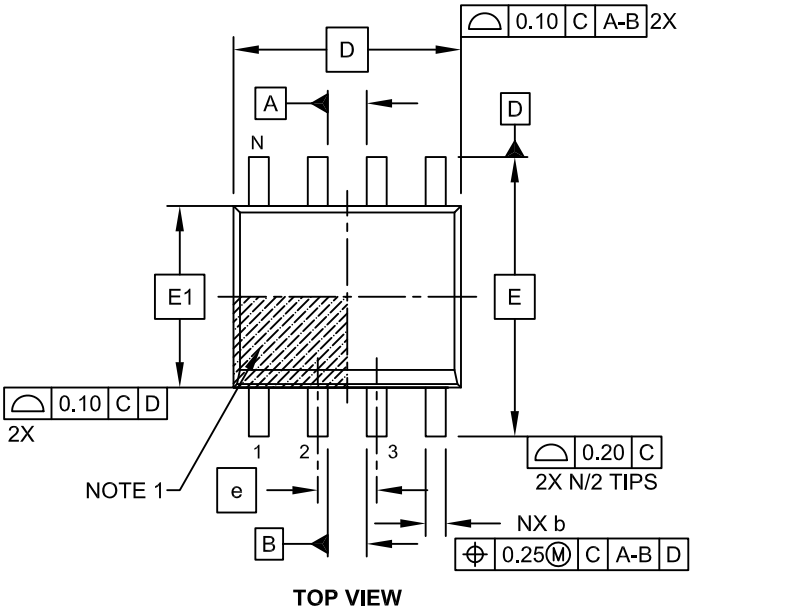
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

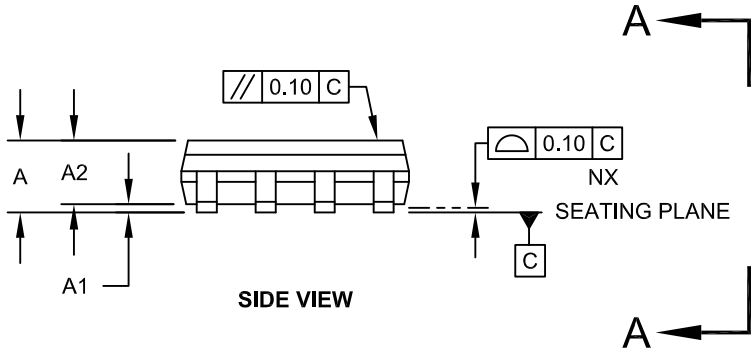
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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

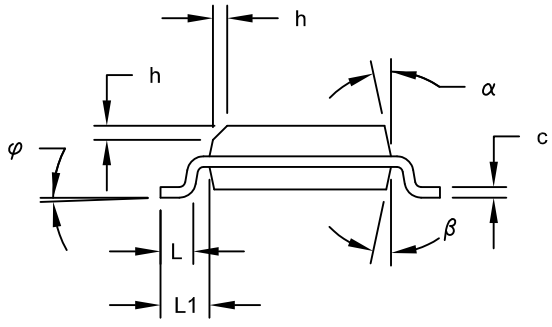
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

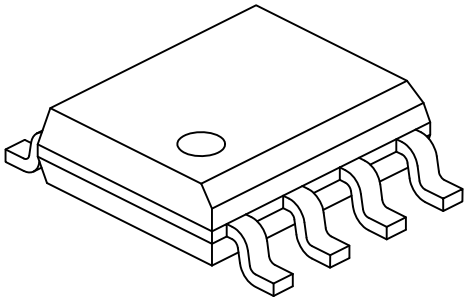


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

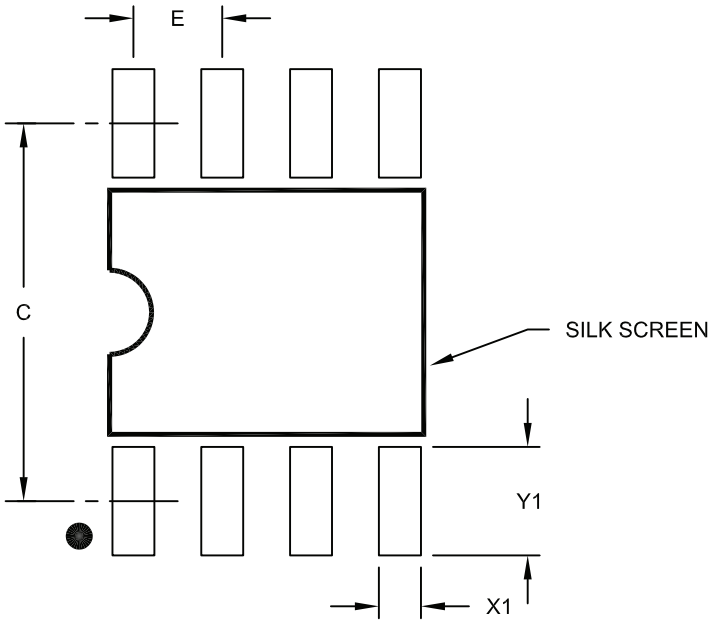
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

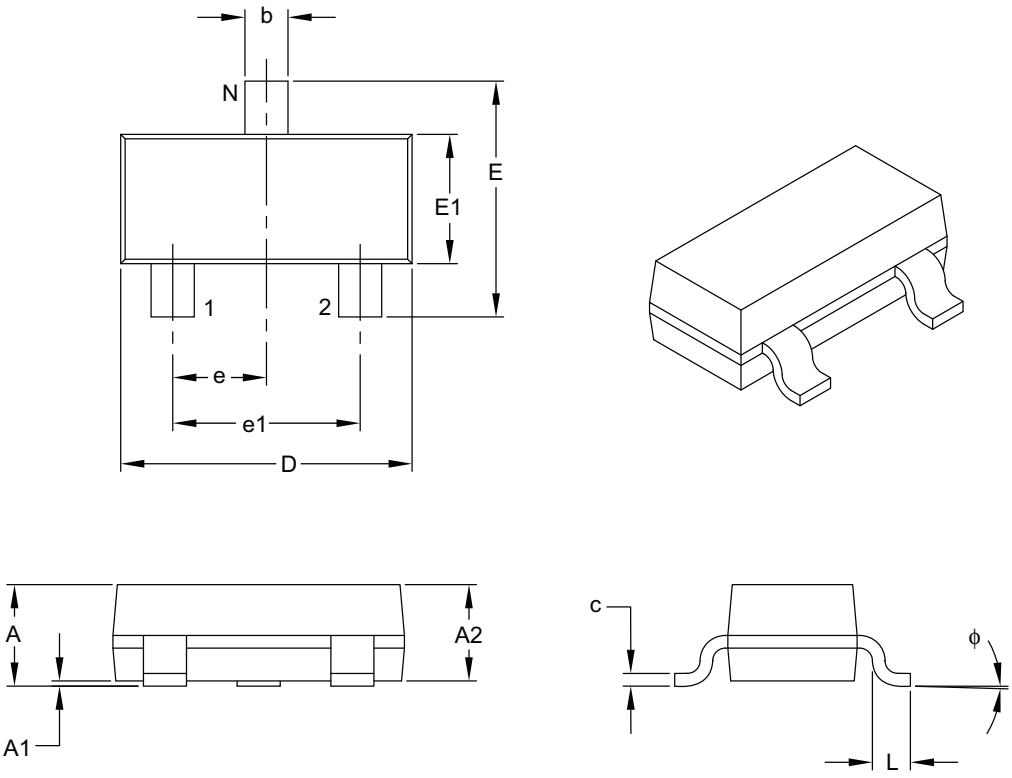
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		3	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.89	–	1.12
Molded Package Thickness	A2	0.79	0.95	1.02
Standoff	A1	0.01	–	0.10
Overall Width	E	2.10	–	2.64
Molded Package Width	E1	1.16	1.30	1.40
Overall Length	D	2.67	2.90	3.05
Foot Length	L	0.13	0.50	0.60
Foot Angle	ϕ	0°	–	10°
Lead Thickness	c	0.08	–	0.20
Lead Width	b	0.30	–	0.54

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

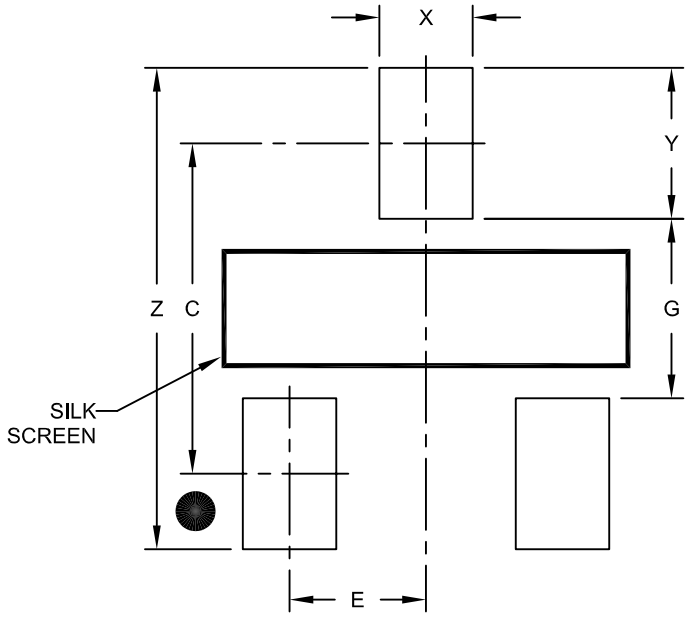
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-104B

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3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.30	
Contact Pad Width (X3)	X			0.65
Contact Pad Length (X3)	Y			1.05
Distance Between Pads	G	1.25		
Overall Width	Z			3.35

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2104A

APPENDIX A: REVISION HISTORY

Revision A (12/2008)

Original release of this document.

Revision B (04/2013)

Revised AC Char. Max. Parameters 3 and 4; Added 11AA02E64 part.

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- Development Systems Information Line

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Device: 11AA02E48/11AA02E64 Literature Number: DS20002122B

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PRODUCT IDENTIFICATION SYSTEM

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PART NO.	X	—	X	/XX
Device	Tape & Reel		Temperature Range	Package

Device:	11AA02E48	=	2 Kbit, 1.8V UNI/O Serial EEPROM with EUI-48™ Node Identity
	11AA02E64	=	2 Kbit, 1.8V UNI/O Serial EEPROM with EUI-64™ Node Identity
Tape & Reel:	T	=	Tape and Reel
	Blank	=	Tube
Temperature Range:	I	=	-40°C to+85°C(Industrial)
Package:	SN	=	8-lead Plastic SOIC (3.90 mm body)
	TT	=	3-lead SOT 23 (Tape and Reel only)

Examples:

a) 11AA02E48T-I/TT = 2 Kbit, 1.8V Serial EEPROM with EUI-48 node identity, Industrial temp., Tape & Reel, SOT-23 package

b) 11AA02E48-I/SN = 2 Kbit, 1.8V Serial EEPROM with EUI-48 node identity, Industrial temp., SOIC package

c) 11AA02E48T-I/SN = 2 Kbit, 1.8V Serial EEPROM with EUI-48 node identity, Industrial temp., Tape & Reel, SOIC package

d) 11AA02E64T-I/TT = 2 Kbit, 1.8V Serial EEPROM with EUI-64 node identity, Industrial temp., Tape & Reel, SOT-23 package

e) 11AA02E64-I/SN = 2 Kbit, 1.8V Serial EEPROM with EUI-64 node identity, Industrial temp., SOIC package

f) 11AA02E64T-I/SN = 2 Kbit, 1.8V Serial EEPROM with EUI-64 node identity, Industrial temp., Tape & Reel, SOIC package

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