

## 96MHz – 400MHz Low Phase Noise XO (for 12 – 25MHz Crystals)

### FEATURES

- Low phase noise output for the 96MHz to 400MHz range (-134 dBc at 10kHz offset).
- Selectable CMOS, PECL and LVDS output.
- 12 to 25MHz crystal input.
- Output Enable selector.
- 3.3V operation.
- Available in DIE (65 mil x 62 mil).

### DESCRIPTIONS

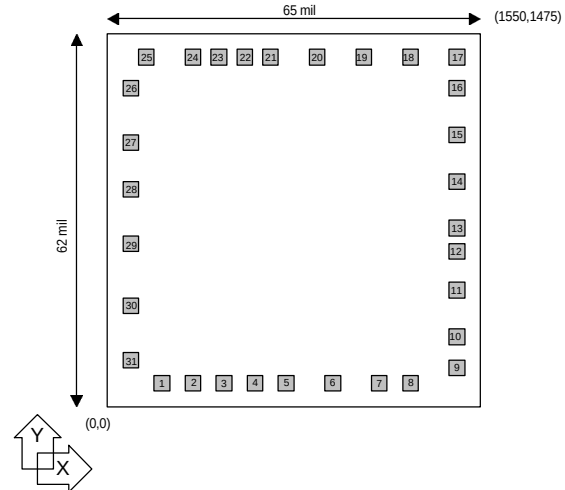
The PLL602-10 is a monolithic low jitter and low phase noise (-134dBc/Hz @ 10kHz offset) XO IC Die, with CMOS, LVDS and PECL output, for 96MHz to 400MHz output range, using a low frequency crystal.

The same die can be used as a XO with output frequencies ranging from  $F_{XIN} \times 8$  to  $F_{XIN} \times 16$  thanks to selector pads allowing bonding options (see Divider Selection Table on this page). This makes the PLL602-10 ideal for a wide range of applications.

### DIE SPECIFICATIONS

| Name           | Value                 |
|----------------|-----------------------|
| Size           | 62 x 65 mil           |
| Reverse side   | GND                   |
| Pad dimensions | 80 micron x 80 micron |
| Thickness      | 10 mil                |

### DIE CONFIGURATION



### MULTIPLIER SELECTION

| Pad #19 | MULTIPLIER          | OUTPUT RANGE  |
|---------|---------------------|---------------|
| 0       | $F_{XIN} \times 16$ | 192 – 400 MHz |
| 1       | $F_{XIN} \times 8$  | 96 – 200 MHz  |

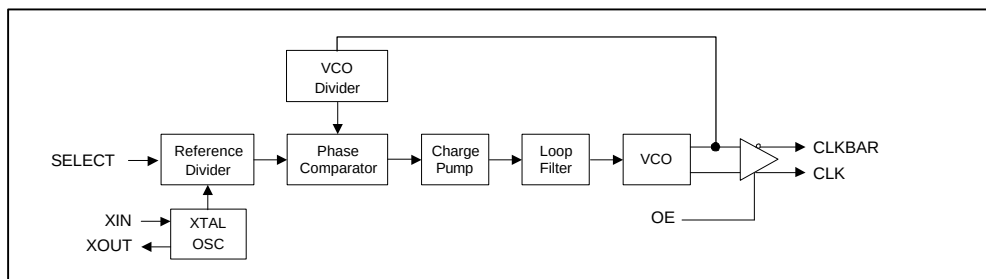
**Note:** Selector pad defaults to '1', wire bond to GND to set to '0'

### OUTPUT SELECTION AND ENABLE

| Pad #18<br>OUTSEL1 | Pad #25<br>OUTSEL0 | Selected Output |
|--------------------|--------------------|-----------------|
| 0                  | 0                  | High Drive CMOS |
| 0                  | 1                  | Standard CMOS   |
| 1                  | 0                  | PECL            |
| 1                  | 1                  | LVDS            |

| OE (Pad #30) | State          |
|--------------|----------------|
| 0            | Tri-state      |
| 1 (Default)  | Output enabled |

### BLOCK DIAGRAM



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### ELECTRICAL SPECIFICATIONS

#### 1. Absolute Maximum Ratings

| PARAMETERS                                | SYMBOL   | MIN.         | MAX.         | UNITS |
|-------------------------------------------|----------|--------------|--------------|-------|
| Supply Voltage                            | $V_{DD}$ |              | 7            | V     |
| Input Voltage, dc                         | $V_I$    | $V_{SS}-0.5$ | $V_{DD}+0.5$ | V     |
| Output Voltage, dc                        | $V_O$    | $V_{SS}-0.5$ | $V_{DD}+0.5$ | V     |
| Storage Temperature                       | $T_S$    | -65          | 150          | °C    |
| Ambient Operating Temperature             | $T_A$    | 0            | 70           | °C    |
| Junction Temperature                      | $T_J$    |              | 125          | °C    |
| Lead Temperature (soldering, 10s)         |          |              | 260          | °C    |
| Input Static Discharge Voltage Protection |          |              | 2            | kV    |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

#### 2. Crystal Specifications

| PARAMETERS                  | SYMBOL       | CONDITIONS                | MIN. | TYP. | MAX. | UNITS    |
|-----------------------------|--------------|---------------------------|------|------|------|----------|
| Crystal Resonator Frequency | $F_{XIN}$    | Parallel Fundamental Mode | 12   |      | 25   | MHz      |
| Crystal Loading Rating      | $C_L$ (xtal) |                           |      | TBD  |      | pF       |
| Recommended ESR             | $R_E$        | AT cut                    |      |      | 30   | $\Omega$ |

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### 3. General Electrical Specifications

| PARAMETERS                                    | SYMBOL          | CONDITIONS                      | MIN. | TYP. | MAX.     | UNITS |
|-----------------------------------------------|-----------------|---------------------------------|------|------|----------|-------|
| Supply Current, Dynamic (with Loaded Outputs) | I <sub>DD</sub> | PECL/LVDS/CMOS                  |      |      | 80/60/35 | mA    |
| Operating Voltage                             | V <sub>DD</sub> |                                 | 3.13 |      | 3.47     | V     |
| Output Clock Duty Cycle                       |                 | @ 1.4V (CMOS)                   | 45   | 50   | 55       | %     |
|                                               |                 | @ 1.25V (LVDS)                  | 45   | 50   | 55       |       |
|                                               |                 | @ V <sub>dd</sub> – 1.3V (PECL) | 45   | 50   | 55       |       |
| Short Circuit Current                         |                 |                                 |      | ±50  |          | mA    |

### 4. Jitter and Phase Noise specification

| PARAMETERS                      | CONDITIONS                                                          | MIN. | TYP. | MAX. | UNITS  |
|---------------------------------|---------------------------------------------------------------------|------|------|------|--------|
| Period jitter RMS               | With capacitive decoupling between VDD and GND.                     |      | 7    |      | ps     |
| Accumulated jitter RMS          | With capacitive decoupling between VDD and GND. Over 10,000 cycles. |      | 11   |      | ps     |
| Phase Noise relative to carrier | 155MHz @100Hz offset                                                |      | -90  |      | dBc/Hz |
| Phase Noise relative to carrier | 155MHz @1kHz offset                                                 |      | -114 |      | dBc/Hz |
| Phase Noise relative to carrier | 155MHz @10kHz offset                                                |      | -134 |      | dBc/Hz |
| Phase Noise relative to carrier | 155MHz @100kHz offset                                               |      | -134 |      | dBc/Hz |

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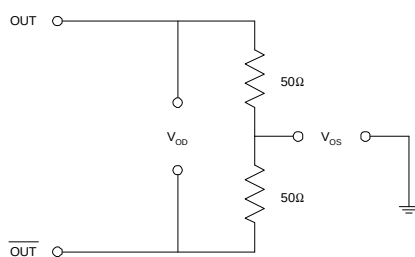
**5. LVDS Electrical Characteristics**

| PARAMETERS                   | SYMBOL          | CONDITIONS                                 | MIN.  | TYP.    | MAX.     | UNITS   |
|------------------------------|-----------------|--------------------------------------------|-------|---------|----------|---------|
| Output Differential Voltage  | $V_{OD}$        | $R_L = 100\ \Omega$<br>(see figure)        | 247   | 355     | 454      | mV      |
| $V_{DD}$ Magnitude Change    | $\Delta V_{OD}$ |                                            | -50   |         | 50       | mV      |
| Output High Voltage          | $V_{OH}$        |                                            |       | 1.4     | 1.6      | V       |
| Output Low Voltage           | $V_{OL}$        |                                            | 0.9   | 1.1     |          | V       |
| Offset Voltage               | $V_{OS}$        |                                            | 1.125 | 1.2     | 1.375    | V       |
| Offset Magnitude Change      | $\Delta V_{OS}$ |                                            | 0     | 3       | 25       | mV      |
| Power-off Leakage            | $I_{OXD}$       | $V_{out} = V_{DD}$ or GND<br>$V_{DD} = 0V$ |       | $\pm 1$ | $\pm 10$ | $\mu A$ |
| Output Short Circuit Current | $I_{OSD}$       |                                            |       | -5.7    | -8       | mA      |

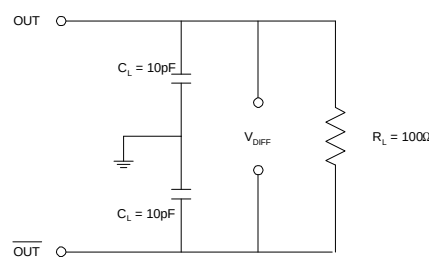
**6. LVDS Switching Characteristics**

| PARAMETERS                   | SYMBOL | CONDITIONS                                            | MIN. | TYP. | MAX. | UNITS |
|------------------------------|--------|-------------------------------------------------------|------|------|------|-------|
| Differential Clock Rise Time | $t_r$  | $R_L = 100\ \Omega$<br>$C_L = 10\ pF$<br>(see figure) | 0.2  | 0.7  | 1.0  | ns    |
| Differential Clock Fall Time | $t_f$  |                                                       | 0.2  | 0.7  | 1.0  | ns    |

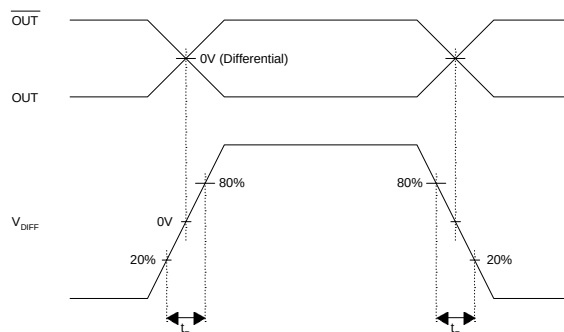
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



## 96MHz – 400MHz Low Phase Noise XO (for 12 – 25MHz Crystals)

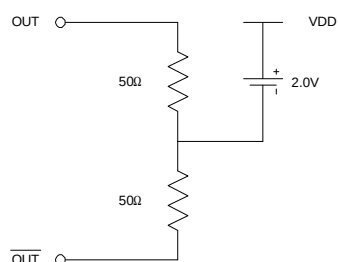
### 7. PECL Electrical Characteristics

| PARAMETERS          | SYMBOL   | CONDITIONS                                           | MIN.             | MAX.             | UNITS |
|---------------------|----------|------------------------------------------------------|------------------|------------------|-------|
| Output High Voltage | $V_{OH}$ | $R_L = 50 \Omega$ to $(V_{DD} - 2V)$<br>(see figure) | $V_{DD} - 1.025$ |                  | V     |
| Output Low Voltage  | $V_{OL}$ |                                                      |                  | $V_{DD} - 1.620$ | V     |

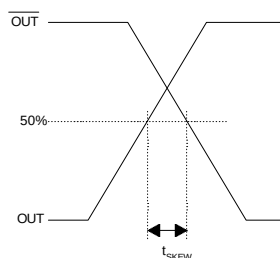
### 8. PECL Switching Characteristics

| PARAMETERS      | SYMBOL | CONDITIONS     | MIN. | TYP. | MAX. | UNITS |
|-----------------|--------|----------------|------|------|------|-------|
| Clock Rise Time | $t_r$  | @20/80% - PECL |      | 0.6  | 1.5  | ns    |
| Clock Fall Time | $t_f$  | @80/20% - PECL |      | 0.5  | 1.5  | ns    |

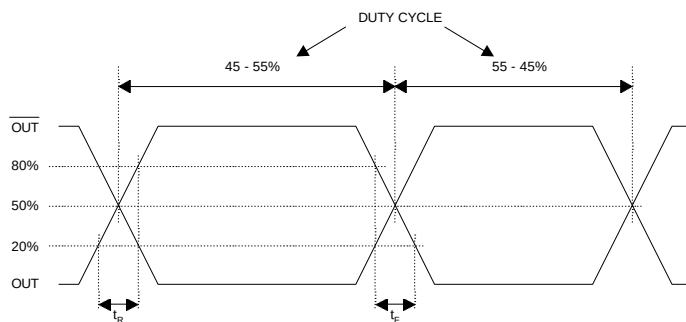
PECL Levels Test Circuit



PECL Output Skew



PECL Transistion Time Waveform



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**PAD ASSIGNMENT**

| Pad # | Name    | X (μm) | Y (μm) |
|-------|---------|--------|--------|
| 1     | GND     | 248    | 109    |
| 2     | GND     | 361    | 109    |
| 3     | GND     | 473    | 109    |
| 4     | GND     | 587    | 109    |
| 5     | GND     | 702    | 109    |
| 6     | N/C     | 874    | 109    |
| 7     | GND     | 1042   | 109    |
| 8     | GNDBUF  | 1171   | 109    |
| 9     | CMOS    | 1400   | 125    |
| 10    | LVDS    | 1400   | 259    |
| 11    | PECL    | 1400   | 476    |
| 12    | VDDBUF  | 1400   | 616    |
| 13    | VDDBUF  | 1400   | 716    |
| 14    | PECLB   | 1400   | 871    |
| 15    | LVDSB   | 1400   | 1089   |
| 16    | CMOSB   | 1400   | 1227   |
| 17    | GNDBUF  | 1389   | 1365   |
| 18    | OUTSEL1 | 1232   | 1365   |
| 19    | FSEL    | 1042   | 1365   |
| 20    | N/C     | 854    | 1365   |
| 21    | VDD     | 659    | 1365   |
| 22    | VDD     | 559    | 1365   |
| 23    | VDD     | 459    | 1365   |
| 24    | VDD     | 358    | 1365   |
| 25    | OUTSEL0 | 194    | 1365   |
| 26    | XIN     | 109    | 1223   |
| 27    | XOUT    | 109    | 1017   |
| 28    | N/C     | 109    | 858    |
| 29    | N/C     | 109    | 646    |
| 30    | OE      | 109    | 397    |
| 31    | N/C     | 109    | 181    |

**96MHz – 400MHz Low Phase Noise XO (for 12 – 25MHz Crystals)**

**ORDERING INFORMATION**

***For part ordering, please contact our Sales Department:***

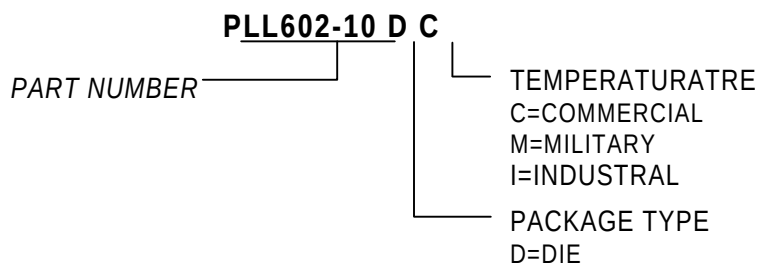
47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:

Device number, Package type and Operating temperature range



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