



# Dual Channel, 12-Bit 105 MSPS IF Sampling A/D Converter with Analog Input Signal Conditioning

## AD10200

### FEATURES

- Dual, 105 MSPS Minimum Sample Rate
- Channel-Channel Isolation, >80 dB
- AC-Coupled Signal Conditioning Included
- Gain Flatness up to Nyquist: < 0.2 dB
- Input VSWR 1.1:1 to Nyquist
- 80 dB Spurious-Free Dynamic Range
- Two's Complement Output Format
- 3.3 V or 5 V CMOS-Compatible Output Levels
- 0.850 W per Channel
- Industrial and Military Grade

### APPLICATIONS

- Radar IF Receivers
- Phased Array Receivers
- Communications Receivers
- Secure Communications
- GPS Antijamming Receivers
- Multichannel, Multimode Receivers

### PRODUCT DESCRIPTION

The AD10200 is a full channel ADC solution with on-module signal conditioning for improved dynamic performance and fully matched channel-to-channel performance. The module

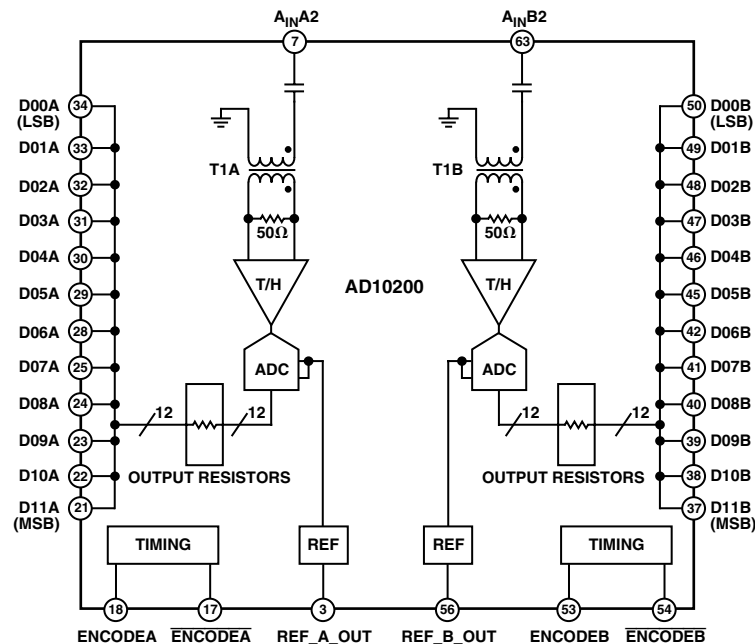
includes two wide-dynamic range ADCs. Each ADC has a transformer coupled front-end optimized for Direct-IF sampling. The AD10200 has on-chip track-and-hold circuitry, and utilizes an innovative architecture to achieve 12-bit, 105 MSPS performance. The AD10200 uses innovative high-density circuit design to achieve exceptional matching and performance while still maintaining excellent isolation, and providing for significant board area savings.

The AD10200 operates with 5.0 V supply for the analog-to-digital conversion. Each channel is completely independent allowing operation with independent encode and analog inputs. The AD10200 is packaged in a 68-lead ceramic chip carrier package. Manufacturing is done on Analog Devices, Inc. MIL-38534 Qualified Manufacturers Line (QML) and components are available up to Class-H (-55°C to +125°C).

### PRODUCT HIGHLIGHTS

- Guaranteed sample rate of 105 MSPS.
- Input signal conditioning with full power bandwidth to 250 MHz.
- Fully tested/characterized performance at 121 MHz  $A_{IN}$ .
- Optimized for IF sampling.

### FUNCTIONAL BLOCK DIAGRAM



REV. A

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# AD10200—SPECIFICATIONS<sup>1</sup> ( $V_{DD} = 3.3\text{ V}$ , $V_{CC} = 5.0\text{ V}$ ; ENCODE = 105 MSPS, unless otherwise noted)

| Parameter   | Temp | Test Level | MIL Subgroup | Min   | Typ              | Max    | Unit   |
|---|------|------------|--------------|-------|------------------|--------|--------|
| RESOLUTION  |      |            |              |       | 12               |        | Bits   |
| DC ACCURACY   |      |            |              |       |                  |        |        |
| Differential Nonlinearity                                       | Full | IV         | 12           | -0.99 | ±0.5             | +0.99  | LSB    |
| Integral Nonlinearity   | Full | IV         | 12           | -3    | ±0.75            | +3     | LSB    |
| No Missing Codes  | Full | I          | 1, 2, 3      |       | Guaranteed       |        |        |
| Gain Error <sup>2</sup>   | Full | I          | 1, 2, 3      | -9    | ±1               | +9     | % FS   |
| Output Offset   | Full | I          | 1, 2, 3      | -12   |                  | +12    | LSB    |
| ANALOG INPUT  |      |            |              |       |                  |        |        |
| Input Voltage Range   | 25°C | V          |              |       | 2.048            |        | V p-p  |
| Input Impedance   | 25°C | V          |              |       | 50               |        | Ω      |
| Input VSWR <sup>3</sup>   | Full | IV         | 12           |       | 1.1:1            | 1.25:1 | Ratio  |
| Analog Input Bandwidth, High                                    | Full | IV         | 12           | 200   | 250              |        | MHz    |
| Analog Input Bandwidth, Low                                     | Full | IV         | 12           | 1     |                  |        | MHz    |
| ANALOG REFERENCE  |      |            |              |       |                  |        |        |
| Output Voltage  | Full | I          | 1, 2, 3      | 2.4   | 2.5              | 2.6    | V      |
| Load Current  | 25°C | V          |              |       | 5                |        | mA     |
| Tempco  | Full | V          |              |       | 50               |        | ppm/°C |
| SWITCHING PERFORMANCE   |      |            |              |       |                  |        |        |
| Maximum Conversion Rate   | Full | I          | 4, 5, 6      | 105   |                  |        | MSPS   |
| Minimum Conversion Rate   | Full | IV         | 12           |       |                  | 10     | MSPS   |
| Duty Cycle  | Full | IV         | 12           | 45    | 50               | 55     | %      |
| Aperture Delay ( $t_A$ )  | 25°C | V          |              |       | 1.0              |        | ns     |
| Aperture Uncertainty (Jitter)                                   | 25°C | V          |              |       | 0.25             |        | ps rms |
| Output Valid Time ( $t_V$ ) <sup>4</sup>                        | Full | IV         | 12           | 3.0   | 5.3              |        | ns     |
| Output Propagation Delay ( $t_{PD}$ ) <sup>4</sup>              | Full | IV         | 12           | 4.5   | 5.5              | 8.0    | ns     |
| Output Rise Time ( $t_R$ )                                      | 25°C | V          | 12           |       | 3.5              |        | ns     |
| Output Fall Time ( $t_F$ )                                      | 25°C | V          | 12           |       | 3.3              |        | ns     |
| DIGITAL INPUTS  |      |            |              |       |                  |        |        |
| Encode Input Common Mode  | Full | IV         | 12           | 1.2   | 1.6              | 2.0    | V      |
| Differential Input (Enc, $\bar{\text{Enc}}$ )                   | Full | IV         | 12           | 0.4   |                  | 5.0    | V      |
| Logic "1" Voltage   | Full | IV         | 12           | 2.0   |                  |        | V      |
| Logic "0" Voltage   | Full | IV         | 12           |       |                  | 0.8    | V      |
| Input Resistance  | Full | IV         | 12           | 3     | 5                | 8      | kΩ     |
| Input Capacitance   | 25°C | V          |              |       | 4.5              |        | pF     |
| DIGITAL OUTPUTS   |      |            |              |       |                  |        |        |
| Logic "1" Voltage <sup>4</sup>                                  | Full | VI         | 1, 2, 3      | 3.1   | 3.3              |        | V      |
| Logic "0" Voltage <sup>4</sup>                                  | Full | VI         | 1, 2, 3      |       | 0                | 0.2    | V      |
| Output Coding   |      |            |              |       | Two's Complement |        |        |
| POWER SUPPLY <sup>5</sup>                                       |      |            |              |       |                  |        |        |
| Power Dissipation <sup>6</sup>                                  | Full | I          | 1, 2, 3      |       | 1800             | 2200   | mW     |
| Power Supply Rejection Ratio                                    | Full | IV         | 12           |       | ±0.5             | ±5     | mV/V   |
| I ( $DV_{DD}$ ) Current   | Full | I          | 1, 2, 3      |       | 25               | 40     | mA     |
| I ( $AV_{CC}$ ) Current   | Full | I          | 1, 2, 3      |       | 340              | 410    | mA     |
| DYNAMIC PERFORMANCE   |      |            |              |       |                  |        |        |
| Signal-to-Noise Ratio (SNR) <sup>7</sup><br>(Without Harmonics) |      |            |              |       |                  |        |        |
| $f_{IN} = 10\text{ MHz}$  | 25°C | V          |              |       | 67               |        | dBFS   |
|   | Full | V          |              |       | 66               |        | dBFS   |
| $f_{IN} = 41\text{ MHz}$  | 25°C | I          | 4            | 64    | 66.5             |        | dBFS   |
|   | Full | II         | 5, 6         | 62    | 65               |        | dBFS   |
| $f_{IN} = 71\text{ MHz}$  | 25°C | I          | 4            | 62.5  | 66.4             |        | dBFS   |
|   | Full | II         | 5, 6         | 61.5  | 64               |        | dBFS   |
| $f_{IN} = 121\text{ MHz}$                                       | 25°C | I          | 4            | 61    | 65               |        | dBFS   |
|   | Full | II         | 5, 6         | 61    | 64               |        | dBFS   |

| Parameter   | Temp | Test Level | MIL Subgroup | Min  | Typ  | Max | Unit |
|---|------|------------|--------------|------|------|-----|------|
| DYNAMIC PERFORMANCE                                     |      |            |              |      |      |     |      |
| (Continued)   |      |            |              |      |      |     |      |
| Signal-to-Noise Ratio (SINAD) <sup>8</sup>              |      |            |              |      |      |     |      |
| (With Harmonics)  |      |            |              |      |      |     |      |
| $f_{IN} = 10$ MHz                                       | 25°C | V          |              |      | 66   |     | dBFS |
|   | Full | V          |              |      | 63   |     | dBFS |
| $f_{IN} = 41$ MHz                                       | 25°C | I          | 4            | 63   | 65.5 |     | dBFS |
|   | Full | II         | 5, 6         | 60.5 | 63   |     | dBFS |
| $f_{IN} = 71$ MHz                                       | 25°C | I          | 4            | 61   | 63.5 |     | dBFS |
|   | Full | II         | 5, 6         | 57   | 60   |     | dBFS |
| $f_{IN} = 121$ MHz                                      | 25°C | I          | 4            | 56   | 58.5 |     | dBFS |
|   | Full | II         | 5, 6         | 53   | 55   |     | dBFS |
| Spurious Free Dynamic Range <sup>9</sup>                |      |            |              |      |      |     |      |
| $f_{IN} = 10$ MHz                                       | 25°C | V          |              |      | 81   |     | dBFS |
|   | Full | V          |              |      | 70   |     | dBFS |
| $f_{IN} = 41$ MHz                                       | 25°C | I          | 4            | 73   | 81   |     | dBFS |
|   | Full | II         | 5, 6         | 67.5 |      |     | dBFS |
| $f_{IN} = 71$ MHz                                       | 25°C | I          | 4            | 67   | 74   |     | dBFS |
|   | Full | II         | 5, 6         | 60   |      |     | dBFS |
| $f_{IN} = 121$ MHz                                      | 25°C | I          | 4            | 61   | 65   |     | dBFS |
|   | Full | II         | 5, 6         | 55.5 | 58   |     | dBFS |
| Two-Tone Intermodulation Distortion <sup>10</sup> (IMD) |      |            |              |      |      |     |      |
| $f_{IN} = 10$ MHz; $f_{IN} = 12$ MHz                    | 25°C | V          |              |      | 86   |     | dBc  |
|   | Full | V          |              |      | 81   |     | dBc  |
| $f_{IN} = 71$ MHz; $f_{IN} = 72$ MHz                    | 25°C | V          |              |      | 70   |     | dBc  |
|   | Full | V          |              |      | 65   |     | dBc  |
| $f_{IN} = 121$ MHz; $f_{IN} = 122$ MHz                  | 25°C | I          | 4            | 55.5 | 62   |     | dBc  |
|   | Full | II         | 5, 6         | 53   | 57   |     | dBc  |
| Channel-to-Channel Isolation <sup>11</sup>              |      |            |              |      |      |     |      |
| $f_{IN} = 121$ MHz                                      | Full | IV         | 12           | 80   | 85   |     | dB   |

## NOTES

<sup>1</sup>All ac specifications tested by driving ENCODE and  $\overline{\text{ENCODE}}$  differentially.

<sup>2</sup>Gain Error measured at 2.5 MHz.

<sup>3</sup>Input VSWR guaranteed 10 MHz to 200 MHz.

<sup>4</sup> $t_V$  and  $t_{PD}$  are measured from the transition points of the ENCODE input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of  $\pm 40$  mA.

<sup>5</sup>Supply voltages should remain stable within  $\pm 5\%$  for normal operation.

<sup>6</sup>Power dissipation measured with encode at rated speed and 0 dBm analog input.

<sup>7</sup>Analog Input signal power at -1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first 5 harmonic removed). Encode = 105 MSPS. SNR is reported in dBFS, related back to converter full scale.

<sup>8</sup>Analog Input signal power at -1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics. Encode = 105 MSPS. SINAD is reported in dBFS, related back to converter full scale.

<sup>9</sup>Analog Input signal equal -1 dBFS; SFDR is ratio of converter full scale to worst spur.

<sup>10</sup>Both input tones at -7 dBFS; two tone intermodulation distortion (IMD) rejection is the ratio of either tone to the worst third order intermod product.  $f_1 = x$  MHz  $\pm 100$  kHz,  $f_2 = x$  MHz  $\pm 100$  kHz.

<sup>11</sup>Channel-to-Channel isolation tested with A Channel/50  $\Omega$  terminated ( $A_{IN}A_2$ ) grounded and a full-scale signal applied to B Channel ( $A_{IN}B_2$ ).

Specifications subject to change without notice.

# AD10200

## ABSOLUTE MAXIMUM RATINGS<sup>1,2</sup>

|                              |                                   |
|------------------------------|-----------------------------------|
| V <sub>DD</sub>              | 6 V                               |
| V <sub>CC</sub>              | 6 V                               |
| Analog Inputs                | 5 V <sub>p-p</sub> (18 dBm)       |
| Digital Inputs               | -0.5 V to V <sub>DD</sub> + 0.5 V |
| Digital Output Current       | 20 mA                             |
| Operating Temperature        | -55°C to +125°C                   |
| Storage Temperature          | -65°C to +150°C                   |
| Maximum Junction Temperature | 175°C                             |
| Maximum Case Temperature     | 150°C                             |

### NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

<sup>2</sup>Typical thermal impedances for “Z” package:

$$\theta_{JC} = 2.22^{\circ}\text{C}/\text{W}; \theta_{JA} = 24.3^{\circ}\text{C}/\text{W}.$$

## EXPLANATION OF TEST LEVELS

### Test Level

- I. 100% production tested.
- II. 100% production tested at 25°C and sample tested at specific temperatures.
- III. Sample tested only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.
- VI. 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range.

**Table I. Output Coding (VREF = 2.5 V) (Two’s Complement)**

| Code  | A <sub>IN</sub> (V) | Digital Output |
|-------|---------------------|----------------|
| +2047 | +1.024              | 0111 1111 1111 |
| •     | •                   | •              |
| •     | •                   | •              |
| 0     | 0                   | 0000 0000 0000 |
| -1    | -0.00049            | 1111 1111 1111 |
| •     | •                   | •              |
| •     | •                   | •              |
| -2048 | -1.024              | 1000 0000 0000 |

## ORDERING GUIDE

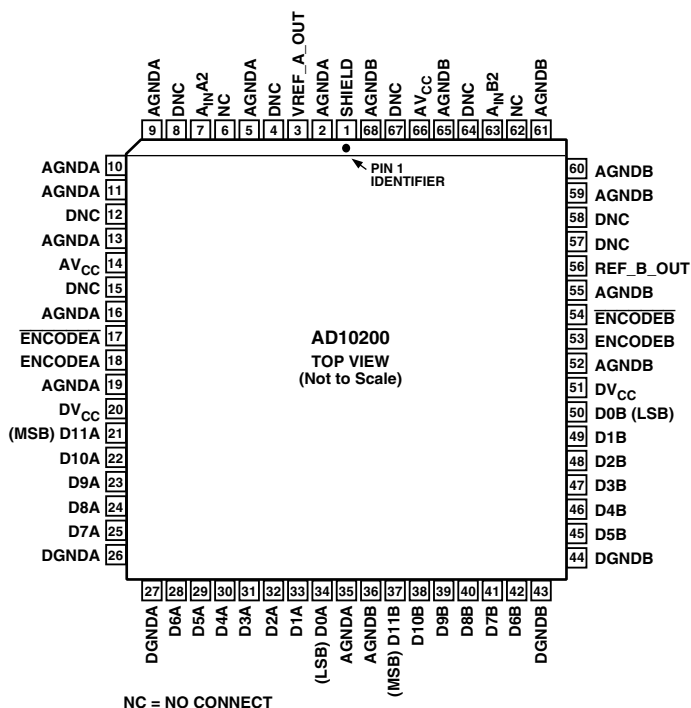
| Model           | Temperature Range      | Package Description                 | Package Option |
|-----------------|------------------------|-------------------------------------|----------------|
| AD10200BZ       | -40°C to +85°C (Case)  | 68-Lead Ceramic Leaded Chip Carrier | Z-68B          |
| 5962-9961002HXA | -40°C to +85°C (Case)  | 68-Lead Ceramic Leaded Chip Carrier | Z-68B          |
| 5962-9961001HXA | -55°C to +125°C (Case) | 68-Lead Ceramic Leaded Chip Carrier | Z-68B          |
| AD10200/PCB     |                        | Evaluation Board with AD10200BZ     |                |

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD10200 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION



## PIN FUNCTION DESCRIPTIONS

| Pin No.                      | Mnemonic                    | Function   |
|------------------------------|-----------------------------|--|
| 1                            | SHIELD                      | Internal Ground Shield between Channels  |
| 2, 5, 9–11, 13, 16, 19, 35   | AGNDA                       | A Channel Analog Ground. A and B grounds should be connected as close to the device as possible. |
| 3                            | VREF_A_OUT                  | A Channel Internal Voltage Reference   |
| 6, 62                        | NC                          | No Connection  |
| 7                            | A <sub>IN</sub> A2          | Analog Input for A Side ADC  |
| 4, 8, 12, 15, 57, 58, 64, 67 | DNC                         | Do Not Connect   |
| 14, 66                       | AV <sub>CC</sub>            | Analog Positive Supply Voltage (Nominally 5.0 V)   |
| 17                           | $\overline{\text{ENCODEA}}$ | Complement of Encode   |
| 18                           | ENCODEA                     | Data conversion initiated on the rising edge of ENCODE input.                                    |
| 20                           | DV <sub>CC</sub>            | Digital Positive Supply Voltage (Nominally 3.3 V)  |
| 21–25, 28–34                 | D11A–D7A,<br>D6A–D0A        | Digital Outputs for ADC A. D0 (LSB)  |
| 26, 27                       | DGNDA                       | A Channel Digital Ground   |
| 36, 52, 55, 59–61, 65, 68    | AGNDB                       | B Channel Analog Ground. A and B grounds should be connected as close to the device as possible. |
| 37–42, 45–50                 | D11B–D6B,<br>D5B–D0B        | Digital Outputs for ADC B. D0 (LSB)  |
| 43, 44                       | DGNDB                       | B Channel Digital Ground   |
| 51                           | DV <sub>CC</sub>            | Digital Positive Supply Voltage (Nominally 3.3 V)  |
| 53                           | ENCODEB                     | Data conversion initiated on rising edge of ENCODE input.  |
| 54                           | $\overline{\text{ENCODEB}}$ | Complement of Encode   |
| 56                           | VREF_B_OUT                  | B Channel Internal Voltage Reference   |
| 63                           | A <sub>IN</sub> B2          | Analog Input for B Side ADC  |

# AD10200

## DEFINITION OF SPECIFICATIONS

### Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

### Aperture Delay

The delay between the 50% point on the rising edge of the ENCODE command and the instant at which the analog input is sampled.

### Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

### Differential Nonlinearity

The deviation of any code from an ideal 1 LSB step.

### Encode Pulsewidth/Duty Cycle

Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in Logic “1” state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. At a given clock rate, these specs define an acceptable Encode duty cycle.

### Harmonic Distortion

The ratio of the rms signal amplitude to the rms value of the worst harmonic component.

### Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a “best straight line” determined by a least square curve fit.

### Minimum Conversion Rate

The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

### Maximum Conversion Rate

The encode rate at which parametric testing is performed.

### Output Propagation Delay

The delay between the 50% point of the rising edge of ENCODE command and the time when all output data bits are within valid logic levels.

### Overvoltage Recovery Time

The amount of time required for the converter to recover to 0.02% accuracy after an analog input signal of the specified percentage of full scale is reduced to midscale.

### Power Supply Rejection Ratio

The ratio of a change in output offset voltage to a change in power supply voltage.

### Signal-to-Noise-and-Distortion (SINAD)

The ratio of the rms signal amplitude (set a 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc. [May be reported in dBc (i.e., degrades as signal levels is lowered) or in dBFS (always related back to converter full scale)].

### Signal-to-Noise Ratio (without Harmonics)

The ratio of the rms signal amplitude (set a 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc. [May be reported in dBc (i.e., degrades as signal levels is lowered) or in dBFS (always related back to converter full scale).]

### Spurious-Free Dynamic Range

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. [May be reported in dBc (i.e., degrades as signal levels is lowered) or in dBFS (always related back to converter full scale).]

### Transient Response

The time required for the converter to achieve 0.02% accuracy when a one-half full-scale step function is applied to the analog input.

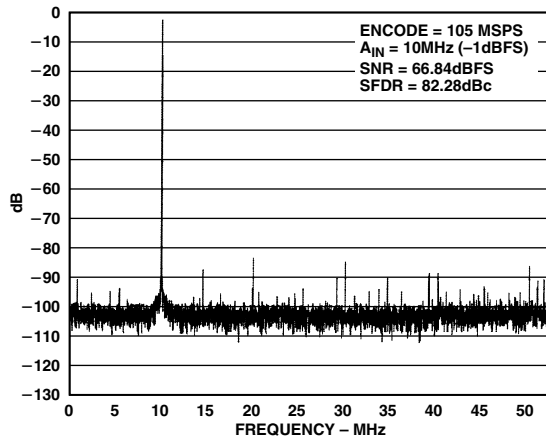
### Two-Tone Intermodulation Distortion Rejection

The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

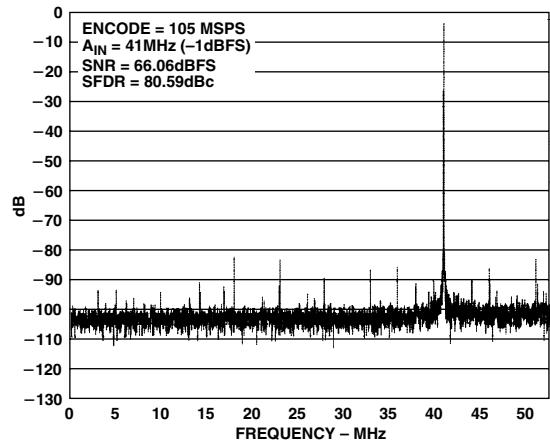
### Voltage Standing-Wave Ratio (VSWR)

The ratio of the amplitude of the electric field at a voltage maximum to that at an adjacent voltage minimum.

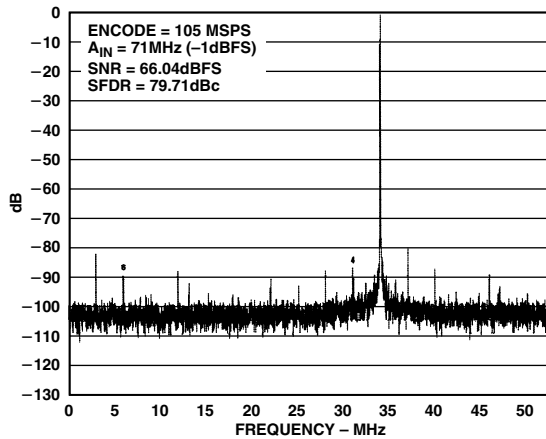
# Typical Performance Characteristics—AD10200



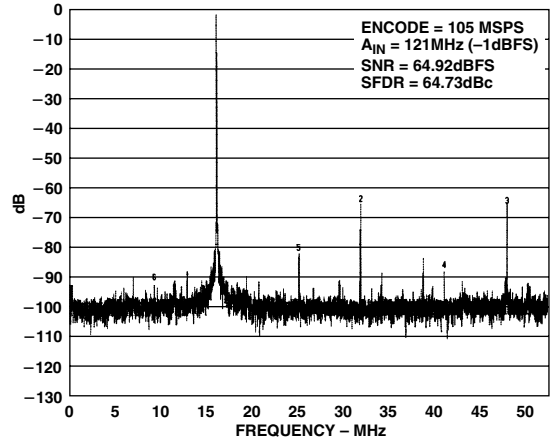
TPC 1. Single Tone @ 10 MHz



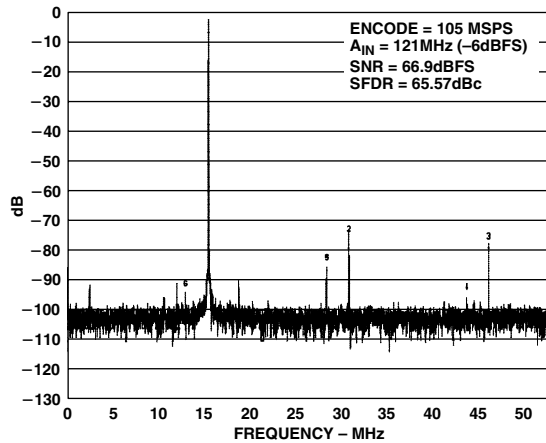
TPC 4. Single Tone @ 41 MHz



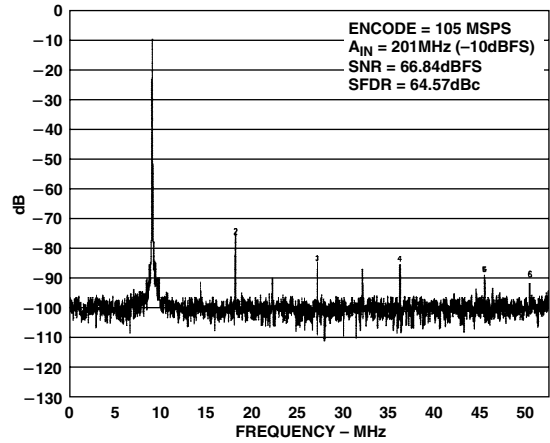
TPC 2. Single Tone @ 71 MHz



TPC 5. Single Tone @ 121 MHz

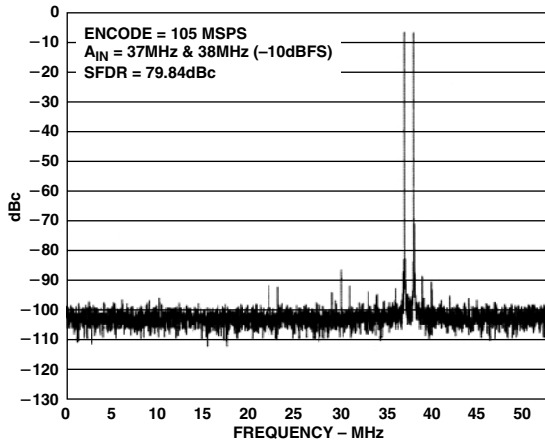


TPC 3. Single Tone @ 121 MHz

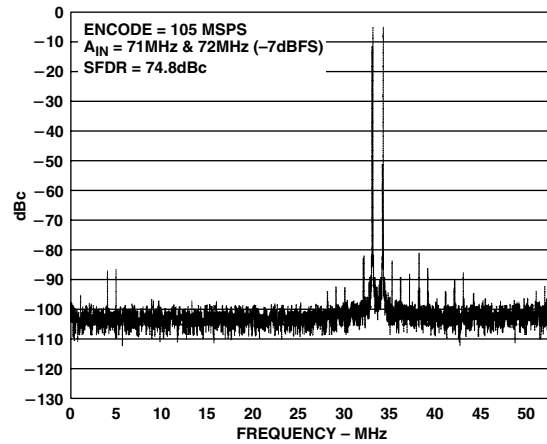


TPC 6. Single Tone @ 201 MHz

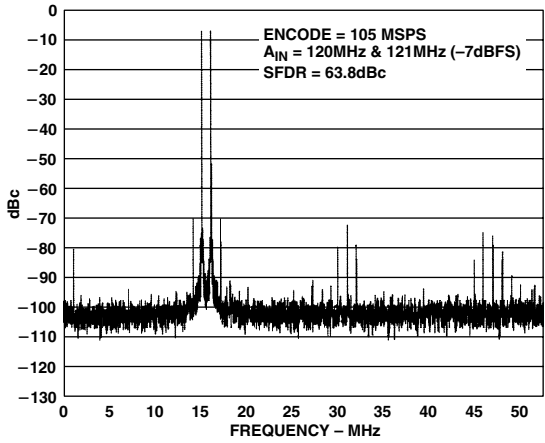
# AD10200



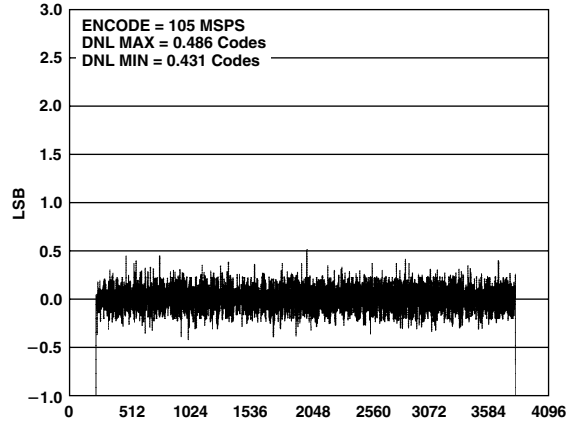
TPC 7. Two-Tone @ 37 MHz/38 MHz



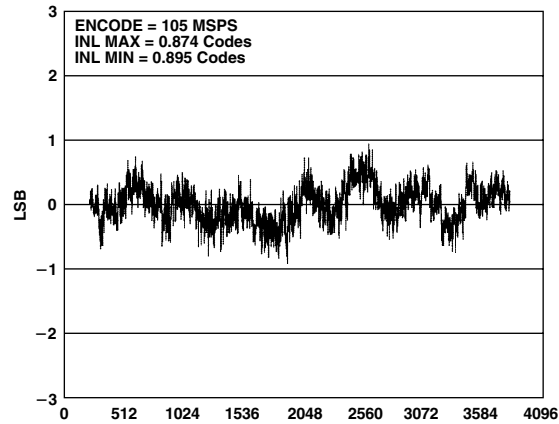
TPC 10. Two-Tone @ 71 MHz/72 MHz



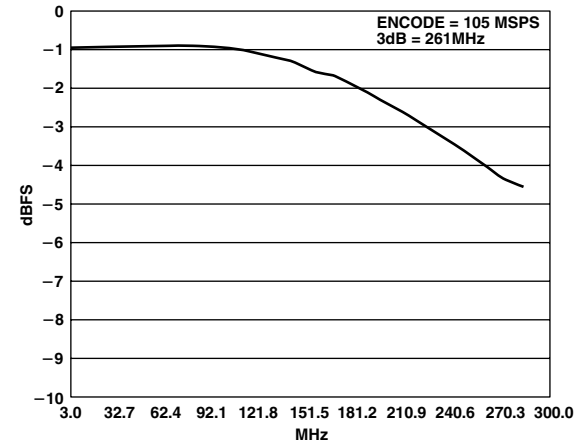
TPC 8. Two-Tone @ 120 MHz/121 MHz



TPC 11. Differential Nonlinearity

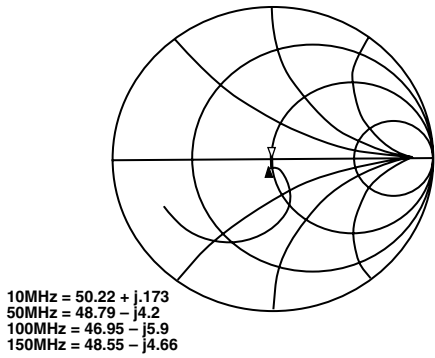


TPC 9. Integral Nonlinearity

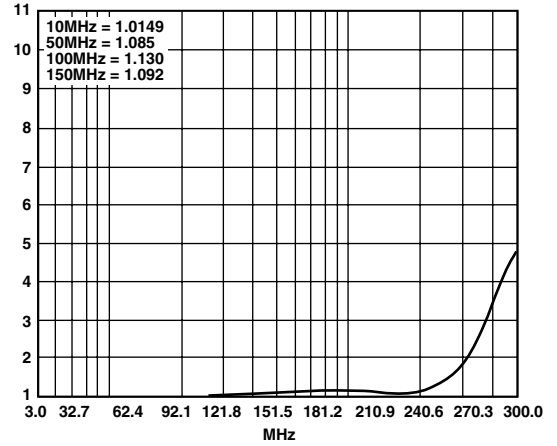


TPC 12. Gain Flatness





TPC 13. Input Impedance S11



TPC 14. Voltage Standing Wave Ratio (VSWR)

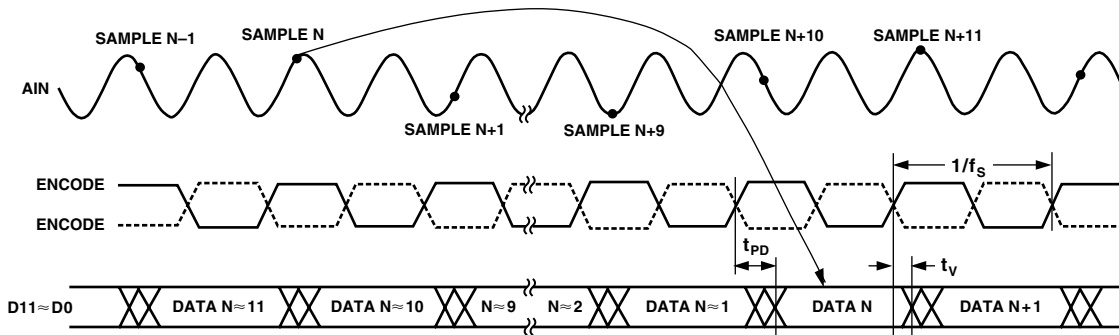


Figure 1. Timing Diagram

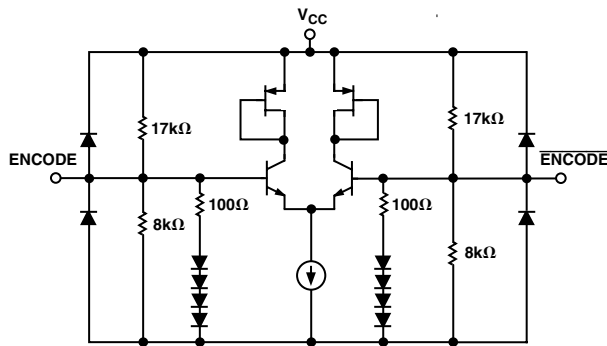


Figure 2. Equivalent Encode Input Circuit

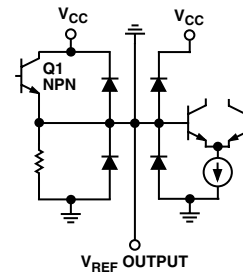


Figure 4. Equivalent Voltage Reference Output Circuit

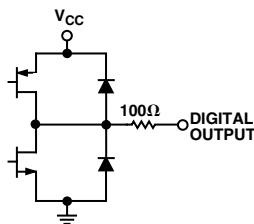


Figure 3. Equivalent Digital Output Circuit

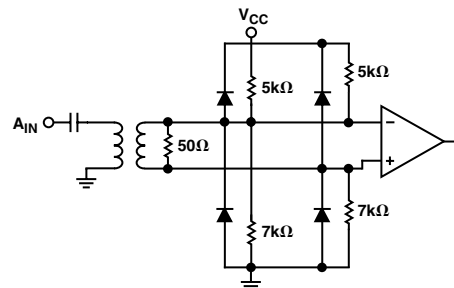


Figure 5. Equivalent Analog Input Circuit

# AD10200

## APPLICATION NOTES

### Theory of Operation

The AD10200 is a high-dynamic range dual 12-bit, 105 MHz subrange pipeline converter that uses switched capacitor architecture. The analog input section uses  $A_{IN}A2/A_{IN}B2$  at 2.048 V p-p with an input impedance of 50  $\Omega$ . The analog input includes an ac-coupled wide-band 1:1 transformer, which provides high-dynamic range and SNR while maintaining VSWR and gain flatness. The ADC includes a high-bandwidth linear track/hold that gives excellent spurious performance up to and beyond the Nyquist rate. The high-bandwidth track/hold has a low jitter of 0.25 ps rms, leading to excellent SNR and SFDR performance. AC-coupled differential PECL/ECL encode inputs are recommended for optimum performance.

### USING THE AD10200

#### ENCODE Input

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track/hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD10200, and the user is advised to give commensurate thought to the clock source. The ENCODE input are fully TTL/CMOS compatible. For optimum performance, the AD10200 must be clocked differentially.

Note that the ENCODE inputs cannot be driven directly from PECL level signals ( $V_{IHD}$  is 3.5 V max). PECL level signals can easily be accommodated by ac coupling as shown in Figure 6. Good performance is obtained using an MC10EL16 in the circuit to drive the encode inputs.

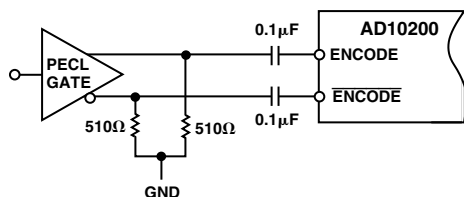


Figure 6. AC Coupling to ENCODE Inputs

#### ENCODE Voltage Level Definition

The voltage level definitions for driving ENCODE and  $\overline{\text{ENCODE}}$  in differential mode are shown in Figure 7.

#### ENCODE Inputs

|   |                           |
|---|---------------------------|
| Differential Signal Amplitude ( $V_{ID}$ )    | 500 mV min,<br>750 mV nom |
| High Differential Input Voltage ( $V_{IHD}$ ) | 5.0 V max                 |
| Low Differential Input Voltage ( $V_{ILD}$ )  | 0 V min                   |
| Common-Mode Input ( $V_{ICM}$ )               | 1.25 V min, 1.6 V nom     |

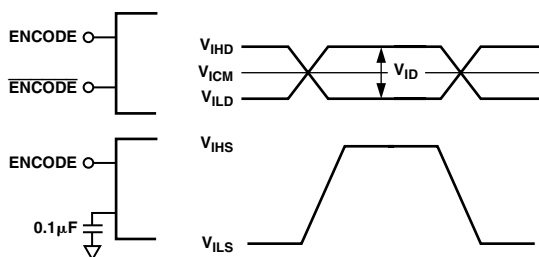


Figure 7. Differential Input Levels

Often, the cleanest clock source is a crystal oscillator producing a pure sine wave. In this configuration, or with any roughly symmetrical clock input, the input can be ac-coupled and biased to a reference voltage that also provides the ENCODE. This ensures that the reference voltage is centered on the encode signal.

#### Digital Outputs

The digital outputs are TTL/CMOS-compatible and a separate output power supply pin supports interfacing with 3.3 V logic.

#### Analog Input

The analog input is a single ended ac-coupled high performance 1:1 transformer with an input impedance of 50  $\Omega$  to 105 MHz. The nominal full scale input is 2.048 V p-p.

Special care was taken in the design of the analog input section of the AD10200 to prevent damage and corruption of data when the input is overdriven.

#### Voltage Reference

A stable and accurate 2.5 V voltage reference is designed into the AD10200 (VREFOUT). An external voltage reference is not required.

#### Timing

The AD10200 provides latched data outputs, with 10 pipeline delays. Data outputs are available one propagation delay ( $t_{PD}$ ) after the rising edge of the encode command (see Figure 1). The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD10200; these transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate of the AD10200 is 10 MSPS. At internal clock rates below 10 MSPS, dynamic performance may degrade. Therefore, input clock rates below 10 MHz should be avoided.

## GROUNDING AND DECOUPLING

### Analog and Digital Grounding

Proper grounding is essential in any high speed, high resolution system. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power schemes. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling to the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path and manage the power and ground currents. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

### LAYOUT INFORMATION

The schematic of the evaluation board (Figure 8) represents a typical implementation of the AD10200. The pinout of the AD10200 is very straightforward and facilitates ease of use and the implementation of high frequency/high resolution design practices. It is recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. All capacitors can be standard high quality ceramic chip capacitors.

Care should be taken when placing the digital output runs. Because the digital outputs have such a high-slew rate, the capacitive loading on the digital outputs should be minimized. Circuit traces for the digital outputs should be kept short and connect directly to the receiving gate. Internal circuitry buffers the outputs of the ADC through a resistor network to eliminate the need to externally isolate the device from the receiving gate.

### EVALUATION BOARD

The AD10200 evaluation board (Figure 9) is designed to provide optimal performance for evaluation of the AD10200 analog-to-digital converter. The board encompasses everything needed to ensure the highest level of performance for evaluating the AD10200. The board requires an analog input signal, encode clock and power supply inputs. The clock is buffered on-board to provide clocks for the latches. The digital outputs and out clocks are available at the standard 40-pin connectors J1 and J2.

Power to the analog supply pins is connected via banana jacks. The analog supply powers the associated components and the analog section of the AD10200. The digital outputs of the AD10200 are powered via banana jacks with 3.3 V. Contact the factory if additional layout or applications assistance is required.

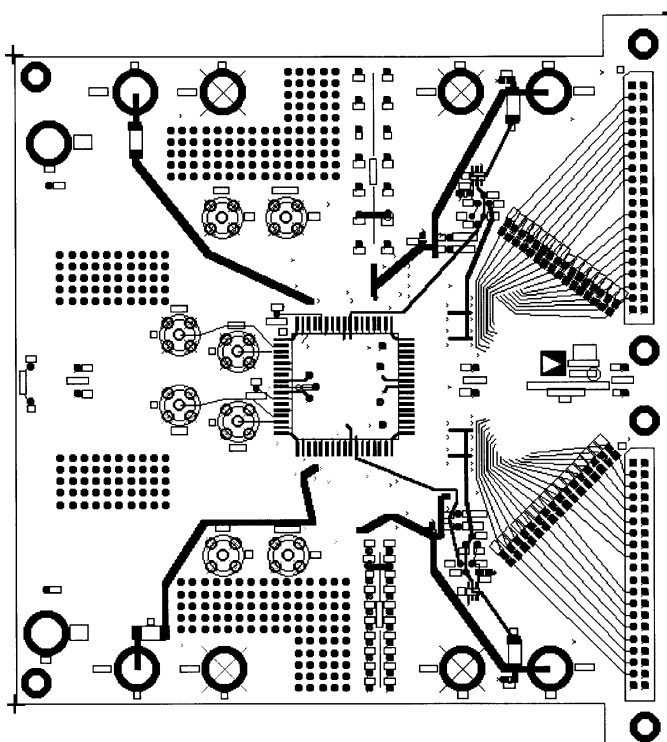


Figure 8. Evaluation Board Mechanical Layout

# AD10200

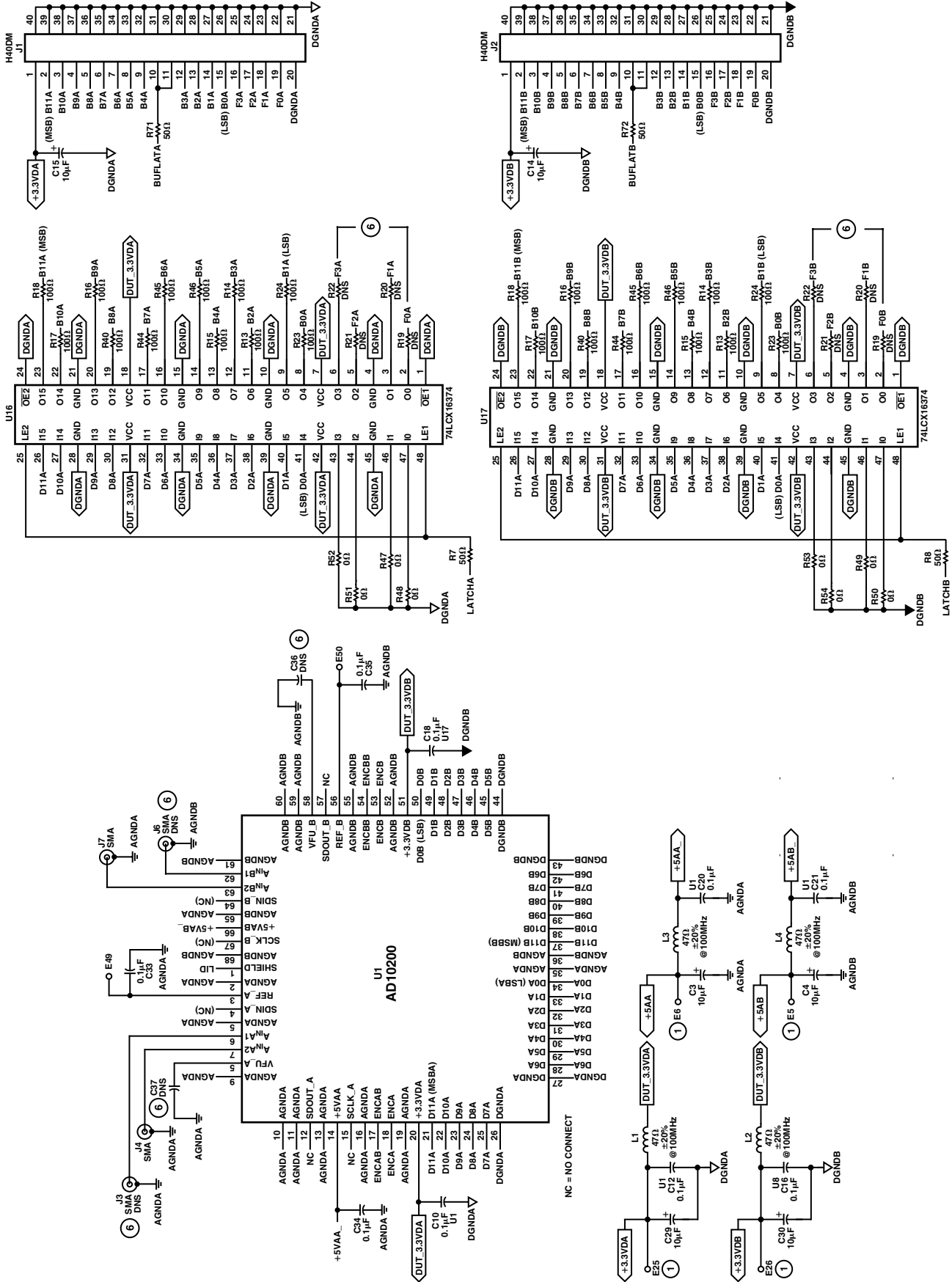


Figure 9a. Evaluation Board

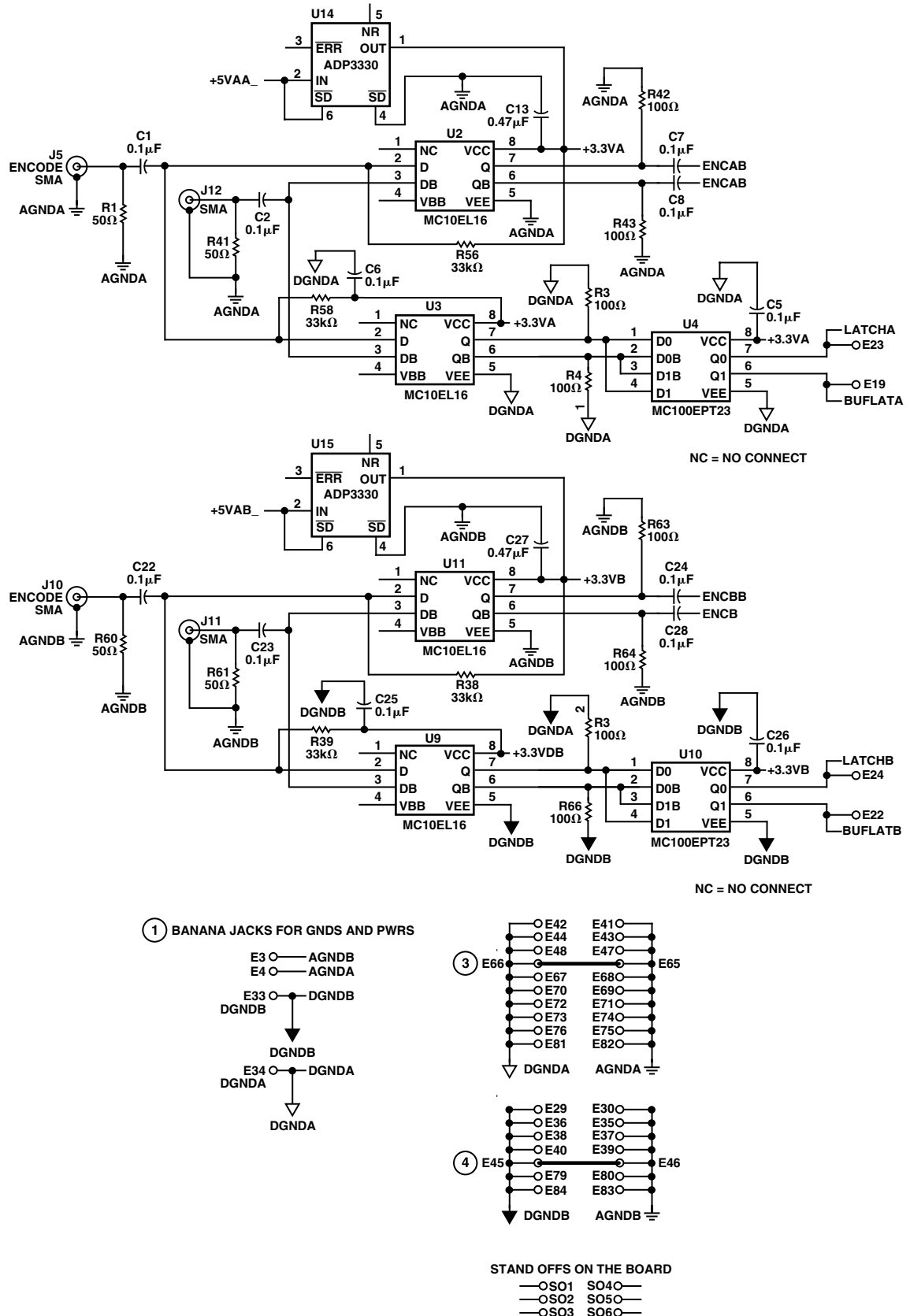


Figure 9b. Evaluation Board

# AD10200

## BILL OF MATERIALS LIST FOR AD10200 EVAL BOARD

| Qty. | Component Name | Ref Des  | Value         | Description                               | M/S P/Ns                               |
|------|----------------|--|---------------|---|--|
| 2    | 74LCX16373MTD  | U16, U17   |               |   | 74LCX16374MTD (Fairchild)              |
| 1    | AD10200BZ      | U1   |               |   | AD10200BZ                              |
| 2    | ADP3330        | U14, U15   |               | SM 3.3 V Regulator                        | ADP3330ART-3.3-RL7 (Analog)            |
| 4    | BRES0805       | R38, R39, R56, R58   | 33 k $\Omega$ | SM 0805 Resistor                          | ERJ6GEYJ333V (Panasonic)               |
| 4    | BRES0805       | R1, R41, R60,<br>R61   | 50 $\Omega$   | SM 0805 Resistor                          | ERJ6GEYJ510V (Panasonic)               |
| 8    | BRES0805       | R3, R4, R42, R43,<br>R63, R64, R65, R66  | 100 $\Omega$  | SM 0805 Resistor                          | ERJ6GEYJ101V (Panasonic)               |
| 23   | CAP2           | C1, C2, C5, C6,<br>C7, C8, C9, C10,<br>C12, C16, C17, C18,<br>C20, C21, C22, C23,<br>C24, C25, C26, C28,<br>C33, C34, C35            | 0.1 $\mu$ F   | SM 0805 Capacitor                         | GRM40X7R104K025BL<br>(MENA)            |
| 4    | CAP2           | C13, C27, C38, C39   | 0.47 $\mu$ F  | SM 1206 Capacitor                         | VJ1206U474MFXMB<br>(VITRAMON)          |
| 2    | N49DM          | J1, J2   |               | 2 $\times$ 20 $\times$ 100 Male Connector | TSW-120-08G-D (Samtec)                 |
| 4    | IND2           | L1, L2, L3, L4   | 47 $\Omega$   | Inductor                                  | 2743019447 (Fair Ride)                 |
| 4    | MC10EL16       | U2, U3 U9, U11   |               |   | MC1016EP16D (Motorola)                 |
| 10   | BJACK          | BJ1 – BJ10   |               | POWER JACK                                | 108-0740-001 (Johnson Comp.)           |
| 2    | MC100ELT23     | U4, U10  |               |   | SY100ELT23L (Micrel-Synergy)           |
| 6    | POLCAP2        | C3, C4, C14, C15,<br>C29, C30  | 10 $\mu$ F    | SM 1812 Polar Capacitor                   | T491C106M016A57280<br>(KEMET)          |
| 8    | RES2           | R47, R48, R49,<br>R50, R51, R52,<br>R53, R54   | 0 $\Omega$    | SM 0805 Resistor                          | ERJ-6GEY0R00V (Panasonic)              |
| 4    | RES4           | R7, R8, R71, R72   | 50 $\Omega$   | SM 0805 Resistor                          | ERJ-6GEYJ510V (Panasonic)              |
| 24   | RES2           | R9, R10, R11, R12,<br>R13, R14, R15, R16,<br>R17, R18, R23, R24,<br>R25, R26, R27, R28,<br>R29, R30, R35, R36,<br>R40, R44, R45, R46 |               |   |  |
| 1    | SMA            | J4   |               | A <sub>IN</sub> A2                        | 142-0701-201 (Johnson Comp.)           |
| 1    | SMA            | J7   |               | A <sub>IN</sub> B2                        | 142-0701-201 (Johnson Comp.)           |
| 2    | SMA            | J11, J12   |               | $\overline{\text{ENCODE}}$                | 142-0701-201 (Johnson Comp.)           |
| 2    | SMA            | J5, J10  |               | ENCODE                                    | 142-0701-201 (Johnson Comp.)           |
| 4    | Stand-Off      | S01–S04  |               | Stand-Off                                 | 313-2477-016 (Johnson Comp.)           |
| 4    | Screws         |  |               | Screws (Stand-Off)                        | MPMS 0040005PH (Building<br>Fasteners) |
| 1    | PCB            |  |               | AD10200 Eval Board                        | GS03363 Rev. A                         |

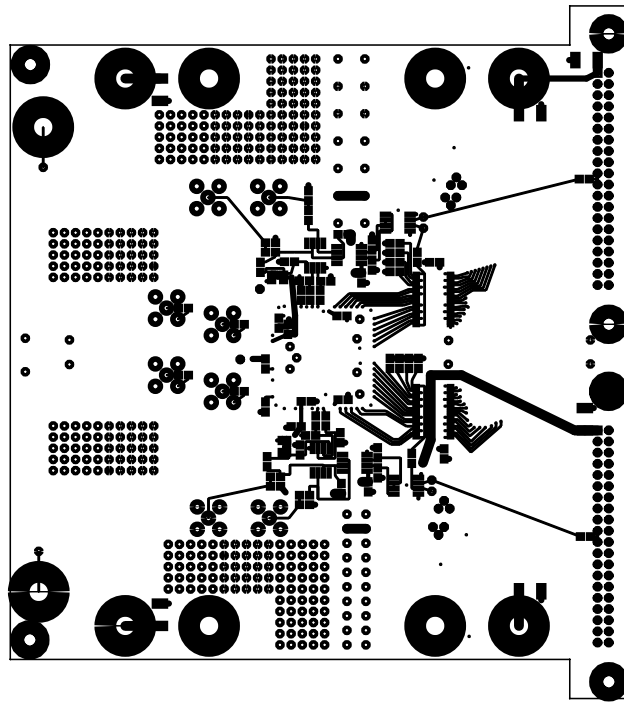


Figure 10a. Bottom View

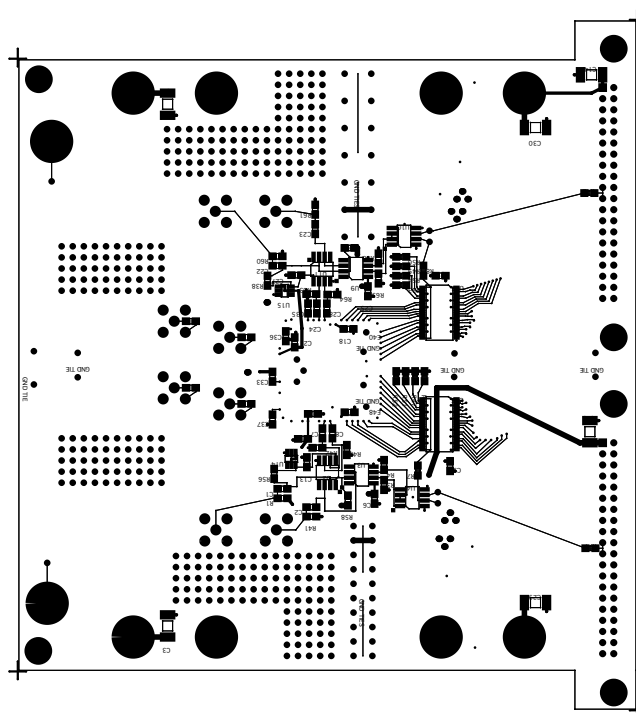


Figure 10b. Bottom Assembly

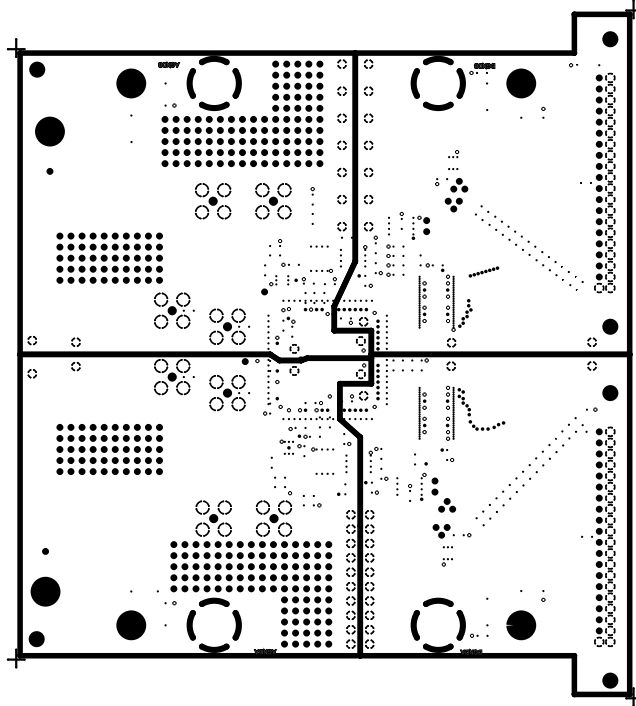


Figure 10c. Ground 1

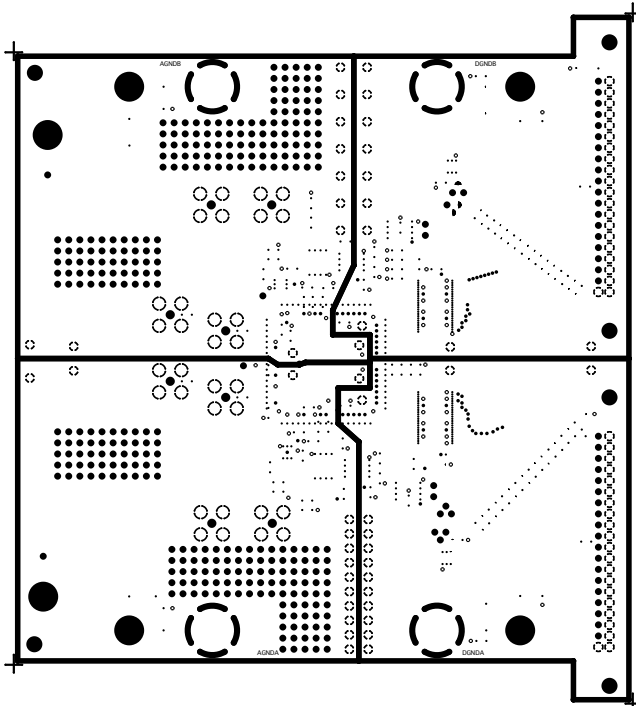


Figure 10d. Ground 2



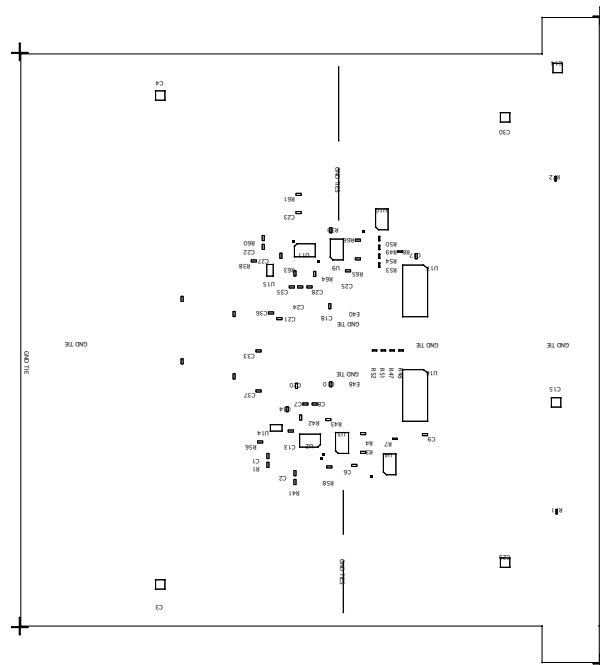


Figure 10e. Bottom Silk

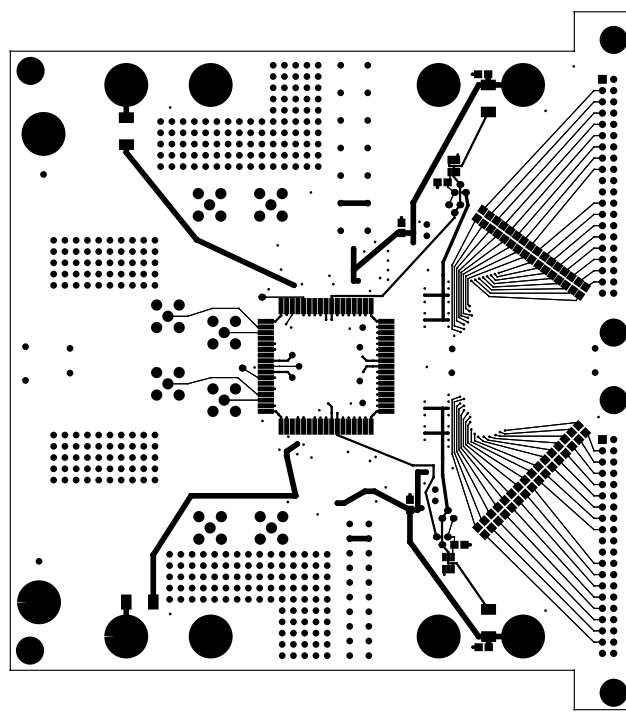


Figure 10f. Top View

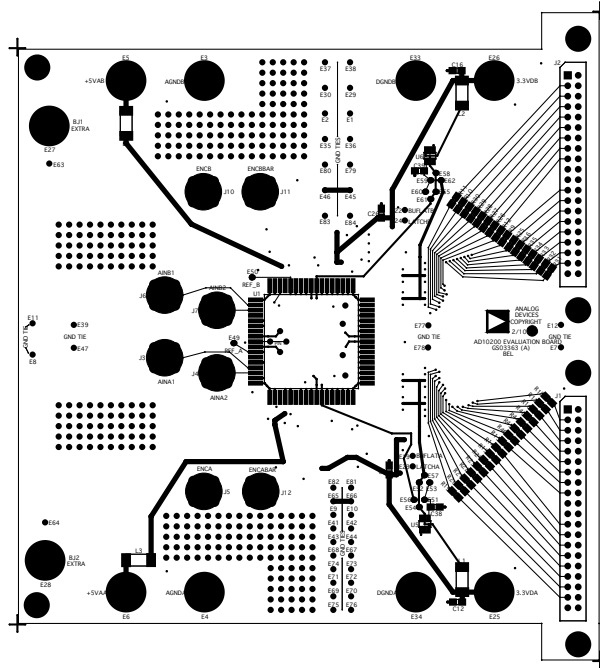


Figure 10g. Top Assembly

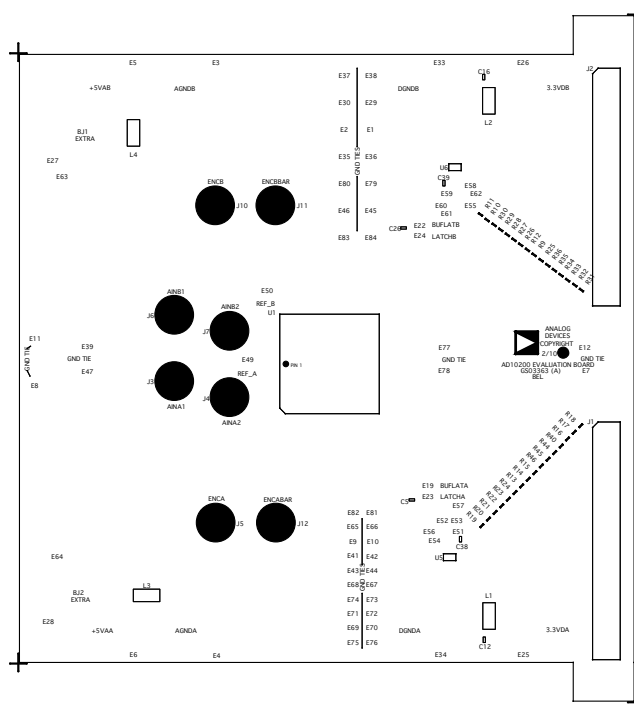
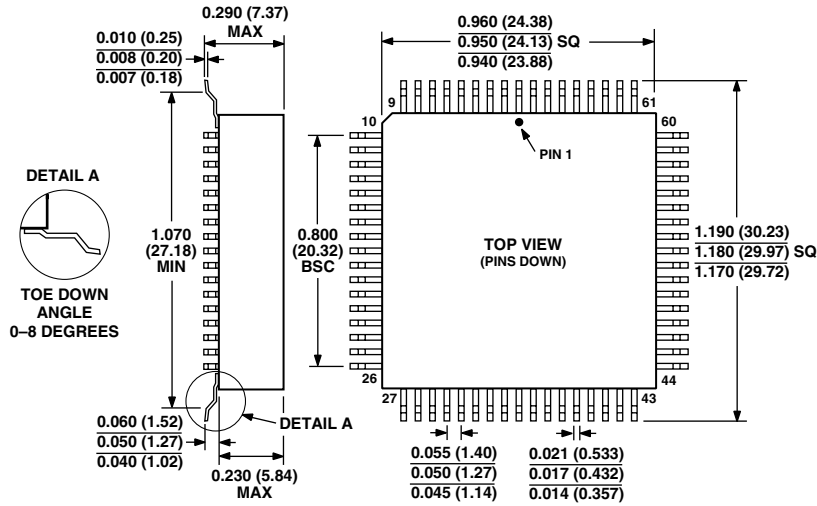


Figure 10h. Top Silk

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

68-Lead Ceramic Leaded Chip Carrier  
(Z-68B)



Revision History

| Location   | Page |
|--|------|
| <b>Data Sheet changed from REV. 0 to REV. A.</b> |      |
| Edit to ABSOLUTE MAXIMUM RATINGS .....           | 4    |
| Edit to Figure 5 .....                           | 9    |
| Edit to ENCODE Inputs section .....              | 10   |
| Edit to Figure 9a .....                          | 12   |



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