NXP Semiconductors
Technical Data

Document Number: MC10XS3425
Rev. 6.0, 8/2018

Quad high-side switch (dual 10 mOhm, dual 25 mOhm)

The 10XS3425 is one in a family of devices designed for low-voltage automotive lighting applications. Its four low $R_{DS(on)}$ MOSFETs (dual 10 mΩ/dual 25 mΩ) can control four separate 55 W/28 W bulbs, and/or Xenon modules, and/or LEDs.

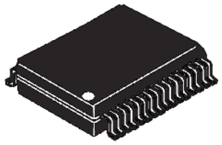
Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew-rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control if desired. The 10XS3425 allows the user to program via the SPI the fault current trip levels and duration of acceptable lamp inrush. The device has Fail-safe mode to provide fail-safe functionality of the outputs in case of MCU damaged. This device is powered by SMARTMOS technology.

Features

- Four protected 10 mΩ and 25 mΩ high-side switches (at 25 °C)
- Operating voltage range of 6.0 to 20 V with sleep current < 5.0 µA, extended mode from 4.0 to 28 V
- 8.0 MHz 16-bit 3.3 V and 5.0 V SPI control and status reporting with daisy chain capability
- PWM module using external clock or calibratable internal oscillator with programmable output delay management
- Smart overcurrent shutdown, severe short-circuit, overtemperature protections with time limited autoretry, and fail-safe mode, in case of MCU damage
- Output off or on openload detection compliant to bulbs or leds and short to battery detection, analog current feedback with selectable ratio and board temperature feedback

10XS3425

HIGH-SIDE SWITCH



EK SUFFIX (PB-FREE)
98ASA00368D
32-PIN EXPOSED PAD SOIC

Applications

- Low-voltage automotive exterior lighting
- Low-voltage industrial lighting
- Halogen lamps
- Incandescent bulbs
- Light-emitting diodes (LEDs)
- HID Xenon ballasts

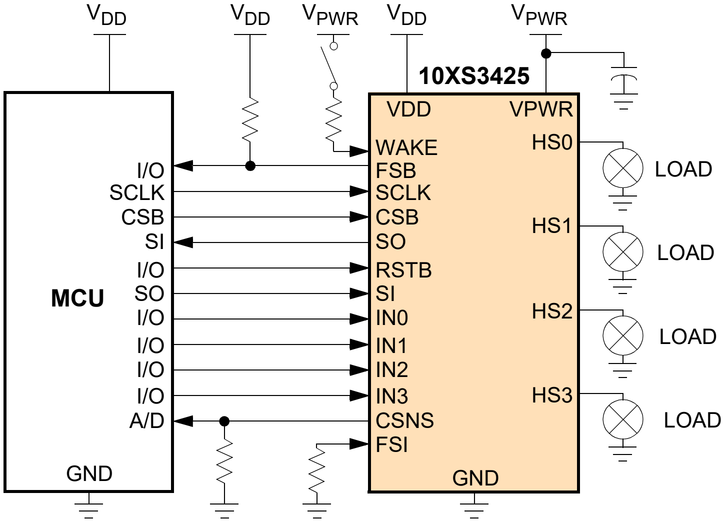


Figure 1. 10XS3425 simplified application diagram

Table of Contents

1 Orderable parts

This section describes the part numbers available to be purchased along with their differences.

Table 1. Orderable part variations

Part number (1)	Temperature (T_A)	Package
Quad version		
MC10XS3425EK	-40 to 125 °C	32-pin SOIC exposed pad

Notes

1. To order parts in tape and reel, add the R2 suffix to the part number.

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com and perform a part number search.

2 Internal block diagram

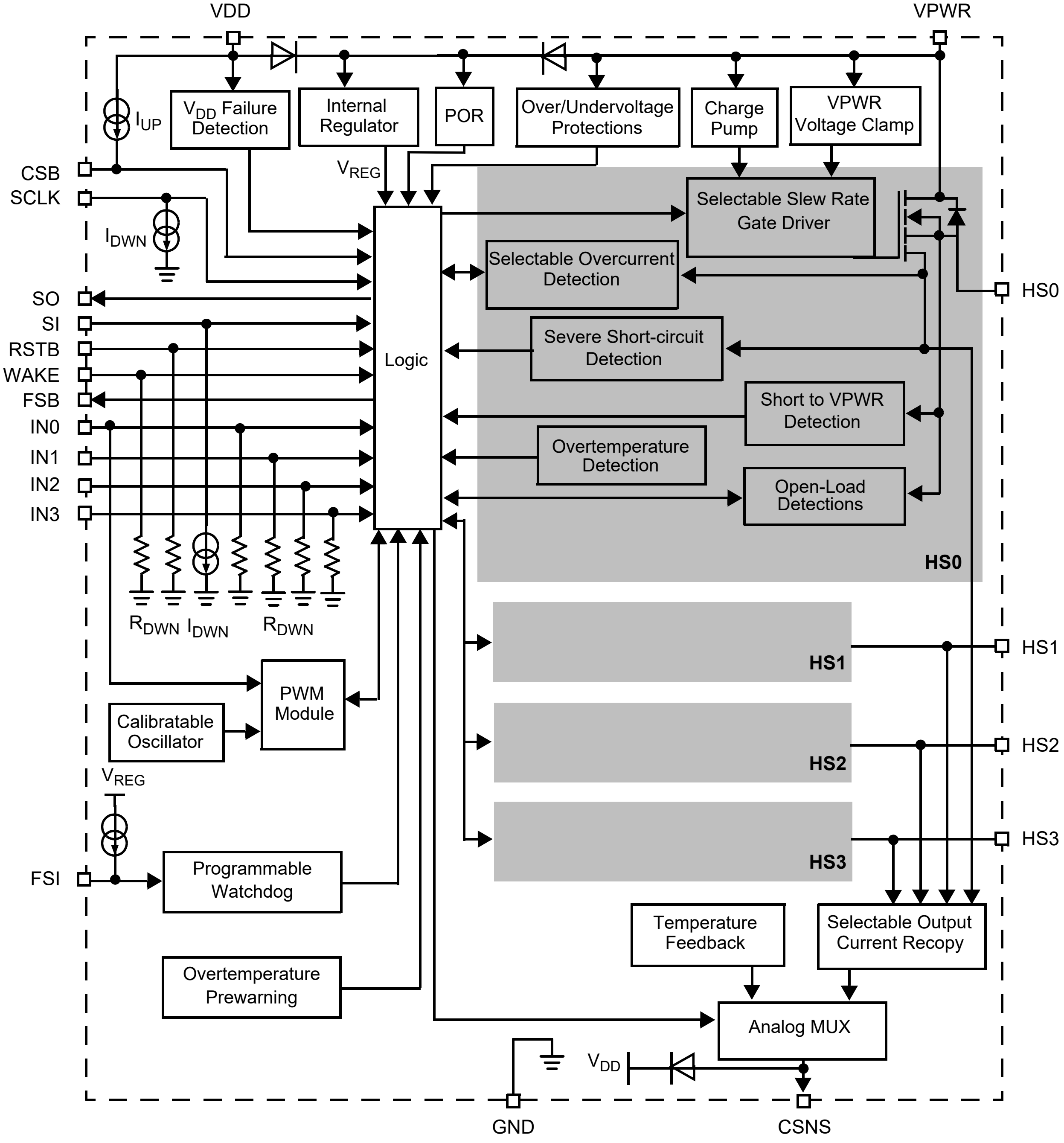


Figure 2. 10XS3425 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

Transparent top view of package

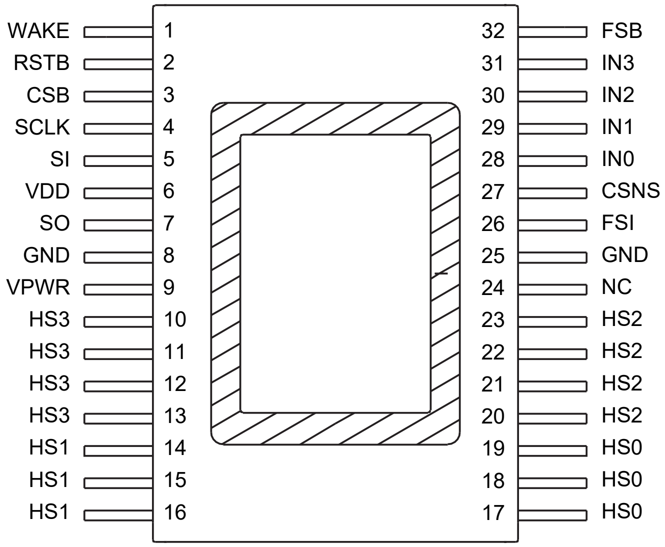


Figure 3. 10XS3425 pin connections

3.2 Pin definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 24.

Table 2. 10XS3425 pin definitions

Pin number	Pin name	Pin function	Formal name	Definition
1	WAKE	Input	Wake	This input pin controls the device mode.
2	RSTB	Input	Reset	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low-current Sleep mode.
3	CSB	Input	Chip select (active low)	This input pin is connected to a chip select output of a master microcontroller (MCU).
4	SCLK	Input	Serial clock	This input pin is connected to the MCU providing the required bit shift clock for SPI communication.
5	SI	Input	Serial input	This pin is a command data input pin connected to the SPI Serial Data Output of the MCU or to the SO pin of the previous device of a daisy-chain of devices.
6	VDD	Power	Digital drain voltage	This pin is an external voltage input pin used to supply power interfaces to the SPI bus.
7	SO	Output	Serial output	This output pin is connected to the SPI Serial Data Input pin of the MCU or to the SI pin of the next device of a daisy-chain of devices.

Table 2. 10XS3425 pin definitions (continued)

Pin number	Pin name	Pin function	Formal name	Definition
8, 25	GND	Ground	Ground	These pins, internally shorted, are the ground for the logic and analog circuitry of the device. These ground pins must be also shorted in the board.
9, 33	VPWR	Power	Positive power supply	This pin connects to the positive power supply and is the source of operational power for the device. Pins 9 and 33 must be externally connected.
10, 11, 12, 13	HS3	Output	High-side output	Protected 25 mΩ high-side power output pins to the load.
14, 15, 16	HS1	Output	High-side output	Protected 10 mΩ high-side power output pins to the load.
17, 18, 19	HS0	Output	High-side output	Protected 10 mΩ high-side power output pins to the load.
20, 21, 22, 23	HS2	Output	High-side output	Protected 25 mΩ high-side power output pins to the load.
24	NC	N/A	No connect	This pin may not be connected.
26	FSI	Input	Fail-safe input	This input enables the watchdog timeout feature.
27	CSNS	Output	Output current monitoring	This pin reports an analog value proportional to the designated HS[0:3] output current or the temperature of the GND flag (pin 14). It is used externally to generate a ground-referenced voltage for the microcontroller (MCU). Current recopy and temperature feedback is SPI programmable.
28 29 30 31	IN0 IN1 IN2 IN3	Input	Direct inputs	Each direct input controls the device mode. The IN[0:3] high-side input pins are used to directly control HS0:HS3 high-side output pins. The PWM frequency can be generated from IN0 pin to PWM module in case of external clock is set.
32	FSB	Output	Fault status (active low)	This pin is an open drain configured output requiring an external pull-up resistor to VDD for fault reporting.

4 Electrical characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{PWR(SS)}$	VPWR supply voltage range • Load dump at 25 °C (400 ms) • Maximum operating voltage • Reverse battery	41 28 -18	V	
V_{DD}	VDD supply voltage range	-0.3 to 5.5	V	
V_{DIG}	Input/output voltage	-0.3 to 5.5	V	(5)
V_{SO}	SO and CSNS output voltage	-0.3 to V_{DD}+0.3	V	
I_{DIG}	Digital input/output current in Clamp mode	100	µA	
$I_{CL(WAKE)}$	WAKE input clamp current	2.5	mA	
$I_{CL(CSNS)}$	CSNS input clamp current	2.5	mA	
$V_{HS[0:3]}$	HS [0:3] voltage • Positive • Negative	41 -24	V	
V_{PWR} - V_{HS}	High-side breakdown voltage	47	V	
$I_{HS[0:3]}$	Output current	6.0	A	(2)
$E_{CL[0:1]}$	HS[0,1] output clamp energy using single pulse method	60	mJ	(3)
$E_{CL[2:3]}$	HS[2,3] output clamp energy using single pulse method	25	mJ	(3)
 V_{ESD1} V_{ESD2} V_{ESD3} V_{ESD4}	ESD voltage (V_{PWR} pins 9 and 33 must be externally connected.) • Human Body Model (HBM) for HS[0:3], VPWR and GND • Human Body Model (HBM) for other pins • Charge Device Model (CDM) Corner pins (1, 13, 19, 21) All other pins (2-12, 14-18, 20, 22-24)	 ±8000 ±2000 ±750 ±500	V	(4)
Thermal ratings				
 T_A T_J	Operating temperature • Ambient • Junction	 -40 to 125 -40 to 150	°C	
T_{STG}	Storage temperature	-55 to 150	°C	

Notes

2. Continuous high-side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
3. Active clamp energy using single-pulse method (L = 2.0 mH, $R_L = 0\ \Omega$, $V_{PWR} = 14$ V, $T_J = 150$ °C initial).
4. Pins 9 and 33 must be externally connected. ESD testing is performed in accordance with the Human Body Model (HBM) ($C_{ZAP} = 100$ pF, $R_{ZAP} = 1500\ \Omega$), the Machine Model (MM) ($C_{ZAP} = 200$ pF, $R_{ZAP} = 0\ \Omega$), and the Charge Device Model (CDM), Robotic ($C_{ZAP} = 4.0$ pF).
5. Input / Output pins are: IN[0:3], RSTB, FSI, SI, SCLK, CSB, and FSB

Table 3. Maximum ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Thermal resistance				
$R_{\theta JC}$ $R_{\theta JA}$	Thermal resistance • Junction to Case • Junction to Ambient	0.5 23	°C/W	(6), (7)
T_{SOLDER}	Peak Pin Reflow Temperature During Solder Mounting	260	°C	(8)

Notes

6. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored
7. Device mounted on a 2s2p test board per JEDEC JESD51-2. 15 °C/W of $R_{\theta JA}$ can be reached in a real application case (4 layers board).
8. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

4.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Power inputs						
V_{PWR}	Battery supply voltage range • Fully operational • Extended mode	 6.0 4.0	 – –	 20 28	V	(9)
V_{PWR} (CLAMP)	Battery clamp voltage	41	47	53	V	(10)
$I_{PWR(ON)}$	V_{PWR} operating supply current • Outputs commanded ON, HS[0:3] open, IN[0:3] > V_{IH}	–	6.5	20	mA	
$I_{PWR(SBY)}$	V_{PWR} supply current • Outputs commanded OFF, OFF openload detection disabled, HS[0:3] shorted to the ground with V_{DD} = 5.5 V WAKE > V_{IH} or RSTB > V_{IH} and IN[0:3] < V_{IL}	–	6.5	7.5	mA	
$I_{PWR(SLEEP)}$	Sleep state supply current V_{PWR} = 12 V, RSTB = WAKE = IN[0:3] < V_{IL}, HS[0:3] shorted to ground • T_A = 25 °C • T_A = 85 °C	 – –	 1.0 –	 5.0 30	µA	
$V_{DD(ON)}$	V_{DD} supply voltage	3.0	–	5.5	V	
$I_{DD(ON)}$	V_{DD} supply current at V_{DD} = 5.5 V • No SPI communication • 8.0 MHz SPI communication	 – –	 1.6 5.0	 2.2 –	mA	(11)
$I_{DD(SLEEP)}$	V_{DD} sleep state current at V_{DD} = 5.5 V	–	–	5.0	µA	
$V_{PWR(OV)}$	Overvoltage shutdown threshold	28	32	36	V	
V_{PWR} (OVHYS)	Overvoltage shutdown hysteresis	0.2	0.8	1.5	V	
$V_{PWR(UV)}$	Undervoltage shutdown threshold	3.3	3.9	4.3	V	(12)
V_{SUPPLY} (POR)	V_{PWR} and V_{DD} power-on reset threshold	0.5	–	0.9	V_{PWR} (UV)	
$V_{PWR(UV)}$ _UP	Recovery undervoltage threshold	3.4	4.1	4.5	V	
$V_{DD(FAIL)}$	V_{DD} supply failure threshold (for V_{PWR} > $V_{PWR(UV)}$)	2.2	2.5	2.8	V	

Notes

9. In extended mode, the functionality is guaranteed but not the electrical parameters. From 4.0 to 6.0 V voltage range, the device is only protected with the thermal shutdown detection.
10. Measured with the outputs open.
11. Typical value guaranteed per design.
12. Output will automatically recover with time limited autoretry to instructed state when V_{PWR} voltage is restored to normal as long as the V_{PWR} degradation level did not go below the undervoltage power-on reset threshold. This applies to all internal device logic that is supplied by V_{PWR} and assumes that the external V_{DD} supply is within specification.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Outputs HS0 TO HS3						
$R_{DS\_01(on)}$	HS[0,1] output Drain-to-Source ON resistance (I_{HS} = 5.0 A, T_A = 25 °C) • V_{PWR} = 4.5 V • V_{PWR} = 6.0 V • V_{PWR} = 10 V • V_{PWR} = 13 V	– – – –	– – – –	36 16 10 10	mΩ	
$R_{DS\_01(on)}$	HS[0,1] output Drain-to-Source ON resistance (I_{HS} = 5.0 A, T_A = 150 °C) • V_{PWR} = 4.5 V • V_{PWR} = 6.0 V • V_{PWR} = 10 V • V_{PWR} = 13 V	– – – –	– – – –	62 27 17 17	mΩ	
$R_{SD\_01(on)}$	HS[0,1] output Source-to-Drain ON resistance (I_{HS} = -5.0 A, $V_{PWR=}$ -18 V) • T_A = 25 °C • T_A = 150 °C	– –	– –	15 20	mΩ	(13)
$R_{DS\_23(on)}$	HS[2,3] output Drain-to-Source ON resistance (I_{HS} = 5.0 A, T_A = 25 °C) • V_{PWR} = 4.5 V • V_{PWR} = 6.0 V • V_{PWR} = 10 V • V_{PWR} = 13 V	– – – –	– – – –	90 40 25 25	mΩ	
$R_{DS\_23(on)}$	HS[2,3] output Drain-to-Source ON resistance (I_{HS} = 5.0 A, T_A = 150 °C) • V_{PWR} = 4.5 V • V_{PWR} = 6.0 V • V_{PWR} = 10 V • V_{PWR} = 13 V	– – – –	– – – –	153 68 42.5 42.5	mΩ	
$R_{SD\_23(on)}$	HS[2,3] output Source-to-Drain ON resistance (I_{HS} = -5.0 A, $V_{PWR=}$ -18 V) • T_A = 25 °C • T_A = 150 °C	– –	– –	37.5 50	mΩ	(13)
R_{SHORT_01}	HS[0,1] maximum severe short-circuit impedance detection	28	67	100	mΩ	(14)
R_{SHORT_23}	HS[2,3] maximum severe short-circuit Impedance detection	70	160	200	mΩ	(14)
I_{OFF}	HS[0-3] output leakage current in OFF state • in Sleep mode • in Normal mode (OS_dis = 1 and OLOFF_dis = 1)	– –	– –	5.0 30	µA	

Notes

13. Source-Drain ON Resistance (reverse Drain-to-Source ON resistance) with negative polarity V_{PWR}.
14. Short-circuit impedance calculated from HS[0:3] to GND pins. Value guaranteed per design.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Outputs HS0 TO HS3 (continued)						
 OCHI1 OCHI2 OC1 OC2 OC3 OC4 OCLO4 OCLO3 OCLO2 OCLO1	HS[0,1] output overcurrent detection levels (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V)	 77.6 46.4 43.6 40.2 31.6 26.2 19.2 12.1 10.3 6.2	 101.6 62 55.6 48.8 40.4 33.2 24.3 15.3 13.1 8.3	 125.6 77.6 67.6 57.4 49.2 40.2 29.4 18.4 15.9 10.3	A	
 C_{SR0} C_{SR1}	HS[0,1] current sense ratio (6.0 V ≤ HS[0:3] ≤ 20 V, CSNS ≤ 5.0 V) CSNS_ratio bit = 0 CSNS_ratio bit = 1	 – –	 1/9900 1/58500	 – –	–	(15)
C_{SR0_ACC}	HS[0,1] current sense ratio (C_{SR0}) accuracy (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) At 25 °C and 125 °C • $I_{HS[0:1]}$ = 12.5 A • $I_{HS[0:1]}$ = 5.0 A • $I_{HS[0:1]}$ = 3.0 A • $I_{HS[0:1]}$ = 1.5 A At -40 °C • $I_{HS[0:1]}$ = 12.5 A • $I_{HS[0:1]}$ = 5.0 A • $I_{HS[0:1]}$ = 3.0 A • $I_{HS[0:1]}$ = 1.5 A	 -12 -13 -16 -20 -18 -20 -25 -30	 – – – – – – – –	 12 13 16 20 18 20 25 30	%	

Notes

15. Current sense ratio = I_{CSNS} / $I_{HS[0:3]}$

C_{SR0_ACC} (CAL)	HS[0,1] current recopy accuracy with one calibration point (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) • $I_{HS[0:1]}$ = 5.0 A	-5.0	–	5.0	%	(16)
$\Delta(C_{SR0})/\Delta(T)$	HS[0,1] CSR0 current recopy temperature drift (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) • $I_{HS[0:1]}$ = 5.0 A	–	–	0.04	%/°C	(17)
C_{SR1_ACC}	HS[0,1] current sense ratio (C_{SR1}) accuracy (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) At 25 °C and 125 °C • $I_{HS[0:1]}$ = 12.5 A • $I_{HS[0:1]}$ = 75A At -40 °C • $I_{HS[0:1]}$ = 12.5 A • $I_{HS[0:1]}$ = 75 A	 -17 -12 -25 -30	 – – – –	 17 12 25 30	%	
C_{SR1_ACC} (CAL)	HS[0,1] current recopy accuracy with one calibration point (6.0 V ≤ $V_{HS[0:1]}$ ≤ 20 V) • $I_{HS[0:1]}$ = 12.5 A	-5.0	–	5.0	%	(16)
$V_{CL(CSNS)}$	Current sense clamp voltage • CSNS Open; $I_{HS[0:3]}$ = 5.0 A with C_{SR0} ratio	V_{DD}+0.25	–	V_{DD}+1.0	V	

Notes

16. Based on statistical analysis. It is not production tested.
17. Based on statistical data: delta (C_{SR0})/delta (T) = {(measured I_{CSNS} at T_1 - measured I_{CSNS} at T_2) / measured I_{CSNS} at room} / {T_1-T_2}. Not production tested.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
OUTPUTS HS0 TO HS3 (CONTINUED)						
$I_{OLD(OFF)}$	OFF openload detection source current	30	–	100	µA	(18)
$V_{OLD(THRES)}$	OFF openload fault detection voltage threshold	2.0	3.0	4.0	V	
$I_{OLD(ON\_LED)}$	ON openload fault detection current threshold with LED ($V_{HS[0:3]}$ = V_{PWR} -0.75 V	2.5	5.0	10	mA	
$I_{OLD(ON)}$	ON openload fault detection current threshold				mA	
	• HS[0,1]	80	360	660		
	• HS[2,3]	55	165	330		
$V_{OSD(THRES)}$	Output short to V_{PWR} detection voltage threshold • Output programmed OFF	V_{PWR}-1.2	V_{PWR}-0.8	V_{PWR}-0.4	V	
V_{CL}	Output negative clamp voltage • 0.5 A ≤ $I_{HS[0:3]}$ ≤ 5.0 A, output programmed OFF	-22	–	-16	V	
T_{SD}	Output overtemperature shutdown for 4.5 V < V_{PWR} < 28 V	155	175	195	°C	
OCHI1	HS[2,3] output overcurrent detection levels (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V)	38.8	50.8	62.8	A	
OCHI2		23.2	31	38.8		
OC1		21.8	27.3	32.8		
OC2		17.3	22.9	28.4		
OC3		14.7	19.2	23.7		
OC4		12.2	15.8	19.4		
OCLO4		9.2	11.9	14.5		
OCLO3		5.8	7.6	9.3		
OCLO2		4.6	6.3	8.0		
OCLO1		2.9	4.1	5.3		
	HS[2,3] current sense ratio (6.0 V ≤ $_{HS[2:3]}$ ≤ 20 V, CSNS ≤ 5.0 V)				–	(19)
C_{SR0}	CSNS_ratio bit = 0	–	1/4670	–		
C_{SR1}	CSNS_ratio bit = 1	–	1/27270	–		
C_{SR0_ACC}	HS[2,3] current sense ratio (C_{SR0}) accuracy (6.0 V ≤ $V_{HS[2:3]}$ ≤ 20 V)				%	
	• $I_{HS[2:3]}$ = 6.25 A	-13	–	13		
	• $I_{HS[2:3]}$ = 2.5 A	-16	–	16		
	• $I_{HS[2:3]}$ = 1.5 A	-17	–	17		
	• $I_{HS[2:3]}$ = 0.75 A	-20	–	20		
C_{SR0_ACC} (CAL)	HS[2,3] current recopy accuracy with one calibration point (6.0 V ≤ $V_{HS[2:3]}$ ≤ 20 V) • $I_{HS[2:3]}$ = 2.5 A	-5.0	–	5.0	%	(20)

Notes

18. Output OFF openload detection current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded OFF. Pull-up current is measured for V_{HS} = $V_{OLD(THRES)}$
19. Current sense ratio = I_{CSNS} / $I_{HS[0:3]}$
20. Based on statistical analysis. It is not production tested.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Outputs HS0 TO HS3 (continued)						
$\Delta(C_{SR0})/\Delta(T)$	HS[2,3] C_{SR0} current recopy temperature drift (6.0 V ≤ $V_{HS[2:3]}$ ≤ 20 V) • $I_{HS[2:3]}$ = 2.5 A	–	–	0.04	%/°C	(21)
C_{SR1_ACC}	HS[2,3] current sense ratio (C_{SR1}) accuracy (6.0 V ≤ $V_{HS[2:3]}$ ≤ 20 V) • $I_{HS[2:3]}$ = 6.25 A • $I_{HS[2:3]}$ = 18.75 A	-20 -18	– –	+20 +18	%	
C_{SR1_ACC} (CAL)	HS[2,3] current recopy accuracy with one calibration point (6.0 V ≤ $V_{HS[2:3]}$ ≤ 20 V) • $I_{HS[2:3]}$ = 6.2 A	-5.0	–	5.0	%	(21)
Control interface						
V_{IH}	Input logic high-voltage	2.0	–	V_{DD}+0.3	V	(22)
V_{IL}	Input logic low-voltage	-0.3	–	0.8	V	(22)
I_{DWN}	Input logic pull-down current (SCLK, SI)	5.0	–	20	µA	(25)
I_{UP}	Input logic pull-up current (CSB)	5.0	–	20	µA	(26)
C_{SO}	SO, FSB tri-state capacitance	–	–	20	pF	(23)
R_{DWN}	Input logic pull-down resistor (RSTB, WAKE and IN[0:3])	125	250	500	kΩ	
C_{IN}	Input capacitance	–	4.0	12	pF	(23)
$V_{CL(WAKE)}$	Wake input clamp voltage • $I_{CL(WAKE)}$ < 2.5 mA	18	25	32	V	(24)
$V_{F(WAKE)}$	Wake input forward voltage • $I_{CL(WAKE)}$ = -2.5 mA	-2.0	–	-0.3	V	
V_{SOH}	SO high state output voltage • I_{OH} = 1.0 mA	V_{DD}-0.4	–	–	V	
V_{SOL}	SO and FSB low state output voltage • I_{OL} = -1.0 mA	–	–	0.4	V	
Control interface						
$I_{SO(LEAK)}$	SO, CSNS and FSB tri-state leakage current • CSB = V_{IH} and 0.0 V ≤ V_{SO} ≤ V_{DD}, or FSB = 5.5 V, or CSNS = 0.0 V	-2.0	0	2.0	µA	
RFS	FSI external pull-down resistance Watchdog disabled Watchdog enabled	– 10	0 Infinite	1.0 –	kΩ	(27)

Notes

21. Based on statistical analysis. It is not production tested.
22. Upper and lower logic threshold voltage range applies to SI, CSB, SCLK, RSTB, IN[0:3], and WAKE input signals. The WAKE and RSTB signals may be supplied by a derived voltage referenced to V_{PWR}.
23. Input capacitance of SI, CSB, SCLK, RSTB, IN[0:3], and WAKE. This parameter is guaranteed by process monitoring but is not production tested.
24. The current must be limited by a series resistance when using voltages > 7.0 V.
25. Pull-down current is with V_{SI} ≥ 1.0 V and V_{SCLK} ≥ 1.0 V.
26. Pull-up current is with V_{CSB} ≤ 2.0 V. CSB has an active internal pull-up to V_{DD}.
27. In Fail-safe, HS[0:3] depends respectively on ON[0:3]. FSI has an active internal pull-up to V_{REG} ≅ 3.0 V.

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Power output timing HS0 TO HS3						
SR_{R00}	HS[0,1] output rising medium slew rate (medium speed slew rate / SR[1:0] = 00)	300	650	1200	mV/µs	
SR_{F00}	HS[0,1] output falling medium slew rate (medium speed slew rate / SR[1:0] = 00)	300	720	1200	mV/µs	
DS_{R_00}	HS[0,1] driver output matching slew rate (SRR /SRF) • PWR = 14 V at 25 °C and for medium speed slew rate (SR[1:0] = 00)	0.8	0.9	1.2		
SR_{R01}	HS[0,1] output rising slow slew rate (slow speed slew rate / SR[1:0] = 01)	150	330	600	mV/µs	
SR_{F01}	HS[0,1] output falling slow slew rate (slow speed slew rate / SR[1:0] = 01)	150	370	600	mV/µs	
SR_{R10}	HS[0,1] output rising fast slew rate (fast speed slew rate / SR[1:0] = 10)	600	1250	2400	mV/µs	
SR_{F10}	HS[0,1] output falling fast slew rate (fast speed slew rate / SR[1:0] = 10)	600	1450	2400	mV/µs	
t_{DLY_ON}	HS[0:1] outputs turn-on delay time • VPWR = 14 for medium speed slew rate (SR[1:0] = 00)	40	64	100	µs	(28),(29)
t_{DLY_OFF}	HS[0:1] outputs turn-off delay time • VPWR = 14 for medium speed slew rate (SR[1:0] = 00)	10	32	60	µs	(28),(29)
Δt_{RF}	HS[0:1] driver output matching time ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) • VPWR = 14 V, f_{PWM} = 240 Hz, PWM duty cycle = 50 %, at 25 °C for medium speed slew rate (SR[1:0] = 00)	10	32	60	µs	(28),(29)
SR_{R00}	HS[2,3] output rising medium slew rate (medium speed slew rate / SR[1:0] = 00)	200	470	800	mV/µs	
SR_{F00}	HS[2,3] output falling medium slew rate (medium speed slew rate / SR[1:0] = 00)	200	570	800	mV/µs	
DS_{R_00}	HS[2,3] driver output matching slew rate (SRR /SRF) • VPWR = 14 V at 25 °C and for medium speed slew rate (SR[1:0] = 00)	0.6	0.8	1.0		
SR_{R01}	HS[2,3] output rising slow slew rate (slow speed slew rate / SR[1:0] = 01)	100	230	400	mV/µs	
SR_{F01}	HS[2,3] output falling slow slew rate (slow speed slew rate / SR[1:0] = 10)	100	300	400	mV/µs	

Notes

28. Turn ON delay time measured from rising edge of any signal (IN[0:3] and CSB) that would turn the output ON to $V_{HS[0:3]} = V_{PWR} / 2$ with R_L = 5.0 Ω resistive load.
29. Turn OFF delay time measured from falling edge of any signal (IN[0:3] and CSB) that would turn the output OFF to $V_{HS[0:3]} = V_{PWR} / 2$ with R_L = 5.0 Ω resistive load.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Power output timing HS0 TO HS3 (Continued)						
SR_{R10}	HS[2,3] output rising fast slew rate (fast speed slew rate / SR[1:0] = 10)	400	900	1600	mV/µs	
SR_{F10}	HS[2,3] output falling fast slew rate (fast speed slew rate / SR[1:0] = 10)	400	1140	1600	mV/µs	
t_{DLY_ON}	HS[2,3] outputs turn-on delay time • VPWR = 14 V for medium speed slew rate (SR[1:0] = 00)	40	87	160	µs	
t_{DLY_OFF}	HS[2,3] outputs turn-off delay time • VPWR = 14 V for medium speed slew rate (SR[1:0] = 00)	15	36	65	µs	
Δt_{RF}	HS[2,3] driver output matching time (tDLY(ON) - tDLY(OFF)) • VPWR = 14 V, f_{PWM} = 240 Hz, PWM duty cycle = 50 %, at 25 °C for medium speed slew rate (SR[1:0] = 00)	10	51	110	µs	
t_{FAULT}	Fault detection blanking time	1.0	5.0	20	µs	(30)
t_{DETECT}	Output shutdown delay time	–	7.0	30	µs	(31)
t_{CNSVAL}	CSNS valid time	–	70	100	µs	(32)
t_{WDTO}	Watchdog timeout	217	310	400	ms	(33)
T_{OLLED}	ON openload fault cyclic detection period with LED • Internal clock (PWM_en bit = 1 & CLOCK_Set = 1) • External clock (PWM_en bit = 1 & CLOCK_Set = 0)	6.4 -	8.3 PWM period	12 -	ms	

Notes

30. Time necessary to report the fault to FSB pin.
31. Time necessary to switch-off the output in case of OT, or OC, or SC, or UV fault detection (from negative edge of FSB pin to HS voltage = 50 % of V_{PWR}.
32. Time necessary for CSNS to be within ±5.0 % of the targeted value (from HS voltage = 50 % of V_{PWR} to ±5.0 % of the targeted CSNS value).
33. For FSI open, the watchdog timeout delay measured from the rising edge of RST, to HS[0,2] output state depends on the corresponding input command.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Power output timing HS0 TO HS3 (continued)						
	HS[0,1] output overcurrent time step				ms	
	• OC[1:0] = 00 (slow by default)					
t_{OC1_00}		4.40	6.30	8.02		
t_{OC2_00}		1.62	2.32	3.00		
t_{OC3_00}		2.10	3.00	3.90		
t_{OC4_00}		2.88	4.12	5.36		
t_{OC5_00}		4.58	6.56	8.54		
t_{OC6_00}		10.16	14.52	18.88		
t_{OC7_00}		73.2	104.6	134.0		
	• OC[1:0] = 01 (fast)					
t_{OC1_01}		1.10	1.57	2.00		
t_{OC2_01}		0.40	0.58	0.75		
t_{OC3_01}		0.52	0.75	0.98		
t_{OC4_01}		0.72	1.03	1.34		
t_{OC5_01}		1.14	1.64	2.13		
t_{OC6_01}		2.54	3.63	4.72		
t_{OC7_01}		18.2	26.1	34.0		
	• OC[1:0] = 10 (medium)					
t_{OC1_10}		2.20	3.15	4.01		
t_{OC2_10}		0.81	1.16	1.50		
t_{OC3_10}		1.05	1.50	1.95		
t_{OC4_10}		1.44	2.06	2.68		
t_{OC5_10}		2.29	3.28	4.27		
t_{OC6_10}		5.08	7.26	9.44		
t_{OC7_10}		36.6	52.3	68.0		
	• OC[1:0] = 11 (very slow)					
t_{OC1_11}		8.8	12.6	16.4		
t_{OC2_11}		3.2	4.6	21.4		
t_{OC3_11}		4.2	6.0	7.8		
t_{OC4_11}		5.7	8.2	10.7		
t_{OC5_11}		9.1	13.1	17.0		
t_{OC6_11}		20.3	29.0	37.7		
t_{OC7_11}		146.4	209.2	272.0		

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
POWER OUTPUT TIMING HS0 TO HS3 (CONTINUED)						
	HS[2,3] output overcurrent time step				ms	
	• OC[1:0] = 00 (slow by default)					
t_{OC1_00}		3.4	4.9	6.4		
t_{OC2_00}		1.1	1.6	2.1		
t_{OC3_00}		1.4	2.1	2.8		
t_{OC4_00}		2.0	2.9	3.8		
t_{OC5_00}		3.4	4.9	6.4		
t_{OC6_00}		8.5	12.2	15.9		
t_{OC7_00}		62.4	89.2	116.0		
	• OC[1:0] = 01 (fast)					
t_{OC1_01}		0.86	1.24	1.61		
t_{OC2_01}		0.28	0.40	0.52		
t_{OC3_01}		0.36	0.52	0.68		
t_{OC4_01}		0.51	0.74	0.96		
t_{OC5_01}		0.78	1.12	1.46		
t_{OC6_01}		2.14	3.06	3.98		
t_{OC7_01}		20.2	22.2	28.9		
	• OC[1:0] = 10 (medium)					
t_{OC1_10}		1.7	2.5	3.3		
t_{OC2_10}		0.5	0.8	1.0		
t_{OC3_10}		0.7	1.0	1.3		
t_{OC4_10}		1.0	1.5	2.0		
t_{OC5_10}		1.7	2.5	3.3		
t_{OC6_10}		4.2	6.1	6.0		
t_{OC7_10}		31.2	44.6	58.0		
	• OC[1:0] = 11 (very slow)					
t_{OC1_11}		6.8	9.8	12.8		
t_{OC2_11}		2.2	3.2	16.7		
t_{OC3_11}		2.9	4.2	5.5		
t_{OC4_11}		4.0	5.8	7.6		
t_{OC5_11}		6.8	9.8	12.8		
t_{OC6_11}		17.0	24.4	31.8		
t_{OC7_11}		124.8	178.4	232.0		

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
POWER OUTPUT TIMING HS0 TO HS3 (continued)						
	HS[0,1] bulb cooling time step				ms	
	• CB[1:0] = 00 or 11 (medium)					
t_{BC1_00}		242	347	452		
t_{BC2_00}		126	181	236		
t_{BC3_00}		140	200	260		
t_{BC4_00}		158	226	294		
t_{BC5_00}		181	259	337		
t_{BC6_00}		211	302	393		
	• CB[1:0] = 01 (fast)					
t_{BC1_01}		121	173	226		
t_{BC2_01}		63	90	118		
t_{BC3_01}		70	100	130		
t_{BC4_01}		79	113	147		
t_{BC5_01}		90	129	169		
t_{BC6_01}	• CB[1:0] = 10 (slow)	105	151	197		
t_{BC1_10}		484	694	1904		
t_{BC2_10}		252	362	472		
t_{BC3_10}		280	400	520		
t_{BC4_10}		316	452	588		
t_{BC5_10}		362	518	674		
t_{BC6_10}		422	604	786		
	HS[2,3] bulb cooling time step					
	• CB[1:0] = 00 or 11 (medium)					
t_{BC1_00}		291	417	542		
t_{BC2_00}		156	224	292		
t_{BC3_00}		178	255	332		
t_{BC4_00}		208	298	388		
t_{BC5_00}		251	359	467		
t_{BC6_00}		314	449	584		
	• CB[1:0] = 01 (fast)					
t_{BC1_01}		146	209	272		
t_{BC2_01}		78	112	146		
t_{BC3_01}		88	127	166		
t_{BC4_01}		101	145	189		
t_{BC5_01}		126	180	234		
t_{BC6_01}		226	324	422		
	• CB[1:0] = 10 (slow)					
t_{BC1_10}		583	834	1085		
t_{BC2_10}		312	448	582		
t_{BC3_10}		357	510	665		
t_{BC4_10}		417	596	775		
t_{BC5_10}		501	717	933		
t_{BC6_10}		628	898	1170		

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
PWM module timing						
f_{IN0}	Input PWM clock range on IN0	7.68	–	30.72	kHz	
$f_{IN0(LOW)}$	Input PWM clock low frequency detection range on IN0	1.0	2.0	4.0	kHz	(35)
$f_{IN0(HIGH)}$	Input PWM clock high frequency detection range on IN0	100	–	400	kHz	(35)
f_{PWM}	Output PWM frequency range using external clock on IN0	31.25	–	781	Hz	
$A_{FPWM(CAL)}$	Output PWM frequency accuracy using calibrated oscillator	-10	–	+10	%	
$f_{PWM(0)}$	Default output PWM frequency using internal oscillator	84	120	156	Hz	
$t_{CSB(MIN)}$	CSB calibration low minimum time detection range	14	20	26	µs	
$t_{CSB(MAX)}$	CSB calibration low maximum time detection range	140	200	260	µs	
$R_{PWM\_}1k$	Output PWM duty cycle range for f_{PWM} = 1.0 kHz for high speed slew rate	10	–	94	%	(35)
$R_{PWM\_}400$	Output PWM duty cycle range for f_{PWM} = 400 Hz	6.0	–	98	%	(35)
$R_{PWM\_}200$	Output PWM duty cycle range for f_{PWM} = 200 Hz	5.0	–	98	%	(35)
Input timing						
t_{IN}	Direct input toggle timeout	175	250	325	ms	
Autoretry timing						
t_{AUTO}	Autoretry period	105	150	195	ms	
Temperature on the GND flag						
T_{OTWAR}	Thermal prewarning detection	110	125	140	°C	(36)
T_{FEED}	Analog temperature feedback at T_A = 25 °C with R_{CSNS} = 2.5 kΩ	1.15	1.20	1.25	V	
DT_{FEED}	Analog temperature feedback derating with R_{CSNS} = 2.5 kΩ	-3.5	-3.7	-3.9	mV/°C	(37)

Notes

34. Clock fail detector available for PWM_en bit is set to logic [1] and CLOCK_sel is set to logic [0].
35. The PWM ratio is measured at V_{HS} = 50 % of V_{PWR} and for the default SR value. It is possible to put the device fully on (PWM duty cycle 100 %) and fully off (duty cycle 0 %). For values outside this range, a calibration is needed between the PWM duty cycle programming and the PWM on the output with R_L = 5.0 Ω resistive load.
36. Typical value guaranteed per design.
37. Value guaranteed per statistical analysis.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SPI interface characteristics(38)						
f_{SPI}	Maximum frequency of SPI operation	–	–	8.0	MHz	
t_{WRSTB}	Required low state duration for RSTB	10	–	–	µs	(39)
t_{CSB}	Rising edge of CSB to falling edge of CSB (required setup time)	–	–	1.0	µs	(40)
t_{ENBL}	Rising edge of RSTB to falling edge of CSB (required setup time)	–	–	5.0	µs	(40)
t_{LEAD}	Falling edge of CSB to rising edge of SCLK (required setup time)	–	–	500	ns	(40)
t_{WSCLKh}	Required high state duration of SCLK (required setup time)	–	–	50	ns	(40)
t_{WSCLKl}	Required low state duration of SCLK (required setup time)	–	–	50	ns	(40)
t_{LAG}	Falling edge of SCLK to rising edge of CSB (required setup time)	–	–	60	ns	(40)
$t_{SI(SU)}$	SI to falling edge of SCLK (required setup time)	–	–	37	ns	(41)
$t_{SI(HOLD)}$	Falling edge of SCLK to SI (required setup time)	–	–	49	ns	(41)
t_{RSO}	SO rise time • C_L = 80 pF	–	–	13	ns	
t_{FSO}	SO Fall Time • C_L = 80 pF	–	–	13	ns	
t_{RSI}	SI, CSB, SCLK, incoming signal rise time	–	–	13	ns	(41)
t_{FSI}	SI, CSB, SCLK, incoming signal fall time	–	–	13	ns	(41)
$t_{SO(EN)}$	Time from falling edge of CSB to SO low-impedance	–	–	60	ns	(42)
$t_{SO(DIS)}$	Time from rising edge of CSB to SO high-impedance	–	–	60	ns	(43)

Notes

38. Parameters guaranteed by design.
39. RSTB low duration measured with outputs enabled and going to OFF or disabled condition.
40. Maximum setup time required for the 10XS3425 is the minimum guaranteed time needed from the microcontroller.
41. Rise and fall time of incoming SI, CSB, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
42. Time required for output status data to be available for use at SO. 1.0 kΩ on pull-up on CSB.
43. Time required for output status data to be terminated at SO. 1.0 kΩ on pull-up on CSB.

4.4 Timing diagrams

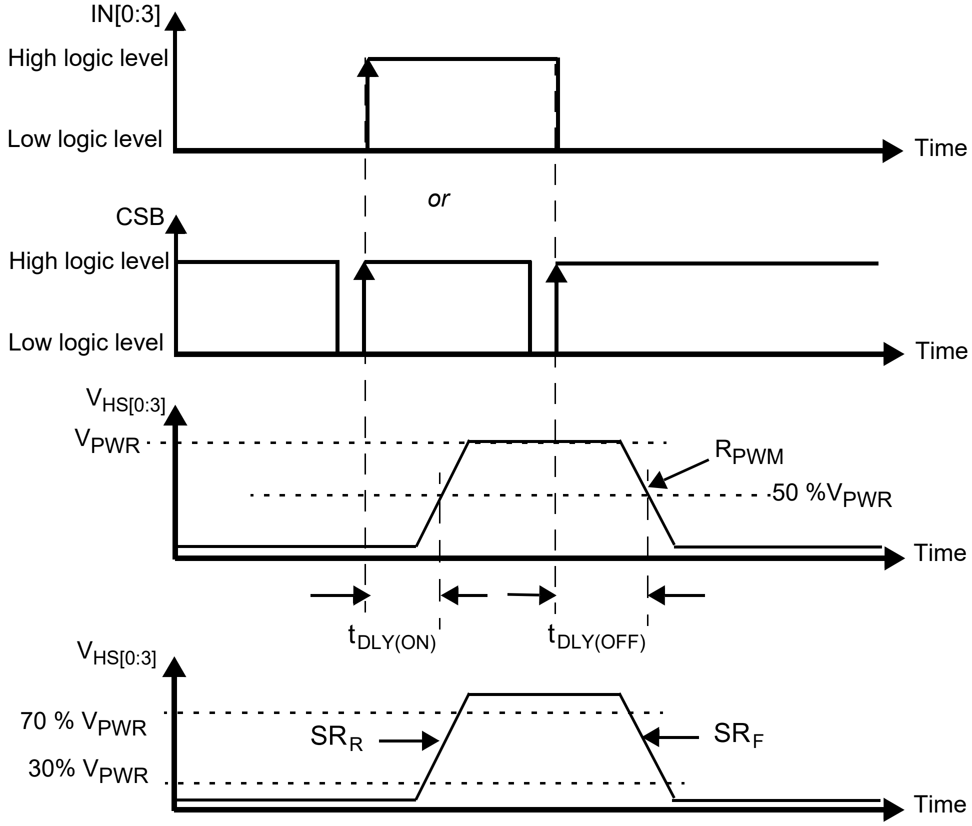


Figure 4. Output slew rate and time delays

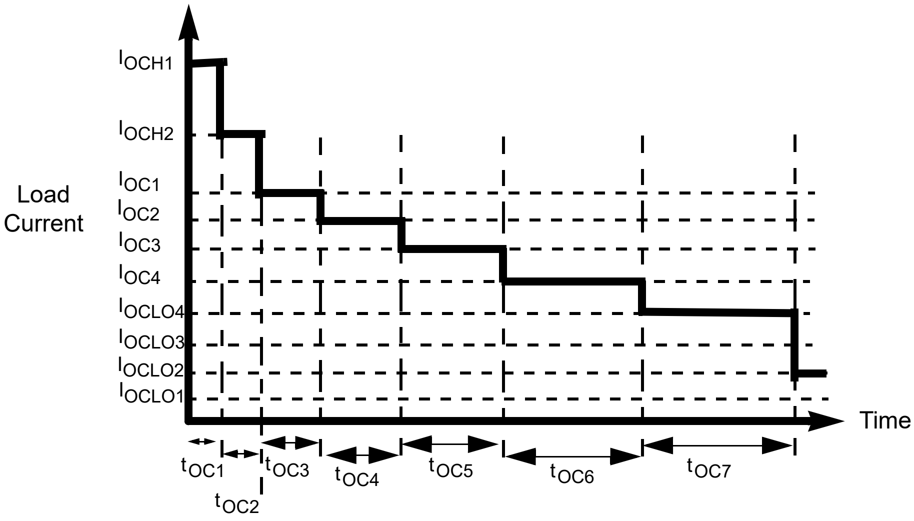


Figure 5. Overcurrent shutdown protection

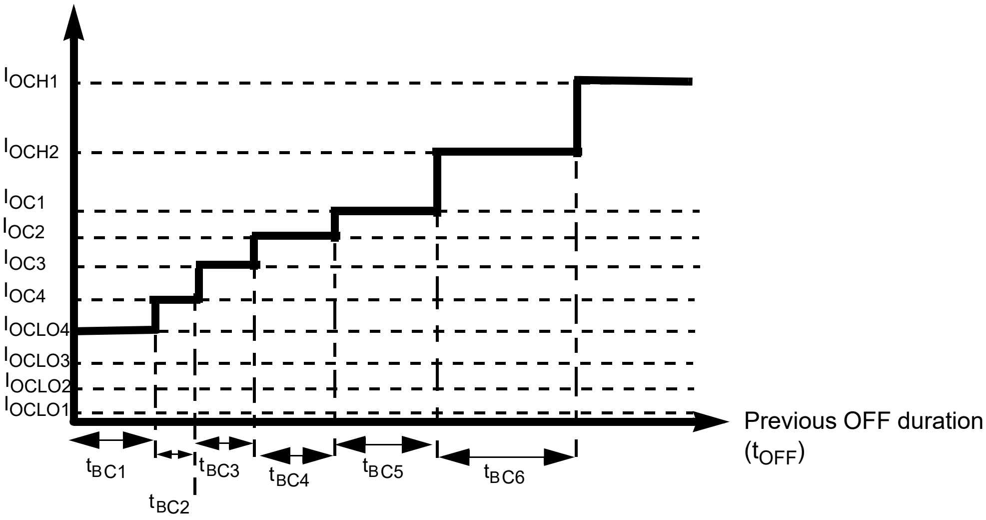


Figure 6. Bulb cooling management

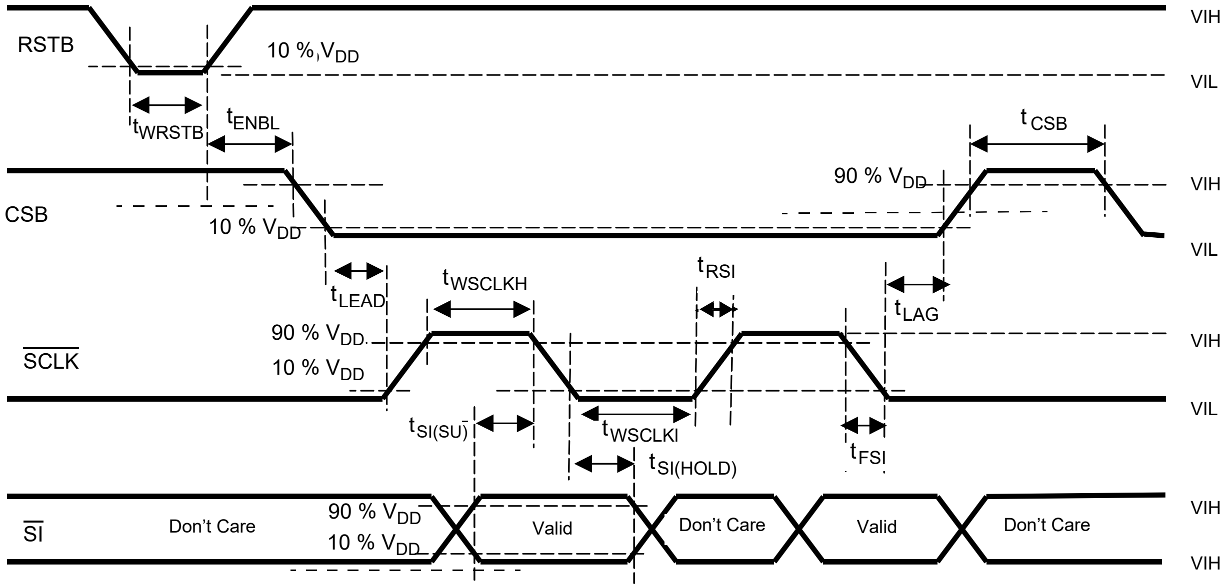


Figure 7. Input timing switching characteristics

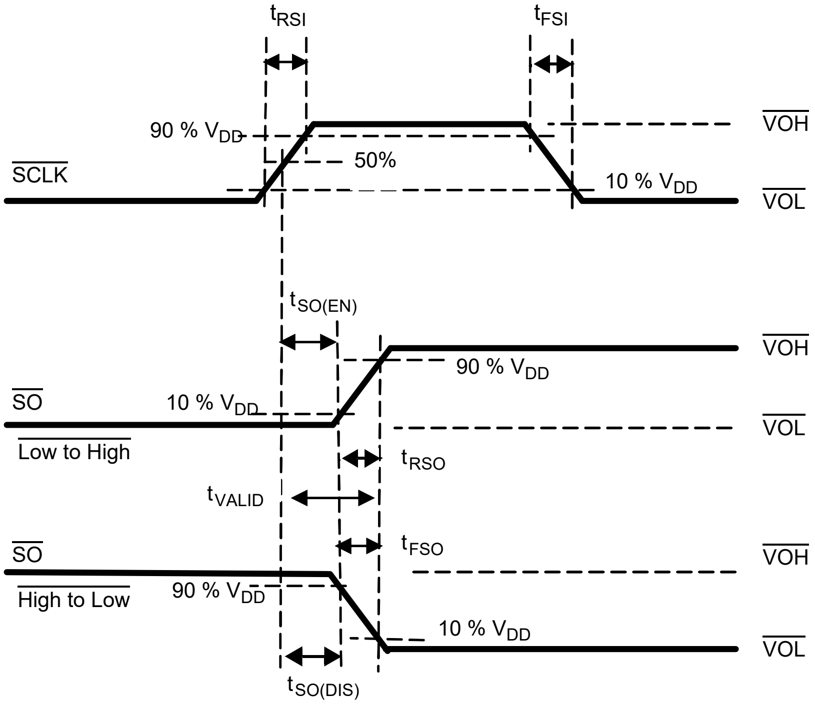


Figure 8. SCLK waveform and valid SO data delay time

5 Functional description

5.1 Introduction

The 10XS3425 is one in a family of devices designed for low-voltage automotive lighting applications. Its four low $R_{DS(on)}$ MOSFETs (dual 10 mΩ, dual 25 mΩ) can control four separate 55 W / 28 W bulbs and/or Xenon modules.

Programming, control, and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control if desired. The 10XS3425 allows the user to program via the SPI the fault current trip levels and duration of acceptable lamp inrush. The device has Fail-safe mode to provide Fail-safe functionality of the outputs in case of MCU damaged.

5.2 Functional pin description

5.2.1 Output current monitoring (CSNS)

The current sense pin provides a current proportional to the designated HS0:HS3 output or a voltage proportional to the temperature on the GND flag. That current is fed into a ground-referenced resistor (3.3 kΩ, typical) and its voltage is monitored by an MCU's A/D. The output type is selected via the SPI. This pin can be tri-stated through the SPI.

5.2.2 Direct inputs (IN0, IN1, IN2, IN3)

Each IN input wakes the device. The IN0:IN3 high-side input pins are also used to directly control HS0:HS3 high-side output pins. If the outputs are controlled by the PWM module, the external PWM clock is applied to the IN0 pin. These pins are to be driven with CMOS levels, and they have a passive internal pull-down, R_{DWN}.

5.2.3 Fault status (FSB)

This pin is an open drain configured output requiring an external pull-up resistor to V_{DD} for fault reporting. If a device fault condition is detected, this pin is active LOW. Specific device diagnostics and faults are reported via the SPI SO pin.

5.2.4 Wake

The wake input wakes the device. An internal clamp protects this pin from high damaging voltages with a series resistor (10 kΩ, typ). This input has a passive internal pull-down, R_{DWN}.

5.2.5 Reset (RSTB)

The reset input wakes the device. This is used to initialize the device configuration and fault registers, as well as place the device in a low-current Sleep mode. The pin also starts the watchdog timer when transitioning from logic [0] to logic [1]. This pin has a passive internal pull-down, R_{DWN}.

5.2.6 Chip select (CSB)

The CSB pin enables communication with the master microcontroller (MCU). When this pin is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the MCU. The 10XS3425 latches in data from the Input Shift registers to the addressed registers on the rising edge of CSB. The device transfers status information from the power output to the Shift register on the falling edge of CSB. The SO output driver is enabled when CSB is a logic [0]. CSB should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. CSB has an active internal pull-up from V_{DD}, I_{UP}.

5.2.7 Serial clock (SCLK)

The SCLK pin clocks the internal shift registers of the 10XS3425 device. The serial input (SI) pin accepts data into the input shift register on the falling edge of the SCLK signal, while the serial output (SO) pin shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important the SCLK pin be in a logic low state whenever CSB makes any transition. For this reason, it is recommended the SCLK pin be in a logic [0] whenever the device is not accessed (CSB logic [1] state). SCLK has an active internal pull-down. When CSB is logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high-impedance) (see Figure 10, page 27). SCLK input has an active internal pull-down, I_{DWN}.

5.2.8 Serial input (SI)

This is a serial interface (SI) command data input pin. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, starting with D15 (MSB) to D0 (LSB). The internal registers of the 10XS3425 are configured and controlled using a 5-bit addressing scheme described in Table 10. Register addressing and configuration are described in Table 11. SI input has an active internal pull-down, I_{DWN}.

5.2.9 Digital drain voltage (VDD)

This pin is an external voltage input pin used to supply power to the SPI circuit. In the event V_{DD} is lost (V_{DD} failure), the device goes to Fail-safe mode.

5.2.10 Ground (GND)

These pins are the ground for the device.

5.2.11 Positive power supply (VPWR)

This pin connects to the positive power supply and is the source of operational power for the device. The VPWR contact is the backside surface mount tab of the package.

5.2.12 Serial output (SO)

The SO data pin is a tri-stateable output from the shift register. The SO pin remains in a high-impedance state until the CSB pin is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, the state of the key inputs, etc. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. SO reporting descriptions are provided in Table 23.

5.2.13 High-side outputs (HS3, HS1, HS0, HS2)

Protected 10 mΩ and 25 mΩ high-side power outputs to the load.

5.2.14 Fail-safe input (FSI)

This pin incorporates an active internal pull-up current source from internal supply (V_{REG}). This enables the watchdog timeout feature. When the FSI pin is opened, the Watchdog circuit is enabled. After a watchdog timeout occurs, the output states depends on IN[0:3]. When the FSI pin is connected to GND, the Watchdog circuit is disabled. The output states depends on IN[0:3] in case of a V_{DD} Failure condition. In case a V_{DD} failure detection is activated (VDD_FAIL_en bit sets to logic [1]).

5.3 Functional internal block description

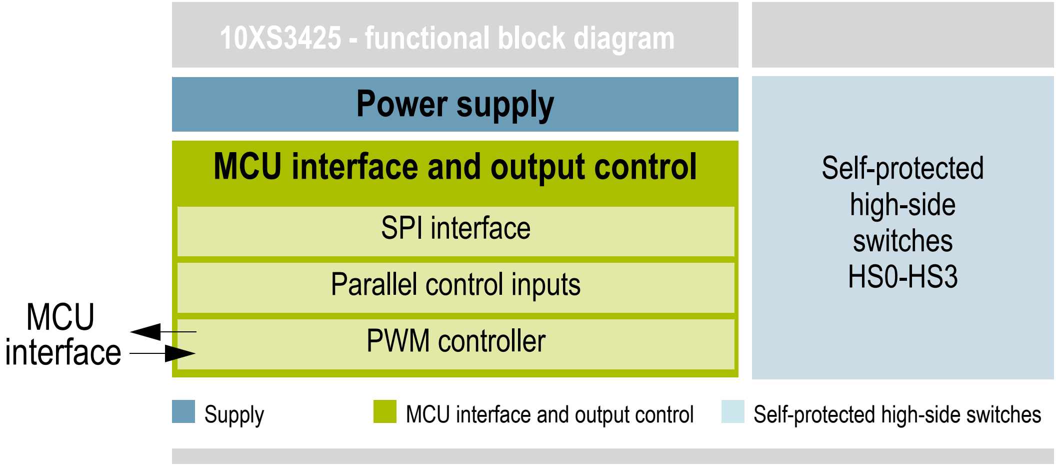


Figure 9. Functional block diagram

5.3.1 Power supply

The 10XS3425 is designed to operate from 4.0 to 28 V on the VPWR pin. Characteristics are provided from 6.0 to 20 V for the device. The VPWR pin supplies power to internal regulator, analog, and logic circuit blocks. The VDD supply is used for Serial Peripheral Interface (SPI) communication in order to configure and diagnose the device. This IC architecture provides a low quiescent current Sleep mode. Applying V_{PWR} and V_{DD} to the device will place the device in the Normal mode. The device will transit to Fail-safe mode during failures on the SPI or/and on VDD voltage.

5.3.2 High-side switches (HS0–HS3)

These pins are the high-side outputs controlling automotive lamps located for the front of vehicle, such as 65 W/55 W bulbs and Xenon-HID modules. Those N-channel MOSFETs with 10 mΩ and 25 mΩ $R_{DS(on)}$ are self-protected and present extended diagnostics in order to detect bulb outage and short-circuit fault condition. The HS output is actively clamped during turn off of inductive loads and inductive battery line. When driving DC motor or Solenoid loads demanding multiple switching, an external recirculation device must be used to maintain the device in its Safe Operating Area.

5.3.3 MCU interface and output control

In Normal mode, each bulb is controlled directly from the MCU through the SPI. A pulse-width modulation control module allows improvement of lamp lifetime with bulb power regulation (PWM frequency range of 100 to 400 Hz) and addressing the dimming application (day running light). An analog feedback output provides a current proportional to the load current or the temperature of the board. The SPI is used to configure and to read the diagnostic status (faults) of high-side outputs. The reported fault conditions are: openload, short-circuit to battery, short-circuit to ground (overcurrent and severe short-circuit), thermal shutdown, and under/overvoltage. Owing to accurate and configurable overcurrent detection circuitry and wire-harness optimization, the vehicle is lighter.

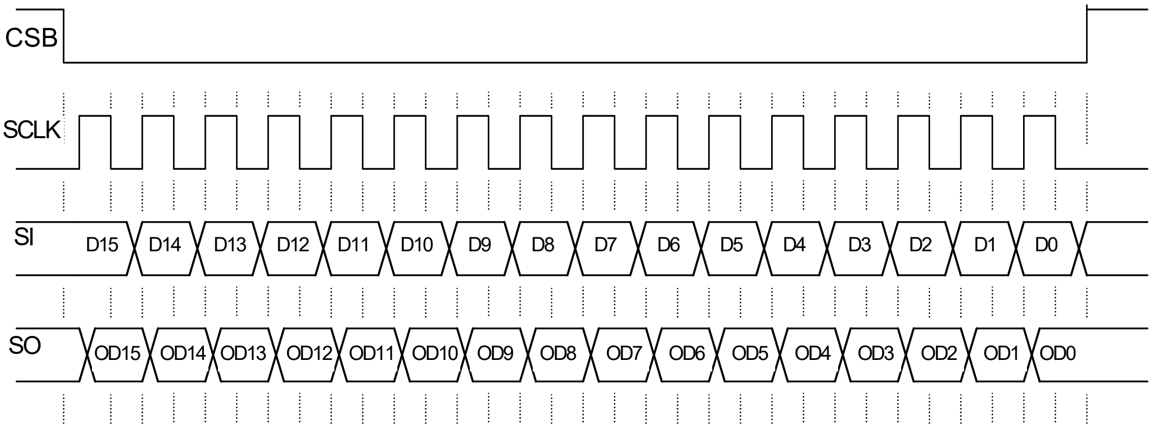
In Fail-safe mode, each lamp is controlled with dedicated parallel input pins. The device is configured in Default mode.

6 Functional device operation

6.1 SPI protocol description

The SPI interface has a full duplex, three-wire synchronous data transfer with four I/O lines associated with it: Serial Input (SI), Serial Output (SO), Serial Clock (SCLK), and Chip Select (CSB).

The SI/SO pins of the 10XS3425 follow a first-in first-out (D15 to D0) protocol, with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 5.0 or 3.3 V CMOS logic levels.



Notes 1. RSTB is a logic [1] state during the above operation.
2. D15:D0 relate to the most recent ordered entry of data into the device.
3. OD15:OD0 relate to the first 16 bits of ordered fault and status data out of the device.

Figure 10. Single 16-bit word SPI communication

6.2 Operational modes

The 10XS3425 has four operating modes: Sleep, Normal, Fail-Safe and Fault. Table 6 and Figure 12 summarize details contained in succeeding paragraphs.

The Figure 11 describes an internal signal called IN_ON[x] depending on IN[x] input.

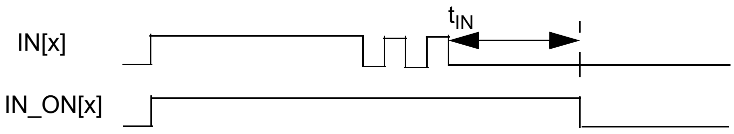


Figure 11. IN_ON[x] internal signal

The 10XS3425 transits to operating modes according to the following signals:

- wake-up = RSTB or WAKE or IN_ON[0] or IN_ON[1] or IN_ON[2] or IN_ON[3],
- fail = (V_{DD} Failure and VDD_FAIL_en) or (Watchdog timeout and FSI input not shorted to ground),
- fault = OC[0:3] or OT[0:3] or SC[0:3] or UV or (OV and $\overline{\text{OV\_dis}}$).

Table 6. 10XS3425 operating modes

Mode	Wake-up	Fail	Fault	Comments
Sleep	0	x	x	Device is in Sleep mode. All outputs are OFF.
Normal	1	0	0	Device is currently in Normal mode. Watchdog is active if enabled.
Fail-Safe	1	1	0	Device is currently in Fail-safe mode due to Watchdog timeout or V_{DD} Failure conditions. The output states are defined with the RFS resistor connected to FSI.
Fault	1	X	1	Device is currently in fault mode. The faulted output(s) is (are) OFF. The safe autoretry circuitry is active to turn-on again the output(s).

x = Don’t care.

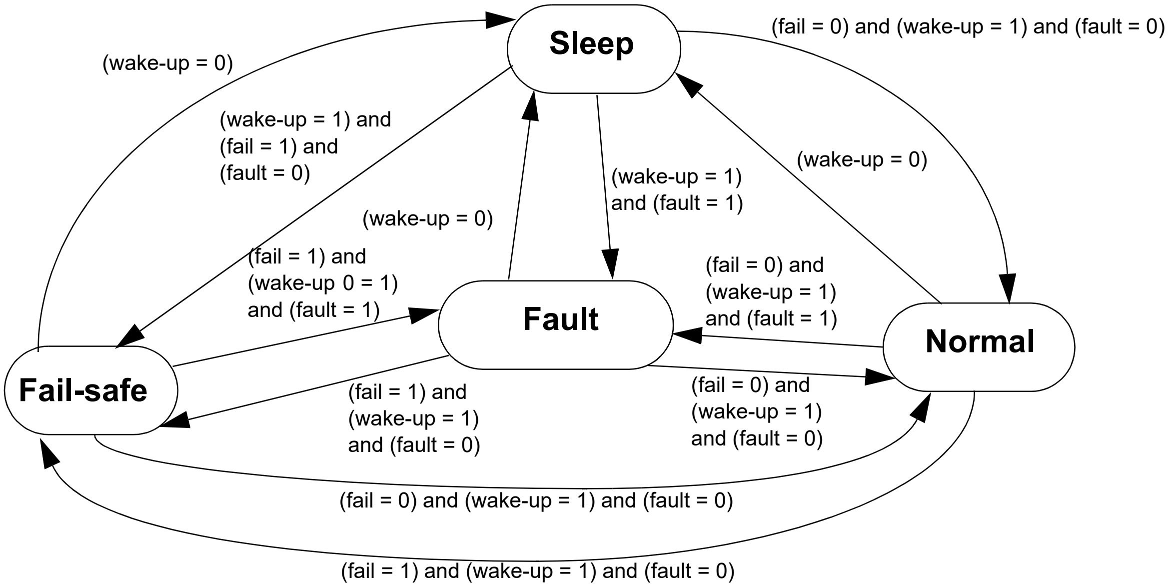


Figure 12. Operating modes

6.2.1 Sleep mode

The 10XS3425 is in Sleep mode when:

- V_{PWR} and V_{DD} are within the normal voltage range,
- wake-up = 0,
- fail = X,
- fault = X.

This is the Default mode of the device after first applying battery voltage (V_{PWR}) prior to any I/O transitions. This is also the state of the device when the WAKE and RSTB and IN_ON[0:3] are logic [0]. In the Sleep mode, the output and all unused internal circuitry, such as the internal regulator, are off to minimize draw current. In addition, all SPI-configurable features of the device are as if set to logic [0].

6.2.2 Normal mode

The 10XS3425 is in Normal mode when:

- V_{PWR} and V_{DD} are within the normal voltage range,
- wake-up = 1,
- fail = 0,
- fault = 0.

In this mode, the NM bit is set to lfault_contrologic [1] and the outputs HS[0:3] are under control, as defined by hson signal:

hson[x] = (((IN[x] and $\overline{\text{DIR\_dis}}$[x]) or On bit[x]) and $\overline{\text{PWM\_en}}$) or (On bit [x] and Duty_cycle[x] and PWM_en).

In this mode and also in Fail-safe, the fault condition reset depends on fault_control signal, as defined by the following:

fault_control[x] = ((IN_ON[x] and $\overline{\text{DIR\_dis}}$[x]) and $\overline{\text{PWM\_en}}$) or (On bit [x]).

6.2.2.1 Programmable PWM module

The outputs HS[0:3] are controlled by the programmable PWM module if PWM_en and the ON bits are set to logic [1].

The clock frequency from IN0 input pin or from internal clock is the factor 2^7 (128) of the output PWM frequency (CLOCK_sel bit). The outputs HS[0:3] can be controlled in the range of 5.0 to 98 % with a resolution of seven bits of duty cycle (Table 7). The state of other IN pin is ignored.

Table 7. Output PWM resolution

On bit	Duty cycle	Output state
0	**X**	**OFF**
1	0000000	PWM (1/128 duty cycle)
1	0000001	PWM (2/128 duty cycle)
1	0000010	PWM (3/128 duty cycle)
1	n	PWM ((n+1)/128 duty cycle)
1	1111111	fully ON

The timing includes seven programmable PWM switching delay (number of PWM clock rising edges) to improve overall EMC behavior of the light module (Table 8).

Table 8. Output PWM switching delay

Delay bits	Output delay
000	no delay
001	16 PWM clock periods
010	32 PWM clock periods
011	48 PWM clock periods
100	64 PWM clock periods
101	80 PWM clock periods
110	96 PWM clock periods
111	112 PWM clock periods

The clock frequency from IN0 is permanently monitored in order to report a clock failure in case the frequency is out of the specified frequency range (from $f_{IN0(LOW)}$ to $f_{IN0(HIGH)}$). In case of a clock failure, no PWM feature is provided, the On bit defines the outputs state and the CLOCK_fail bit reports [1].

6.2.2.2 Calibratable internal clock

The internal clock can vary as much as ±30 %, corresponding to a typical $f_{PWM(0)}$ output switching period.

Using the existing SPI inputs and the precision timing reference already available to the MCU, the 10XS3425 allows clock period setting within ±10 % accuracy. Calibrating the internal clock is initiated by defined word to CALR register. The calibration pulse is provided by the MCU. The pulse is sent on the CSB pin after the SPI word is launched. At the moment, the CSB pin transitions from a logic [1] to [0], until from a logic [0] to [1], determine the period of the internal clock with a multiplicative factor of 128.

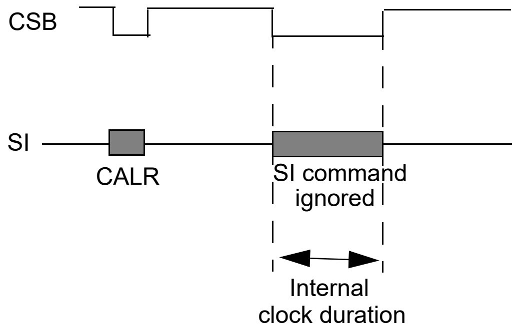


Figure 13. Internal clock calibration diagram

In case a negative CSB pulse is outside a predefined time range (from $t_{CSB(MIN)}$ to $t_{CSB(MAX)}$), the calibration event will be ignored and the internal clock will be unaltered, or reset to the default value ($f_{PWM(0)}$), if this was not calibrated before.

The calibratable clock is used instead of the clock from the IN0 input, when CLOCK_sel is set to [1].

6.2.3 Fail-safe mode

The 10XS3425 is in Fail-safe mode when:

- V_{PWR} is within the normal voltage range,
- wake-up = 1,
- fail = 1,
- fault = 0.

6.2.3.1 Watchdog

If the FSI input is not grounded, the watchdog timeout detection is active when either the WAKE, or IN_ON[0:3], or RSTB input pin transitions from logic [0] to logic [1]. The WAKE input is capable of being pulled up to V_{PWR} with a series of limiting resistance limiting the internal clamp current according to the specification.

The Watchdog timeout is a multiple of an internal oscillator. As long as the WD bit (D15) of an incoming SPI message is toggled within the minimum watchdog timeout period (WDTO), the device will operate normally.

6.2.3.2 Fail-safe conditions

If an internal watchdog timeout occurs before the WD bit for FSI open (Table 9) or in case of a V_{DD} failure condition ($V_{DD} < V_{DD(FAIL)}$) for VDD_FAIL_en bit is set to logic [1], the device will revert to a Fail-safe mode until the WD bit is written to a logic [1] (see fail-safe to normal mode transition paragraph) and V_{DD} is within the normal voltage range.

Table 9. SPI watchdog activation

Typical RFSI (Ω)	Watchdog
0 (shorted to ground)	Disabled
(open)	Enabled

During the Fail-safe mode, the outputs will depend on the corresponding input. The SPI register content is reset to their default value (except POR bit) and fault protections are fully operational. The Fail-safe mode can be detected by monitoring the NM bit is set to [0].

6.2.4 Normal and fail-safe mode transitions

6.2.4.1 Transition fail-safe to normal mode

To leave the Fail-safe mode, V_{DD} must be in nominal voltage and the microcontroller has to send a SPI command with the WDIN bit set to logic [1]; the other bits are not considered. The previous latched faults are reset by the transition into Normal mode (autoretry included).

Moreover, the device can be brought out of the Fail-safe mode due to a watchdog timeout issue, by forcing the FSI pin to logic [0].

6.2.4.2 Transition normal to fail-safe mode

To leave the Normal mode, a fail-safe condition must occurred (fail=1). The previous latched faults are reset by the transition into Fail-safe mode (autoretry included).

6.2.5 Fault mode

The 10XS3425 is in Fault mode when:

- V_{PWR} and V_{DD} are within the normal voltage range
- wake-up = 1
- fail = X
- fault=1

This device indicates the faults below as they occur by driving the FSB pin to logic [0] for RSTB input is pulled up:

- Overtemperature fault
- Overcurrent fault
- Severe short-circuit fault
- Output(s) shorted to VPWR fault in OFF state
- Openload fault in OFF state
- Overvoltage fault (enabled by default)
- Undervoltage fault

The FSB pin will automatically return to logic [1] when the fault condition is removed, except for overcurrent, severe short-circuit, overtemperature, and undervoltage which will be reset by a new turn-on command (each fault_control signal to be toggled).

Fault information is retained in the SPI fault register and is available (and reset) via the SO pin during the first valid SPI communication.

The openload fault in ON state is only reported through SPI register without effect on the corresponding output state (HS[x]) and the FSB pin.

6.2.6 Start-up sequence

The 10XS3425 enters in Normal mode after start-up if following sequence is provided:

- VPWR and VDD power supplies must be above their undervoltage thresholds
- Generate wake-up event (wake-up = 1) from 0 to 1 on RSTB. The device switches to Normal mode with the SPI register content reset (as defined in Table 11 and Table 23). All features of the 10XS3425 will be available after 50 μs (typical), and all SPI registers are set to default values (set to logic [0]).
- Toggle WD bit from 0 to 1

And, in case of the PWM module is used (PWM_en bit is set to logic [1]) with an external reference clock:

- Apply the PWM clock on the IN0 input pin after a maximum of 200 μs (min. 50 μs)

If the correct start-up sequence is not provided, the PWM function is not guaranteed.

6.3 Protection and diagnostic features

6.3.1 Protections

6.3.1.1 Overtemperature fault

The 10XS3425 incorporates overtemperature detection and shutdown circuitry for each output structure.

Two cases need to be considered when the output temperature is higher than T_{SD}:

- If the output command is ON: the corresponding output is latched OFF. FSB will be also latched to logic [0]. To delatch the fault and be able to turn the outputs ON again, the failure condition must disappear and the autoretry circuitry must be active, or the corresponding output must be commanded OFF and then ON (toggling fault_control signal of corresponding output), or $V_{SUPPLY(POR)}$ condition, if V_{DD} = 0.
- If the output command is OFF: FSB will go to logic [0] till the corresponding output temperature will be below T_{SD}.

For both cases, the fault register OT[0:3] bit into the status register will be set to [1]. The fault bits will be cleared in the status register after a SPI read command.

6.3.1.2 Overcurrent fault

The 10XS3425 incorporates output shutdown, to protect each output structure against a resistive short-circuit condition. This protection is composed by eight predefined current levels (time dependent) to fit Xenon-HID manners by default or 55 W (HS[0,1]) or 28 W (HS[2,3]) bulb profiles, selectable by Xenon bit (as illustrated in Figure 17).

At the first turn-on, the lamp filament is cold and the current will be huge. The fault_control signal transition from logic [0] to [1], or an autoretry define this event. In this case, the overcurrent protection will be fitted to inrush current, as shown in Figure 5. This overcurrent protection is programmable: OC[1:0] bits select the overcurrent slope speed and the OCHI1 current step can be removed in case the OCHI bit is set to [1].

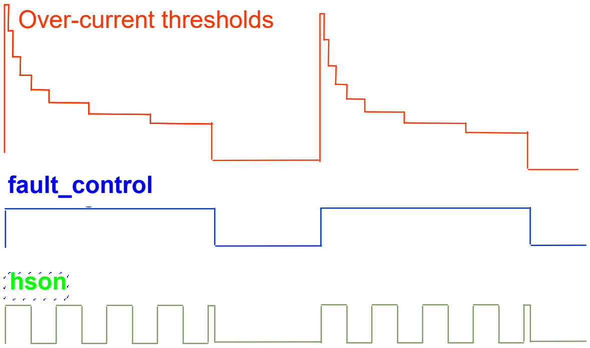


Figure 14. Overcurrent detection profile

In steady state, the wire harness will be protected by a OCLO2 current level by default. Three other DC overcurrent levels are available: OCLO1, or OCLO3, or OCLO4, based on the state of the OCLO[1,0] bits.

If the load current level ever reaches the overcurrent detection level, the corresponding output will latch the output OFF and FSB will be also latched to logic [0]. To delatch the fault and be able to turn the corresponding output ON again, the failure condition must disappear and the autoretry circuitry must be active, or the corresponding output must be commanded OFF and then ON (toggling fault_control signal of corresponding output), or $V_{SUPPLY(POR)}$ condition, if V_{DD} = 0.

The SPI fault report (OC[0:3] bits) is removed after a read operation.

In Normal mode using the internal PWM module, the 10XS3425 also incorporates a cooling bulb filament management, if OC_mode and Xenon are set to logic [1]. In this case, the first step of multi-step overcurrent protection will depend on the previous OFF duration, as illustrated in Figure 6. The following figure illustrates the current level that will be used in the function to the duration of the previous OFF state (t_{OFF}). The slope of the cooling bulb emulator is configurable with OCOFFCB[1:0] bits.

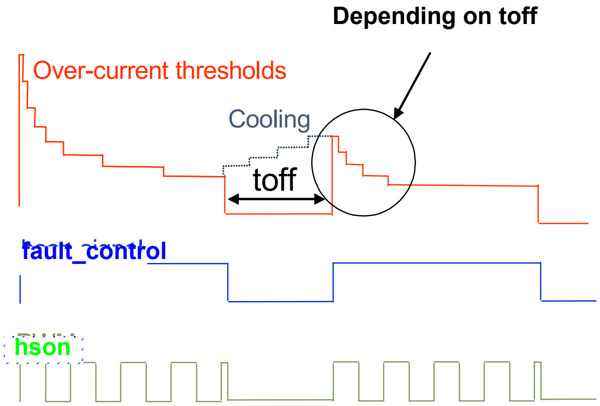


Figure 15. Bulb cooling principle

6.3.1.3 Severe short-circuit fault

The 10XS3425 provides output shutdown to protect each output, in case of a severe short-circuit during the output switching.

If the short-circuit impedance is below $R_{SHORT,}$ the device will latch the output OFF, FSB will go to a logic [0] and the fault register SC[0:3] bit will be set to [1]. To delatch the fault and be able to turn the outputs ON again, the failure condition must disappear, and the corresponding output must be commanded OFF and then ON (toggling fault_control signal of corresponding output), or $V_{SUPPLY(POR)}$ condition if $V_{DD} = 0$.

The SPI fault report (SC[0:3] bits) is removed after a read operation.

6.3.1.4 Overvoltage fault (enabled by default)

By default, the overvoltage protection is enabled. The 10XS3425 shuts down all outputs and FSB will go to a logic [0] during an overvoltage fault condition on the VPWR pin ($V_{PWR} \geq V_{PWR(OV)}$). The outputs remain in the OFF state until the overvoltage condition is removed ($V_{PWR} \leq V_{PWR(OV)} - V_{PWR(OVHYS)}$). When experiencing this fault, the OVF fault bit is set to logic [1] and cleared after either a valid SPI read.

The overvoltage protection can be disabled through the SPI (OV_dis bit is disabled set to logic [1]). The fault register reflects any overvoltage condition ($V_{PWR} \geq V_{PWR(OV)}$). This overvoltage diagnosis, as a warning, is removed after a read operation, if the fault condition disappears. The HS[0:3] outputs are not commanded in $R_{DS(on)}$ above the OV threshold.

6.3.1.5 Undervoltage fault

The output(s) will latch off at some battery voltage below $VPWR_{(UV)}$. As long as the V_{DD} level stays within the normal specified range, the internal logic states within the device will remain (configuration and reporting).

In the case where battery voltage drops below the undervoltage threshold ($V_{PWR} \leq V_{PWR(UV)}$), the outputs will turn off, FSB will go to logic [0], and the fault register UV bit will be set to [1].

Two cases need to be considered when the battery level recovers ($V_{PWR} > V_{PWR(UV)\_UP}$):

- If the output command is low, FSB will go to a logic [1], but the UV bit will remain set to 1 until the next read operation (warning report).
- If the output command is ON, FSB will remain at logic [0]. To delatch the fault and be able to turn the outputs ON again, the failure condition must disappear and the autoretry circuitry must be active, or the corresponding output must be commanded OFF and then ON (toggling fault_control signal of corresponding output), or a $V_{SUPPLY(POR)}$ condition, if $V_{DD} = 0$.

In extended mode, the output is protected by overtemperature shutdown circuitry. All previous latched faults, occurred when V_{PWR} is within the normal voltage range, are guaranteed if V_{DD} is within the operational voltage range, or until $V_{SUPPLY(POR)}$, if VDD = 0. Any new OT fault is detected (VDD failure included) and reported through SPI above $VPWR_{(UV)}$. The output state is not changed, as long as the VPWR voltage does not drop any lower than 3.5 V (typical).

All latched faults (overtemperature, overcurrent, severe short-circuit, over and undervoltage) are reset if:

- $V_{DD} \leq V_{DD(FAIL)}$ with V_{PWR} in nominal voltage range,
- V_{DD} and V_{PWR} supplies is below the $V_{SUPPLY(POR)}$ voltage value.

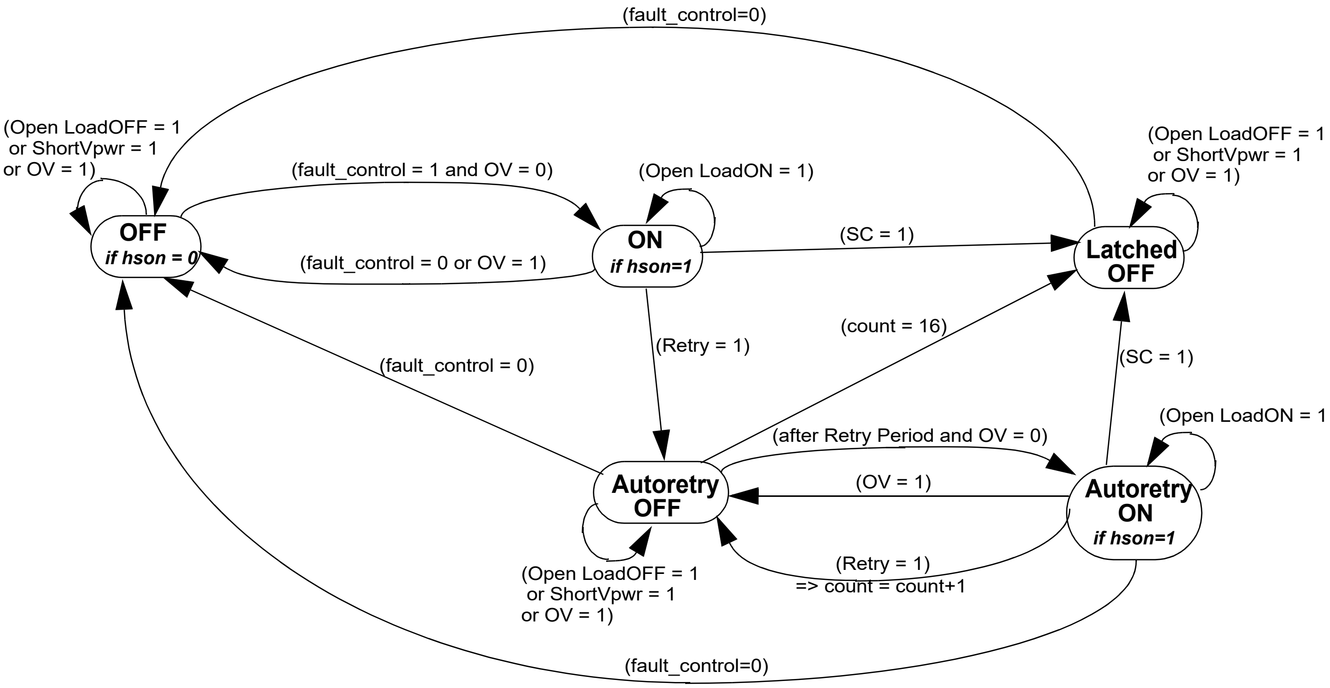


Figure 16. Autoretry state machine

6.3.2 Autoretry

The autoretry circuitry is used to reactivate the output(s) automatically, in case of an overcurrent, overtemperature, or undervoltage failure conditions to provide a high availability of the load.

Autoretry feature is available in Fault mode. It is activated in case of an internal retry signal is set to a logic [1]:

retry[x] = OC[x] or OT[x] or UV.

The feature retries to switch-on the output(s) after one autoretry period (t_{AUTO}) with a limitation in term of the number of occurrences (16 for each output). The counter of retry occurrences is reset in case of Fail-safe to Normal or Normal to Fail-safe mode transitions. At each autoretry, the overcurrent detection will be set to default values in order to sustain the inrush current.

Figure 16 describes the autoretry state machine.

6.3.3 Diagnostic

6.3.3.1 Output shorted to VPWR fault

The 10XS3425 incorporates output shorted to VPWR detection circuitry in the OFF state. An output shorted to VPWR fault is detected if the output voltage is higher than $V_{OSD(THRES)}$ and reported as a fault condition when the output is disabled (OFF). The output shorted to VPWR fault is latched into the status register after the internal gate voltage is pulled low enough to turn OFF the output. The OS[0:3] and OL_OFF[0:3] fault bits are set in the status register and the FSB pin reports the fault in real time. If the output shorted to VPWR fault is removed, the status register will be cleared after reading the register.

The open output shorted to VPWR protection can be disabled through the SPI (OS_DIS[0:3] bit).

6.3.3.2 Openload faults

The 10XS3425 incorporates three dedicated openload detection circuitries on the output to detect in OFF and in ON states.

6.3.3.3 Openload detection in OFF state

The OFF output Openload fault is detected when the output voltage is higher than $V_{OLD(THRES)}$ pulled up with internal current source ($I_{OLD(OFF)}$), and reported as a fault condition when the output is disabled (OFF). The OFF Output openload fault is latched into the status register, or when the internal gate voltage is pulled low enough to turn the output OFF. The OL_OFF[0:3] fault bit is set in the status register. If the openload fault is removed (FSB output pin goes to high), the status register will be cleared after reading the register.

The OFF output openload protection can be disabled through the SPI (OLOFF_DIS[0:3] bit).

6.3.3.4 Openload detection in ON state

The ON output openload current thresholds can be chosen by the SPI to detect a standard bulb or LED (OLLED[0:3] bit set to logic [1]). In the case where the load current drops below the defined current threshold, the OLON bit is set to logic [1], the output stays ON, and FSB is not disturbed.

6.3.3.5 Openload detection in ON state for LED

Openload for LEDs only (OLLED[0:3] set to logic [1]) is detected periodically at each t_{OLLED} (fully-on, D[7:0]=FF). To detect OLLED in a fully ON state, the output must be ON at least t_{OLLED} and PWM module must be enabled (PWM_en = 1 in GCR register).

To delatch the diagnosis, the condition should be removed and a SPI read operation is needed (OL_ON[0:3] bit). The ON output openload protection can be disabled through the SPI (OLON_DIS[0:3] bit).

6.3.4 Analog current recopy and temperature feedback

The CSNS pin is an analog output reporting a current proportional to the designed output current, or a voltage proportional to the temperature of the GND flag (pin #14). The routing is SPI programmable (TEMP_en, CSNS_en, CSNS_s[1,0] and CSNS_ratio_s bits).

In case the current recopy is active, the CSNS output delivers current only during the ON time of the output switch without overshoot. The maximum current is 2.0 mA (typical). The typical value of the external CSNS resistor connected to ground is 2.5 kΩ.

The current recopy is not active in Fail-safe mode.

6.3.4.1 Temperature prewarning detection

In Normal mode, the 10XS3425 provides a temperature prewarning reported via the SPI, in case the temperature of the GND flag is higher than T_{OTWAR}. This diagnosis (OTW bit set to [1]) is latched in the SPI DIAGR0 register. To delatch, a SPI read command is needed.

6.3.5 Active clamp on VPWR

The device provides an active gate clamp circuit, to limit the maximum transient VPWR voltage at $VPWR_{(CLAMP)}$. In case of an overload on an output the corresponding output is turned off, which leads to high voltage at VPWR with an inductive VPWR line. When VPWR voltage exceeds the $VPWR_{(CLAMP)}$ threshold, the turn-off on the corresponding output is deactivated and all HS[0:3] outputs are switched ON automatically, to demagnetize the inductive battery line.

For long battery line (> 10 meters, corresponding to 10 μH of parasitic inductance) between the battery and the device, the smart high-side switch output may be damaged, in cases of short-circuit due to unexpected behavior of internal active gate clamp circuitry. It is essential not to exceed the maximum rating on the VPWR pin (41 V).

6.3.6 Reverse battery on VPWR

The output survives the application of reverse voltage as low as -18 V. Under these conditions, the ON resistance of the output is two times higher than the typical ohmic value in forward mode. No additional passive components are required except on the V_{DD} current path.

6.3.7 Ground disconnect protection

In the event the 10XS3425 ground is disconnected from load ground, the device protects itself and safely turns OFF the output, regardless of the state of the output at the time of disconnection (maximum V_{PWR} = 16 V). A 10 kΩ resistor needs to be added between the MCU and each digital input pin, to ensure that the device turns off during ground disconnects and to prevent this pin from exceeding maximum ratings.

6.3.8 Loss of supply lines

6.3.8.1 Loss of V_{DD}

If the external V_{DD} supply is disconnected (or not within specification: VDD < $VDD_{(FAIL)}$ with the VDD_FAIL_en bit set to a logic [1]), all SPI register content is reset.

The outputs can still be driven by the direct inputs IN[0:3] if V_{PWR} is within specified voltage range. The 10XS3425 uses the battery input to power the output MOSFET-related current sense circuitry, and any other internal logic providing Fail-safe device operation with no V_{DD} supplied. In this state, the overtemperature, overcurrent, severe short-circuit, short to VPWR and OFF openload circuitry, are fully operational with default values corresponding to all SPI bits. These are set to logic [0].

An unexpected Power-On Reset ($V_{SUPPLY(POR)}$) may occur at 4.8 V of V_{PWR}. The extended battery voltage range specified from 4.0 to 28 V is reduced from 5.0 to 28 V. If the battery voltage drops below 5.0 V, the outputs will be turned off by the POR instead of undervoltage (UV). In this case, the outputs will turn on again once the battery voltage recovers to a nominal voltage. The counter of autoretry will be also reset. So, it is recommended to command “off” the outputs when the battery voltage is below 5.0 V.

No current is conducted from V_{PWR} to V_{DD}.

6.3.8.2 Loss of V_{PWR}

If the external V_{PWR} supply is disconnected (or not within specification), the SPI configuration, reporting, and daisy chain features are provided for RSTB to set to a logic [1] under V_{DD} in nominal conditions. This fault condition can be diagnosed with a UV fault in SPI STATR_s registers. The SPI pull-up and pull-down current sources are not operational. The previous device configuration is maintained. No current is conducted from V_{DD} to V_{PWR}.

6.3.8.3 Loss of V_{PWR} and V_{DD}

If the external V_{PWR} and V_{DD} supplies are disconnected (or not within specification: (V_{DD} and V_{PWR}) < $V_{SUPPLY(POR)}$), all SPI register contents are reset with default values corresponding to all SPI bits set to logic [0] and all latched faults are reset.

6.3.9 EMC performances

All following tests are performed on a NXP evaluation board, in accordance with the typical application schematic.

The device is protected, in case of positive and negative transients on the V_{PWR} line (per ISO 7637-2).

The 10XS3425 successfully meets the Class 5 of the CISPR25 emission standard and 200 V/m or BCI 200 mA injection level for immunity tests.

6.4 Logic commands and registers

6.4.1 Serial input communication

SPI communication is accomplished using 16-bit messages. A message is transmitted by the MCU starting with the MSB D15 and ending with the LSB, D0 (Table 10). Each incoming command message on the SI pin can be interpreted using the following bit assignments: the MSB, D15, is the watchdog bit (WDIN). In some cases, output selection is done with bits D14:D13. The next three bits, D12:D10, are used to select the command register. The remaining nine bits, D8:D0, are used to configure and control the outputs and their protection features.

Multiple messages can be transmitted in succession to accommodate those applications where daisy chaining is desirable, or to confirm transmitted data, as long as the messages are all multiples of 16 bits. Any attempt made to latch in a message that is not 16 bits will be ignored.

The 10XS3425 has defined registers, which are used to configure the device and to control the state of the outputs. Table 11 summarizes the SI registers.

Table 10. SI message bit assignment

Bit Sig	SI Msg bit	Message bit description
MSB	D15	Watchdog in: toggled to satisfy watchdog requirements.
	D14:D13	Register address bits used in some cases for output selection (Table 11).
	D12:D10	Register address bits.
	D9	Not used (set to logic [0]).
LSB	D8:D0	Used to configure the inputs, outputs, and the device protection features and SO status content.

Table 11. Serial input address and configuration bit map

SI Register	SI Data															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STATR_s	WDIN	X	X	0	0	0	0	0	0	0	0	SOA4	SOA3	SOA2	SOA1	SOA0
PWMR_s	WDIN	A_1	A_0	0	0	1	0	0 (44)	ON_s	PWM6_s	PWM5_s	PWM4_s	PWM3_s	PWM2_s	PWM1_s	PWM0_s
CONFR0_s	WDIN	A_1	A_0	0	1	0	0	0	0	0	DIR_dis_s	SR1_s	SR0_s	DELAY2_s	DELAY1_s	DELAY0_s
CONFR1_s	WDIN	A_1	A_0	0	1	1	0	0	0	Retry_unlimited_s	Retry_dis_s	OS_dis_s	OLON_dis_s	OLOFF_dis_s	OLLED_en_s	CSNS_ratio_s
OCR_s	WDIN	A_1	A_0	1	0	0	0	Xenon_s	BC1_s	BC0_s	OC1_s	OC0_s	OCHI_s	OLCO1_s	OLCO0_s	OC_mode_s
GCR	WDIN	0	0	1	0	1	0	VDD_FAIL_en	PWM_en	CLOCK_sel	TEMP_en	CSNS_en	CSNS1	CSNS0	X	OV_dis
CALR	WDIN	0	0	1	1	1	0	1	0	1	0	1	1	0	1	1
Register state after RSTB = 0 or $V_{DD(FAIL)}$ or $V_{SUPPLY(POR)}$ condition	0	0	0	X	X	X	0	0	0	0	0	0	0	0	0	0

x = Don't care.
s = Output selection with the bits A_1A_0 as defined in Table 12.

Notes

44. The PWMR_s D8 bit must always be a logic low and never placed in a logic high.

6.4.2 Device register addressing

The following section describes the possible register addresses (D[14:10]) and their impact on device operation.

6.4.2.1 Address XX000—Status register (STATR_S)

The STATR register is used to read the device status and the various configuration register contents without disrupting the device operation or the register contents. The register bits D[4:0] determine the content of the first sixteen bits of SO data. In addition to the device status, this feature provides the ability to read the content of the PWMR_s, CONFR0_s, CONFR1_s, OCR_s, GCR and CALR registers (see Serial output communication (device status return data).

6.4.2.2 Address $A_1A_0$001—Output PWM control register (PWMR_S)

The PWMR_s register allows the MCU to control the state of corresponding output through the SPI. Each output "s" is independently selected for configuration, based on the state of the D14:D13 bits (Table 12).

Table 12. Output selection

A_1 (D14)	A_0 (D13)	HS selection
0	0	HS0 (default)
0	1	HS1
1	0	HS2
1	1	HS3

Bit D7 sets the output state. A logic [1] enables the corresponding output switch and a logic [0] turns it OFF (if IN input is also pulled down). Bits D6:D0 set the output PWM duty-cycle to one of 128 levels for PWM_en is set to logic [1], as shown Table 7.

6.4.2.3 Address $A_1A_0$010—Output configuration register (CONFR0_S)

The CONFR0_s register allows the MCU to configure corresponding output switching through the SPI. Each output "s" is independently selected for configuration based on the state of the D14:D13 bits (Table 12).

For the selected output, a logic [0] on bit D5 (DIR_DIS_s) will enable the output for direct control. A logic [1] on bit D5 will disable the output from direct control (in this case, the output is only controlled by the On bit).

D4:D3 bits (SR1_s and SR0_s) are used to select the high, medium, or low speed slew rate for the selected output, the default value [00] corresponds to the medium speed slew rate (Table 13).

Table 13. Slew rate speed selection

SR1_s (D4)	SR0_s (D3)	Slew rate speed
0	0	medium (default)
0	1	low
1	0	high
1	1	Not used

Incoming message bits D2:D0 reflect the desired output that will be delayed of predefined PWM clock rising edges number, as shown Table 8 (only available for PWM_en bit is set to logic [1]).

6.4.2.4 Address $A_1A_0$011—Output configuration register (CONFR1_S)

The CONFR1_s register allows the MCU to configure corresponding output fault management through the SPI. Each output “s” is independently selected for configuration, based on the state of the D14:D13 bits (Table 12).

A logic [1] on bit D6 (RETRY_unlimited_s) disables the autoretry counter for the selected output, the default value [1] corresponds to enable autoretry feature without time limitation.

A logic [1] on bit D5 (RETRY_dis_s) disables the autoretry for the selected output, the default value [0] corresponds to enable this feature.

A logic [1] on bit D4 (OS_dis_s) disables the output hard shorted to V_{PWR} protection for the selected output, the default value [0] corresponds to enable this feature.

A logic [1] on bit D3 (OLON_dis_s) disables the ON output openload detection for the selected output, the default value [0] corresponds to enable this feature (Table 14).

A logic [1] on bit D2 (OLOFF_dis_s) disables the OFF output openload detection for the selected output, the default value [0] corresponds to enable this feature.

A logic [1] on bit D1 (OLLED_en_s) enables the ON output openload detection for LEDs for the selected output, the default value [0] corresponds to ON output openload detection is set for bulbs (Table 14).

Table 14. ON openload selection

OLON_dis_s (D3)	OLLED_en_s (D1)	ON openload detection
0	0	enable with bulb threshold (default)
0	1	enable with LED threshold
1	X	disable

A logic [1] on bit D0 (CSNS_ratio_s) selects the high ratio on the CSNS pin for the corresponding output. The default value [0] is the low ratio (Table 15).

Table 15. Current sense ratio selection

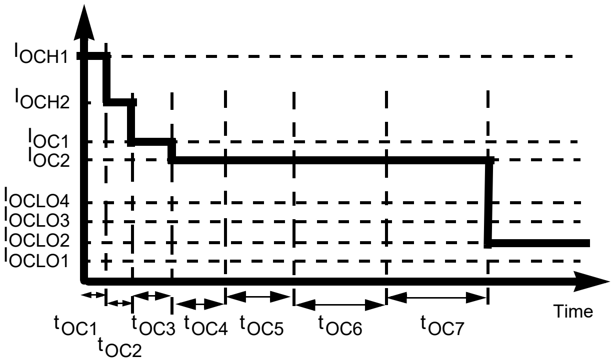
CSNS_high_s (D0)	Current sense ratio
0	CRS0 (default)
1	CRS1

6.4.2.5 Address $A_1A_0$100—Output overcurrent register (OCR)

The OCR_s register allows the MCU to configure corresponding output overcurrent protection through the SPI. Each output “s” is independently selected for configuration based on the state of the D14:D13 bits (Table 12).

A logic [1] on bit D8 ($\overline{\text{Xenon\_s}}$) disables the Xenon bulb overcurrent profile, as shown in Figure 17.

$\overline{\text{Xenon}}$ bit set to logic [0]:



$\overline{\text{Xenon}}$ bit set to logic [1]:

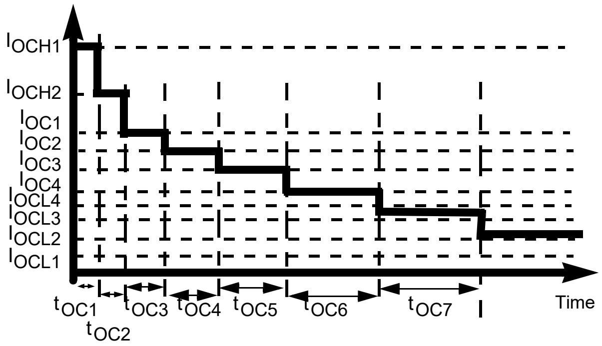


Figure 17. Overcurrent profile depending on $\overline{\text{xenon}}$ bit

D[7:6] bits allow to MCU to programmable the bulb cooling curve and D[5:4] bits inrush curve for the selected output, as shown Table 16 and Table 17.

Table 16. Cooling curve selection

BC1_s (D7)	BC0_s (D6)	Profile curves speed
0	0	medium (default)
0	1	slow
1	0	fast
1	1	medium

Table 17. Inrush curve selection

OC1_s (D5)	OC0_s (D4)	Profile curves speed
0	0	slow (default)
0	1	fast
1	0	medium
1	1	very slow

A logic [1] on bit D3 (OCHI_s bit) the OCHI1 level is replaced by OCHI2 during t_{OC1}, as shown Figure 18.

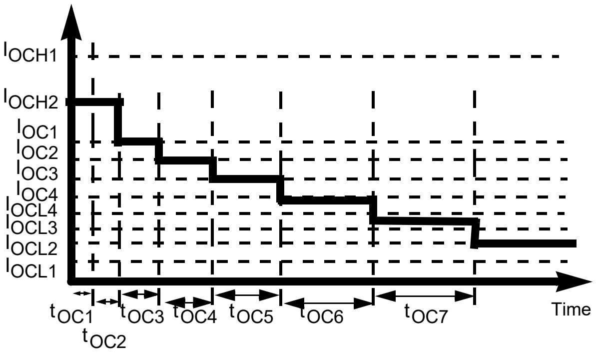


Figure 18. Overcurrent profile with OCHI bit set to ‘1’

The wire harness is protected by one of four possible current levels in steady state, as defined in Table 18.

Table 18. Output steady state selection

OCLO1 (D2)	OCLO0 (D1)	Steady state current
0	0	OCLO2 (default)
0	1	OCLO3
1	0	OCLO4
1	1	OCLO1

Bit D0 (OC_mode_sel) allows to select the overcurrent mode, as described Table 19.

Table 19. Overcurrent mode selection

OC_mode_s (D0)	Overcurrent mode
0	only inrush current management (default)
1	inrush current and bulb cooling management

6.4.2.6 Address 00101—Global configuration register (GCR)

The GCR register allows the MCU to configure the device through the SPI.

Bit D8 allows the MCU to enable or disable the VDD failure detector. A logic [1] on VDD_FAIL_en bit allows switch of the outputs HS[0:3] with PWMR register device in Fail-safe mode in case of $V_{DD} < V_{DD(FAIL)}$.

Bit D7 allows the MCU to enable or disable the PWM module. A logic [1] on PWM_en bit allows control of the outputs HS[0:3] with PWMR register (the direct input states are ignored).

Bit D6 (CLOCK_sel) allows to select the clock used as reference by PWM module, as described in the following Table 20.

Table 20. PWM module selection

PWM_en (D7)	CLOCK_sel (D6)	PWM module
0	X	PWM module disabled (default)
1	0	PWM module enabled with external clock from IN0
1	1	PWM module enabled with internal calibrated clock

Bits D5:D4 allow the MCU to select one of two analog feedbacks on CSNS output pin, as shown in Table 21.

Table 21. CSNS reporting selection

TEMP_en (D5)	CSNS_en (D4)	CSNS reporting
0	0	CSNS tri-stated (default)
X	1	current recopy of selected output (D3:2] bits)
1	0	temperature on GND flag

Table 22. Output current recopy selection

CSNS1 (D3)	CSNS0 (D2)	CSNS reporting
0	0	HS0 (default)
0	1	HS1
1	0	HS2
1	1	HS3

The GCR register disables the overvoltage protection (D0). When this bits is [0], the overvoltage is enabled (default value).

6.4.2.7 Address 00111—calibration register (CALR)

The CALR register allows the MCU to calibrate internal clock, as explained in Figure 16.

6.4.3 Serial output communication (device status return data)

When the CSB pin is pulled low, the output register is loaded. Meanwhile, the data is clocked out MSB- (OD15-) first, as the new message data is clocked into the SI pin. The first sixteen bits of data clocking out of the SO, and following a CSB transition, is dependent upon the previously written SPI word.

Any bits clocked out of the Serial Output (SO) pin after the first 16 bits will be representative of the initial message bits clocked into the SI pin since the CSB pin first transitioned to a logic [0]. This feature is useful for daisy chaining devices as well as message verification.

A valid message length is determined following a CSB transition of [0] to [1]. If there is a valid message length, the data is latched into the appropriate registers. A valid message length is a multiple of 16 bits. At this time, the SO pin is tri-stated and the fault status register is now able to accept new fault status information.

SO data will represent information ranging from fault status to register contents, user selected by writing to the STATR bits OD4, OD3, OD2, OD1, and OD0. The value of the previous bits SOA4 and SOA3 will determine which output the SO information applies to for the registers, which are output specific; viz., Fault, PWMR, CONFR0, CONFR1, and OCR registers.

Note that the SO data will continue to reflect the information for each output (depending on the previous SOA4, SOA3 state) that was selected during the most recent STATR write until changed with an updated STATR write.

The output status register correctly reflects the status of the STATR-selected register data at the time that the CSB is pulled to a logic [0] during SPI communication, and/or for the period of time since the last valid SPI communication, with the following exception:

- The previous SPI communication was determined to be invalid. In this case, the status will be reported as though the invalid SPI communication never occurred.
- The V_{PWR} voltage is below 4.0 V, the status must be ignored by the MCU.

6.4.4 Serial output bit assignment

The 16 bits of serial output data depend on the previous serial input message, as explained in the following paragraphs. Table 23, summarizes SO returned data for bits OD15:OD0.

- Bit OD15 is the MSB; it reflects the state of the watchdog bit from the previously clocked-in message
- Bits OD14:OD10 reflect the state of the bits SOA4:SOA0 from the previously clocked-in message
- Bit OD9 is set to logic [1] in Normal mode (NM)
- The contents of bits OD8:OD0 depend on bits D4:D0 from the most recent STATR command SOA4:SOA0 as explained in the paragraphs following Table 23.

Table 23. Serial output bit map description

	Previous STATR					SO returned data															
	SOA4	**SOA3**	**SOA2**	**SOA1**	**SOA0**	**OD15**	**OD14**	**OD13**	**OD12**	**OD11**	**OD10**	**OD9**	**OD8**	**OD7**	**OD6**	**OD5**	**OD4**	**OD3**	**OD2**	**OD1**	**OD0**
STATR_s	A_1	A_0	0	0	0	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	POR	UV	OV	OLON_s	OLOFF_s	OS_s	OT_s	SC_s	OC_s
PWMR_s	A_1	A_0	0	0	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	0	ON_s	PWM6_s	PWM5_s	PWM4_s	PWM3_s	PWM2_s	PWM1_s	PWM0_s
CONFR0_s	A_1	A_0	0	1	0	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	X	DIR_dis_s	SR1_s	SR0_s	DELAY2_s	DELAY1_s	DELAY0_s
CONFR1_s	A_1	A_0	0	1	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	Retry_unlimited_s	Retry_dis_s	OS_dis_s	OLON_dis_s	OLOFF_dis_s	OLLED_en_s	CSNS_ratio_s
OCR_s	A_1	A_0	1	0	0	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	Xenon_s	BC1_s	BC0_s	OC1_s	OC0_s	OCHI_s	OCLO1_s	OCLO0_s	OC_mode_s
GCR	0	0	1	0	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	VDD_FAIL_en	PWM_en	CLOCK_sel	TEMP_en	CSNS_en	CSNS1	CSNS0	X	OV_dis
DIAGR0	0	0	1	1	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	X	X	X	X	CLOCK_fail	CAL_fail	OTW
DIAGR1	0	1	1	1	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	X	X	IN3	IN2	IN1	IN0	WD_en
DIAGR2	1	0	1	1	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	X	X	X	X	0	1	1
Register state after RST=0 or $V_{DD(FAIL)}$ or $V_{SUPPLY(POR)}$ condition	N/A	N/A	N/A	N/A	N/A	0	0	0	0	0	0	0	X	0	0	0	0	0	0	0	0

s = Output selection with the bits A_1A_0 as defined in Table 12

6.4.4.1 Previous address SOA4:SOA0 = $A_1A_0$000 (STATR_S)

The returned data OD8 reports logic [1] in case of previous power-on reset condition ($V_{SUPPLY(POR)}$). This bit is only reset by a read operation.

Bits OD7:OD0 reflect the current state of the Fault register (FLTR) corresponding to the output previously selected with the bits SOA4:SOA3 = A_1A_0 (Table 23).

- OC_s: overcurrent fault detection for a selected output
- SC_s: severe short-circuit fault detection for a selected output
- OS_s: output shorted to V_{PWR} fault detection for a selected output
- OLOFF_s: openload in OFF state fault detection for a selected output
- OLON_s: openload in ON state fault detection (depending on current level threshold: bulb or LED) for a selected output,
- OV: overvoltage fault detection
- UV: undervoltage fault detection
- POR: power on reset detection

The FSB pin reports all faults. For latched faults, this pin is reset by a new Switch OFF command (toggling fault_control signal).

6.4.4.2 Previous address SOA4:SOA0 = $A_1A_0$001 (PWMR_S)

The returned data contains the programmed values in the PWMR register for the output selected with A_1A_0.

6.4.4.3 Previous address SOA4:SOA0 = $A_1A_0$010 (CONFR0_S)

The returned data contains the programmed values in the CONFR0 register for the output selected with A_1A_0.

6.4.4.4 Previous address SOA4:SOA0 = $A_1A_0$011 (CONFR1_S)

The returned data contains the programmed values in the CONFR1 register for the output selected with A_1A_0.

6.4.4.5 Previous address SOA4:SOA0 = $A_1A_0$100 (OCR_S)

The returned data contains the programmed values in the OCR register for the output selected with A_1A_0.

6.4.4.6 Previous address SOA4:SOA0 = 00101 (GCR)

The returned data contains the programmed values in the GCR register.

6.4.4.7 Previous address SOA4:SOA0 = 00111 (DIAGR0)

The returned data OD2 reports logic [1] in case of PWM clock on IN0 pin is out of specified frequency range.

The returned data OD1 reports logic [1] in case of calibration failure.

The returned data OD0 reports logic [1] in case of overtemperature prewarning (temperature of GND flag is above T_{OTWAR}).

6.4.4.8 Previous address SOA4:SOA0 = 01111 (DIAGR1)

The returned data OD4: OD1 report in real time the state of the direct input IN[3:0].

The OD0 indicates if the watchdog is enabled (set to logic [1]) or not (set to logic [0]). OD4:OD1 report the output state in case of Fail-safe state due to watchdog time-out as explained in the following Table 24.

Table 24. Watchdog activation report

WD_en (OD0)	SPI watchdog
0	disabled
1	enabled

6.4.4.9 Previous address SOA4:SOA0 = 10111 (DIAGR2)

The returned data is the product ID. Bits OD2:OD0 are set to 011 for Protected Dual 10 mΩ and 25 mΩ high-side switches.

6.4.5 Default device configuration

The default device configuration is explained by the following:

- HS output is commanded by corresponding IN input or ON bit through the SPI. The medium slew rate is used.
- HS output is fully protected by the Xenon overcurrent profile by default, the severe short-circuit protection, the undervoltage, and the overtemperature protection. The autoretry feature is enabled.
- Openload in ON and OFF state and HS shorted to V_{PWR} detections are available
- No current recopy and no analog temperature feedback active
- Overvoltage protection is enabled
- SO reporting fault status from HS0
- V_{DD} failure detection is disabled

7 Typical applications

7.1 Introduction

The following figure shows a typical automotive lighting application (only one vehicle corner) using an external PWM clock from the main MCU. A redundancy circuitry has been implemented to substitute light control (from MCU to watchdog) in case of a Fail-safe condition.

It is recommended to locate a 22 nF decoupling capacitor to the module connector.

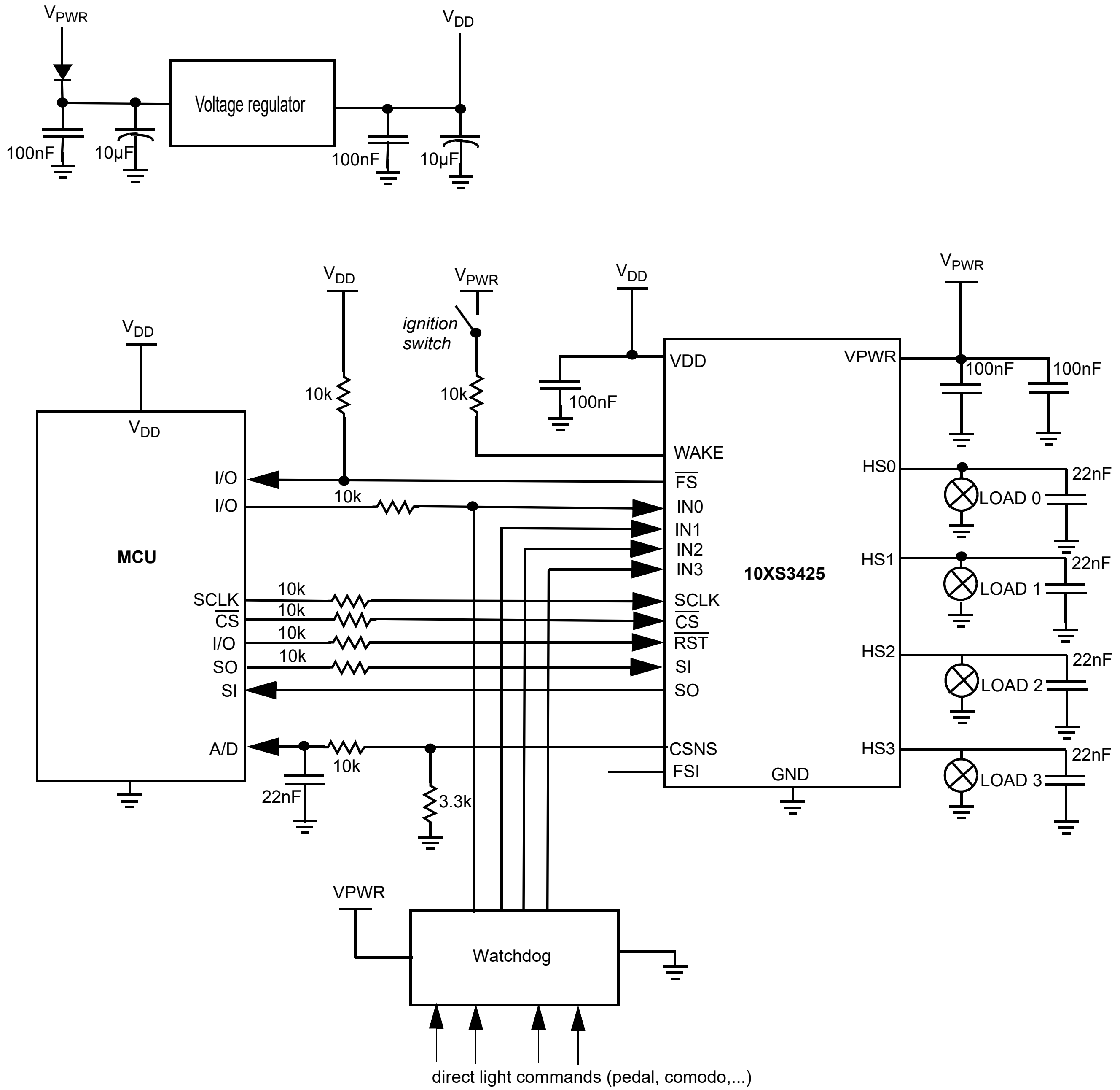


Figure 19. Typical automotive lighting (one corner)

8 Packaging

8.1 Soldering information

The 10XS3425 was qualified in accordance with JEDEC standards J-STD-020C Pb-free reflow profile. The maximum peak temperature during the soldering process should not exceed 260 °C for 40 seconds maximum duration.

8.2 Marking information

The device is identified by the part number: 10XS3425.

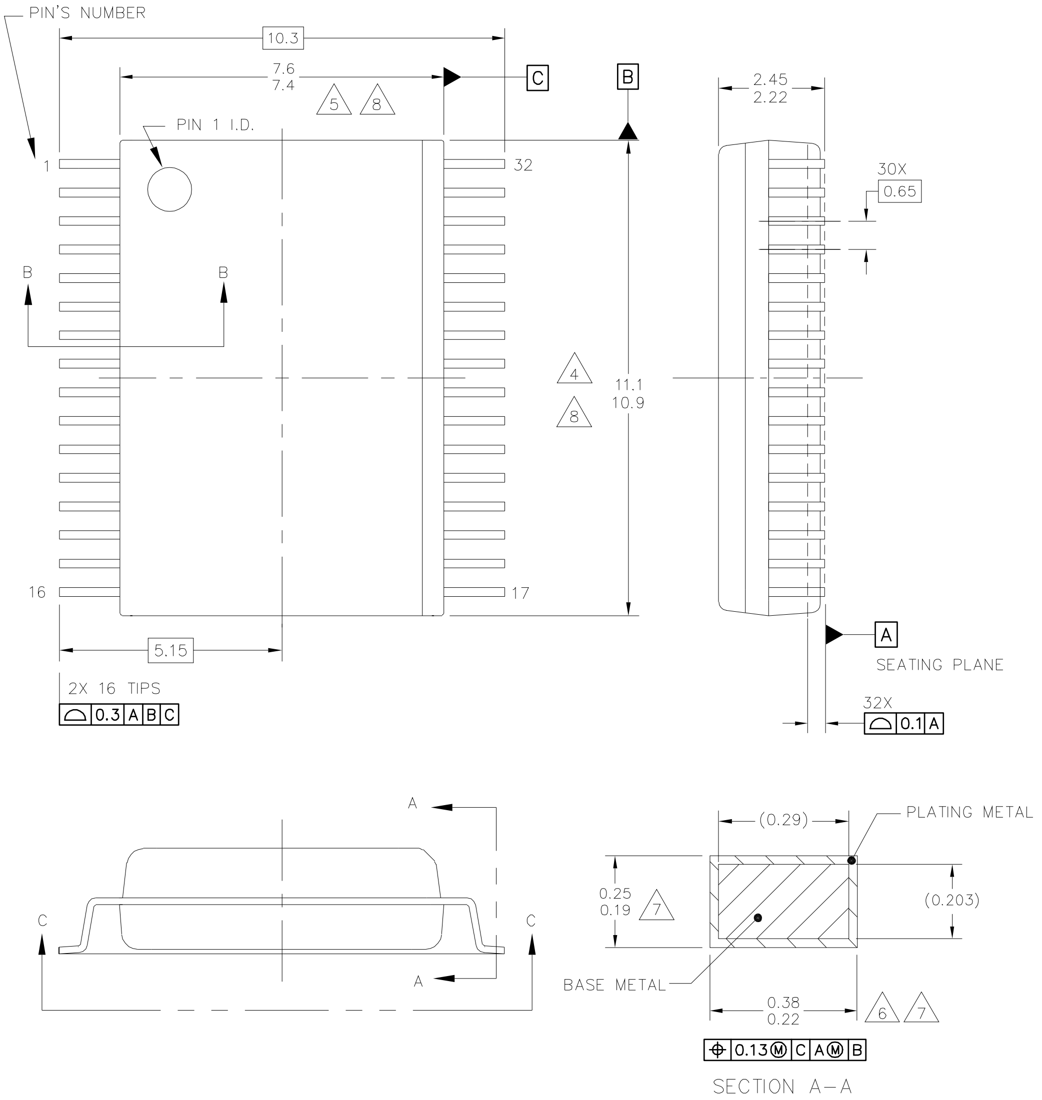
Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the nine character build information code (e.g. “CTKAH0929”). The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “1329” indicates the 29th week of the year 2013.

8.3 Package mechanical dimensions

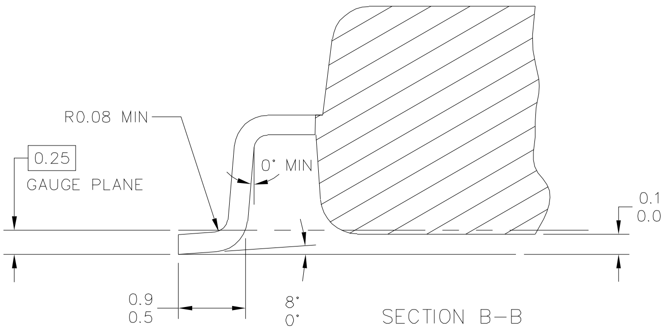
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing’s document number.

Table 25. Package outline

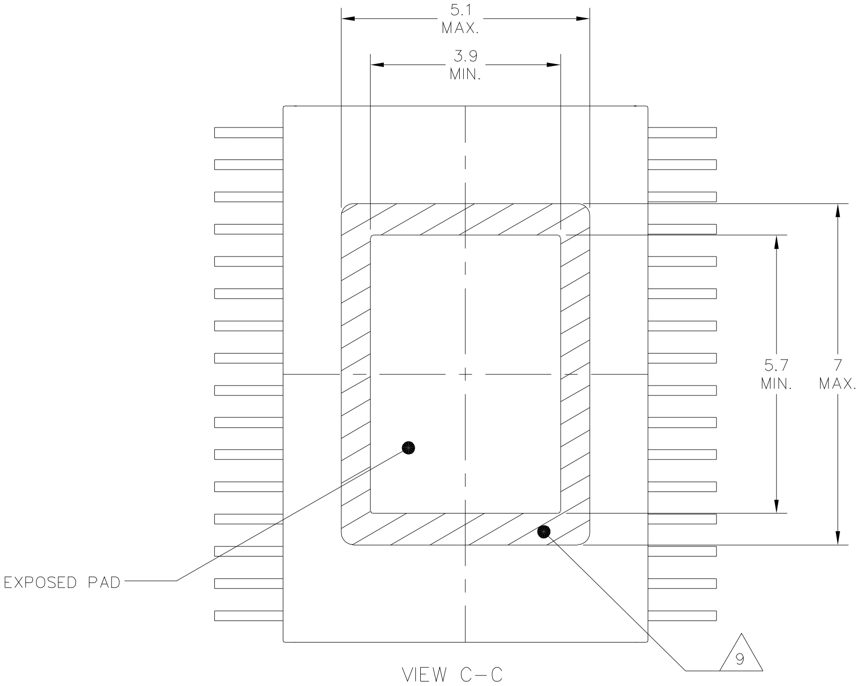
Package	Suffix	Package outline drawing number
32-pin SOIC-EP	EK	98ASA00368D



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: SOIC W/B, 32 TERMINAL, 0.65 PITCH, 6.4 X 4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00368D REV: A	
	STANDARD: NON–JEDEC	
	SOT1746–2 07 JAN 2016	



SECTION B–B



VIEW C–C

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: SOIC W/B, 32 TERMINAL, 0.65 PITCH, 6.4 X 4.5 EXPOSED PAD		DOCUMENT NO: 98ASA00368D REV: A
		STANDARD: NON–JEDEC
		SOT1746–2 07 JAN 2016

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

△4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

△5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

△6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.

△7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.

△8. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

△9. HATCHED AREA TO BE KEEP-OUT ZONE FOR PCB ROUTING.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: SOIC W/B, 32 TERMINAL, 0.65 PITCH, 6.4 X 4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00368D	REV: A
	STANDARD: NON-JEDEC	
	SOT1746-2	07 JAN 2016

9 Revision history

Revision	Date	Description of changes
1.0	4/2013	• Initial release
2.0	2/2014	• Changed orderable part number to MC10XS3425AEK • Corrected how Thermal resistance is represented • Improved definition of some Static and Dynamic parameter characteristic descriptions. No limits were changed.
3.0	3/2015	• Corrected part number in ordering information

4.0	1/2016	• Deleted the 28W mode references as per PB 17063
		  • Table 4 - relabeled parameter descriptions, conditions, and symbols
		  • Table 5 - relabeled parameter descriptions, conditions, and symbols
		  • Table 11 - changed the PWMR_s D8 bit
		  • Table 23 - changed the PWMR_s D8 bit
		• Added note (44) for Table 11

	1/2016	• Corrected note (44) placement
	1/2016	• Detailed a description for the 28W mode change
	7/2016	• Updated NXP document form and style
5.0	2/2018	• Updated Table 5 (added power output timing for HS2 to HS3)

6.0	8/2018	• Updated as per CIN 201808007I
		  • Corrected T_{OLLED} values in Table 5, Dynamic electrical characteristics
		  • Updated Openload detection in ON state for LED (added clarification for the usage of openload LED function and changed D[6:0]=7F to D[7:0]=FF)

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Document Number: MC10XS3425
Rev. 6.0
8/2018

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