## 25W+25W

# Full Digital Speaker Amplifier with built-in DSP 

BM5449MWV

## - General Description

BM5449MWV is a Full Digital Speaker Amplifier with built-in DSP (Digital Sound Processor) designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of $25 \mathrm{~W}+25 \mathrm{~W}$. This IC employs state-of-the-art Bipolar, CMOS, and DMOS (BCD) process technology that eliminates turn-on resistance in the output power stage and internal loss due to line resistances up to an ultimate level. With this technology, the IC can achieve high efficiency of $90 \%$ ( $10 \mathrm{~W}+10 \mathrm{~W}$ output with $8 \Omega$ load). In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 40 W . This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

- Features
- With wide range of power supply voltage. ( $\mathrm{V}_{\mathrm{CC}}=10$ to 26 V )
- This IC includes the DSP (digital sound processor) for Audio signal processing for Flat TVs.
Synchronous SRC, Surround, 8 Band EQ, 1 Band EQ (for Sub), Volume, 2 Band DRC, Delay RAM for phase revised Close Over Filter, 512 Taps FIR Filter, P²Volume, P²Base+, Higher Sound Complement (High Generator), Soft Clipper, Hard Clipper
- This IC has two inputs systems of digital audio interface.

I ${ }^{2}$ S / LJ / RJ format, LRCLK: 8 to 192 kHz , BCLK: 32fs / 48fs / 64fs, SDATA: 16 / 20 / 24bits
BCLK: 32fs / 48fs / 64fs, SDATA: 16 / 20 / 24bits

- Two Digital Audio Output for Audio DAC and headphone.
- One PWM Output for Subwoofer.
- The sound quality decrease by the power supply variation is prevented with the output feedback circuit. In addition, a low noise and a low distortion are achieved. Mass electrolytic capacitor is unnecessary because it is strong in the power supply variation.
- It contributes to miniaturizing, making to the thin type, and the power saving of the system by highly effective (10W+10W output and $8 \Omega$ on-load) $90 \%$ and low generation of heat.
- Low current at the Power down Mode.
- The pop noise at power supply on/off is prevented, and a more high-quality soft mute function is built into. Highly reliable design with built-in various protection functions.
$\square$ The component side product can be decreased because of small package (UQFN056V7070).
$\square$ The maximum output in the stereo is $25 \mathrm{~W}+25 \mathrm{~W}$ (VCC=20.5V, $8 \Omega$ load).
$\square$ The maximum output in the monaural(PBTL) is $50 \mathrm{~W}(\mathrm{VCC}=20.5 \mathrm{~V}, 4 \Omega$ load $)$


Figure 1. Typical application circuit

## -Pin Configuration



Figure 2. Pin configuration (Top View)
Pin Description

| No. | Name | I/O | No. | Name | I/O | No. | Name | I/O | No. | Name | I/O |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | LRCKO | I/O | 15 | TEST2 | I | 29 | OUT2P | O | 43 | OUT1P | O |
| 2 | BCLKO | I/O | 16 | SW2N | O | 30 | N.C. | - | 44 | N.C. | - |
| 3 | MCLKO | I/O | 17 | SW2P | O | 31 | GNDP2 | - | 45 | VCCP1 | - |
| 4 | SDATA1 | I | 18 | SW1N | O | 32 | GNDP2 | - | 46 | VCCP1 | - |
| 5 | SDATA2 | I | 19 | SW1P | O | 33 | N.C. | - | 47 | GAIN1 | I/O |
| 6 | LRCK | I | 20 | GNDA | - | 34 | OUT2N | O | 48 | GAIN2 | I/O |
| 7 | BCLK | I | 21 | IN_ERR | I | 35 | OUT2N | O | 49 | MUTEX | I |
| 8 | XI | I | 22 | FILP | O | 36 | OUT1N | O | 50 | PDX | I |
| 9 | XO | O | 23 | REG5 | O | 37 | OUT1N | O | 51 | RSTX | I |
| 10 | VSS | - | 24 | REGG | O | 38 | N.C. | - | 52 | SCL | I |
| 11 | PLL | O | 25 | VCCA | - | 39 | GNDP1 | - | 53 | SDA | I/O |
| 12 | DVDD | - | 26 | VCCP2 | - | 40 | GNDP1 | - | 54 | ADDR | I |
| 13 | TEST1 | I | 27 | VCCP2 | - | 41 | N.C. | - | 55 | SDATAO2 | I/O |
| 14 | REG15 | O | 28 | OUT2P | O | 42 | OUT1P | O | 56 | SDATAO1 | I/O |

Absolute Maximum Ratings $\left(\mathrm{Ta}=25^{\circ} \mathrm{C}\right)$

| Item | Symbol | Limit | Unit | Conditions |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply voltage | $\mathrm{V}_{\text {cc }}$ | -0.3 to 30 | V | Pin 25, 26, 27, 45, 46 | *1 *2 |
|  | $V_{D D}$ | -0.3 to 4.5 |  | Pin 12 | *1 *2 |
| Power dissipation | Pd | 4.29 | W |  | *3 |
|  |  | 4.83 |  |  | *4 |
| Input voltage | $\mathrm{V}_{\text {IN }}$ | -0.3 to 4.5 | V | Pin 4 to 8, 13, 15, 49to54 | *1 |
| Terminal voltage1 | $V_{\text {PIN1 }}$ | -0.3 to 4.5 | V | Pin 1 to 3, 9, 16to19, 47, 48, 55, 56 | *1 |
| Terminal voltage 2 | $V_{\text {PIN2 }}$ | -0.3 to 7.0 | V | Pin 22 to 24 | *1 |
| Terminal voltage 3 | $V_{\text {PIN3 }}$ | -0.3 to 30 | V | Pin 28, 29, 34 to 37, 42, 43 | *1 *5 |
| Operating temperature range | $\mathrm{T}_{\text {opr }}$ | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |  |  |
| Storage temperature range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |  |  |
| Maximum junction temperature | $\mathrm{T}_{\text {jmax }}$ | +150 | ${ }^{\circ} \mathrm{C}$ |  |  |

*1 The voltage that can be applied reference to GND(Pin 10, 20, 31, 32, 39, 40)
*2 Do not, however exceed Pd and Tjmax $=150^{\circ} \mathrm{C}$.
*3 $74.2 \mathrm{~mm} \times 74.2 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ FR4, 4-layer glass epoxy board (Top and bottom layer back copper foil size : $34.09 \mathrm{~mm}^{2}$, 2nd, 3rd layer back copper foil size:5505mm ${ }^{2}$ )
Derating in done at $34.3 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for operating above $\mathrm{Ta}=25^{\circ} \mathrm{C}$. There are thermal via on the board.
*4 $74.2 \mathrm{~mm} \times 74.2 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ F FR4, 4-layer glass epoxy board (Copper area 5505 mm 2 )
Derating in done at $38.6 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for operating above $\mathrm{Ta}=25^{\circ} \mathrm{C}$. There are thermal via on the board.
*5 It should use it below this ratings limit including the AC peak waveform (overshoot) for all conditions. At only undershoot, it is admitted using at $\leqq 10$ nse and $\leqq 30 \mathrm{~V}$ by the VCC reference. (Please refer following figure.)


RecommendedOperating Ratings ( $\mathrm{Ta}=25^{\circ} \mathrm{C}$ )

| Item | Symbol | Limit | Unit | Conditions |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply voltage | $\mathrm{V}_{\text {cc }}$ | 10 to 26 | V | Pin 25, 26, 27, 45, 46 | *1 *2 |
|  | $V_{D D}$ | 3.0 to 3.6 |  | Pin 12 | *1 *2 |
| Minimum load impedance | $\mathrm{R}_{\mathrm{L}}$ | 3.6 | $\Omega$ | Vcc $\leqq 18 \mathrm{~V}$, Stereo BTL mode | *6 |
|  |  |  |  | Monaural Parallel BTL mode | *6 |
|  |  | 5.4 | $\Omega$ | Vcc $\leqq 26 \mathrm{~V}$, Stereo BTL mode | *6 |

*6 Do not, however exceed Pd.

- Electrical characteristics
(Unless otherwise specified $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{Vcc}=18 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=3.3 \mathrm{~V}$, fin $=1 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=8 \Omega$, RSTX $=3.3 \mathrm{~V}, \mathrm{PDX}=3.3 \mathrm{~V}, \mathrm{MUTEX}=3.3 \mathrm{~V}$ $\mathrm{fs}=48 \mathrm{kHz}$, GAIN=20dB, DSP : Through, Output LC filter : $\mathrm{L}=22 \mu \mathrm{H}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{Cg}=0.068 \mu \mathrm{~F}$ )

| Item | Symbol | Limit |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |
| Total circuit |  |  |  |  |  |  |
| Circuit current (Power down mode) | $\mathrm{I}_{\mathrm{CC} 1}$ | - | 0.1 | 0.2 | mA | Pin 25, 26, 27, 45, 46 No load RSTX $=3.3 \mathrm{~V}, \mathrm{PDX}=0 \mathrm{~V}, \mathrm{MUTEX}=0 \mathrm{~V}$ |
|  | ldD1 | - | 3.7 | 7.5 |  | $\begin{aligned} & \text { Pin 12, Noload } \\ & \text { RSTX }=3.3 \mathrm{~V}, \mathrm{PDX}=0 \mathrm{~V}, \mathrm{MUTEX}=0 \mathrm{~V} \end{aligned}$ |
| Circuit current (mute mode) | Icc2 | - | 7.0 | 25 | mA | $\begin{aligned} & \text { Pin } 25,26,27,45,46 \text { No load } \\ & \text { RSTX }=3.3 \mathrm{~V}, \text { PDX }=3.3 \mathrm{~V} \text {, MUTEX }=0 \mathrm{~V} \end{aligned}$ |
|  | $\mathrm{I}_{\mathrm{D} 2}$ | - | 25 | 70 |  |  |
| Circuit current (Normal mode) | Icca | - | 50 | 80 | mA | $\begin{aligned} & \text { Pin } 25,26,27,45,46 \text { No load } \\ & \text { RSTX }=3.3 \mathrm{~V}, \text { PDX }=3.3 \mathrm{~V} \text {, } \text { MUTEX }=3.3 \mathrm{~V} \end{aligned}$ |
|  | $\mathrm{I}_{\mathrm{DD} 3}$ | - | 30 | 70 |  | $\begin{aligned} & \text { Pin } 12 \text { Noload } \\ & \text { RSTX }=3.3 \mathrm{~V}, \text { PDX }=3.3 \mathrm{~V}, \text { MUTEX }=3.3 \mathrm{~V} \end{aligned}$ |
| Regulator output voltage | $\mathrm{V}_{\text {REG15 }}$ | 1.3 | 1.5 | 1.7 | V | Pin 14 |
|  | $\mathrm{V}_{\text {REG5 }}$ | 4.7 | 5.0 | 5.3 |  | Pin 23 |
|  | $V_{\text {REGG }}$ | 4.7 | 5.0 | 5.3 |  | Pin 24 |
| ERROR WARNING terminal <br> L level voltage | $V_{\text {ERR }}$ | - | 0.4 | 0.8 | V | Pin 47, 48, $\mathrm{l}_{\mathrm{o}}=0.1 \mathrm{~mA}$ |
| H level input voltage | $\mathrm{V}_{\mathrm{H}}$ | $\begin{array}{r} \mathrm{V}_{\mathrm{DD}} \\ \times 0.8 \\ \hline \end{array}$ | - | - | V | Pin 4 to 7, 13, 15, 21, 49 to 54 |
| L level input voltage | $\mathrm{V}_{\text {IL }}$ | - | - | $\begin{gathered} V_{D D} \\ \times 0.2 \end{gathered}$ | V | Pin 4 to 7, 13, 15, 21, 49 to 54 |
| Input current (Input pull-up terminal) | ILL | 50 | 100 | 150 | $\mu \mathrm{A}$ | Pin 4 to $7, \mathrm{VIN}=0 \mathrm{~V}$ |
| Input current(Input pull-down terminal) | $\mathrm{IIH}^{\text {H }}$ | 30 | 70 | 105 | $\mu \mathrm{A}$ | Pin 49 to 51, 54, VIN = 3.3V |
| Input current(SCL, SDA terminal) | 1 | - | 0 | 1 | $\mu \mathrm{A}$ | Pin 52, 53, VIN $=3.3 \mathrm{~V}$ |
| Input current (SCL, SDA terminal) | Io | -1 | 0 | - | $\mu \mathrm{A}$ | Pin 52, 53, VIN = 0V |
| Digital Audio Signal Output H level voltage 1 | $\mathrm{V}_{\text {OH1 }}$ | $\begin{aligned} & V_{D D} \\ & -0.5 \\ & \hline \end{aligned}$ | - | $V_{\text {DD }}$ | V | Pin 1 to $3,55,56, \mathrm{lo}=1 \mathrm{~mA}$ |
| PWM for Subwoofer Output H level voltage 2 | Voh2 | $\begin{gathered} V_{D D} \\ -0.5 \end{gathered}$ | - | $V_{\text {DD }}$ | V | Pin 16 to 19, $\mathrm{lo}=1 \mathrm{~mA}$ |
| Digital Audio Signal Output L level voltage 1 | $\mathrm{V}_{\text {OL1 }}$ | 0 | - | 0.5 | V | Pin 1 to $3,55,56, \mathrm{lo}=1 \mathrm{~mA}$ |
| PWM for Subwoofer Output L level voltage 2 | Vol2 | 0 | - | 0.5 | V | Pin 16 to 19, $\mathrm{lo}=1 \mathrm{~mA}$ |


| Speaker output |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum output | Po1 | - | 10 | - | W | Vcc=13V, THD+n=10\%, Gain=20dB *7 |
|  | P 02 | - | 20 | - | W | Vcc=18V, THD+n=10\%, Gain=22dB *7 |
|  | Po3 | - | 25 | - | W | $\mathrm{Vcc}=20.5 \mathrm{~V}, ~ \mathrm{THD}+\mathrm{n}=10 \%$, Gain=23dB*7 |
| Total harmonic distortion | THD | - | 0.05 | - | \% | $\mathrm{P}_{\mathrm{O}}=1 \mathrm{~W}, \mathrm{BW}=20$ to 20 kHz *7 |
| Crosstalk | CT | 60 | 80 | - | dB | $\mathrm{P}_{\mathrm{O}}=1 \mathrm{~W}, \mathrm{BW}=\mathrm{IHF}-\mathrm{A}$ *7 |
| PSRR | PSRR | - | 70 | - | dB | Vripple=1Vrms, f=1KHz *7 |
| Output noise voltage | $\mathrm{V}_{\mathrm{NO}}$ | - | 80 | 140 | $\mu \mathrm{V}$ rms | $-\infty \mathrm{dBFS}, \mathrm{BW}=1 \mathrm{HF}-\mathrm{A}$ |
| PWM sampling frequency | $\mathrm{f}_{\text {PWM } 1}$ | - | 384 | - | KHz | fs $=8 \mathrm{kHz}, 16 \mathrm{kHz}, 32 \mathrm{kHz}$ *7 |
|  | $\mathrm{f}_{\text {PWM2 }}$ | - | 352.8 | - |  | $\begin{aligned} \mathrm{fs}= & 11.025 \mathrm{kHz}, 22.05 \mathrm{kHz}, 44.1 \mathrm{kHz}, \\ & 88.2 \mathrm{kHz} \end{aligned}$ |
|  | $\mathrm{f}_{\text {PWм }}$ | - | 384 | - |  | fs $=12 \mathrm{kHz}, 24 \mathrm{kHz}, 48 \mathrm{kHz}, 96 \mathrm{kHz} \quad$ *7 |

[^0]Typical Performance Curves
$\left(\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{Vcc}=18 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=3.3 \mathrm{~V}, \mathrm{fin}=1 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=8 \Omega, \mathrm{RSTX}=3.3 \mathrm{~V}, \mathrm{PDX}=3.3 \mathrm{~V}, \mathrm{MUTEX}=3.3 \mathrm{~V}, \mathrm{fs}=48 \mathrm{kHz}, \mathrm{GAIN}=23 \mathrm{~dB}, \mathrm{DSP}\right.$ through $)$ Measured by ROHM designed 4-layer board.


Power supply - Current consumption


Figure 5.
. Output power - Efficiency


Figure 4.
Power supply - Current consumption


Figure 6.
Output power - Current consumption

Continued on next page.

- Typical Performance Curves (Continuation on previous page)


Figure 7.
Waveform at smooth start


Figure 8.
Waveform at smooth mute

## - Typical Performance Curves

$\left(\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{Vcc}=18 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=3.3 \mathrm{~V}\right.$, fin $=1 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=8 \Omega, \mathrm{RSTX}=3.3 \mathrm{~V}, \mathrm{PDX}=3.3 \mathrm{~V}, \mathrm{MUTEX}=3.3 \mathrm{~V}, \mathrm{fs}=48 \mathrm{kHz}, \mathrm{GAIN}=23 \mathrm{~dB}, \mathrm{DSP}$ through $)$ Measured by ROHM designed 4 layer board.


Figure 9.
Output voltage - Power voltage ( $\mathrm{R}_{\mathrm{L}}=8 \Omega$ ).


Figure 11.
Output voltage - Power voltage ( $\mathrm{R}_{\mathrm{L}}=6 \Omega$ ).


Figure 10.
Output power - Current consumption ( $\mathrm{R}_{\mathrm{L}}=8 \Omega$ )


Figure 12.
Output power - Current consumption ( $\mathrm{R}_{\mathrm{L}}=6 \Omega$ )

Continued on next page.

## - Typical Performance Curves (Continuation on previous page)



Figure 13.
Output voltage - Power voltage ( $\mathrm{R}_{\mathrm{L}}=4 \Omega$ ).


Figure 14.
Output power - Current consumption $\left(\mathrm{R}_{\mathrm{L}}=4 \Omega\right)$

## - Typical Performance Curves

$\left(\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{Vcc}=18 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=3.3 \mathrm{~V}, \mathrm{fin}=1 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=4 \Omega, \mathrm{RSTX}=3.3 \mathrm{~V}, \mathrm{PDX}=3.3 \mathrm{~V}, \mathrm{MUTEX}=3.3 \mathrm{~V}, \mathrm{fs}=48 \mathrm{kHz}, \mathrm{GAIN}=20 \mathrm{~dB}, \mathrm{DSP}\right.$ through, Output LCfilter: $\mathrm{L}=10 \mathrm{uH}, \mathrm{C}=0.68 \mathrm{uF}, \mathrm{Cg}=0.15 \mathrm{uF}$, Monaural Parallel BTL mode) Measured by ROHM designed 4-layer board.


Figure 15.
Output voltage - Power voltage ( $\mathrm{R}_{\mathrm{L}}=4 \Omega$, Monaural Parallel BTL mode)

## - Typical Performance Curves

$\left(\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{Vcc}=18 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=3.3 \mathrm{~V}, \mathrm{fin}=1 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=8 \Omega, \mathrm{RSTX}=3.3 \mathrm{~V}, \mathrm{PDX}=3.3 \mathrm{~V}, \mathrm{MUTEX}=3.3 \mathrm{~V}, \mathrm{fs}=48 \mathrm{kHz}, \mathrm{GAIN}=20 \mathrm{~dB}, \mathrm{DSP}\right.$ through, Output LCfilter:L=22uH,C=0.33uF,Cg=0.068uF)
Measured by ROHM designed 4-layer board.


Figure 16.
FFT of output noise voltage ( $\mathrm{R}_{\mathrm{L}}=8 \Omega$ )


Figure 18.
Output power - THD $+\mathrm{N}\left(\mathrm{R}_{\mathrm{L}}=8 \Omega\right)$


Figure 17.
Frequency - Output power $\left(\mathrm{R}_{\mathrm{L}}=8 \Omega\right)$


Figure 19
Frequency - THD $+\mathrm{N}\left(\mathrm{R}_{\mathrm{L}}=8 \Omega\right)$

[^1]-Typical Performance Curves (Continuation on previous page)


Figure 20.
Frequency - Crosstalk ( $\mathrm{R}_{\mathrm{L}}=8 \Omega$ )

## - Typical Performance Curves

$\left(\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{Vcc}=18 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=3.3 \mathrm{~V}, \mathrm{fin}=1 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=6 \Omega, \mathrm{RSTX}=3.3 \mathrm{~V}, \mathrm{PDX}=3.3 \mathrm{~V}, \mathrm{MUTEX}=3.3 \mathrm{~V}, \mathrm{fs}=48 \mathrm{kHz}, \mathrm{GAIN}=20 \mathrm{~dB}, \mathrm{DSP}\right.$ through, Output LCfilter:L=15uH,C=0.47uF,Cg=0.1uF)
Measured by ROHM designed 4-layer board.


Figure 21.
FFT of output noise voltage $\left(\mathrm{R}_{\mathrm{L}}=6 \Omega\right)$


Output power - THD $+\mathrm{N}\left(\mathrm{R}_{\mathrm{L}}=6 \Omega\right)$


Figure 22.
Frequency - Output power $\left(\mathrm{R}_{\mathrm{L}}=6 \Omega\right)$


Figure 24.
Frequency - THD $+\mathrm{N}\left(\mathrm{R}_{\mathrm{L}}=6 \Omega\right)$

Continued on next page.

- Typical Performance Curves (Continuation on previous page)


Figure 25.
Frequency - Crosstalk ( $\mathrm{R}_{\mathrm{L}}=6 \Omega$ )

## - Typical Performance Curves

$\left(\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{Vcc}=18 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=3.3 \mathrm{~V}, \mathrm{fin}=1 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=4 \Omega, \mathrm{RSTX}=3.3 \mathrm{~V}, \mathrm{PDX}=3.3 \mathrm{~V}, \mathrm{MUTEX}=3.3 \mathrm{~V}, \mathrm{fs}=48 \mathrm{kHz}, \mathrm{GAIN}=20 \mathrm{~dB}, \mathrm{DSP}\right.$ through, Output LCfilter: $\mathrm{L}=10 \mathrm{uH}, \mathrm{C}=0.68 \mathrm{uF}, \mathrm{Cg}=0.15 \mathrm{uF}$ )
Measured by ROHM designed 4-layer board.


Figure 26.
FFT of output noise voltage ( $\mathrm{R}_{\mathrm{L}}=4 \Omega$ )


Figure 28.
Output power - THD $+\mathrm{N}\left(\mathrm{R}_{\mathrm{L}}=4 \Omega\right)$


Figure 27.
Frequency - Output power $\left(R_{L}=4 \Omega\right)$


Figure 29.
Frequency $-\mathrm{THD}+\mathrm{N}\left(\mathrm{R}_{\mathrm{L}}=4 \Omega\right)$

Continued on next page.

- Typical Performance Curves (Continuation on previous page)


Figure 30.
Frequency - Crosstalk ( $\mathrm{R}_{\mathrm{L}}=4 \Omega$ )

About external setting pin
(1) RSTX pin, PDX pin, MUTEX pin function

| RSTX <br> (51pin) | PDX <br> (50pin) | MUTEX <br> (49pin) | PWM output <br> (OUT1P, 1N, 2P, 2N) | ERROR <br> output | WARNING <br> output |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | L or H | L or H | HiZ_L <br> (Power down mode) | H | H |
| $H$ | L | L or H | HiZ_L <br> (Power down mode) | H | H |
| $H$ | $H$ | L | HiZ_L <br> (MUTE ON) | H | H |
| $H$ | $H$ | $H$ | Normal <br> (MUTE OFF) | H | H |


| RSTX <br> (51pin) | PDX <br> (50pin) | MUTEX <br> (49pin) | PWM output <br> (OUT1P, 1N, 2P, 2N) | ERROR <br> output | WARNING <br> output |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | L or H | HiZ_L <br> (Power down mode) | H | H |
| $H$ | L | L or H | HiZ_L <br> (Power down mode) | H | H |
| $H$ | $H$ | L | HiZ_L <br> (MUTE ON) | H | H |
| $H$ | $H$ | $H$ | HiZ_L <br> (Latch) | L |  |


| RSTX <br> (51pin) | PDX <br> (50pin) | MUTEX <br> (49pin) | PWM output <br> (OUT1P, 1N, 2P, 2N) | ERROR <br> output | WARNING <br> output |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | L or H | L or H | HiZ_L <br> (Power down mode) | H | H |
| $H$ | L | L or H | HiZ_L <br> (Power down mode) | H | H |
| $H$ | $H$ | L | HiZ_L <br> (MUTE ON) | H | H |
| $H$ | $H$ | $H$ | $H$ | L |  |

* RSTX, PDX and MUTEX pin are set Low, internal registers are initialized.
(2) ADDR pin function

| ADDR <br> (54pin) | $I^{2} \mathrm{C}$ BUS <br> Slave address |
| :---: | :---: |
| L | 80 (hex) |
| H | 82 (hex) |

* ADDR pin is set to low level, internal resisters are initialized
(3) GAIN pin function

| GAIN2 <br> (48pin) | GAIN1 <br> $(47 \mathrm{pin})$ | Speaker output <br> setting gain | Speaker output limitation power <br> $(* 1)$ |
| :---: | :---: | :---: | :---: |
| L | L | 13.7 dB | $3.3 \mathrm{~W}(\mathrm{THD}+\mathrm{n}=1 \%)$ |
| L | H | 18.9 dB | $11.0 \mathrm{~W}(\mathrm{THD}+\mathrm{n}=1 \%)$ |
| H | L | 15.9 dB | $5.5 \mathrm{~W}(\mathrm{THD}+\mathrm{n}=1 \%)$ |
| H | H | 20.7 dB | $16.5 \mathrm{~W}(\mathrm{THD}+\mathrm{n}=1 \%)$ |

*1: It provides for the limitation power in the speaker output by the speaker maximum output when $\mathrm{RL}=8 \Omega, \mathrm{DSP}=0 \mathrm{~dB}, 0 \mathrm{dBFS}$ corresponding is input. Please set it according to the speaker used. $18 \mathrm{~dB}, 20 \mathrm{~dB}, 22 \mathrm{~dB}$, and 23 dB can be set by the command besides the above-mentioned, set gain.
(4) Level diagram


Speaker output signal
(BTL output)

$$
\begin{aligned}
& V_{O_{-} D S P}=\frac{V D D}{2 \sqrt{2}}\left(10^{\frac{V_{I N}+G_{\text {DSP }}-0.3}{20}}\right) \quad[\mathrm{Vrms}] \\
& V_{O_{-} S P}=V_{O_{-} D S P} \times 10^{\left(\frac{G_{D R V}}{20}\right)} \times \frac{R_{L}}{2\left(r_{D S}+r_{D C}\right)+R_{L}} \times 2[\mathrm{Vrms}] \\
& \text { VIN : I }{ }^{2} \text { S input level [dBFS] } \\
& \text { GDSP : DSP gain [dB] } \\
& \text { GDRV : Feedback driver gain [dB] } \\
& \text { VCC : Power supply for power amp [V] } \\
& \text { VDD : Power supply for DSP [V] } \\
& \mathrm{R}_{\mathrm{L}} \quad \text { : Speaker load resistance }[\Omega] \\
& r_{\text {DS }} \quad \text { : Output FET resistance[ } \Omega \text { ] } \\
& \text { (TYP = 0.16 }) \\
& r_{D C} \\
& P_{O(T H D=1 \%)}=\frac{\left[\frac{V D D}{2 \sqrt{2}}\left(10^{\frac{V_{I N}+G_{D S P}-0.3}{20}}\right) \times 10^{\left(\frac{G_{D R V}}{20}\right)} \times \frac{R_{L}}{2\left(r_{D S}+r_{D C}\right)+R_{L}[\mathrm{~W}]} \times 2\right]^{2}}{R_{L}}
\end{aligned}
$$

- Power supply start-up sequence

- Power supply start-up sequence

- About the protection function

| Protection function | Detecting \& Releasing condition |  | Speaker PWM output | ERROR <br> flag output | WARNING flag output |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output short protection | Detecting condition | Detecting current $=10 \mathrm{~A}$ (TYP.) | HiZ_Low (Latch) | L | H |
| DC voltage protection | Detecting condition | Speaker PWM output fixes 40 msec or more by Duty $=0 \%$ or $100 \%$. | HiZ_Low (Latch) | L | H |
| High temperature protection | Detecting condition | Chip temperature to be over $150^{\circ} \mathrm{C}$ (TYP.) | $\begin{gathered} \text { HiZ_Low } \\ \text { (Auto return) } \end{gathered}$ | H | L |
|  | Releasing condition | Chip temperature to be under $120^{\circ} \mathrm{C}$ (TYP.) | Normal |  | H |
| Under voltage protection | Detecting condition | Power supply voltage to be below 8 V (TYP.) | $\begin{aligned} & \text { HiZ_Low } \\ & \text { (Auto return) } \end{aligned}$ | H | L |
|  | Releasing condition | Power supply voltage to be above 9V (TYP.) | Normal |  | H |
| Over voltage protection | Detecting condition | Power supply voltage to be above 29 V (TYP.) | $\begin{gathered} \text { HiZ_Low } \\ \text { (Auto return) } \end{gathered}$ | H | L |
|  | Releasing condition | Power supply voltage to be below 28 V (TYP.) | Normal |  | H |
| Clock stop protection | Detecting condition | BCLK or LRCK stops $100 \mu \mathrm{sec}$ (default) or more stops. | $\begin{gathered} \text { HiZ_Low } \\ \text { (Auto return) } \end{gathered}$ | H | L |
|  | Releasing condition | BCLK and LRCK normal input it. | Normal |  | H |

* It doesn't return automatically even if abnormal state is released when becoming a latch state. It is possible to release it by the method of the following (1) or(2).
(1)After the terminal MUTEX is made Low (10 time maintained in Low $=\mathrm{msec}(\mathrm{Min}$.$) ) once, it returns it to High again.$
(2)Please reenter the power supply after it drops to power-supply voltage Vcc<3V that the internal power-on reset circuit operates (10msec(Min.) maintenance).
* GAIN1 and GAIN2 pin can respectively be changed to the WARNING flag output pin and the ERROR flag output pin by the command.
* The stop detection time of BCLK and LRCK can respectively be changed with \&h09 and \&h08.
- Output selection of Stereo or Monaural on Main side.

Main side output can be set to stereo or monaural output. Initial value is set to "stereo output".
Default $=0 \mathrm{~h}$

| Select Address | Value | Explanation of operation | R/W |
| :---: | :---: | :--- | :---: |
| \&hFO [ 7 ] | 0 | Stereo output on main side. (Normal BTL Output) | R/W |
|  | 1 | Monaural output on main side. (Parallel BTL Output) |  |

Default $=01 \mathrm{~h}$

| Select Address | Value | Explanation of operation | R/W |
| :---: | :---: | :--- | :---: |
| \&hF1 [ 7] | 0 | Reserved. (This bit should be set to "0") | R/W |
| \&hF1 [ 6 ] | 0 | Stereo output on main side. (Normal BTL Output) | R/W |
|  | 1 | Monaural output on main side. (Parallel BT Output) |  |
| \&hF1 [ 5:3] | 0 | Reserved. (This bit should be set to "0") | R/W |
| \&hF1 [ 2:0] | 1 | Transmit address | R |

After it sets it as follows, Channel Mixer 2 is set to set it to monaural.
(1) Write 1 h to \&hF0 [7] register.
(2) Write 41 h to HhF [7:0] register.
(3) Write 01h to \&hF8 [7:0] register.

When the Main side is output by the monaural output, the output of the DSP side is set to the monaural output with Channel Mixer 2. The example of setting that time is as follows.
(1) When you use $L$ ch as a monaural output
\& h26 = 19h : $L$ out set to $L$ in, $R$ out set to inverse $L$ in.
(2) When you use R ch as a monaural output
\& $26=2 A h \quad: L$ out set to $R$ in, $R$ out set to inverse $R$ in.
(3) When you use $L$ ch as a monaural output
\&h26 $=3 B h \quad:$ L out set to $(L c h+R c h) / 2, R$ out set to inverse $(L c h+R c h) / 2$.
*Changing the stereo or monaural should be done after MUTEX terminal set to "L".
Please refer to "4-11. The channel setting with the phase reversing function" for details of Channel Mixer 2.

## - Output selection of Stereo or Monaural on Sub side.

The output of the Sub side can be set to the stereo or monaural as well as the Main side. An initial value is a stereo output. If the Sub side is monaural output, it should be set to monaural output by Channel Mixer 3 of the DSP.
The example of setting that time is as follows.
(1) When you use $L$ ch as a monaural output
\& h27 = 19h : $L$ out set to $L$ in, $R$ out set to inverse $L$ in.
(2) When you use R ch as a monaural output
\& $27=2 \mathrm{Ah} \quad: L$ out set to $R$ in, $R$ out set to inverse $R$ in.
(3) When you use $L$ ch as a monaural output
\& $\mathrm{h} 27=3 \mathrm{Bh}:$ L out set to $($ Lch +Rch$) / 2, \mathrm{R}$ out set to inverse $(\mathrm{Lch}+\mathrm{Rch}) / 2$
*Changing the stereo or monaural should be done after MUTEX terminal set to " L ".
Please refer to "4-11. The channel setting with the phase reversing function" for details of Channel Mixer 3.

- Change of GAIN1 and GAIN2 pin

After address \&hF0 [3] is set to 1 , it is necessary to set to 1 in \&hF8 [0] to change the terminal GAIN1 and the terminal GAIN2 to the WARNING flag output and the ERROR flag output terminal respectively.
Moreover, the gain value can be changed by writing 1 in $\& \mathrm{hF} 8$ [0] after the speaker output setting gain value also similarly sets the gain value to $\& \mathrm{hFO}[6: 4]$. Please set $\& \mathrm{hFO}$ [3] to 1 when you set the gain by this command.
Restrictions on output power supply for 3W speaker

| Select Address | Value | Explanation of operation | R/W |
| :---: | :---: | :---: | :---: |
| \&hFO[ $6: 4]$ | 0 | 13.7dB <br> (Output power limitter for 3W speaker) | R/W |
|  | 1 | 19.0dB <br> (Output power limitter for 10W speaker) |  |
|  | 2 | $15.9 \mathrm{~dB}$ <br> (Output power limitter for 5W speaker) |  |
|  | 3 | $20.7 \mathrm{~dB}$ <br> (Output power limitter for 15 W speaker) |  |
|  | 4 | 18.0 dB |  |
|  | 5 | 20.0 dB |  |
|  | 6 | 22.0 dB |  |
|  | 7 | 23.0dB |  |
| \&hF0 [3] | 0 | Gain setting by external pin | R/W |
|  | 1 | Output flag setting for WARNING/ERROR |  |
| \&hF0 [ 2:0] | 0 | Transmit address | R |

Default=0h

| Select Address | Value | Explanation of operation | R/W |
| :---: | :---: | :--- | :---: |
| \&hF8 [ 1 ] | 0 | Force stop transmission invalid | R/W |
|  | 1 | Force stop transmission valid |  |
| \&hF8 [0] | 0 | Stop transmission | Start transmission <br> (This bit is cleared 0 by automatically) |
|  | 1 |  |  |

*The address from \&hF1 to \&hF7 is register for LSI test. Please don't access these register.

- Reading of ERROR and WARNING flag with $I^{2} C$

It is also possible to read it through $I^{2} \mathrm{C} I / F$ though WARNING and the ERROR flag can be output to the terminal GAIN1 and the terminal GAIN2 respectively. The reading address is as follows.

| Select Address | Value | Explanation of operation | R/W |
| :---: | :---: | :--- | :---: |
| \&hE8 [7] ] | 0 | ERROR state | R |
|  | 1 | Normal |  |
| \&hE8 [ 6 ] | 0 | WARNING state |  |

## - Output short protection (Short to the power supply)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output pin becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.
Releasing method - (1)After MUTEX pin is set Low once over the soft mute transition time(Min.:10msec), MUTEX pin is returned to High again.

(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

## - Output short protection (Short to GND)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output terminal becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.
Releasing method - (1)After MUTEX pin is set Low once over the soft mute transition time(10msec(Min.)), MUTEX pin is returned to High again.
(2)Turning on the power supply again ( $\mathrm{Vcc}<3 \mathrm{~V}, 10 \mathrm{msec}($ Min. $)$ )

(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.
-DC voltage protection in the speaker
When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.
Detecting condition - It will detect when MUTEX pin is set High and PWM output Duty=0\% or $100 \%$ over 40 msec . Once detected, The PWM output instantaneously enters the state of HiZ-Low, and IC does the latch.
Releasing method - (1)After MUTEX pin is set Low once over the soft mute transition time(10msec(Min.)), MUTEX pin is returned to High again.
(2)Turning on the power supply again ( $\mathrm{Vcc}<3 \mathrm{~V}, 10 \mathrm{msec}(\mathrm{Min})$ ).


[^2]- High temperature protection

This IC has the high temperature protection circuit that prevents thermal reckless driving under an abnormal state for the temperature of the chip to exceed Tjmax $=150^{\circ} \mathrm{C}$.

Detecting condition - It will detect when MUTEX pin is set to High and the temperature of the chip becomes $150^{\circ} \mathrm{C}$ (TYP.) or more. The speaker output is muted when detected.
Releasing condition - It will release when MUTEX pin is set High and the temperature of the chip becomes $120^{\circ} \mathrm{C}$ (TYP.) or less. The speaker output is outputted when released.

(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

OUnder voltage protection
This IC has the under voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition - It will detect when MUTEX pin is set to High and the power supply voltage becomes lower than 8 V . The speaker output is muted when detected.
Releasing condition - It will release when MUTEX pin is set to High and the power supply voltage becomes more than 9 V . The speaker output is outputted when released


[^3]
## - Over voltage protectione

This IC has the over voltage protection circuit that make speaker output mute once detecting extreme drop of the ower supply voltage.

Detecting condition - It will detect when MUTEX pin is set High and the power supply voltage becomes more than 29V.
The speaker output is muted when detected.
Releasing condition - It will release when MUTEX pin is set High and the power supply voltage becomes less than 28 V . The speaker output is outputted when released.

(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

## - Clock stop protection

This IC has the clock stop protection circuit that make the speaker output mute when the BCLK and LRCLK frequency of the digital sound input are decreased.

Detecting condition - It enters the state of detection when BCLK or LRCK stops at $100 \mu \mathrm{sec}$ or more when the MUTE pin is High. The speaker output instantaneously enters the state of HiZ-Low if detected.
Releasing condition - A It enters the state of release if BCLK or LRCK returns to a normal clock motion when the terminal MUTEX is High. The speaker output returns to the signal output state through a soft start when released.

(*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.
-DSP part Functional specification

1. Command Interface

BM5449MWV uses $I^{2} C$-bus system for the command interface with a host CPU.
The register of BM5449MWV has Write-mode and Read-mode.
BM5449MWV specifies a slave address and 1 byte of selection address, and it performs writing and read-back.
The slave mode format of $I^{2} C$ bus is shown below.

| MSB LSB |  | MSB |  | LSB | MSB |  | LSB |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| S | Slave Address | A | Select Address | A | Data | A | P |

## S: Start condition

Slave Address: After the slave address (7 bits) set up by I2CADR, bit of a read-mode (H") and a write-mode (L") is attached, and a total of 8 -bit data is sent. (MSB first)
A: Acknowledge an acknowledge bit is added on to each bit of data transmitted.
When data transmission is being done correctly, "L" is transmitted.
"H" transmission means there was no acknowledge.
Select Address: BM5449MWV uses a 1-byte select address. (MSB first)
$\begin{array}{ll}\text { Data: } & \text { Data byte, transmitted data (MSB first) } \\ \text { P: } & \text { Stop condition }\end{array}$


1-1. Data Write-In


ADDR=0
MSB

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ADDR=1
MSB

| A6 | A5 | A4 | A 3 | A2 | A1 | A 0 | R/W |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |


| S | Slave Address | A | Select Address | A | Data | A | Data |  | A | Data | A | P |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| (ex.) | 80h |  | 20h |  | 00h |  | 00h |  | 00'h |  |  |  |

Write-in Procedure

| Step | Clock | Master | Slave(BM5449) |  |
| :---: | :---: | :--- | :--- | :--- |
| 1 |  | Start Condition |  | Note |
| 2 | 7 | Slave Address |  | \&h80 (\&h82) |
| 3 | 1 | R/W (0) |  |  |
| 4 | 1 |  | Acknowledge |  |
| 5 | 8 | Select Address |  | Write-in target register: 8bit |
| 6 | 1 |  | Acknowledge |  |
| 7 | 8 | Data |  | 8bit write-in data |
| 8 | 1 |  | Acknowledge |  |
| 9 |  | Stop Condition |  |  |

OWhen transmitting continuous data, the auto-increment function moves the select address up by one.
Repeat steps 7 and 8.

## 1-2. Data Read-Out

During read-out, the corresponding read-out address is first written into the \&hD0 address register (\&h20h in the example). In the following stream, the data is read out after the slave address. Do not return an acknowledge after completing the reception.

| S | Slave Address | A | Req_Addr | A | Select Address | A | P |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Ex.) | 80h |  | DOh |  | 20h |  |  |  |



Read-out Procedure

| Step | Clock | Master | Slave(BM5449) |  |
| :---: | :---: | :--- | :--- | :--- |
| 1 |  | Start Condition |  | Note |
| 2 | 7 | Slave Address |  | \&h80 (\&h82) |
| 3 | 1 | R/W (0) |  |  |
| 4 | 1 |  | Acknowledge |  |
| 5 | 8 | Req_Addr |  | I $^{2}$ C read-out address \&hD0 |
| 6 | 1 |  | Acknowledge |  |
| 7 | 8 | Select Address |  |  |
| 8 | 1 |  | Acknowledge |  |
| 9 | 1 | Stop Condition |  |  |
| 10 | 1 | Start Condition |  |  |
| 11 | 7 | Slave Address |  | \&h81 (\&h83) |
| 12 | 1 | R/W (1) |  |  |
| 13 | 1 |  | Acknowledge |  |
| 14 | 8 |  | Data |  |
| 15 | 1 | Acknowister: 8bit |  |  |
| 16 |  | Stop Condition |  |  |

OWhen transmitting continuous data, the auto-increment function moves up the select address by one.
Repeat steps 14 and 15.

1-3. Control Signal Specifications
OElectrical Characteristics and Timing for Bus Line and I/O Stage


Figure 31. Timing Chart

Table 1-1: SDA and SCL Bus Line Characteristics ( $\mathrm{Ta}=25^{\circ} \mathrm{C}$ and $\mathrm{DVDD}=3.3 \mathrm{~V}$ )

| Parameters |  | Symbol | High-Speed Mode |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Max. |  |
| 1 | SCL clock frequency |  | fSCL | 0 | 400 | kHz |
| 2 | Bus free time between "stop" condition and "start" condition | tBUF | 1.3 | - | $\mu \mathrm{s}$ |
| 3 | Hold time (re-transmit) "start" condition. <br> After this period, the first clock pulse is generated. | tHD;STA | 0.6 | - | $\mu \mathrm{s}$ |
| 4 | SCL clock LOW state hold time | tLOW | 1.3 | - | $\mu \mathrm{s}$ |
| 5 | SCL clock HIGH state hold time | tHIGH | 0.6 | - | $\mu \mathrm{s}$ |
| 6 | Re-transmit set-up time of "start" condition | tSU;STA | 0.6 | - | $\mu \mathrm{S}$ |
| 7 | Data hold time | tHD;DAT | $0^{1)}$ | - | $\mu \mathrm{s}$ |
| 8 | Data setup time | tSU;DAT | 2/(XI frequency) | - | ns |
| 9 | SDA and SCL signal stand-up time | tR | $20+0.1 \mathrm{Cb}$ | 300 | ns |
| 10 | SDA and SCL signal stand-down time | tF | $20+0.1 \mathrm{Cb}$ | 300 | ns |
| 11 | Set-up time for "stop" condition | tSU;STO | 0.6 | - | $\mu \mathrm{S}$ |
| 12 | Each bus line's capacitive load | Cb | - | 400 | pF |

The values above correspond with $\mathrm{V}_{\mathbb{I H} \text { min }}$ and $\mathrm{V}_{\text {IL max }}$ levels.

1) Because the transmission device exceeds the undefined domain of the SCL fall edge, it is necessary to internally provide a minimum
300 ns hold time for the SDA signal (of $\mathrm{V}_{\mathrm{H}}$ min of SCL signal).

The above-mentioned characteristic is a theory value in IC design and it doesn't be guaranteed by shipment inspection.
When problem occurs by any chance, we talk in good faith and correspond.
Neither terminal SCL nor terminal SDA correspond to 5V tolerant. Please use it within absolute maximum rating 4.5V.
2. Data and system clock distribution diagram

The audio input data and audio output data distribution diagram of BM5449MWV is shown below.

3. S-P conversion

In BM5449MWV, the conversion circuit from serial data to parallel data is built in.
S-P conversion is blocks which receive 3-line serial input audio data from pins and convert it to parallel data.
The three input formats are IIS, left-justified and right-justified. The bit clock frequency may be selected from either 64fs or 48fs or 32fs. 16bit, 20bit and 24bit output may be selected for each format.
The timing chart of each transmission mode is shown in the following figure.

Bit clock frequency: 64fs form
$1^{2}$ S 64fs Format


Left-Justified 64fs Format


Right-Justified 64fs Format


Bit clock frequency: 48fs form
$I^{2}$ S 48fs Format


Left-Justified 48fs Format





Right-Justified 48fs Format

| LRCK | Left Channel |  |  |  |  |  |  |  | Right Channel |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SDATA | s 14 13 12 11 10 9 | 8 | $7{ }^{6}$ | 5 | 4 | 3 | 2 | 1 |  |  |  | 14\|1312 | $2 \mid 1110$ | 9 | 8 | 7 | 6 | 5 | 3 | 2 | 1 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 20 bit Mode |  |  |  |  |  |  |  |  |  | 20 bit Mode |  |  |  |  |  |  |  |  |  |  |  |

Bit clock frequency: 32fs form
$I^{2}$ S 32fs Format
$\qquad$ Left Channel Right Channel而


16bit Mode 16bit Mode

Left-Justified 32fs Format



1 16bit Mode

Right-Justified 32fs Format




3-1. Timing reset setup of input 3 -line serial data circuit
After changing into parallel data from serial data, the timing which takes in data is adjusted.
(Synchronization)
This function is used when the time of power supply starting of IC and an input sampling rate change or 3 -line serial-data input format change.
When data taking-in timing shifts more than fixed, it adjusts automatically.

Default = 0

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h03 [6] | 0 | Auto adjustment function is invalid |
|  | 1 | Auto adjustment function is valid |

It resets by \&h04[0] = 1 after the stability of PLLA.
This Resister is cleared automatically, after Reset function is finished.

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h04 [0] | 1 | Synchronous counter reset |

3-2. Bit clock frequency setup of 3-line serial-data input
Default $=0$

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&h03 $[5: 4]$ | 0 | 64 fs form |
|  | 1 | 48 fs form |
|  | 2 | $32 f s$ form |

## 3-3. Serial data format

Default = 0

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h03 [3:2] | 0 | IIS format |
|  | 1 | Left-justified format |
|  | 2 | Right-justified format |

3-4. Data bit width
Default = 2

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&h03 [1:0] | 0 | 16 bit |
|  | 1 | 20 bit |
|  | 2 | 24 bit |

3-5. LRCK flame error flag

When the phase of LRCK shifts by $\pm 2 \%$ or more, the frame error becomes " H ".


Setting the number of times of the conclusion of the LRCK frame error
When detecting a frame error above the number of times which was set here, \&h04 [2] becomes "1".
Default $=1 \mathrm{~h}$

| Select Address | Value |  |
| :---: | :---: | :--- |
| $\& h 04$ [6:4] | 0 | Inhibit |
|  | 1 | 1 time |
|  | 2 | 2 times |
|  | $:$ | $:$ |
|  | 7 | 7 times |

Please set to 1 h or more

The flame error is read out by \&h04 [2].

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h04 [2] | 0 | Normal |
|  | 1 | Detect the LRCK flame error |

It clears the LRCK frame error flag which latches in executing \&h04 [1] command.
Operation is automatically cleared about the register after complete.
Default = 0

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| $\& 04[1]$ | 0 | Normal |
|  | 1 | Clear the LRCK flame error flag |

3-6. Audio interface signal specification

OElectric specification and timings of BCLK,LRCK and SDATA


Figure 32. Audio interface timings

| Parameter |  | Symbol |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Max. |  |
| 1 | LRCK |  | fLRCK | 8 | 96 | kHz |
| 2 |  | dLRCK | 40 | 60 | \% |
| 3 | BCLK | tBCK | 162.76 | - | ns |
| 4 |  | tBCKH | 65 | - | ns |
| 5 |  | tBCKL | 65 | - | ns |
| 6 | Time from the rising edge of BCLK to the edge of LRCK *1 | tBLRDG | 20 | - | ns |
| 7 | Time from the edge of LRCK to the rising edge of BCLK *1 | tLBRDG | 20 | - | ns |
| 8 | Setup time of SDATA | tSU;SD | 20 | - | ns |
| 9 | Hold time of SDATA | tHD;SD | 20 | - | ns |

[^4]
## 4. Digital Sound Processing (DSP)

The digital sound processing (DSP) part of BM5449MWV is composed of the special hard ware which is the optimal for FPD-TV, the Mini/Micro Compo. BM5449MWV does the following processing using this special DSP.

Pre-scaler, Channel mixer, DC cut HPF, P2Volume, Surround, P2Bass+, 8 Band P-EQ, 512Tap FIR, Cross Over Filter, Fine Master Volume, Balance Volume, 2 Band DRC, Post-scaler, Hard Clipper

The outline and signal flow of the DSP part

| Data width: | 32 bit (DATA RAM) |
| :--- | :--- |
| Machine cycle: | $20.3 \mathrm{~ns} \quad(1024 \mathrm{fs}, \mathrm{fs}=48 \mathrm{kHz})$ |
| Multiplier: | $32 \times 24 \rightarrow 56 \mathrm{bit}$ |
| Adder: | $56+56 \rightarrow 56$ bit |
| Data RAM: | $512 \times 32$ bit |
| Coefficient RAM: | $512 \times 24$ bit |
| Sampling frequency : | $\mathrm{fs}=8 \mathrm{k}, 11.025 \mathrm{k}, 12 \mathrm{k}, 16 \mathrm{k}, 22.05 \mathrm{k}, 32 \mathrm{k}$, |
|  | $44.1 \mathrm{k}, 48 \mathrm{k}, 88.2 \mathrm{k}, 96 \mathrm{k}, 176.4 \mathrm{k}, 192 \mathrm{kHz}$ |

The input sampling frequency is converted into 48 kHz or 44.1 kHz in SRC.


The digital signal from 16 bits to 24 bits is inputted to the DSP but extends 8 bit ( +42 dB ) as the overflow margin to the upper side. When doing the processing which exceeds this range, it processes a clip in the DSP. Incidentally, in case of the 2nd IIR-type (BQ) filter which is often used generally as the digital filter, because it consumes a lot of overflow margins, the output of the multiplier and the adder inside needs note.

The output of multipliers and the adding machine might exceed +48 dB by the coefficient of a1, a2, b0, b1, and b2. In that case, data becomes saturation power. Therefore, the output of the filter cannot obtain the aimed characteristic.


Direct form 1
-1 is multiplied by the coefficient of a1 and a2.

The management of audio data is as follows by each block.


It is using 2 bits of extension of 8 times over sampling parts for the calculation by the soft clipper function.
It is 2 bits shifted to the upper side when delivering data to the PWM processor, it makes up of 0 and it delivers 0 to 2 bits of lower ranks as the 24-bit data.

## 4-1. Bypass

It passes in the each function of the DSP by the command. Because it left the set value of the each function can be passed in, it is possible to do the confirmation of ON/OFF of the sound effect easily.
The effect which is possible about the bypass, 1) P2Volume, 2) The surround 3) P2Bass + (The suspected low voice), 4) 8Band BQ/1Band BQ, 5) 512 Tap FIR Filter, 6) 4 BQ Cross Over Filter, 7)2Band DRC/1Band DRC and the whole DSP can be passed.


Default $=00 \mathrm{~h}$

| Select Address | bit | Explanation of operation |
| :---: | :---: | :---: |
| \& h02 [ 7:0] | 7 | $\begin{aligned} & \text { Bypass of } \mathrm{P}^{2} \text { Volume }(\mathrm{SW} 1) \\ & 0: \text { Nomal, } 1: \text { Bypass } \end{aligned}$ |
|  | 6 | Bypass of Surround(SW2) <br> 0 : Normal, 1: Bypass |
|  | 5 | $\text { Bypass of } P^{2} \text { Bass }+(S W 3)$ <br> 0 : Normal, 1 : Bypass |
|  | 4 | Bypass of 8Band/1Band BQ(SW4) <br> 0 : Normal, 1 : Bypass |
|  | 3 | Bypass of Scaler and 512 Taps FIR Filter(SW5) <br> 0 : Normal, 1 : Bypass |
|  | 2 | Bypass of 4 BQ Cross Over Filter(SW6) <br> 0 : Normal, 1 : Bypass |
|  | 1 | Bypass of 2 Band/1Band DRC(SW7) <br> 0 : Normal, 1 : Bypass |
|  | 0 | Bypass of the whole DSP(SW8) <br> 0 : Normal, 1 : Bypass |

## 4-2. Pre-scaler

To overflow when the level sometimes is full scale entry in case of the digital signal which is inputted to the sound DSP and does surround and equalizer processing, it adjusts an entry gain with Pre-scaler. The adjustable-range can be set from +48 dB to -79 dB with the $0.5-\mathrm{dB}$ step. (Lch/Rch concurrency control)
Pre-scaler doesn't have a soft transfer feature. Input1 and Input2 become an independent control.

Default $=60 \mathrm{~h}$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| Input1 \&h21 [ 7:0] | Command Value | Gain |
| Input2 \&h22 [7:0] | 00 | +48dB |
|  | 01 | $+47.5 \mathrm{~dB}$ |
|  | : | : |
|  | 60 | OdB |
|  | 61 | $-0.5 \mathrm{~dB}$ |
|  | 62 | -1dB |
|  | ! | : |
|  | FE | -79dB |
|  | FF | - - |

## 4-3. Channel setup with a phase inversion function (Channel Mixer 1)

It sets a mixing in the sound on the left channel and the right channel of the digital signal which was inputted to the DSP. It makes a stereo signal a monaural here. Also, the phase-inversion, the mute on each channel can be set. The sound of Input1 and Input2 can be replaced and be added, too.


DSP Input1: The data inputted into Lch (1) of DSP is inverted.
Default $=0$

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h24 [7] | 0 | Normal |  |
|  | 1 | Invert |  |

DSP Input1: The data inputted into Lch (1) of DSP is mixed.
Default = 1

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h24 [6:4 ] | 0 | Mute |
|  | 1 | Input Lch(1) |
|  | 2 | Input Rch(1) |
|  | 3 | Input $(\operatorname{Lch}(1)+\operatorname{Rch}(1)) / 2$ |
|  | 4 | Input $\operatorname{Lch}(2)$ |
|  | 5 | $\operatorname{Input} \operatorname{Rch}(2)$ |
|  | 6 | $\operatorname{Input}(\operatorname{Lch}(2)+\operatorname{Rch}(2)) / 2$ |
|  | 7 | $\operatorname{Input} \operatorname{Lch}(1)+\operatorname{Lch}(2)$ |

DSP Input1: The data inputted into Rch (1) of DSP is inverted.
Default $=0$

| Select Address | Value |  |
| :---: | :---: | :--- |
| $\&$ h24 [3] | 0 | Normal |
|  | 1 | Invert |

DSP Input1: The data inputted into Rch (1) of DSP is mixed.
Default $=2$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h24 [2:0] | 0 | Mute |
|  | 1 | Input $\operatorname{Lch}(1)$ |
|  | 2 | Input $\operatorname{Rch}(1)$ |
|  | 3 | Input $(\operatorname{Lch}(1)+\operatorname{Rch}(1)) / 2$ |
|  | 4 | Input $\operatorname{Lch}(2)$ |
|  | 5 | Input $\operatorname{Rch}(2)$ |
|  | 6 | $\operatorname{Input}(\operatorname{Lch}(2)+\operatorname{Rch}(2)) / 2$ |
|  | 7 | $\operatorname{Input} \operatorname{Lch}(1)+\operatorname{Lch}(2)$ |

DSP Input2: The data inputted into Lch (2) of DSP is inverted.

Default $=0$

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&h25 [7] | 0 | Normal |
|  | 1 | Invert |

DSP Input2: The data inputted into Lch (2) of DSP is mixed.
Default $=4$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h25 [6:4] | 0 | Mute |
|  | 1 | Input Lch(1) |
|  | 2 | Input Rch(1) |
|  | 3 | Input $(\operatorname{Lch}(1)+\operatorname{Rch}(1)) / 2$ |
|  | 4 | Input Lch(2) |
|  | 5 | Input $\operatorname{Rch}(2)$ |
|  | 6 | Input $(\operatorname{Lch}(2)+\operatorname{Rch}(2)) / 2$ |
|  | 7 | Input $\operatorname{Lch}(1)+\operatorname{Lch}(2)$ |

DSP Input2: The data inputted into Rch (2) of DSP is inverted.
Default $=0$

| Select Address | Value |  |
| :---: | :---: | :--- |
| $\& \mathrm{~h} 25[3]$ | 0 | Normal |
|  | 1 | Invert |

DSP Input2: The data inputted into Rch (2) of DSP is mixed.
Default = 5

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h25[2:0] | 0 | Mute |
|  | 1 | Input Lch(1) |
|  | 2 | Input $\operatorname{Rch}(1)$ |
|  | 3 | Input $(\operatorname{Lch}(1)+\operatorname{Rch}(1)) / 2$ |
|  | 4 | Input $\operatorname{Lch}(2)$ |
|  | 5 | Input $\operatorname{Rch}(2)$ |
|  | 6 | Input $(\operatorname{Lch}(2)+\operatorname{Rch}(2)) / 2$ |
|  | 7 | $\operatorname{Input} \operatorname{Lch}(1)+\operatorname{Lch}(2)$ |

4-4. 1st HPF for DC cut
It cuts the DC offset component of the digital signal which is inputted to the sound DSP with this HPF. The cut off frequency fc of HPF is using 1 Hz and the degree is using the 1st filter.

Default $=1$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| Input1 \&h28 [ 3 ] | 0 | Not use DC cut HPF |
| Input2 \&h28 [ 2 ] | 1 | Use DC cut HPF |

## 4-5. 2 Band $P^{2}$ Volume

When the sound suddenly grows like blasts that exist in the TV commercial and the action picture, the volume is automatically controlled. Moreover, a sound small as the serif can be caught even if the volume is squeezed in the bedroom of nighttime is enlarged, and the loud sound is suppressed. The compression can operate each two bands (the low and the high pass). Use as one band is also possible according to the command setting. Moreover, it is also possible that the sound below the set value is soft muted.


It works, dividing $P^{2}$ Volume feature into the area of (1) and (2) and (3) according to the input level.
(1) $\mathrm{V}_{\text {Inff }}(-\infty)-\mathrm{V}_{\text {Imin }}$

It prevents $P^{2}$ Volume feature's generating noise.
(2) Input level is more than $\mathrm{V}_{\mathrm{Imin}}$, and Output level is less than $\mathrm{V}_{\text {omax }}$

$$
V_{0}=V_{1}+\beta
$$

$\beta$ : It lifts the whole power level for offset value beta.
(3) When power level $\mathrm{V}_{0}$ exceeds $\mathrm{V}_{\text {omax }}$

$$
V_{0}=\alpha \cdot V_{1}+\beta
$$

$\alpha$ : The inclination to suppress a D-range (P2V_ $\alpha$ )
The power level can be made constant, too.

Selection of using the $P^{2}$ Volume function.

$$
\text { Default = } 0
$$



| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h02 [7] | 0 | Use $\mathrm{P}^{2}$ Volume function |
|  | 1 | Not use $\mathrm{P}^{2}$ Volume function |

Selection of using the 2 Band $P^{2}$ Volum function for high frequency

$$
\text { Default = } 0
$$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h40 [7] | 0 | Not use the 2 Band $\mathrm{P}^{2}$ Volum function for high frequency |
|  | 1 | Use the 2 Band $\mathrm{P}^{2}$ Volum function for high frequency |

Selection of using the 2 Band $P^{2}$ Volum function for high frequency
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h40 [6] | 0 | Not use the 2 Band $\mathrm{P}^{2}$ Volum function for low frequency |
|  | 1 | Use the 2 Band $\mathrm{P}^{2}$ Volum function for high frequency |

[Attention] It uses it only for the high frequency when using it as 1Band P2Volume.

Selection of using soft mute when the small signal inputs in operating $\mathrm{P}^{2}$ Volum.

$$
\text { Default = } 0
$$

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h41 [ 2 ] | 0 | Not mute |  |
|  | 1 | Mute |  |

\&h56 and the \&h57 command adjust to the setting when attacking and releasing it.

The setting of $\mathrm{V}_{\text {Imin }}$
As for P2V_MIN, to cancel that noise and so on are lifted by P2Volume, P2Volume sets a functioning minimum level.
Default $=00 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| for high freq. \&h54 [ 4:0] | Command | Gain | Command | Gain | Command | Gain | Command | Gain |
| for low freq. \&h5C [ 4:0] | 00 | - | 08 | -76dB | 10 | -60dB | 18 | $-44 \mathrm{~dB}$ |
|  | 01 | -90dB | 09 | -74dB | 11 | -58dB | 19 | -42dB |
|  | 02 | -88dB | OA | -72dB | 12 | -56dB | 1A | -40dB |
|  | 03 | -8608 | ов | -70dB | 13 | -54dB | 1 B | -38dB |
|  | 04 | $-84 \mathrm{~dB}$ | oc | -68dB | 14 | -52dB | $1{ }^{1}$ | -36dB |
|  | 05 | -82dB | OD | -66dB | 15 | -50dB | $1{ }^{1}$ | $-34 \mathrm{~dB}$ |
|  | 06 | -80dB | OE | $-64 d \mathrm{~B}$ | 16 | -48dB | 1 E | -32dB |
|  | 07 | -78dB | OF | -62dB | 17 | -46dB | 1 F | -30dB |

The setting of $V_{\text {omax }}$
P2V_MAX sets an output suppression level. The input level VI whena setting " 80 h "
When $\alpha=80 \mathrm{~h}$ (slope 0 ) is set, output power level $\mathrm{V}_{\text {omax }}$ at level $\mathrm{VI}=0 \mathrm{~dB}$ input time is shown.
Default $=40 \mathrm{~h}$

| Select Address | Explanation of operatio |  |
| :---: | :---: | :---: |
| High frequency band \&h50[ 6:0] | Command | Threshold |
| Low frequency band \&h58[6:0] | 00 | -32dB |
|  | ${ }_{3 F}$ | ${ }_{-0.5 d B}$ |
|  | 40 | OdB |
|  | 41 | +0.5dB |
|  | : | : |
|  | 58 | +12dB |

a setting
$\alpha$ sets the slope of $D$ range.
Default $=00 \mathrm{~h}$

| Select Address | Explanation of operation |
| :---: | :---: |
| High frequency band \&h51[7:0] <br> Low frequency band \&h59[ 7:0] |  <br> Specify $X, Y$, and TH and request the slope a. <br> Record the expression from which the slope $a$ is requested in the following. a converts the value requested by the calculation into 8bit Hex data of the 2's complement. $\alpha=\frac{10^{\frac{Y}{20}}-10^{\frac{T H}{20}}}{10^{\frac{X}{20}}} \times 128$ <br> TH is P2V_MAX, $X$ is an input level, and $Y$ is an output power level. Ex.) Request the a at $P 2 V \_M A X=-12 d B, X=0 d B$, and $Y=-6 d B$. $\begin{aligned} & \alpha=\frac{10^{\frac{-6}{20}}-10^{\frac{-12}{20}}}{10^{\frac{0}{20}}} \times 128 \\ & \alpha=32 \rightarrow 20_{\mathrm{H}} \end{aligned}$ <br> Set obtained 20 H to \&h51 and the \&h59 command. |

$\beta$ setting
A small voice is made the offset level $\beta$ easy to hear by lifting the entire output power level.
Default $=18 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| High frequency band \&h55[4:0] | Command | Gain | Command | Gain | Command | Gain | Command | Gain |
|  | 00 | OdB | ${ }^{08}$ | +8dB | 10 | +16dB | 18 | ${ }^{+24 \mathrm{~dB}}$ |
| Low frequency band \&h5D[4:0] | 01 | +1dB | 09 | +9dB | 11 | +17dB | 19 | - |
|  | 02 | +2dB | OA | +10dB | 12 | +18dB | ${ }^{14}$ | - |
|  | 03 | +308 | ов | +11dB | 13 | +19dB | 1 B | - |
|  | 04 | +4dB | oc | +12dB | 14 | +20dB | $1{ }^{1}$ | - |
|  | 05 | +5dB | OD | +13dB | 15 | +21dB | $1{ }^{10}$ | - |
|  | 06 | +6dB | OE | +14dB | 16 | +22dB | 1 E | - |
|  | 07 | +7dB | OF | +15dB | 17 | +23dB | 1 F | - |

[Attention] The setting change of the offset level $\beta$ should be made to $\& \mathrm{~h} 40[7]=0$ and $\& \mathrm{~h} 40[6]=0$ and be done.

The setting of a transition time in attack (1)
A_RATE is the transition time setting when the condition of the $P^{2}$ Volume feature transfers from (2) to (3).
Default $=3$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| High frequency band \&h52[6:4] | Command A_RATE time Command A_RATE time <br> Low frequency band \&h5A[6:4] 0 1 ms 4 <br> 5 ms    <br>   1 2 ms <br>  2 3 10 ms <br>   3 ms 6 <br> 20 ms    <br>   4 ms 7 |  |  |  |

The setting of a transition time in release (1)
R_RATE is the transition time setting when the condition of the $P^{2}$ Volume feature transfers from (3) to (2).
Default $=\mathrm{Bh}$

| Select Address | Explanation of operation |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| High frequency band \&h52[3:0] |  | Command | R_RATE time | Command | R_RATE time |
| Low frequency band \&h5A[3:0] |  | 0 | 0.125 s | 8 | 2 s |
|  |  | 1 | 0.1825 | 9 | 2.5 s |
|  |  | 2 | 0.25 s | A | 3 s |
|  |  | 3 | 0.5 s | B | 4 s |
|  |  | 4 | 0.75 s | C | 5 s |
|  |  | 5 | 1 s | D | 6 s |
|  |  | 6 | 1.25 s | E | 7 s |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

Explanation for A_RATE andR_RATE(from (2) to (3) area)


Attack detection time setup (1)
A_TIME is the transfer operation beginning setting of P2Volume feature. When the output power level when changing A_TIME time continues from (2) to (3), the state transition of P2Volume is begun.
Default = 1

| Select Address | Explanation of operation |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| High frequency band \&h53[7:4] |  | Command | A_TIME time | Command | A_TIME time |
| Low frequency band \&h5B[7:4] |  | 0 | 0 ms | 8 | 6 ms |
|  |  | 1 | 0.5 ms | 9 | 7 ms |
|  |  | 2 | 1 ms | A | 8 ms |
|  |  | 3 | 1.5 ms | B | 9 ms |
|  |  | 4 | 2 ms | C | 10 ms |
|  |  | 5 | 3 ms | D | 20 ms |
|  |  | 6 | 4 ms | E | 30 ms |
|  |  | 7 | 5 ms | F | 40 ms |

Release detection time setup (1)
R_TIME is the transfer operation beginning setting of P2Volume feature. When the output power level when changing continuous R_TIME time continues from (3) to (2), the state transition of P2Volume is begun.
Default $=3$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| High frequency band \&h53[2:0] | Command R_TIME time Command R_TIME time <br> Low frequency band \&h5B[2:0] 0 5 ms 4 <br>  100 ms   <br>  1 10 ms 5 <br> 200 ms    <br>   2 25 ms <br>  6 50 ms 7 <br>  400 ms   |  |  |  |

Explanation for A_RATE_Low and R_RATE_Low(from (1) to (2) area)


The setting of a transition time in attack (2)
A_RATE_LOW is the transition time setting when the condition of the P2Volume feature transfers from (2) to (1). Default $=\mathrm{Bh}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| High frequency band \&h56 [3:0] | Command | A_RATE_LOW | Command | A_RATE_LOW |
| Low frequency band \&h5E [3:0] | 0 | 0.125 s | 8 | 2 s |
|  |  | 1 | 0.1825 s | 9 |
|  | 2.5 s |  |  |  |
|  |  | 2 | 0.25 s | A |

The setting of a transition time in release (2)
R_RATE_LOW is the transition time setting when the condition of the P2Volume feature transfers from (1) to (2).
Default $=3$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| High frequency band \&h56 [6:4] | Command R_RATE_LOW Command R_RATE_LOW  <br> Low frequency band \&h5E [6:4] 0 1 ms 4 5 ms <br>  1 2 ms 5 10 ms <br>  2 3 ms 6 20 ms <br>   3 4 ms 7 |  |  |  |
|  |  | 40 ms |  |  |

The setting of attack detection time (2)
A_TIME_LOW is the transfer operation beginning setting of P2Volume feature. When the input level below $\mathrm{V}_{\text {Imin }}$ continues above continuation A_TIME_LOW at the time of (2) or (3), it begins the state transition of P2Volume to the condition of (1).

Default $=3$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| High frequency band \&h57 [2:0] | Command A_TIME_LOW Command A_TIME_LOW  <br> Low frequency band \&h5F [2:0] 0 5 ms 4 100 ms <br>  1 10 ms 5 200 ms <br>  2 25 ms 6 300 ms <br>   3 50 ms 7 <br> 400 ms     |  |  |  |

The setting of release detection time (2)
R_TIME_LOW is the transfer operation beginning setting of $P^{2}$ Volume feature. In case of (1), it begins the state transition of $P^{2}$ Volume to the condition of (2) or (3), when the input level of (2) or (3) continues above R_TIME_LOW.

Default $=1 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| High frequency band \&h57 [7:4] | Command | R_TIME_LOW | Command | R_TIME_LOW |
|  | 0 | Prohibition | 8 | 6 ms |
| Low frequency band \&h5F [7.4] | 1 | 0.5 ms | 9 | 7 ms |
|  | 2 | 1 ms | A | 8 ms |
|  | 3 | 1.5 ms | B | 9 ms |
|  | 4 | 2 ms | c | 10 ms |
|  | 5 | 3 ms | D | 20 ms |
|  | 6 | 4 ms | E | 30 ms |
|  | 7 | 5 ms | F | 40 ms |

OThe scene changing detection and the high-speed recovery facility
There are some scenes in which sound suddenly becomes large like plosive sound in TV Commercial or Movie.
$\mathrm{P}^{2}$ Volume function automatically controls the volume and adjusts the output level. When a sound that pulses and is big is input, the recovery operation is done from $1 / 4$ to $1 / 32$ times the speed.

Use selection of scene change detection function
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| High frequency band \&h41[4] | 0 | Not use the scene changing detection |
| Low frequency band \&h41[3] | 1 | Use the scene changing detection |

Setting of release time at operating time when scene change detection function is used (R_RATE)
Release time is as (R_RATE / selection at operating time when scene is detected)
Default $=0$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| High frequency band \&h45[5:4] | Command Time <br> Low frequency band \&h45[1:0] 0 <br>  4 x <br>   <br> 2 8 x <br>   <br>  16 x <br>   |  |

Setting of scene change detection time
Default $=0$

| Select Address | Explanation of operation |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| High frequency band \&h43[6:4] | Command | Detection Time | Command | Detection Time |  |
| Low frequency band \&h44[6:4] | 0 | 50 ms | 4 | 300 ms |  |
|  | 1 | 100 ms | 5 | 400 ms |  |
|  |  | 2 | 150 ms | 6 | 500 ms |
|  | 3 | 200 ms | 7 | 600 ms |  |

Behavior level setting of scene change detection function
Begin operation of the difference with the value detected now based on the value immediately before.
Default $=0$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| High frequency band \&h43[3:0] | Command | Detection level\| | Command | Detection level |
|  | 0 | -50dB | 8 | -34dB |
|  | 1 | -48dB | 9 | -32dB |
|  | 2 | -46dB | A | -30dB |
|  | 3 | -44dB | B | -28dB |
|  | 4 | -42dB | C | - |
|  | 5 | -40dB | D | - |
|  | 6 | -38dB | E | - |
|  | 7 | -36dB | F | - |

Selection of 2Band P2Volume composition
The standard is used with 2Band P2Volume, and use as 1 Band $P^{2}$ Volume is also possible.
Select HPF and APF of the crossover filter and select a through setting to compose 1Band $\mathrm{P}^{2}$ Volume.
When using it with 1Band $P^{2}$ Volume, band on high frequency side is used. Therefore, please set it only for the high frequency side.
[Procedure]

1) $\& h 91=12$ h: Select the HPF of 2 Band $P^{2}$ Volume
2) $\& \mathrm{~h} 92=60 \mathrm{~h}:$ Select the Filter through
3) $\& \mathrm{~h} 96=01 \mathrm{~h}$ : Please start to transfer to coefficient RAM
4) $\& h 91=13 \mathrm{~h}$ : Select the APF of 2 Band $P^{2}$ Volume
5) \&h92 $=60 \mathrm{~h}$ : Select the filter through
6) $\& h 96=01 \mathrm{~h}$ : Please start to transfer to coefficient RAM

Please refer to the chapter of 4-8 parametric equalizer for the setting of the crossover filter that divides a high region and a low region of 2 Band $P^{2}$ Volume.

## 4-6. Surround

Surround 1 emphasizes the stereo feeling, and is suitable for the music source.
Surround 2 is effective of a pseudostereo. Because the monaural voice is pseudomade a stereo, it is suitable for the talk show etc. of the studio recording.

Surround1 function ON/OFF
Default $=0$

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h80 [7] | 0 | Surround1 OFF |  |
|  | 1 | Surround1 ON |  |

Surround2 function ON/OFF
Default $=0$

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h80 [6] | 0 | Surround2 OFF |  |
|  | 1 | Surround2 ON |  |

## Surround1

\& $\mathrm{h} 86[7: 0]$
$+48 \mathrm{~dB} \sim-79 \mathrm{~dB},-\infty$
(0.5dB step)

Lch


Please refer to the chapter of 4-8 parametric equalizer for the setting of BQ1 and BQ2.
BQ1 recommends the setting of High Pass Filter.
BQ2 recommends the setting of Low Pass Filter.

Delay value of feedback part setting for surround effect 1 (Delay1)
Default $=1 \mathrm{~h}$

| Select Address | Explanation of operation |
| :---: | :--- |
| \&h81 [ 3:0] | The command value becomes the amount of the delay. <br> One sample delay is about 21 $\mu \mathrm{s}$. <br> "0" is a set prohibition. |

Delay value of input part setting for surround effect 1 (Delay2)
Default = Oh

| Select Address | Explanation of operation |
| :---: | :--- |
| \&h82 [7:4] | The command value becomes the amount of the delay. <br> One sample delay is about $21 \mu \mathrm{~s}$. |

Delay value of input part setting for surround effect 1 (Delay3)
Default $=1 \mathrm{~h}$

| Select Address | Explanation of operation |
| :---: | :--- |
| \&h82 [3:0] | The command value becomes the amount of the delay. <br> One sample delay is about $21 \mu \mathrm{~s}$. <br> " 0 " is a set prohibition. |

Additive gain setting for surround effect 1 (G1, G2, G3)
Default = FFh

| Select Address | Explanation of operation |  |  |
| :---: | :---: | :---: | :---: |
| G1: \&h83 [7:0] |  | Command | Gain |
| G2: \&884 [7:0] | 00 | +48 dB |  |
| G3: \&h85 [7:0] |  | 01 | +47.5 dB |
|  |  | $\vdots$ | $\vdots$ |
|  |  | 60 | 0 dB |
|  |  | 61 | -0.5 dB |
|  |  | 62 | -1 dB |
|  |  | $\vdots$ | $\vdots$ |
|  |  | FE | -79 dB |
|  |  | FF | $-\infty$ |

Additive gain setting for surround effect 1 (G4)
Default $=60 \mathrm{~h}$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| \&h86 [7:0] | Command | Gain |
|  | 00 | +48dB |
|  | 01 | $+47.5 \mathrm{~dB}$ |
|  | : | ! |
|  | 60 | OdB |
|  | 61 | $-0.5 \mathrm{~dB}$ |
|  | 62 | -1dB |
|  | : | : |
|  | FE | -79dB |
|  | FF | - |

Additive gain setting for surround effect 1 (G5)
Default = FFh

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| \& h 87 [ 7:0] | Command | Gain |
|  | 00 | +48dB |
|  | 01 | +47.5dB |
|  | ! | ! |
|  | 60 | OdB |
|  | 61 | $-0.5 \mathrm{~dB}$ |
|  | 62 | -1dB |
|  | ! | : |
|  | FE | -79dB |
|  | FF | $-\infty$ |

Surround2


Select of surround effect 2 APF All Pass Filter)
Select which channel of L/Rch to insert APF.
Default $=0$

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h88 [7] | 0 | Lch |  |
|  | 1 | Rch |  |

Cut off frequency of APF setting for surround effect 2
Default $=0$

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&h88 [6:4] | 0 | 22 Hz |
|  | 1 | 47 Hz |
|  | 2 | 100 Hz |
|  | 3 | 220 Hz |
|  | 4 | 470 Hz |

LR mixing gain setting for surround effect 2
Change the LR mix gain in surround effect 2 . The sound extends to the setting of about big gain.
Default $=0 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| \&h88 [2:0] | Command Gain Command Gain <br>  0 $x 0$ 4 <br> 1 $x 0.05$ 5 $x 0.2$ <br>   2 $x 0.1$ <br> 3 $x 0.15$ 7 $x 0.3$ <br>   7 $x 0.35$ |  |  |  |
|  |  |  |  |  |

Output gain setting for surround effect 2
Change the gain of the channel opposite to the channel selected with \&h88 [7].
Default $=60 \mathrm{~h}$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| \&h89 [7:0] | Command Gain  <br>  00 +48 dB <br>   01 <br> $\vdots$ +47.5 dB  <br>   $\vdots$ <br>   00 <br>  0 dB  <br>   -0.5 dB <br>   -1 dB <br> $\vdots$ $\vdots$  <br>   -79 dB <br>   $-\infty$ |  |

## 4-7. Pseudo bass ( $\mathrm{P}^{2}$ Bass + )

A Pseudo bass function is a function which turns into that it is possible to emphasize low frequency sound effectively also to the low speaker of low-pass reproduction capability.

In order to be audible as the fundamental wave is sounding in false by adding 2 double sounds and 3 -time sound to a fundamental wave, the reproduction capability of the band of a fundamental wave becomes possible.
Although use independently is also possible for a pseudo bass function, low-pitched sound can be emphasized more by combining with P2Bass function.
Moreover, since it is possible to change the band to emphasize, optimizing to the frequency characteristic of the speaker to be used is possible.


## Pseudobass ON/OFF

The effect of the bass emphasis of a pseudobass (overtone) is used.
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h8C [ 7 ] | 0 | Not use pseudobass (overtone) |
|  | 1 | Use pseudobass (overtone) |

Setting of pseudo bass input HPF1 (The super-low element of the fundamental harmonic input to the overtone generator can be cut.)

Default $=0 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| \&h8C [ 3:0 ] |  | Command | Frequency | Command | Frequency |
|  | 0 | OFF | 8 | 82 Hz |  |
|  |  | 1 | 22 Hz | 9 | 100 Hz |
|  |  | 2 | 27 Hz | A | 120 Hz |
|  |  | 3 | 33 Hz | B | 150 Hz |
|  |  | 4 | 39 Hz | C | 180 Hz |
|  |  | 6 | 47 Hz | D | 220 Hz |
|  |  | 6 | 56 Hz | E | 270 Hz |
|  |  | 7 | 68 Hz | F | 330 Hz |

Pseudobass input LPF1 selection. (The low element of the fundamental harmonic that the overtone generator inputs is extracted)

Default $=0 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| \& h 8 D [ 7:4] | Command | Frequency | Command | Frequency |
|  | 0 | 68 Hz | 8 | 330 Hz |
|  | 1 | 82 Hz | 9 | 390 Hz |
|  | 2 | 100Hz | A | 470Hz |
|  | 3 | 120 Hz | B | 560 Hz |
|  | 4 | 150 Hz | c | 680 Hz |
|  | 5 | 180Hz | D | 820 Hz |
|  | 6 | 220 Hz | E | 1000Hz |
|  | 7 | 270 Hz | F | 1200 Hz |

LPF2 setting for 2 overtones and 3 overtones. (The harmonic content of the overtone is suppressed with this LPF)
Default $=0 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| \&h8D [ 3:0] | Command | Frequency | Command | Frequency |
|  | 0 | 68 Hz | 8 | 330 Hz |
|  | 1 | 82 Hz | 9 | 390 Hz |
|  | 2 | 100 Hz | A | 470 Hz |
|  | 3 | 120 Hz | B | 560 Hz |
|  | 4 | 150 Hz | c | 680 Hz |
|  | 5 | 180 Hz | D | 820Hz |
|  | 6 | 220 Hz | E | 1000 Hz |
|  | 7 | 270 Hz | F | 1200 Hz |

Additive gain setting for 3 overtones
When the input of the fundamental wave component is assumed to be 0 dB , the output of the fundamental wave component from the overtone generator becomes -3 dB .
(Output = Input - 3dB)
Default $=7 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| \&h8E [ 7:4] | Command | Gain | Command | Gain |
|  | 0 | $-\infty$ | 8 | 7 dB |
|  | 1 | OdB | 9 | 8 dB |
|  | 2 | 1 dB | A | 9dB |
|  | 3 | 2 dB | B | 10dB |
|  | 4 | 3 dB | C | 11dB |
|  | 5 | 4 dB | D | 12dB |
|  | 6 | 5 dB | E | 13dB |
|  | 7 | 6dB | F | 14dB |

Additive gain setting for 2 overtones
When the input of the fundamental wave component is assumed to be 0 dB , the output from the overtone generator becomes -6dB.
(Output = Input -6 dB )
Default $=7 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| \&h8E [ 3:0] | Command | Gain | Command | Gain |
|  | 0 | $-\infty$ | 8 | 1 dB |
|  | 1 | -6dB | 9 | 2dB |
|  | 2 | -5dB | A | 3 dB |
|  | 3 | -4dB | B | 4 dB |
|  | 4 | -3dB | c | 5 dB |
|  | 5 | -2dB | D | 6 dB |
|  | 6 | -1dB | E | 7 dB |
|  | 7 | OdB | F | 8dB |

Subtraction gain setting for 3 overtones (recommendation value: -8 dB or -6 dB )
Default $=4 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| \&h8F [6:4] | Command Gain Command Gain <br>  0 $-\infty$ 4 <br> 1 $-6 d B$   <br> 2 -12 dB 5 -4 dB <br>   -10 dB 6 <br>  -2 dB   <br>   -8 dB 7 |  |  |  |
|  |  |  |  |  |

Setting at blind time of odd-order overtone generation circuit
The high frequency signal that cannot be attenuated with LPF is included in the LPF1 outgoing signal input to the overtone generation circuit. It is set the blind time to do an unnecessary zero-cross point masking.


Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h8F [ 1:0 ] | 0 | $1.25 \mathrm{~ms}($ LPF1 Fc $=47 \mathrm{~Hz}$ to 180 Hz$)$ |
|  | 1 | $0.625 \mathrm{~ms}($ LPF1 Fc $=220 \mathrm{~Hz}$ to 390 Hz$)$ |
|  | 2 | $0.3125 \mathrm{~ms}($ LPF1 Fc $=470 \mathrm{~Hz}$ to 800 Hz$)$ |

## 4-8. Parametric Equalizer

In this IC, the following block has the feature of the parametric equalizer.
Crossover filter of the P2Volume block, Two BQ (Bi-Quad Filter) of surround 1 block, 8Band BQ (Main-output), 1Band BQ (Sub-output), Four BQ of Main clossover filter block, Four BQ of Sub clossover filter, Clossover filter of 2Band DRC block and $B Q$ of the smooth transition.
The shape is used peaking filter, low shelf filter, high shelf filter, lowpass filter, highpass filter and all path filter.
The setting is to choose F, Q, Gain, and changes into the coefficient of the digital filter in the IC and it transfers to the coefficient RAM. 8Band BQ (Main) and 1Band BQ (Sub) have the soft transfer feature. Incidentally, the detailed order of the parameter setting refer to the following PEQ setting method.

The coefficient RAM that stores a filter coefficient owns four banks and the command can choose it. The coefficient RAM for the parametric equalizer can set a coefficient to the bank-memory but the bank-memory during sound reconstruction.

Select of bank memory for coefficient RAM used to reproduce
Default $=0 h$

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&hA1 [7:6] | 0 | BANK1 |  |
|  | 1 | BANK2 |  |
|  | 2 | BANK3 |  |
|  | 3 | BANK4 |  |

Select of bank memory used to set coefficient

> Default = 0h

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&hA1 [5:4 ] | 0 | BANK1 |
|  | 1 | BANK2 |
|  | 2 | BANK3 |
|  | 3 | BANK4 |

Sampling frequency selection of coefficient automatic calculated circuit
Default $=0 \mathrm{~h}$

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&h90 [1:0] | 0 | For 48 kHz |
|  | 1 | For 44.1 kHz |
|  | 2 | For 32 kHz |

Select of PEQ setting
Lch and Rch are set same value.

| Select Address | Explanation of operation |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| \&h91 [ 4:0] | Command | PEQ | Command | PEQ | Command | PEQ | Command | PEQ |
|  | 00 | 8BandBQ(1) | 08 | 1BandBQ | 10 | Sub XOVF BQ4 | 18 | - |
|  | 01 | 8BandBQ(2) | 09 | Main XOVF BQ1 | 11 | Smooth Tran.BQ | 19 | - |
|  | 02 | 8BandBQ(3) | OA | Main XOVF BQ2 | 12 | $\mathrm{P}^{2}$ Volume HPF | 1 A | - |
|  | 03 | 8BandBQ(4) | OB | Main XOVF BQ3 | 13 | $\mathrm{P}^{2}$ Volume APF | 1B | - |
|  | 04 | 8BandBQ(5) | OC | Main XOVF BQ4 | 14 | 2BandDRC HPF | 1 C | - |
|  | 05 | 8BandBQ(6) | OD | Sub XOVF BQ1 | 15 | 2BandDRC APF | 1D | - |
|  | 06 | 8BandBQ(7) | OE | Sub XOVF BQ2 | 16 | Surround HPF | 1E | - |
|  | 07 | $8 \mathrm{BandBQ}(8)$ | OF | Sub XOVF BQ3 | 17 | Surround LPF | 1F | - |

$8 B$ and $B Q, 1$ Band $B Q$ :
$B Q$ is Bi -Quad-type digital filter.
$B Q$ for smooth transition:
It is a filter without the switch shock sound to do as for the coefficient setting and the change of $8 B$ and $B Q$ and 1 Band BQ.
Main/Sub XOVF (CrossOver Filter):
The crossover filter of the eighth Linkwitz-Riley type can be composed by using four BQ.
$P^{2}$ Volume HPF/APF:
The crossover filter of 2Band P2Volume block should be set to high path filter and all pass filter.
2 Band DRC HPF/APF:
The crossover filter of 2Band DRC block should be set to high path filter and all pass filter.
Surround HPF/LPF:
BQ1 recommends the setting of high pass filter, and BQ2 recommends the setting of low pass filter to two BQ in the surround block.

Select of filter type
Default $=0 \mathrm{~h}$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :---: |
| \& h 92 [ 6:4] | 0 | Peaking Filter |
|  | 1 | Low Shelf Filter |
|  | 2 | High Shelf Filter |
|  | 3 | Low Pass Filter |
|  | 4 | High Pass Filter |
|  | 5 | All Pass Filter |
|  | 6 | Filter through |

Select of smooth transition
Default $=0 \mathrm{~h}$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h92 [ 2 ] | 0 | Use smooth transition |
|  | 1 | Not use smooth transition |

Setting of smooth transition time
Default $=0 \mathrm{~h}$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h92 [1:0] | 0 | 21.4 ms |
|  | 1 | 10.7 ms |
|  | 2 | 5.4 ms |

Setting of frequency ( $\mathrm{F}_{0}$ )
Default $=0 \mathrm{Eh}$


Setting of quality factor ( Q )
Default $=5 \mathrm{~h}$

| $\begin{gathered} \text { Select Address } \\ \hline \text { \&h94 [4:0] } \end{gathered}$ | Explanation of operation |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Command | Q | Command | Q | Command | Q | Command | Q |
|  | 00 | 0.33 | 08 | 1.2 | 10 | 5.6 | 18 | 1.932 |
|  | 01 | 0.39 | 09 | 1.5 | 11 | 6.8 | 19 | 0.51 |
|  | 02 | 0.47 | OA | 1.8 | 12 | 8.2 | 1A | 0.601 |
|  | 03 | 0.56 | OB | 2.2 | 13 | 0.707 | 1 B | 0.9 |
|  | 04 | 0.68 | oc | 2.7 | 14 | 0.541 | 1 C | 2.563 |
|  | 05 | 0.75 | OD | 3.3 | 15 | 1.307 | 1 D | - |
|  | 06 | 0.82 | OE | 3.9 | 16 | 0.518 | 1 E | - |
|  | 07 | 1.0 | OF | 4.7 | 17 | 0.707 | 1 F | - |

Second butterworth is set to 13h. (BQx1) Fourth butterworth is set to $14 \mathrm{~h}, 15 \mathrm{~h}$. (BQx2)
Sixth butterworth is set to $16 \mathrm{~h}, 17 \mathrm{~h}, 18 \mathrm{~h}$. (BQx1) Eighth butterworth is set to $19 \mathrm{~h}, 1 \mathrm{Ah}, 1 \mathrm{Bh}, 1 \mathrm{Ch} .(\mathrm{BQx4})$
Setting of gain (Gain)
Default = 40h

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| \&h95 [ 6:0] | Command | Gain |
|  | 1 C | -18dB |
|  | : | : |
|  | 38 | -1dB |
|  | 39 | $-0.5 \mathrm{~dB}$ |
|  | 40 | OdB |
|  | 41 | +0.5dB |
|  | 42 | +1dB |
|  | ! | ! |
|  | 64 | +18dB |

When the each coefficient (b0, b1, b2, a1, a2) exceeds $\pm 4$, it is not possible to set it.
Transfer start setting to coefficient RAM
Default = 0

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h96 [0] | 0 | Transfer stop |
|  | 1 | Transfer start (After transferring is completed, it becomes 0 by the <br> automatic operation.) |

Setting of smooth transition start
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h97 [0] | 0 | Stop the smooth transition operation |
|  | 1 | Start the smooth transition operation (After the transition is completed, <br> it becomes 0 by the automatic operation) |

[^5]Read-out smooth transition status

| Select Address | Explanation of operation |
| :---: | :--- |
| \&h98 [ 0 ] | "1" is read while software is changing. <br> "0" is read usually. |

[Attention] The data of coefficient RAM can be read. Set values such as F, Q, and Gain cannot be read.
[Example of coefficient setting procedure 1]
Ex) Set fc=1kHz, Q=1.0, Gain=+6dB, and Filter type=Peaking Filter to 8Band BQ1 by using the soft transition function.
Sampling frequency: fs $=48 \mathrm{kHz}$, Smooth transition time: 21.4 ms , Bank memory: BANK0

1) \&hA1 $[7: 6]=0 h * 1 \quad$ : Set the BANKO
2) \&hA1 $[5: 4]=0 h$ *1 : Set the BANKO
3) $\& \mathrm{~h} 90$ [1:0] $=0 \mathrm{~h} \quad$ : Set sampling frequency to 48 kHz
4) \&h91 [4:0] = 00h : Select 8Band BQ1
5) $\& \mathrm{~h} 92[7: 0]=00 \mathrm{~h}$
\&h92 [6:4] = Oh : Select Peaking Filter
\& 92 [2] = 0h : Use smooth transition
\&h92 [1:0] = Oh : Set smooth transition time to 21.4 ms
6) \& h93 [5:0] $=22 \mathrm{~h} \quad$ : Set frequency to $1 \mathrm{kHz}(\mathrm{f0})$
7) \&h94 [4:0] $=07 \mathrm{~h} \quad$ : Set quality factor to 1.0
8) \&h95 [6:0] $=4 \mathrm{Ch} \quad$ : Set gain level to +6 dB
9) \&h96 [0] = 1h
: Transferring start to coefficient RAM for smooth transition
(After transferring is completed, it is cleared automatically to Oh.)
10) Even the transferring completion waits for about $150 \mu \mathrm{~s}$.
11) \&h97 [0] = $1 \mathrm{~h} \quad$ : Smooth transition start
(After smooth transition is completed, it is cleared automatically to 0 h. )
12) About 21.4 ms stands by to the smooth transition completion. Or, it stands by until 0 is read, and command $\& \mathrm{~h} 98$ is cleared to 0 h .
*1 When the clock stop automatic return function is made effective, $\& \mathrm{hA} 1$ [5:4] is set by the automatic operation depending on the input sampling frequency. (However, the value of this register is not reflected.)
Therefore, if the coefficient is written, the setting of \&hA1 [5:4] should set Oh when the input sampling frequency is 48 kHz . And it should be set to 1 h when sampling frequency is 44.1 kHz .
[Example of coefficient setting procedure 2]
Ex) Set $\mathrm{fc}=200 \mathrm{~Hz}, \mathrm{Q}=0.707$ and Filter type=Peaking Filter to 1 Band BQ by using the soft transition function.
13) \&hA1 $[5: 4]=0 h \quad$ : Set BANKO
14) $\&$ h90 $[1: 0]=1 \mathrm{~h} \quad$ : Set sampling frequency to 44.1 kHz
15) \&h91 $[4: 0]=08 \mathrm{~h} \quad$ : Select 1Band BQ
16) $\& h 92[7: 0]=34 \mathrm{~h}$
\&h92 [6:4] $=3 \mathrm{~h} \quad$ : Select Low Pass Filter
\&h92 [2] = 1h : Not use smooth transition
17) \&h93 [5:0] $=14 \mathrm{~h} \quad:$ Set frequency to $200 \mathrm{~Hz}(\mathrm{FO})$
18) \&h94 [4:0] = 17h : Set quality factor to 0.707 (Q)
19) \&h95 [6:0] = 40h : Because Low Pass Filter was selected; the setting of the gain can be omitted.
20) \&h96 [0] = 1h : Transferring start to coefficient RAM for smooth transition
(After transferring is completed, it is cleared automatically to Oh.)
21) Even the transferring completion waits for about $150 \mu \mathrm{~s}$.

## 4-9. Scaler

Scaler adjusts the gain in order to prevent the overflow in DSP. Adjustable range is +24 dB to -79 dB and can be set by the step of 0.5 dB . Scaler 1 does not incorporate the smooth transition function.

Default $=60 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |
| :---: | :---: | :---: | :---: |
| \&h23 [7:0] |  | Command | Gain |
|  | 00 | +48 dB |  |
|  |  | 01 | +47.5 dB |
|  |  | $\vdots$ | $\vdots$ |
|  |  | 60 | 0 dB |
|  |  | 61 | -0.5 dB |
|  |  | 62 | -1 dB |
|  |  | $\vdots$ | $\vdots$ |
|  |  | FE | -79 dB |
|  |  | FF | $-\infty$ |

4-10. 512 Tap FIR Filter x 2ch
The FIR filter of 512 taps is used for adjusting speaker characteristics for a flat or preparing the acoustic feature of a listening room.

Many bands near the adjustment point influence and P-EQ of the IIR type filter mutually. Although a desirable result is obtained, the number of times of an IIR filter of trial and error may increase.

Since a FIR filter has many Tap numbers, it can be brought close to an ideal acoustic feature easily.
Moreover, when doing fine adjustment with a P-EQ filter, a "ringing noise" and a "smearing (dirt of sound) noise" may occur. With a FIR filter, it is satisfactory.

Straighten the sound characteristic of the audio all bandwidth by using 512Tap FIR Filter for the music centre of two way compositions. Afterwards, use 4BQ Crossover filter and divide into the frequency for the tweeter and for woofer. The number of taps of FIR filters becomes 512 taps or less per channel. A characteristic that three operation modes, and is different by Lch and Rch can be set.
The coefficient expresses $\pm 1$ by 24bit composition.


MODE I 512 Taps mode (The coefficient of Lch/Rch is common.)

- Coefficient RAM is 2 BANK system.
- 257Taps to 512 Taps (Empty Tap is "0")


MODE I
FIR Coefficient


MODE II 256 Taps mode (The coefficient of Lch/Rch is common.)

- Coefficient RAM is 4 BANK system.
- 64 Taps to 256 Taps (Empty Tap is "0")

MODE II


MODEIII 256 Taps mode (The coefficient of Lch/Rch is independence.)

- Coefficient RAM is 2 BANK system.
- 64 Taps to 256 Taps (Empty Tap is "0")

MODEIII


FIR Coefficient


FIR filter mode setting
Default $=0 \mathrm{~h}$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hA0 [1:0] | 0 | MODE I :512Tap to 257Tap (Lch/Rch same coefficient) |
|  | 1 | MODE II:256Tap to 64Tap (Lch/Rch same coefficient) |
|  | 2 | MODE III:256Tap to 64Tap (Lch/Rch independent coefficient) |

FIR filter bank memory setting
Default $=0 \mathrm{~h}$

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&hA1 [3:2] | 0 | BANK1 |
|  | 1 | BANK2 |
|  | 2 | BANK3 |
|  | 3 | BANK4 |

When MODE I and MODEIII are used, BANK3 and 4 cannot be selected.
Memory address specification of Filter coefficient
It is used \&hA2 and \&hA3 commands when you write the coefficient of the FIR filter.

- MODE I (Lch/Rch same coefficient)

| 24bit Coefficient Number | \&hA2 | \&hA3 |
| :---: | :---: | :---: |
| K0 | 00 | 00 |
| K1 | 00 | 01 |
| K2 | 00 | 02 |
| $\vdots$ | $:$ | $\vdots$ |
| K255 | 00 | FF |
| K256 | 01 | 00 |
| K257 | 01 | 01 |
| $\vdots$ | $:$ | $\vdots$ |
| K509 | 01 | FD |
| K510 | 01 | FE |
| K511 | 01 | FF |

- MODE II (Lch/Rch same coefficient)

| 24bit Coefficient Number | \&hA2 | \&hA3 |
| :---: | :---: | :---: |
| K0 | 00 | 00 |
| K1 | 00 | 01 |
| K2 | 00 | 02 |
| $:$ | $:$ | $\vdots$ |
| K253 | 00 | FD |
| K254 | 00 | FE |
| K255 | 00 | FF |

- MODEIII(Lch/Rch independent coefficient)

| 24bit Coefficient Number | \&hA2 | \& hA 3 | 24bit Coefficient Number | \&hA2 | \&hA3 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| KOL | 00 | 00 | KOR | 01 | 00 |
| K1L | 00 | 01 | K1R | 01 | 01 |
| K2L | 00 | 02 | K2R | 01 | 02 |
| : | : | : | : | : | : |
| K253L | 00 | FD | K253R | 01 | FD |
| K254L | 00 | FE | K254R | 01 | FE |
| K255L | 00 | FF | K255R | 01 | FF |

About transferring coefficient data to coefficient RAM
Transferring 24bits coefficient to coefficient RAM specified with \&hA2 and \&hA3.
Default $=0 h$

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&hA7 [0] | 0 | Stop transferring |
|  | 1 | Start transferring |

After forwarding is completed, it is cleared to " 0 " automatically.
[Procedure 1] Writing sequence

1) $\& \mathrm{hAO}=00 \mathrm{~h}$
: Select MODE I
2) $\& \mathrm{hA} 1=$ *Oh : Select BANK0
3) $\& \mathrm{hA} 2=00 \mathrm{~h} \quad:$ When the address of K256 or more is specified, it is assumed 01 h .
4) $\& \mathrm{hA} 3=00 \mathrm{~h} \quad:$ Memory address specification in which coefficient is written
5) \&hA4 $=$ **h : Specify the coefficient data [23:16]
6) $\& h A 5=* * h \quad$ Specify the coefficient data [15:7]
7) $\& \mathrm{hA6}=* * \mathrm{~h} \quad$ : Specify the coefficient data $[7: 0]$
8) $\& h A 7=01 \mathrm{~h} \quad:$ Transferring start to coefficient RAM
9) Wait for more than $100 \mu \mathrm{~s}$.

Repeat procedure from 4) to 9 ) when continuously writing it. (When the address of K256 or more is specified, it is set \&hA2 to 01h.)
[Procedure 2] Reading sequence

1) \&hA1 = *Oh : Select BANKO
2) $\& \mathrm{hA} 2=00 \mathrm{~h} \quad:$ When the address of K256 or more is specified, it is assumed 01 h .
3) $\& \mathrm{hA} 3=00 \mathrm{~h} \quad$ : Memory address specification in which coefficient is read
4) \&hD0 = ABh : Set reading register address
5) Read upper 8 bits ([23:16]) among coefficients 24 bit. (\&hAB[7:0])
6) Read middle 8bits ([15:8]) among coefficients 24bit. (\&hAC[7:0])
7) Read lower 8bits ([7:0]) among coefficients 24bit. (\&hAD[7:0])

Repeat procedure from 3) to 7) when continuously reading it. (When the address of K256 or more is specified, it is set \&hA2 to 01h.)

4-11. Channel setting with phase inversion function (Channel Mixer 2, 3)
Set the mixing of the sound of a left channel and a right channel of the digital signal output from DSP. The output of making to monaural from the stereo signal can be done. The difference signal of Lch and Rch can be output. Moreover, the phase inversion and the mute of each channel can be set. Channel Mixer2 is for the Main-output. Channel Mixer3 is for the Sub-output.

Channel Mixer 2, 3


Invert the output data to L out.
Default $=0$

| Select Address |  | Value | Explanation of operation |  |
| :---: | :---: | :--- | :--- | :---: |
| Mixer2 | \&h26 [7] | 0 | Normal (Not invert) |  |
|  | Mixer3 | \&h27 [7] | 1 |  | Invert $\quad$.

Select the output data to L out
Default = 1

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| Mixer2 \&h26 [6:4 ] <br> Mixer3 \&h27 [6:4 ] | 0 | Mute |
|  | 1 | Output the data of L in |
|  | 2 | Output the data of R in |
|  | 3 | Output the data of (Lch + Rch) / 2 |
|  | 4 | Output the data of (Lch - Rch) |
|  | 5 | Output the data of (Rch - Lch) |

Invert the output data to R out.
Default = 0

| Select AddressMixer2\% 26 [3] | Value | Explanation of operation |
| :---: | :---: | :---: |
|  | 0 | Normal (Not invert) |
| Mixer3 \&h27 [3] | 1 | Invert |

Select the output data to R out
Default $=2$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| Mixer2 \&h26 [ 2:0] | 0 | Mute |
| Mixer3 \&h27 [ 2:0] | 1 | Output the data of L in |
|  | 2 | Output the data of R in |
|  | 3 | Output the data of (Lch + Rch) / 2 |
|  | 4 | Output the data of (Lch - Rch) |
|  | 5 | Output the data of (Rch - Lch) |

4-12. 4 Band BQ x 2ch for Cross Over Filter (Main, Sub)
It is 4Band Bi-Quad Filter that can be used as Linkwitz-Riley type crossover filter.

- Lch/Rch simultaneous control
- Four coefficient memory bank function
- A coefficient automatic calculating mode and a direct set mode can be used.
- The filter property can be changed by the soft transition function while reproducing.


Refer to the chapter of 4-8 parametric equalizer for the setting.

## 4-13. Volume

Volume is from +24 dB to -103 dB , and can be selected by the step of 0.25 dB . At the time of switching of Volume, smooth transition is performed. Soft transition duration is optional with the command.
It becomes the following formula at the transition from AdB to BdB . C is smooth transition duration selected by \&h20 [5:4] command.

$$
\text { Transition time }=\left|\left(10^{\frac{\mathrm{A}}{20}}-10^{\frac{\mathrm{B}}{20}}\right) * \mathrm{C} \mathrm{~ms}\right|
$$

Setting of soft transition time
Default $=0$

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h20 [5:4 ] | 0 | 21.4 ms |  |
|  | 1 | 42.7 ms |  |
|  | 2 | 85.4 ms |  |

Setting of volume
Default $=$ FFh


Setting of fine volume
This command becomes effective by sending the following command after setting.
When using this command, it is possible to set a volume in 0.125 dB carving.
Setting of fine volume
Default $=0 h$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| Main \&h10[1:0] | 0 | 0 dB |
| Sub \&h12[1:0] | 1 | -0.125 dB |
| Moni1 \&h14[1:0] | 2 | -0.25 dB |
| Moni2 \&h16[1:0] | 3 | -0.375 dB |

## [Note1]

It is possible to use with the $0.5-\mathrm{dB}$ step in changing only \&h11 [7:0] when $\& \mathrm{~h} 10$ [1:0] $=0$.
(Sub, Moni1 and Moni2 are the same)
[Note2]
It is possible to use with the $0.125-\mathrm{dB}$ step in setting both $\& \mathrm{~h} 10$ [1:0] and $\& \mathrm{~h} 11$ [7:0]. (Sub, Moni1 and Moni2 are the same)

In case of \&h10 [1:0] $=0$, it becomes the set value of \&h11 [7:0].
In case of \&h10 [1:0] $=1$, it becomes the -0.125 dB set value of \&h11 [7:0].
In case of $\& h 10[1: 0]=2$, it becomes the -0.25 dB set value of $\& \mathrm{~h} 11[7: 0]$.
In case of $\& \mathrm{~h} 10$ [1:0] $=3$, it becomes the -0.375 dB set value of $\& \mathrm{~h} 11$ [7:0].
Because it is fixed by the transfer of \&h11 in any case, the soft transfer can be beforehand begun in the set value for the direct following of the purpose in setting \&h11 after setting in \&h10.


4-14. Balance
As for balance, it is possible to be attenuated at 1dB step width from volume setting value. The switch operation becomes a smooth transition. When the balance changes, smooth transition is done. Smooth transition duration becomes the same formula as the volume.

Setting of L/R balance
Default $=80 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |
| :---: | :---: | :---: | :---: |
| Main \&h18[7:0] | Command | Lch | Rch |
|  | 00 | OdB | - - |
| Sub \&h19[7:0] | 01 | OdB | $-126 \mathrm{~dB}$ |
| Moni1 \&h1A[7:0] | $7 E$ | $\stackrel{\vdots}{\square}$ |  |
| Moni2 \&h1B[7:0] | 7 E 7 F | OdB | - ${ }_{\text {- }}^{\text {OdB }}$ |
|  | 80 | OdB | OdB |
|  | 81 | -1dB | OdB |
|  | : | : | : |
|  | FE | -126dB | OdB |
|  | FF | - - | OdB |

4-15. 2 band DRC (Main)
This DRC is used in order to prevent speaker protection and the clip output of a large audio signal.
In addition to two bands of DRC for low and high frequency, there is DRC for the whole frequency in the latter part.
Non-clip output is possible. DRC for low frequency band and DRC for high frequency band can set up two threshold value levels. Moreover, it is possible to also change slope.

```
2 Band DRC block diagram
```



DRC transition figure


DRC input-and-output gain characteristics


The formula which asks for Slope alpha is described below.
Alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation.
$\alpha=\frac{10^{\frac{y}{20}}-10^{\frac{x}{20}}}{10^{\frac{T H}{20}}-10^{\frac{x}{20}}} \times 128$
TH is AGC_TH1. $x$ is input level. $y$ is output level.
Ex) It asks for alpha at the time of AGC_TH1 $=-12 d B, x=0 d B y=-$ 6dB
$\alpha=\frac{10^{\frac{-6}{20}}-10^{\frac{0}{20}}}{10^{\frac{-12}{20}}-10^{\frac{0}{20}}} \times 128$
$\alpha=85.266 \rightarrow 55_{\mathrm{H}}$
55 H calculated is set as $\& \mathrm{~h} 25$ or $\& \mathrm{~h} 2 \mathrm{~A}$

Volume Curve


ON/OFF setting of DRC for all frequency band.
OFF is through output.
Default = 1

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h40[1] | 0 | Not use |  |
|  | 1 | Use |  |

ON/OFF setting of DRC1 for high frequency band. (DRC which can perform slope variable)
OFF is through output.
Default = 1

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h40[5] | 0 | Not use |  |
|  | 1 | Use |  |

ON/OFF setting of DRC2 for high frequency band. (Compressor)
OFF is through output.
Default = 1

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&h40[4] | 0 | Not use |
|  | 1 | Use |

ON/OFF setting of DRC1 for low frequency band. (DRC which can perform slope variable)
OFF is through output.
Default = 1

| Select Address | Value |  |
| :---: | :---: | :--- |
| $\& 40[3]$ | 0 | Not use |
|  | 1 | Use |

ON/OFF setting of DRC2 for low frequency band. (Compressor)
OFF is through output.
Default $=1$

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&h40[2] | 0 | Not use |
|  | 1 | Use |

The volume curve at the time of an attack (A_RATE) is selected.
Default $=0$

| Select Address | Value | Explanation of operation |  |
| :---: | :---: | :--- | :--- |
| hh42[7] | 0 | Linear curve |  |
|  | 1 | Exponential curve |  |

The volume curve at the time of a release (R_RATE) is selected.
Default $=0$

| Select Address | Value | Explanation of operation |  |
| :---: | :---: | :--- | :--- |
| $42[3]$ | 0 | Linear curve |  |
|  | 1 | Exponential curve |  |

The choice of the DRC composition
It uses a standard in 2Band DRC but it is possible to use as 1Band DRC, too.
To make the composition of 1Band DRC, it chooses through setting in HPF and APF of the crossover filter.
[Procedure]

1) $\& h 91=14 \mathrm{~h}$ : It chooses HPF of the 2Band DRC.
2) $\& \mathrm{~h} 92=60 \mathrm{~h}$ : It chooses Filter through.
3) $\& \mathrm{~h} 96=01 \mathrm{~h}$ : It starts a transfer to the coefficient RAM.
4) $\&$ h91 $=15 \mathrm{~h}$ : It chooses APF of 2Band DRC.
5) $\&$ h92 $=60 \mathrm{~h}$ : It chooses Filter through.
6) $\& h 96=01 \mathrm{~h}$ : It starts a transfer to the coefficient RAM.

To set the crossover filter which divides the high frequency band and the low frequency band of 2Band DRC, therefore, it is referred to the chapter 4-8.

AGC_TH setting of DRC for all band.
When using according to either of the DRC for the high area or the DRC for the low area bigger AGC_TH setting, the distortion in the crossover point can be suppressed.

Default $=40 \mathrm{~h}$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| \&h70[6:0] |  Command Threshold <br>  00 -32 dB <br>   $\vdots$ <br>  $\vdots$  <br>   3 F <br>   -0.5 dB <br>   40 <br>  0 dB  <br>   +0.5 dB <br>   $\vdots$ <br>    <br>   +12 dB |  |

A_RATE setting of DRC for all band. (The compression curve transition time in attack)
Default $=3 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| \&h72[6:4] | Command A_RATE time Command A_RATE time <br>  0 1 ms 4 <br> 5 ms    <br>  1 2 ms 5 <br> 10 ms    <br>  2 3 ms 6 <br> 20 ms    <br>   4 ms 7 | 40 ms |  |  |

R_RATE setting of DRC for all band. (The expansion curve transition time in release)
Default $=\mathrm{Bh}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| \&h72[3:0] | Command | R_RATE time | Command | R_RATE time |
|  | 0 | 0.125s | 8 | 2s |
|  | 1 | $0.1825 s$ | 9 | 2.5s |
|  | 2 | 0.25s | A | 3 s |
|  | 3 | 0.5 s | B | 4s |
|  | 4 | 0.75 s | c | 5 s |
|  | 5 | 1s | D | 6 s |
|  | 6 | 1.25s | E | 7s |
|  | 7 | 1.5 s | F | 8 s |

A_TIME setting of DRC for all band. (Setting of detection time for attack operation)
Default $=1 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| \& 73 [7:4] | Command | A_TIME time | Command | A_TIME time |
|  | 0 | Oms | 8 | 6 ms |
|  | 1 | 0.5 ms | 9 | 7 ms |
|  | 2 | 1 ms | A | 8 ms |
|  | 3 | 1.5 ms | B | 9 ms |
|  | 4 | 2 ms | c | 10 ms |
|  | 5 | 3 ms | D | 20 ms |
|  | 6 | 4 ms | E | 30 ms |
|  | 7 | 5 ms | F | 40 ms |

R_TIME setting of DRC for all band. (Setting of detection time for release operation)
Default $=3 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| \&h73 [2:0] | Command R_TIME time Command R_TIME time  <br>  0 5 ms 4 100 ms <br>   1 10 ms 5 <br> 200 ms     <br>   25 ms 6 300 ms <br>   5 50 ms 7 |  |  |  |

Slope ( $\alpha$ ) setting of DRC1 for high frequency band
Default $=80 \mathrm{~h}$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| \&h61 [7:0] |  | The formula which asks for Slope alpha is described below. <br> Alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation. $\alpha=\frac{10^{\frac{y}{20}}-10^{\frac{x}{20}}}{10^{\frac{T H}{20}}-10^{\frac{x}{20}}} \times 128$ <br> TH is AGC_TH1. $x$ is input level. $y$ is output level. <br> Ex) It asks for alpha at the time of AGC_TH1 $=-12 d B, x=0 d B y=-6 d B$ $\begin{aligned} & \alpha=\frac{10^{\frac{-6}{20}}-10^{\frac{0}{20}}}{10^{\frac{-12}{20}}-10^{\frac{0}{20}}} \times 128 \\ & \alpha=85.266 \rightarrow 55_{\mathrm{H}} \end{aligned}$ <br> 55 H calculated is set as \& h61 or \&h69 |

AGC_TH1 setting of DRC1 for high frequency band
Please set below to the setting value of AGC_TH2.
Default $=40 \mathrm{~h}$

| Select Address | Explanat | peration |
| :---: | :---: | :---: |
| \&h60 [6:0] | Command | Threshold |
|  | 00 | -32dB |
|  | ! | ! |
|  | 3F | -0.5dB |
|  | 40 | OdB |
|  | 41 | +0.5dB |
|  | ! | ! |
|  | 58 | +12dB |

AGC_TH2 setting of DRC2 for high frequency band
Default $=40 \mathrm{~h}$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| \&h64 [6:0] |  Command Threshold <br>  00 -32 dB <br>   $\vdots$ <br> 3 F -0.5 dB  <br>   40 <br> 1 0 dB  <br>   +0.5 dB <br>   $\vdots$ <br> 58 +12 dB  |  |

High frequency band A_RATE setting (It is the transition time of a compression curve at the time of an attack.) DRC1 and DRC2 for high frequency band are individually setting.
Default $=3 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| DRC1 \& h62 [6:4] | Command | A_RATE time | Command | A_RATE time |
| DRC2 \&h66 [6:4] | 0 | 1 ms | 4 | 5 ms |
|  | 1 | 2 ms | 5 | 10 ms |
|  | 2 | 3 ms | 6 | 20 ms |
|  | 3 | 4 ms | 7 | 40 ms |

High frequency band R_RATE setting (It is the transition time of an extension curve at the time of release.)
DRC1 and DRC2 for high frequency band are individually setting.
Default $=\mathrm{Bh}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| DRC1 \& $62[3: 0]$ | Command | R_RATE time | Command | R_RATE time |
| DRC2 \& $666[3: 0]$ | 0 | 0.125s | 8 | 2 s |
|  | 1 | 0.1825 s | 9 | 2.5s |
|  | 2 | 0.25s | A | 3 s |
|  | 3 | 0.5s | B | 4 s |
|  | 4 | 0.75 s | C | 5 s |
|  | 5 | 1s | D | 6 s |
|  | 6 | 1.25s | E | 7 s |
|  | 7 | 1.5s | F | 8 s |

A_TIME1 setting of DRC1 for high frequency band (Detection time setting of attack operation) DRC1 and DRC2 for high frequency band are individually setting.
Default $=1 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| DRC1 \& h63 [7:4] | Command | A_TIME time | Command | A_TIME time |
| DRC2 \&h67 [7:4] | 0 | Oms | 8 | 6 ms |
|  | 1 | 0.5 ms | 9 | 7 ms |
|  | 2 | 1 ms | A | 8 ms |
|  | 3 | 1.5 ms | B | 9 ms |
|  | 4 | 2 ms | C | 10 ms |
|  | 5 | 3 ms | D | 20 ms |
|  | 6 | 4 ms | E | 30 ms |
|  | 7 | 5 ms | F | 40ms |

R_TIME setting of DRC for high frequency band (Detection time setting of release operation)
DRC1 and DRC2 for high frequency band are individually setting.
Default $=3 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| DRC1 \& 663 [2:0] | Command | R_TIME time | Command | R_TIME time |
| DRC2 \& 667 [2:0] | 0 | 5 ms | 4 | 100 ms |
|  | 1 | 10 ms | 5 | 200 ms |
|  | 2 | 25 ms | 6 | 300 ms |
|  | 3 | 50 ms | 7 | 400 ms |

Slope ( $\alpha$ ) setting of DRC1 for low frequency band
Default $=80 \mathrm{~h}$


AGC_TH1 setting of DRC1 for low frequency band
Please set below to the setting value of AGC_TH2.
Default $=40 \mathrm{~h}$

| Select Address | Explanat | operation |
| :---: | :---: | :---: |
| \& $\mathrm{h68}$ [6:0] | Command | Threshold |
|  | 00 | -32dB |
|  | ! | : |
|  | 3F | -0.5dB |
|  | 40 | OdB |
|  | 41 | $+0.5 \mathrm{~dB}$ |
|  | ! | ! |
|  | 58 | +12dB |

AGC_TH2 setting of DRC2 for low frequency band Default $=40 \mathrm{~h}$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| \&h6C [6:0] | Command | Threshold |
|  | 00 | -32dB |
|  | ! | : |
|  | 3F | -0.5dB |
|  | 40 | OdB |
|  | 41 | +0.5dB |
|  | : | ! |
|  | 58 | +12dB |

Low frequency band A_RATE setting (It is the transition time of a compression curve at the time of an attack.)
DRC1 and DRC $\overline{2}$ for low frequency band are individually setting.
Default $=3 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DRC1 \&h6A [6:4] | Command A_RATE time Command A_RATE time <br> DRC2 \&h6E [6:4] 0 1 ms 4 <br> 1 2 ms 5 10 ms <br>   2 3 ms <br> 3 4 ms 7 20 ms <br>   40 ms  |  |  |  |
|  |  |  |  |  |

Low frequency band R_RATE setting (It is the transition time of an extension curve at the time of release.)
DRC1 and DRC2 for low frequency band are individually setting.
Default $=\mathrm{Bh}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| DRC1 \& h 6 A [3:0] | Command | R_RATE time | Command | R_RATE time |
| DRC2 \&h6E[3:0] | 0 | 0.125 s | 8 | 2s |
|  | 1 | 0.1825 s | 9 | 2.5s |
|  | 2 | 0.25s | A | 3 s |
|  | 3 | 0.5s | B | 4s |
|  | 4 | 0.75 s | C | 5 s |
|  | 5 | 1 s | D | 6 s |
|  | 6 | 1.25 s | E | 7s |
|  | 7 | 1.5s | F | 8s |

A_TIME1 setting of DRC1 for low frequency band (Detection time setting of attack operation)
DRC1 and DRC2 for low frequency band are individually setting.
Default $=1 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| DRC1 \& h6B [7:4] | Command | A_TIME time | Command | A_TIME time |
| DRC1 \& 6 6F [7:4] | 0 | Oms | 8 | 6 ms |
|  | 1 | 0.5 ms | 9 | 7 ms |
|  | 2 | 1 ms | A | 8 ms |
|  | 3 | 1.5 ms | B | 9 ms |
|  | 4 | 2 ms | C | 10 ms |
|  | 5 | 3 ms | D | 20 ms |
|  | 6 | 4 ms | E | 30 ms |
|  | 7 | 5 ms | F | 40 ms |

R_TIME setting of DRC for low frequency band (Detection time setting of release operation)
DRC1 and DRC2 for low frequency band are individually setting.
Default $=3 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DRC1 \&h6B [2:0] | Command R_TIME time Command R_TIME time <br> DRC2 \&h6F [2:0] 0 5 ms 4 <br>  100 ms   <br>   10 ms 5 <br> 200 ms    <br>   25 ms 6 <br> 300 ms    <br>   50 ms 7 | 400 ms |  |  |

[Question]
What is the purpose of DRC for all frequency band?

[Answer]
The purpose is for keeping constant the output level in the crossover point of low frequency band and high frequency band. A frequency characteristic figure with a cross over frequency 1.2 kHz of DRC for low frequency band and DRC for high frequency band is shown below.


Next, the graph of AGC_TH=0dB, cross over frequency $=1.2 \mathrm{kHz}$, and the frequency vs. output gain when not using all the DRC for all frequency bands is shown.


Input level 0 dB is a flat. However, on an input level of +6 dB or +12 dB , it is over 0 dB of a compression level near the cross over frequency.
In order to prevent this phenomenon, DRC for all frequency band is used. However, when this phenomenon does not exist in a problem, I think that it is not necessary to use DRC for all frequency band.
AGC_TH of DRC for all frequency band sets up AGC_TH2 value of the higher one, when AGC_TH2 differ by DRC for high frequency band, and DRC for low frequency band.
[Question]
Recommendation value setting of 2 band DRC?
[Answer]
The recommendation value of 2 band DRC was examined to speaker protection using FPD TV.
-A_RATE : 4ms
-R_RATE : 2s or more
-A_TIME : 0.5 ms
-R_TIME : 50ms or more
It is not uncomfortable to a music source to arrange all DRC (low frequency band, high frequency band, all frequency band) with the same value.
[Question]
When master volume is increased, why is it that only the sound of a high region becomes large?
[Answer]
It investigated about the cross over frequency and the relation of AGC_TH2 of DRC for high frequency band.
Its sound energy decreases, so that music data becomes high frequency. When a cross over frequency is set up highly, unless it lowers AGC_TH2 of DRC for high frequency band, when master volume is increased, the effect by limit cannot be heard.

The red line shows the Peak level.


About the amount of adjustments of AGC_TH2 of DRC for high frequency band.


Please use as a standard of the adjustment value from AGC_TH2 value of DRC for low frequency band.
Moreover, the amount of adjustments decreases by setting up a cross over frequency lowness.

4-16. DRC for Sub-output
This DRC is used in order to prevent speaker protection and the clip output of a large audio signal.
In to set three threshold levels, it is possible to do compression and expansion more smoothly in the sound.


DRC transition figure


DRC input-and-output gain characteristics


The formula which asks for Slope alpha1 and alpha2 is described below. Alpha changes into 8 bit Hex data of the complement of 2 the value calculated by calculation.
$x$ is input level, AGC_TH is output level.
$\mathrm{Ex}) \mathrm{x} 1=-12 \mathrm{~dB}, \mathrm{x} 2=-3 \mathrm{~dB}, \mathrm{x} 3=+3 \mathrm{~dB}, \mathrm{TH} 1=-12 \mathrm{~dB}, \mathrm{TH} 2=-8 \mathrm{~dB}$, TH3 $=-6 \mathrm{~dB}$
$\alpha 1=\frac{10^{\frac{-8}{20}}-10^{\frac{-3}{20}}}{10^{\frac{-12}{20}}-10^{\frac{-3}{20}}} \times 128, \quad \alpha 2=\frac{10^{\frac{-12}{20}}-\left(10^{\frac{-6}{20}}-10^{\frac{3}{20}}\right) \cdot \alpha 1-10^{\frac{3}{20}}}{10^{\frac{-8}{20}}-\left(10^{\frac{-12}{20}}-10^{\frac{3}{20}}\right) \cdot \alpha 1-10^{\frac{3}{20}}} \times 128$
$\alpha 1=86.828 \rightarrow 56_{\mathrm{H}} \quad \alpha 2=82.051 \rightarrow 52_{\mathrm{H}}$
Calculated $\alpha 1=56 \mathrm{H}$ is set as $\& h 75$, calculated $\alpha 2=52 \mathrm{H}$ is set as $\& \mathrm{~h} 79$.

## Volume Curve



ON/OFF setting of DRC1 for Sub-output.
OFF is through output.
Default $=1$

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h41 [7] | 0 | Not use |  |
|  | 1 | Use |  |

ON/OFF setting of DRC2 for Sub-output.
OFF is through output.
Default = 1

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h41 [6] | 0 | Not use |  |
|  | 1 | Use |  |

ON/OFF setting of DRC2 for Sub-output.(Compressor)
OFF is through output.
Default = 1

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&h41 [5] | 0 | Not use |
|  | 1 | Use |

The volume curve at the time of an attack (A_RATE) is selected.
Default $=0$

| Select Address | Value | Explanation of operation |  |
| :---: | :---: | :--- | :--- |
| $\& 42[6]$ | 0 | Linear curve |  |
|  | 1 | Exponential curve |  |

The volume curve at the time of a release (R_RATE) is selected.
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h42 [ 2 ] | 0 | Linear curve |
|  | 1 | Exponential curve |

Slope ( $\alpha$ ) setting of DRC1 and DRC2 for Sub-output
Default $=80 \mathrm{~h}$

| Select Address | Explanation of operation |
| :---: | :---: |
| $\begin{aligned} & \text { DRC1( } \alpha 1) ~ \& h 75[7: 0] \\ & \operatorname{DRC2(\alpha 2)~\& h79~[~7:0~]~} \end{aligned}$ |  <br> The formula which asks for Slope alpha1 and alpha2 is described below. Alpha changes into 8 bit Hex data of the complement of 2 the value calculated by calculation. $\alpha 1=\frac{\frac{\mathrm{TH2} 2}{10^{20}}-10^{\frac{x^{2}}{20}}}{10^{\frac{\mathrm{HI} 1}{20}}-10^{\frac{x^{2}}{20}}} \times 128, \quad \alpha 2=\frac{\frac{\mathrm{TH3}}{10^{20}}-\left(10^{\frac{\mathrm{TH1}}{201}}-10^{\frac{x^{3}}{20}}\right) \cdot \alpha 1-10^{\frac{x^{3}}{20}}}{10^{\frac{\mathrm{HD} 20}{20}}-\left(10^{\frac{\mathrm{TH1}}{20}}-10^{\frac{x^{3}}{20}}\right) \cdot \alpha 1-10^{\frac{x^{3}}{20}}} \times 128$ <br> $x$ is input level, AGC_TH is output level. <br> $\mathrm{Ex}) \times 1=-12 \mathrm{~dB}, \mathrm{x} 2=-3 \mathrm{~dB}, \times 3=+3 \mathrm{~dB}, \mathrm{TH} 1=-12 \mathrm{~dB}, \mathrm{TH} 2=-8 \mathrm{~dB}$, TH3 $=-6 \mathrm{~dB}$ $\alpha 1=\frac{\frac{-\frac{8}{20}}{10^{\frac{-12}{}}-10^{\frac{-3}{20}}}}{10^{\frac{-1}{20}}-10^{\frac{-3}{20}}} \times 128, \quad \alpha 2=\frac{\frac{-\frac{12}{20}}{10^{\frac{-8}{-\frac{6}{20}}}-\left(10^{\frac{3}{20}}-10^{\frac{-12}{20}}\right) \cdot \alpha 1-10^{\frac{3}{20}}} 110^{20}-\left(10^{\frac{30}{20}}-10^{\frac{3}{20}}\right) \cdot \alpha 1-10^{\frac{3}{20}}}{128}$ $\alpha 1=86.828 \rightarrow 56_{\mathrm{H}} \quad \alpha 2=82.051 \rightarrow 52_{\mathrm{H}}$ <br> Calculated $\alpha 1=56 \mathrm{H}$ is set as $\& \mathrm{~h} 75$, calculated $\alpha 2=52 \mathrm{H}$ is set as $\& \mathrm{~h} 79$. |

AGC_TH1, AGC_TH2 and AGC_TH3 setting of DRC for Sub-output
Please set to the value as below.
AGC_TH3 > AGC_TH2 > AGC_TH1
Default $=40 \mathrm{~h}$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| AGC_TH1 \&h74 [6:0] | Command | Threshold |
| AGC_TH2 \&h78 [6:0] | 00 | -32dB |
| AGC_TH3 \&h7C [6:0] | : | : |
|  | 3F | -0.5dB |
|  | 40 | 0dB |
|  | 41 | +0.5dB |
|  | ! | ! |
|  | 58 | +12dB |

A_RATE setting of DRC for Sub-output(It is the transition time of a compression curve at the time of an attack.)
Default $=3 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DRC1 \&h76 [6:4] | Command A_RATE time Command A_RATE time <br> DRC2 \&h7A [6:4] 0 1 ms 4 <br> DRC3 \&h7E [6:4] 1 2 ms 5 | 2 | 3 ms |  |
|  | 3 | 4 ms | 6 | 20 ms |
|  |  | 7 | 40 ms |  |

R_RATE setting of DRC for Sub-output (It is the transition time of an extension curve at the time of release.)
Default $=\mathrm{Bh}$

| Select Address | Explanation of operation |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DRC1 \&h76[3:0] | Command | R_RATE time | Command | R_RATE time |  |
| DRC2 \&h7A[3:0] | 0 | 0.125 s | 8 | 2 s |  |
| DRC3 \&h7E[3:0] | 1 | 0.1825 s | 9 | 2.5 s |  |
|  | 2 | 0.25 s | A | 3 s |  |
|  |  | 3 | 0.5 s | B | 4 s |
|  |  | 4 | 0.75 s | C | 5 s |
|  |  | 6 | 1 s | D | 6 s |
|  | 7 | 1.25 s | E | 7 s |  |
|  |  | 1.5 s | F | 8 s |  |

A_TIME setting of DRC for Sub-output (Detection time setting of attack operation.)
Default $=1 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| DRC1 \&h77 [7:4] | Command | A_TIME time | Command | A_TIME time |
| DRC2 \&h7B [7:4] | 0 | 0 ms | 8 | 6 ms |
| DRC3 \&h7F [7:4] | 1 | 0.5 ms | 9 | 7 ms |
|  | 2 | 1 ms | A | 8 ms |
|  | 3 | 1.5 ms | B | 9 ms |
|  | 4 | 2 ms | C | 10 ms |
|  | 5 | 3 ms | D | 20 ms |
|  | 6 | 4 ms | E | 30 ms |
|  | 7 | 5 ms | F | 40 ms |

R_TIME setting of DRC for Sub-output (Detection time setting of release operation.)
Default $=3 \mathrm{~h}$

| Select Address |  | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DRC1 | \&h77 [2:0] | Command R_TIME time Command R_TIME time <br>  DRC2 \&h7B [2:0] 0 <br> 5 ms 4 100 ms  <br> DRC3 \&h7F [2:0] 1 10 ms <br>   2 25 ms <br>  3 50 ms 7 <br> 200 ms    <br>   700 ms  <br>   400 ms  |  |  |  |

4-17. Post-scaler (DSP part)
To prevent from an overflow in the DSP, it adjusts a gain with the scaler. An adjustable range can be set up at a 0.5 dB step from +48 dB to -79 dB . Post-scaler does not have a smooth transition function.

$$
\text { Default }=60 \mathrm{~h}
$$

| Select Address |  | Explanation of operation |  |
| :---: | :---: | :---: | :---: |
| Main | \&h1C [7:0] |  | Command |
| Sub | \&h1D [7:0] | Gain |  |
| Moni1 | \&h1E [7:0] | 00 | +48 dB |
| Moni2 | \&h1F [7:0] |  | 01 |
|  |  | +47.5 dB |  |
|  |  | $\vdots$ |  |
|  |  | 60 | OdB |
|  |  | 62 | -0.5 dB |
|  |  | -dB |  |
|  |  | $\vdots$ | $\vdots$ |
|  |  | FE | -79 dB |

## 4-18. Hard Clipper (DSP part)

Signed 24bit data that cuts upper 6bits and lower 2bit of 32bit DSP is output to eight times over sampling digital filter part. It becomes saturation output for data that exceeds $\pm 12 \mathrm{~dB}$.


## $4-19$. Soft clipper

When measuring the rated output of the television, THD+N measures in $10 \%$. It can be made to clip with any output amplitude by using a clipper function. For example, the rated output of 10 W or 5 W can be gained using the amplifier of 15 W output.
Selection of a soft clip or a hard clip can be performed by this IC.

Soft clip

Clip level: OdB
Clip level:-3dB
Clip level: +3 dB

$\square$ clipper circuit

[Question]
Why does the soft clipper output lower than in the set clip level?
[Answer]
For example, when clipper level is set to 0 dB , it is as follows.
OdB input: $20^{*} \log \left(1-0.146 / 10^{\wedge}\left((0 / 20)^{*} 2\right)\right)=-1.37 \mathrm{~dB}$.
$6 d B$ input : $20^{*} \log \left(1-0.146 / 10^{\wedge}\left((6 / 20)^{*} 2\right)\right)=-0.32 d B$.

Hard clip

Clip level: OdB
clip level:-3dB
clip level: +3 dB


Clipper setting
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :---: |
| Main \&h35 [5:4] | 0 | Clipper function is not used. |
| Sub \&h35 [1:0] | 1 | Soft clipper function is used. |
|  | 2 | Hard clipper function is used. |

Clip level selection
Default $=\mathrm{E} 1 \mathrm{~h}$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| Main \&h36 [7:0] | Command | Gain |
| Sub \&h37 [7:0] | 00 | -22.5dB |
|  | ! | : |
|  | E0 | -0.1dB |
|  | E1 | OdB |
|  | E2 | +0.1dB |
|  | ! | ! |
|  | FF | +3dB |

4-20. Post-scaler (x8 Over sampling Digital Filter part)
Level adjustment in $x 8$ over sampling DF block. An adjustable range can be set up at a 0.1 dB step from +12 dB to -32 dB . Lch/Rch is independently controllable.
\&h38[0], \&h3A[0], \&h3C[0] and \&h3E[0] is MSB, and \&h3B[7:0], \&h3D[7:0], \&h3F[7:0] is LSB.
Post-scaler does not have a smooth transition function.
Default $=0 \mathrm{D} 2 \mathrm{~h}$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| Main Lch \&h38[0] | Command | Gain |
| Main Lch \&h39[ 7:0] | 000 | -32dB |
| Main Rch \&h3A[0] | : | : |
| Main Rch \&h3B[ 7:0] | 13F | -0.1dB |
| Sub Lch \&h3C[0] | 140 | OdB |
| Sub Lch \&h3D[ 7:0] | 141 | +0.1dB |
| Sub Rch \&h3E[0] | : | : |
| Sub Rch \& h 3 F [ 7:0] | 1B8 | +12dB |
|  | (Initial value:0D2h $\rightarrow-11 \mathrm{~dB}$ ) |  |

## 4-21. DC cut HPF (Latter part of DSP processing part)

DC offset element of the digital signal outputted from audio DSP is cut by this HPF.
The cutoff frequency fc of HPF uses the 1 Hz filter, and the degree uses the first-order filter.
Default = 1

| Select Address | Value |  |
| :--- | :---: | :--- |
| Main \&h28[1] | 0 | Not use |
| Sub \&h28[0] | 1 | Use |

## 4-22. Hard Clipper (x8 Over Sampling Digital Filter part)

The audio data is changed from <S1.22> to <S0.23> format. It is outputted to PWM Modulator.
As for insufficient subordinate position 1 bit, " 0 " data is inserted. It becomes saturation output when overflowing.


## 4-23. Higher sound complement (High Generator)

The higher frequency sound deleted when it encoded in MP3 form is complemented in pseudo.
This circuit consists of High Generator circuit and high shelf filter.
The High shelf filter part is used to make the effect of the high frequency band.


High generator setting for Main-output
Default = 0

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hB4 [7] | 0 | Not use High Generator |
|  | 1 | Use High Generator |

High generator setting for Sub-output
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hB4 [6] | 0 | Not use High Generator |
|  | 1 | Use High Generator |

Mute mode setting
Only the complemented sound can listen by this register setting.
Default $=0$

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&hB4 [5] | 0 | Mute OFF |  |
|  | 1 | Mute ON |  |

Please set to 0 at normally use.

High generator high shelf filter $f_{0}$ setting
It makes up the ON/OFF sense of the high generator function by this register.
Default $=0$

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :---: | :---: |
| \&hB4 [1:0] | 0 | 3.9 kHz |  |
|  | 1 | 4.7 kHz |  |
|  | 2 | 5.6 kHz |  |
|  | 3 | 6.8 kHz |  |

High generator HPF1 cut off frequency setting
Cut an unnecessary inside low element from the sound input to the high generator function.
Default = 0

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hB5 [6:4] | 0 | 5.6 kHz |
|  | 1 | 6.2 kHz |
|  | 2 | 6.8 kHz |
|  | 3 | 7.5 kHz |
|  | 4 | 8.2 kHz |
|  | 5 | 9.1 kHz |

High generator HPF2 cut off frequency setting
Cut the high pass element that became unnecessary after the generating harmonic of the even-ordered.
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hB5 [2:0] | 0 | 11.2 kHz |
|  | 1 | 12.4 kHz |
|  | 2 | 13.6 kHz |
|  | 3 | 15 kHz |
|  | 4 | 16.4 kHz |
|  | 5 | 18.2 kHz |
|  | 6 | 20 kHz |

High generator additional gain setting
Default $=0 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Main \&hB6 [7:4] | Command | Gain | Command | Gain |
| Sub \&hB7 [7:4] | 0 | $-\infty$ | 8 | 7dB |
| Sub \&hB7 [7.4] | 1 | OdB | 9 | 8 dB |
|  | 2 | 1dB | A | 9dB |
|  | 3 | 2dB | B | 10dB |
|  | 4 | 3dB | c | 11dB |
|  | 5 | 4 dB | D | 12dB |
|  | 6 | 5dB | E | - |
|  | 7 | 6 dB | F | - |

High shelf filter boost gain setting
Default $=0$

| Select Address | Value |  |
| :---: | :---: | :--- |
| Main \&hB6 [2:0] <br> Sub \&hB7 [2:0] | 0 | 0 dB |
|  | 1 | 1 dB |
|  | 2 | 2 dB |
|  | 3 | 3 dB |
|  | 4 | 4 dB |
|  | 5 | 5 dB |
|  | 6 | 6 dB |

The graph of frequency characteristic of ON/OFF of the high generator function is shown. Input data is a white noise made the MP3 of 128 kbps by sampling 44.1 kHz .

High generator OFF
Input source : White noise
Frequency : 20 to 40kHz


High generator ON HPF cut off : 5.6 kHz Additional gain : +3 dB


## 4-24. RAM clear

The data RAM of DSP and SRC, coefficient RAM, and NS register inside PWM processor block are cleared. $40 \mu \mathrm{~s}$ or more is required until all the data is cleared.

Clear of the data RAM and SRC
Default $=1$

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \& $01[7]$ | 0 | Normal |  |
|  | 1 | Clear operation |  |

Clear of coefficient RAM (BANK1, BANK2)
Default = 1

| Select Address | Value | Explanation of operation |  |
| :---: | :---: | :--- | :--- |
| \&h01 [6] | 0 | Normal |  |
|  | 1 | Clear operation |  |

Clear of PWM NS register inside PWM processor block
Default $=1$

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h01 [5] | 0 | Normal |  |
|  | 1 | Clear operation |  |

## 4-25. Audio Output Level Meter

It is possible to output the peak level of the PCM data inputted into a PWM processor.
A peak value can be read using an $I^{2} C$ command interface as 16 bit data of an absolute value.
The interval holding a peak value can be selected from 6 steps ( 50 ms step) from 50 ms to 300 ms .
A peak hold result can be selected from $L$ channel, $R$ channel, and a monophonic channel $\{(L c h+R c h) / 2\}$.

Audio Output Level Meter block diagram


Setting of the peak level hold time interval of Audio Output Level Meter
Default $=00 \mathrm{~h}$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| \&hB8[2:0] | Command | Hold time |
|  | 0 | 50 ms |
|  | 1 | 100 ms |
|  | 2 | 150 ms |
|  | 3 | 200 ms |
|  | 4 | 250 ms |
|  | 5 | 300 ms |

The signal of Audio Level Meter read-back is selected.
A value will be taken into a read-only register if a setting value is written in.
In order to update this register value, it is necessary to write in a setting value again.
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hB9 [ 2:0 ] | 0 | The peak level of Main-output L channel |
|  | 1 | The peak level of Main-output R channel |
|  | 2 | The peak level of Main-output monophonic channel $\{($ Lch + Rch $) / 2\}$ |
|  | 3 | The peak level of Sub-output L channel |
|  | 4 | The peak level of Sub-output R channel |
|  | 5 | The peak level of Sub-output monophonic channel $\{($ Lch + Rch $) / 2\}$ |

## Read-back of Audio Output Level

\&hBA (upper 8 bits) and a \&hBB (lower 8 bits) commands are read for the maximum within the period appointed by the command \&hB8 using an I2C interface.

## (Example)

When FFFFh is read, mean 1.0 ( 0 dBFs ).
When 8000 h is read, mean 0.5 (-6dBFs).

## 4-26. Audio Signal Selector Setting

It selects the audio signal of the SUB output, the MONI1 output, the MONI2 output inside the DSP.
Output select of SDATA1 and SDATA2
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| $\& 2$ h2 [6] | 0 | MONI1/MONI2 |
|  | 1 | Main/Sub (output of 128/ch Delay RAM) |

Sub-output select
The selector which is between the DSP part and $x 8$ over sampling filter parts Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| $\& \mathrm{~h} 2 \mathrm{~A}[5: 4]$ | 0 | DSP Sub output |
|  | 1 | DSP Main output |
|  | 2 | DSP MONI1 output |
|  | 3 | DSP MONI2 output |

Input select for Sub calculation of audio DSP part
Default $=5$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h2A [2:0] | 0 | Input2-HPF |
|  | 1 | Input1-HPF |
|  | 2 | P $^{2}$ Volume |
|  | 3 | Surround |
|  | 4 | 8 Band-BQ |
|  | 5 | FIR Filter |

The DSP part MONI1 channel selection Default = 1

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&h2B [6:4] | 0 | Input2-HPF |
|  | 1 | Input1-HPF |
|  | 2 | P $^{2}$ Volume |
|  | 3 | Surround |
|  | 4 | 8 Band-BQ |
|  | 5 | FIR Filter |
|  | 6 | Channel Mixer 3 |

The DSP part MONI2 channel selection Default = 1

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h2B [2:0] | 0 | Input2-HPF |
|  | 1 | Input1-HPF |
|  | 2 | P $^{2}$ Volume |
|  | 3 | Surround |
|  | 4 | 8 Band-BQ |
|  | 5 | FIR Filter |
|  | 6 | Channel Mixer 3 |

DAIF output selection for IC evaluation
It outputs audio output from the DSP part for the monitor in the DAIF.
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h2C [ 1:0 ] | 0 | Main output (128/ch Delay RAM) |
|  | 1 | Sub output (128/ch Delay RAM) |
|  | 2 | MONI1 |
|  | 3 | MONI2 |

5. Setting and reading method of parametric equalizer

It explains a detailed sequence of the setting method and the reading method of the parametric equalizer separately for usage. Please read while referring to Chapter 4-4.

## 5-1 PEQ coefficient setting

The parametric equalizer consists of Bi-quad filter as follows. Each coeffiect of Bi-quad filter can be written directly. It is S2.21 format, and setting range is $-4 \leqq x<+4$.
Moreover, the coefficient address is shown in Table 1.


5-1-1 Writing sequence (It sets up in number order)

1. BANK1 to 4 is appointed. (\&hA1[5:4])
2. Address setting (\&hA3) (*1) Table 1 is referred to.
3. 24bit coefficient Upper[23:16]bit setting (\&hA4[7:0])
4. 24bit coefficient Middle[15:8]bit setting (\&hA5[7:0])
5. 24bit coefficient Lower [7:0]bit setting (\&hA6[7:0])
6. The writing of coefficients are performed.(\&hA7[1:0] = 2) (*2)
(*2) After a writing complete of coefficients is cleared automatically. It is not necessary to transmit h34[0] =L. Coefficient writing takes about $100 \mu \mathrm{sec} .100 \mu \mathrm{sec}$ should not change an address setup and several 24 -bit setup after coefficient write-in execution.
(ex) When 0x3DEDE7 is written in BANK1, Lch, 8band(1) b0
7. $\& \mathrm{hA} 1=0 * \mathrm{~h}$ (BANK1 is appointed.)
8. $\& \mathrm{hA} 3=00 \mathrm{~h}$ ( 8 band ( 1 l bO is appointed)
9. $\& h \mathrm{~A} 4=3 \mathrm{Dh}$ (Upper [23:16] is setting)
10. $\& \mathrm{hA} 5=\mathrm{EDh}$ (Middle [15:8] is setting)
11. \&hA6 $=\mathrm{E} 7 \mathrm{~h}$ (Lower $[7: 0]$ is setting)
12. $\& \mathrm{hA} 7=02 \mathrm{~h}$ (Coefficient transfer) $\left({ }^{*} 3\right.$ )
(*3) After a writing complete of coefficients is cleared automatically.
13. $100 \mu \mathrm{sec}$ or more $\mu \mathrm{sec}$ wait

The writing of other coefficients is performed.

5-1-2 Read-back sequence (It sets up in number order)

1. BANK1 to 4 is appointed. (\&hA1 [0])
2. Address setting (\&hA3) (*4) Table 1 is referred to.
3. Setting of a read-back register address (\&hD0)
4. Read-back of the 24bit coefficient Upper [23:16] bit (\&hA8 [7:0])
5. Read-back of the 24bit coefficient Middle [15:8] bit (\&hA9 [7:0])
6. Read-back of the 24bit coefficient Lower [7:0] bit (\&hAA [7:0])

Table1. Specified coefficient

| \&hA3 | Specified coefficient | \&hA3 | Specified coefficient | \&hA3 | Specified coefficient | \&hA3 | Specified coefficient |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 00 | 8BandBQ1 b0 | 23 | 8BandBQ8 b0 | 46 | SubXOV2 b0 | 69 | DRC_APF b0 |
| 01 | 8BandBQ1 b1 | 24 | 8BandBQ8 b1 | 47 | SubXOV2 b1 | 6A | DRC_APF b1 |
| 02 | 8BandBQ1 b2 | 25 | 8BandBQ8 b2 | 48 | SubXOV2 b2 | 6B | DRC_APF b2 |
| 03 | 8BandBQ1 a1 | 26 | 8BandBQ8 1 | 49 | SubXOV2 a1 | 6C | DRC_APF a1 |
| 04 | 8BandBQ1 a2 | 27 | 8BandBQ8 ${ }^{\text {a }}$ | 4A | SubXOV2 a2 | 6D | DRC_APF a2 |
| 05 | 8BandBQ2 b0 | 28 | 1BandBQ b0 | 4B | SubXOV3 b0 | 6E | SRND_BQ1 b0 |
| 06 | 8BandBQ2 b1 | 29 | 1BandBQ b1 | 4C | SubXOV3 b1 | 6 F | SRND_BQ1 b1 |
| 07 | 8BandBQ2 b2 | 2 A | 1BandBQ b2 | 4D | SubXOV3 b2 | 70 | SRND_BQ1 b2 |
| 08 | 8BandBQ2 a1 | 2B | 1BandBQ a1 | 4E | SubXOV3 a1 | 71 | SRND_BQ1 1 |
| 09 | 8BandBQ2 a2 | 2C | 1BandBQ a2 | 4F | SubXOV3 a2 | 72 | SRND_BQ1 a2 |
| OA | 8BandBQ3 b0 | 2D | MainXOV1 b0 | 50 | SubXOV4 b0 | 73 | SRND_BQ2 b0 |
| OB | 8BandBQ3 b1 | 2E | MainXOV1 b1 | 51 | SubXOV4 b1 | 74 | SRND_BQ2 b1 |
| OC | 8BandBQ3 b2 | 2F | MainXOV1 b2 | 52 | SubXOV4 b2 | 75 | SRND_BQ2 b2 |
| OD | 8BandBQ3 a1 | 30 | MainXOV1 a1 | 53 | SubXOV4 a1 | 76 | SRND_BQ2 a1 |
| 0E | 8BandBQ3 a2 | 31 | MainXOV1 a2 | 54 | SubXOV4 a2 | 77 | SRND_BQ2 a2 |
| OF | 8BandBQ4 b0 | 32 | MainXOV2 b0 | 55 | Smooth BQ b0 |  |  |
| 10 | 8BandBQ4 b1 | 33 | MainXOV2 b1 | 56 | Smooth BQ b1 |  |  |
| 11 | 8BandBQ4 b2 | 34 | MainXOV2 b2 | 57 | Smooth BQ b2 |  |  |
| 12 | 8BandBQ4 a1 | 35 | MainXOV2 a1 | 58 | Smooth BQ a1 |  |  |
| 13 | 8BandBQ4 a2 | 36 | MainXOV2 a2 | 59 | Smooth BQ a2 |  |  |
| 14 | 8BandBQ5 b0 | 37 | MainXOV3 b0 | 5A | P2V_HPF b0 |  |  |
| 15 | 8BandBQ5 b1 | 38 | MainXOV3 b1 | 5B | P2V_HPF b1 |  |  |
| 16 | 8BandBQ5 b2 | 39 | MainXOV3 b2 | 5C | P2V_HPF b2 |  |  |
| 17 | 8BandBQ5 a1 | 3A | MainXOV3 a1 | 5D | P2V_HPF a1 |  |  |
| 18 | 8BandBQ5 a2 | 3B | MainXOV3 a2 | 5E | P2V_HPF a2 |  |  |
| 19 | 8BandBQ6 b0 | 3C | MainXOV4 b0 | 5F | P2V_APF b0 |  |  |
| 1A | 8BandBQ6 b1 | 3D | MainXOV4 b1 | 60 | P2V_APF b1 |  |  |
| 1B | 8BandBQ6 b2 | 3E | MainXOV4 b2 | 61 | P2V_APF b2 |  |  |
| 1 C | 8BandBQ6 a1 | 3F | MainXOV4 a1 | 62 | P2V_APF a1 |  |  |
| 1D | 8BandBQ6 a2 | 40 | MainXOV4 a2 | 63 | P2V_APF a2 |  |  |
| 1E | 8BandBQ7 b0 | 41 | SubXOV1 b0 | 64 | DRC_HPF b0 |  |  |
| 1F | 8BandBQ7 b1 | 42 | SubXOV1 b1 | 65 | DRC_HPF b1 |  |  |
| 20 | 8BandBQ7 b2 | 43 | SubXOV1 b2 | 66 | DRC_HPF b2 |  |  |
| 21 | 8BandBQ7 a1 | 44 | SubXOV1 a1 | 67 | DRC_HPF a1 |  |  |
| 22 | 8BandBQ7 a2 | 45 | SubXOV1 a2 | 68 | DRC_HPF a2 |  |  |

## 6. P-S conversion

Two parallel serial conversion circuits are built in BM5449.
P-S conversion 1 convert the Main output of DSP from SDATAO1, LRCKO, and BCKO into three line serial data and output the data. P-S conversion 2 convert the sub output of DSP from SDATAO1, LRCKO, and BCKO into three line serial data and output the data. Output audio data can be selected by \&h2A and \&h2B command.
Sampling frequency of output audio data is same as synchronous SRC. $<32 \mathrm{kHz} / 44.1 \mathrm{kHz} / 48 \mathrm{kHz}>$
Transfer clock form is fixed 64fs.
Output format has the IIS mode, left-align mode, and right-align mode. 16 each bit, 20bit, and 24bit output can also be selected. The figure below shows the timing chart of each transmission mode.

Bit clock frequency : 64fs


Left-Justified 64fs Format


Right-Justified 64fs Format

$6-1$. Format setting of three line serial output
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h05 [3:2] | 0 | IIS mode |
|  | 1 | left-align mode |
|  | 2 | right-align mode |

6-2. Setting data bit width of three line serial output
Default $=2$

| Select Address | Value |  |
| :---: | :---: | :--- |
| \&h05 [1:0] | 0 | 16 bits |
|  | 1 | 20 bits |
|  | 2 | 24 bits |

6-3. About the I/O timing of the cereal audio data
LRCKO and the BCLKO signal output from BM5449MWV generate the internal clock from the BCLK signal.
The clock is divided frequency and output. Therefore, the LRCKO signal output becomes an output of the LRCK input signal and the asynchronous system.


It is output delaying 645 clocks or 646 clocks when the delay of LRCKO is expressed with internal clock ( 1024 xfs ).
7. The mute function by a terminal

BM5449MWV has a mute function of audio DSP by a terminal.
It is possible to perform mute of the output from Audio DSP by setting a MUTEX terminal to "L."

Transition time setting at the time of mute is as follows.
Smooth transition mute time setting
The transition time when changing to a mute state is selected.
The soft transition time at the time of mute release is 10.7 ms fixed.
Default = 0

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| $\& \mathrm{~h} 20[1: 0]$ | 0 | 85.4 ms |
|  | 1 | 42.7 ms |
|  | 2 | 21.4 ms |
|  | 3 | 10.7 ms |

\&h20[1:0] Mute time setting
It is only operated by mute terminal.


Smooth transition mute release time setting
Time after detecting mute release until it actually begins mute release operation is set up.
Default = 0

| Select Address | Value |  |
| :---: | :---: | :--- |
| $\& \mathrm{~h} 20[3: 4]$ | 0 | 0 ms |
|  | 1 | 100 ms |
|  | 2 | 200 ms |
|  | 3 | 300 ms |

Operation of mute delay \&h20[3:2]

[Question]
When mute release is performed, what happens during mute operation?
Moreover, when there is release delay time, what happens?
[Answer]
When mute release is performed during mute operation, mute release operation is started in an instant.
(When delay setting is 0 ) Return time at this time becomes shorter than mute release time (for example, 10 ms ).
Next, when there is setting of release delay time, a delay timer starts a count from the time of performing mute release,
and mute release operation is started after delay time completing.
When mute release time setting is set to 10 ms , it is designing so that a mute release curve may draw f curve.

8. The notes at the time of reset

Since the state of IC is not stable at the time of the power supply ON, please perform IC reset action. [RSTX = "L"]
The input of the reset signal of BM5449MWV is performing noise removal using a clock signal.
Therefore, in order for IC reset to become valid, 10 times or more of clocks need to be inputted from a XI terminal in the state of RSTX=L.
9. The cautions at the time of starting

Please be sure to send the following command after the IC reset release containing the power supply ON.

9-1. When you do not use the clock stop automatic operation return function (Chapter 16-3)
0 . Power supply turn on
$\downarrow$
OPlease input a clock from XI terminal. When the clock is not inputted, reset does not start normally. $\downarrow$

1. Reset release (RSTX = H)

Please input serial digital audio data.(LRCLK, BCLK, SDATA) If the input of serial audio data is while it is so far from a power supply injection, it is never satisfactory.
$\downarrow$
2. Release power down mode(PDX = H)

OPlease wait for about 20 ms until PLL is stabilized
$\downarrow$
3. \&h0A [2:0] = 7h : Input clock disappearance flag is cleared.
$\downarrow$
4. \&hE9 [7:0] = 34h : The system clock inside IC is set up.
$\downarrow$
5. \&h03 [5:0] = *h : 3-line serial audio input format is set up. Refer to Chapter 3 for a setting value
$\downarrow$
6. $\& h 04[0]=1 \quad$ : Adjust the input data incorporation position.
$\downarrow$
OWait for about 1 ms until the adjustment of the incorporation position is completed.
$\downarrow$
7. \&h04 [1] = $1 \quad$ : Clear LRCK frame error flag.
$\downarrow$
8. \&h07 [0] = $1 \quad$ : Clear LRCK-synchronous error signal.
$\downarrow$
9. $\& \mathrm{~h} 01[7: 5]=0 \mathrm{~h} \quad:$ RAM clear OFF
$\downarrow$
10. \&hC8[7:0] $=05 \mathrm{~h}:$ Main PWM set up.
11. $\& h C 9[7: 0]=01 \mathrm{~h}:$ Main PWM set up.
12. \&hCA[7:0] = 0Fh $:$ Main PWM set up.
$\downarrow$
13. $\& h C B[7: 0]=0 B h \quad:$ Main PWM set up.
$\downarrow$
14. $\& h C C[7: 0]=06 h \quad:$ Sub PWM set up.
$\downarrow$
15. $\& h C D[7: 0]=01 \mathrm{~h}:$ Sub PWM set up.
$\downarrow$
16. \&hCE[7:0] = 0Fh : Sub PWM set up.
$\downarrow$
17. \&hCF[7:0] = 09h : Sub PWM set up.
$\downarrow$
18. Set other register
Ex) \&h10 [1:0] = Oh
: Set master fine volume for main output
\&h11 [7:0] = 30h $\quad:$ Release mute of master volume for main output (In case of 030h = 0dB)
$\downarrow$
19. Release mute terminal (MUTEX ="H")

9-2. When you use the clock stop automatic operation return function (Chapter 16-3)
0 . Power supply turn on
$\downarrow$
OPlease input a clock from XI terminal. When the clock is not inputted, reset does not start normally. $\downarrow$

1. Reset release ( $\mathrm{RSTX}=\mathrm{H}$ )

Please input serial digital audio data. (LRCLK, BCLK, SDATA) If the input of serial audio data is while it is so far from a power supply injection, it is never satisfactory.
$\downarrow$
2. Release power down mode (PDX = H)

OPlease wait for about 20 ms until PLL is stabilized.
$\downarrow$
3. \&hE9 [7:0] = 34h : The system clock inside IC is set up.
$\downarrow$
4. \&h03 [5:0] = *h : 3-line serial audio input format is set up. Refer to Chapter 3 for a setting value.
$\downarrow$
5. \&h01 [7:0] = 00h : RAM clear OFF
$\downarrow$
6. $\& h C 8[7: 0]=05 h \quad:$ Main PWM set up.
$\downarrow$
7. \&hC9[7:0] = 01h : Main PWM set up.
$\downarrow$
8. \&hCA[7:0] $=0$ Fh : Main PWM set up.
$\downarrow$
9. \&hCB[7:0] $=0 B h \quad:$ Main PWM set up.

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10. $\& h C C[7: 0]=06 h \quad:$ Sub PWM set up.
$\downarrow$
11. $\& h C D[7: 0]=01 \mathrm{~h}:$ Sub PWM set up.
$\downarrow$
12. $\& h C E[7: 0]=0 F h \quad:$ Sub PWM set up.
$\downarrow$
13. \&hCF[7:0] = 09h : Sub PWM set up.
$\downarrow$
14. Set other register

Ex) \&h10 [1:0] = Oh: Set master fine volume for main output
\&h11 [7:0] = 30h: Release mute of master volume for main output (In case of 030h = 0dB)
$\downarrow$
15. Release mute terminal (MUTEX $=$ " ${ }^{\prime \prime}$ ")

## 10. Power Down Mode

There is a down of power mode in this IC. PLL and the internal clock stop when changing to this mode, and power consumption can be lowered. A set value of the register and the data of RAM are maintained even if it sets it to this mode. Please execute the following procedure to set it to this mode.

10-1. When you do not use the clock stop automatic operation return function (Chapter 16-3)

10-1-1. Shift to power down mode

1. Mute with terminal (MUTEX $=$ " ${ }^{\prime \prime}$ ")

OX ms or more is waited for until MUTE hangs completely. $X=$ (Mute transition duration setting) +50 ms $\downarrow$
2. \&h01 [4] = $1 \quad$ : The PWM output is made "L" fixed output.
$\downarrow$
3. \&hE1 [7] = $1 \quad$ : The output of the serial digital audio data is stopped.
$\downarrow$
4. \&hE9 $[7: 0]=35 \mathrm{~h} \quad:$ The clock supply by PLL is stopped. $\downarrow$
5. Power down with terminal (PDX = " L ")
$\downarrow$
6. Serial digital audio data input is stopped.

10-1-2.Return from power down mode

1. Please input the serial digital audio data.
$\downarrow$
2. Power down release with terminal (PDX =" H ")
$\downarrow$
3. \&h0A [2:0] = 7h : The input clock disappearance flag is cleared.

OPlease wait for about 20 ms (Min.) until PLL is stabilized.
$\downarrow$
4. \&hE9 [7:0] $=34 \mathrm{~h} \quad:$ The clock supply by PLL is started.
$\downarrow$
5. \&hE1 [7] = $0 \quad:$ The serial digital audio data output starts.
$\downarrow$
6. \&h01 [7:5] = 7h : RAM clear is executed.

Olt makes to $\& \mathrm{~h} 01[4]=0$, and PWM is put into the state of normal output at the same time. $\downarrow$
7. \&h03[5:0] $=$ *h :3-line serial audio input format is set up. Refer to Chapter 3 for a setting value. $\downarrow$
8. $\& \mathrm{~h} 04[0]=1 \quad$ :Adjust the input data incorporation position.

Olt is about 1 ms wait until the adjustment of the incorporation position is completed.
$\downarrow$
9. $\& h 04[1]=1 \quad$ :Clear LRCK frame error flag.
$\downarrow$
10. $\& \mathrm{~h} 07[0]=1 \quad$ :Clear LRCK-synchronous error signal.
$\downarrow$
11. \& $\mathrm{h} 01[7: 0]=00 \mathrm{~h} \quad:$ RAM clear OFF
$\downarrow$
12. Release mute terminal (MUTEX $=$ " ${ }^{\prime \prime}$ ")

10-2. When you use the clock stop automatic operation return function (Chapter 16-3)
10-2-1.Shift to power down mode

1. Mute with terminal (MUTEX ="L")

OX ms or more is waited for until MUTE hangs completely.
$X=$ (Mute transition duration setting) +50 ms
$\downarrow$
2. \&h01 [4] = $1 \quad$ : The PWM output is made "L" fixed output.
$\downarrow$
3. $\& \mathrm{hE} 1[7]=1 \quad:$ The output of the serial digital audio data is stopped.
$\downarrow$
4. \&hE9 $[7: 0]=35 \mathrm{~h} \quad$ : The clock supply by PLL is stopped.
$\downarrow$
5. Power down with terminal (PDX = " L ")
$\downarrow$
6. Serial digital audio data input is stopped.

## 10-2-2. Return from power down mode

1. Please input the serial digital audio data.
$\downarrow$
2. Power down release with terminal (PDX ="H")

OPlease wait for about 20 ms (Min.) until PLL is stabilized.
$\downarrow$
3. \&hE9 $[7: 0]=34 \mathrm{~h} \quad$ : The clock supply by PLL is started.
$\downarrow$
4. \&hE1 [7] $=0 \quad:$ The serial digital audio data output starts.
$\downarrow$
5. \&h01 [7:5] = 7h : RAM clear is executed.

Olt makes to $\& h 01[4]=0$, and PWM is put into the state of normal output at the same time.
$\downarrow$
6. \&h03[5:0] $=$ *h : 3-line serial audio input format is set up. Refer to Chapter 3 for a setting value.
$\downarrow$
7. \& $\mathrm{h} 01[7: 0]=00 \mathrm{~h} \quad:$ RAM clear OFF
$\downarrow$
8. Release mute terminal (MUTEX =" H ")

## 11. Sampling Rate and Clock Change

Please transmit the following command when you change of the serial audio data format, the sampling rate and the clock.
Please execute this procedure when you do not use the clock stop automatic operation return function (Chapter 16-3).

1. Mute with terminal (MUTEX ="L")
$\downarrow$
Please change serial digital audio data.(LRCLK, BCLK, SDATA)
$\downarrow$
2. $\& \mathrm{~h} 0 \mathrm{~A}[2: 0]=7 \mathrm{~h} \quad:$ The input clock disappearance flag is cleared.
$\downarrow$
OPlease wait for about 20 ms (Min.) until PLL is stabilized.
$\downarrow$
3. \&hE9 [7:0] $=34 \mathrm{~h} \quad:$ The system clock in IC is set.
$\downarrow$
4. \&h01 [7:0] = F0h : Execute RAM clear
$\downarrow$
5. \&h03[5:0] $=$ *h $\quad$ 3-line serial audio input format is set up. Refer to Chapter 3 for a setting value.
$\downarrow$
6. $\& h 04[0]=1 \quad$ : Adjust the input data incorporation position.
$\downarrow$
Olt is about 1 ms wait until the adjustment of the incorporation position is completed.
$\downarrow$
7. \&h04 [1] = $1 \quad$ : Clear LRCK frame error flag.
$\downarrow$
8. \&h07 [1] = $1 \quad$ : Clear LRCK-synchronous error signal.
$\downarrow$
9. \&h01 [7:0] = 00h : RAM clear OFF
$\downarrow$
10. Set other register
$\downarrow$
11. Release mute terminal (MUTEX $=$ " ${ }^{\prime \prime}$ )
12. Setting of sampling rate and PLL

12-1. Sampling frequency setting
This IC does the settings such as sampling rates and PLL by the automatic operation in using X 'tal (12.288MHz). In this case, please set only the bit clock frequency of audio serial input data. Please follow the following tables about the setting.

- Table for sampling rate

| Input sampling frequency [kHz] | Bit clock frequency (\&h03[5:4]) |  |  |
| :---: | :---: | :---: | :---: |
|  | 32fs | 48fs | 64fs |
| 8.000 | - | - | $\bigcirc$ |
| 11.025 | - | - | $\bigcirc$ |
| 12.000 | - | - | $\bigcirc$ |
| 16.000 | $\bigcirc$ | - | $\bigcirc$ |
| 22.050 | $\bigcirc$ | - | $\bigcirc$ |
| 24.000 | $\bigcirc$ | - | $\bigcirc$ |
| 32.000 | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| 44.100 | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| 48.000 | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| 88.200 | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| 96.000 | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| 176.400 | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |
| 192.000 | $\bigcirc$ | $\bigcirc$ | $\bigcirc$ |

Moreover, it is also possible to change the setting of the sampling frequency with the manual.

Input sampling frequency change setting
Default = 1

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hOB [5] | 0 | Manually setting |
|  | 1 | Automatically setting (Initial) |

SRC output setting
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hOB [4 ] | 0 | 48 kHz (Setting, except for Fs $=8 \mathrm{k}, 16 \mathrm{k}$, and 32 kHz ) |
|  | 1 | 32 kHz (Setting in case of Fs=8k, 16 k , and 32 kHz ) |

Input sampling rate setting
Default = 8h

| Select Address | Explanation of operation |  |  |
| :---: | :--- | :--- | :--- |
| \&hOB [ 3:0] | $0: 8 \mathrm{kHz}$ | $4: 22.05 \mathrm{kHz}$ | $9: 88.2 \mathrm{kHz}$ |
|  | $1: 11.025 \mathrm{kHz}$ | $5: 24 \mathrm{kHz}$ | $\mathrm{A}: 96 \mathrm{kHz}$ |
|  | $2: 12 \mathrm{kHz}$ | $6: 32 \mathrm{kHz}$ | $\mathrm{B}: 176.4 \mathrm{kHz}$ |
|  | $3: 16 \mathrm{kHz}$ | $7: 44.1 \mathrm{kHz}$ | $\mathrm{C}: 192 \mathrm{kHz}$ |
|  | $8: 48 \mathrm{kHz}$ (Initial) | Other : Inhibit |  |

Automatic change setting of clock of BCLK dividing frequency
Default = 1

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h0D [ 1] | 0 | Manually setting |
|  | 1 | Automatically setting |

BCLK dividing setting
Default = 0

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| \&h0D [0] | 0 | 192 (Initial) |  |
|  | 1 | 128 |  |

*The following refer to details.

## 【Reference】

- Ratio of dividing frequency selection to PLLA when ratio of BCLK dividing frequency setting is made manual operation

| Input sampling <br> frequency | 8 kHz | 11.025 kHz <br> $/ 12 \mathrm{kHz}$ | 16 kHz | 22.05 kHz <br> $/ 24 \mathrm{kHz}$ | 32 kHz | 44.1 kHz <br> $/ 48 \mathrm{kHz}$ | 88.2 kHz <br> $/ 96 \mathrm{kHz}$ | 176.4 kHz <br> $/ 192 \mathrm{kHz}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| \&hOD[0] | 0 h | h <br> $(128)$ | 0 h <br> Initial: 0 h | $(192)$ | 1 h | 0 h | 1 h | 1 h |
| $(128)$ | $(192)$ | $(128)$ | $(128)$ | $(128)$ |  |  |  |  |

When \&h0D [1] is made "0" (manual setting), it becomes effective. Initial value of \&hOD [1] is "1" (automatic setting)

12-2. PLL setting when PWM sampling frequency is changed
To avoid the interference with the AM Radio Frequency belt, BM5449MWV can change the PWM sampling frequency (PWM hopping function). To change the PWM sampling frequency, \&h30, \&hE9, and \&hEC register are set. The relation of the PWM career frequency to the setting of this register is as follows.

Relation of PWM sampling frequency to input sampling frequency

| Input sampling frequency [kHz] | \& $\mathrm{h} 30[3: 2]$ | \& hE 9 | \&hEC | PWM career frequency [kHz] |
| :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} 8,12,16,24,32 \\ 48,96,192 \end{gathered}$ | Oh | 34h | XXh | 384 |
|  | 2h | 70h | 00h | 288 |
|  | 1h |  | 10h | 336 |
| $\begin{gathered} 11.025,22.05,44.1 \\ 88.2,176.4 \end{gathered}$ | Oh | 34h | XXh | 352.8 |
|  | 2h | 70h | 00h | 264.6 |
|  | 1h |  | 10h | 308.7 |

*XXh means "Don't care"

PWM hopping setting
Default = 0

| Select Address | Value |  |
| :---: | :---: | :--- |
| $\& h 30[3: 2]$ | 0 | $8 f s$ |
|  | 1 | 7 fs |
|  | 2 | 6 fs |

PLL7 clock setting when PWM hopping function is used.
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hE9 [ 6 ] | 0 | Use X'tal clock (When PWM hopping function is not used) |
|  | 1 | Use PLL7 clock (When PWM hopping function is used) |

PLL7 operation setting 1 when PWM hopping function is used.

Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hEC [4] | 0 | 6 times multiply clocks (When you choose 6fs by the PWM hopping <br> setting) |
|  | 1 | 7 times multiply clocks (When you choose 7fs by the PWM hopping <br> setting) |

PLL7 operation setting 2 when PWM hopping function is used.
Default $=1$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hEC $[0]$ | 0 | PLL7 is activated. |
|  | 1 | PLL7 is deactivated. |

Please go according to the following procedure when you change the PWM sampling frequency

1. Mute with terminal (MUTEX = "L")

OX msec or more is waited for until MUTE hangs completely.
$X=$ (Mute transition duration setting) +50 msec
$\downarrow$
2. $\& h E C[0]=0 \mathrm{~h} \quad: \mathrm{PLL} 7$ is activated (Normaly, it is deactivated )
3. \&hEC[4] = *h : Setting of PLL7 multiplier ("0" : 6 times multiply, "1" : 7 times multiply).
$\downarrow$
4. \&h30 [3:2] = *h : Setting for PWM hopping ("0" : 8 times multiply, " 1 " : 7 times multiply, " 2 " : 6 times multiply)
$\downarrow$
5. $\& \mathrm{hE}[7: 0]=70 \mathrm{~h} \quad:$ The system clock inside IC is set up.
$\downarrow$
OPlease wait for about 20 ms until PLL7 is stabilized.
$\downarrow$
6. Release mute terminal (MUTEX = " H ")

## 13. Small signal input detection function

There is a function which detects the audio data input of a non-signal or a small signal. This function is used in order to reduce the standby power consumption of an audio set. Setting of a detection level and detection time can be performed.

If the signal below a setting detection level continues in both $L$ channel and $R$ channel, a small signal detection flag will become " H ". A detection result can be read from command \&hB3 [2:0]. The point which acts as a monitor of the small signal becomes input data of audio DSP block.

## Block diagram



Mask setting for INPUT1 and INPUT2
Default = 0

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| INPUT1 \&hB0 [7] | 0 | Not mask input signal |
| INPUT2 \&hB0 [6] | 1 | Mask input signal |

Detection level setting
Default $=00 \mathrm{~h}$

| Select Address | Explanation of operation |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| \& hB0 [4:0] | Command | Level | Command | Level | Command | Level |
|  | 00 | $-\infty$ | 08 | -77dB | 10 | -69dB |
|  | 01 | -96dB | 09 | -76dB | 11 | -68dB |
|  | 02 | -92dB | OA | -75dB | 12 | -67dB |
|  | 03 | -88dB | ов | -74dB | 13 | $-66 \mathrm{~dB}$ |
|  | 04 | -84dB | oc | -73dB | 14 | -65dB |
|  | 05 | -80dB | OD | -72dB | 15 | -64dB |
|  | 06 | -79dB | OE | -71dB | 16 | -62dB |
|  | 07 | -78dB | OF | -70dB | 17 | -60dB |

Detection time setting
Default = 0

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h2 [5:4] | 0 | 42.7 ms |
|  | 1 | 85.3 ms |
|  | 2 | 170.7 ms |
|  | 3 | 341.3 ms |

* Sampling frequency is value of $F s=48 \mathrm{kHz}$. In the case of $F s=44.1 \mathrm{kHz}$, it will be about 1.09 times the setting value.

Detection flag read-back (Read Only)

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| hB3 [0] | 0 | Un-detecting. |  |
|  | 1 | Detecting |  |

## 14. Monaural / Stereo detection

This block judges whether the input signal is monaural or stereo, and outputs the flag.
When the peak value of the difference between Lch and Rch of the input signal is detected, and the signal below the set value is consecutive, it is judged monaural. Afterwards, the flag of the register reading outputs H .
However, judge monaural for a no input signal and the signal taken with an AD convertor together with the small signal detecting function in Chapter 11. (It is judged monaural and the flag outputs H to the no sound part between tunes. Have the same meaning as the no sound part of the stereo signal because the small signal detection flag also outputs H in this case.)
The detection result can be read from command \&hB3 [2:1]. The place that monitors signals becomes an entrance in the DSP block.


Explanation of monaural/stereo detection block


Detection time setting
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| $\& \mathrm{hB2}[1: 0]$ | 0 | 42.7 ms |
|  | 1 | 85.3 ms |
|  | 2 | 170.7 ms |
|  | 3 | 341.3 ms |

*It is a value at sampling frequency $F s=48 \mathrm{kHz}$ time. In case of $F s=44.1 \mathrm{kHz}$, increases to about 1.09 times that of the set value.

LR difference detection level setting
Default $=0 \mathrm{~h}$

| Select Address | Explanation of operation |  |
| :---: | :---: | :---: |
| \&hB1 [ 2:0] | Command | Detection level |
|  | 0 | $-\infty \mathrm{dB}$ |
|  | 1 | Under -96dB |
|  | 2 | Under -90dB |
|  | 3 | Under -84dB |
|  | 4 | Under -78dB |
|  | 5 | Under -72dB |
|  | 6 | Under -66dB |
|  | 7 | Under -60dB |

Detection flag reading (Read Only)

| Select Address | Value |  | Explanation of operation |
| :---: | :---: | :--- | :--- |
| Input1 \&hB3 [2] | 0 | Not detect |  |
| Input2 $\&$ hB3 [ 1] | 1 | Detect |  |

## 15. Channel delay memory

In the main output and the sub output, there are delay memories for the phase correction for 128 samples or less.

Delay mode setting
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| $\& \mathrm{~h} 30[1: 0]$ | 0 | All of 4ch is possible the delay. |
|  | 1 | Only Main Lch and Main Rch are possible the delay. |
|  | 2 | Only Sub Lch and Sub Rch are possible the delay. |

Method of setting delay memory

- Delay Value = Od\{Command Value\} / Fs [s]

Ex)
Sampling frequency Fs $=48 \mathrm{kHz}$
Setting value $=33 \mathrm{~h} \rightarrow$ Converts 33h into the decimal number 0d51.
Delay value $=51 / 48000$

$$
=1.0625 \mathrm{~ms}
$$

It corresponds to the delay of about 37 cm when assuming speed of sound $346 \mathrm{~m} / \mathrm{s}$.

Lch delay setting command for Main output: \&h31 [6:0]
Rch delay setting command for Main output: \&h32 [6:0]
Lch delay setting command for Sub output: \&h33 [6:0]
Rch delay setting command for Sub output: \&h34 [6:0]
16. Clock stop detection and synchronous blank detection

16-1 Clock stop detection
A necessary clock for the audio processing is generated by supplying two or more clocks in this IC, and using these clocks. The clock for the audio processing might stop, too, when the clock supplied from the outside stops and the detector to evade these is needed. The detected clock has detected the state with XI, BCLK, and LRCK with internal CVCO clock.


When the clock stops at the time set depending on the command, the stop detection condition of each clock is detected. As for the detection result, reading from the register is possible. As a result of the judgment as the stop once, it is not cleared until a clear command is transmitted even if the state of the clock returns normally.

XI, LRCK, BCLK stop detection time setting
Default = Oh

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| XI \&h08 [6:4] | 0 | About $100 \mu \mathrm{~s}$ |
| LRCK \&h08 [ 2:0 $]$ <br> BCLK \&h09 [6:4 ] | 1 | About $200 \mu \mathrm{~s}$ |
|  | 2 | About $300 \mu \mathrm{~s}$ |
|  | 3 | About $400 \mu \mathrm{~s}$ |
|  | 4 | About $500 \mu \mathrm{~s}$ |
|  | 5 | About $600 \mu \mathrm{~s}$ |
|  | 6 | About $700 \mu \mathrm{~s}$ |
|  | 7 | About $800 \mu \mathrm{~s}$ |

*The above-mentioned detection time reaches the value when the clock stop decision circuit operates by 27.125 MHz .
Clock stop flag reading register (Read Only)

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hOA [ 6 ] | 0 | Normal |
|  | 1 | XI clock stop detect |
| \&hOA [ 5 ] | 0 | Normal |
|  | 1 | LRCK clock stop detect |
| \&hOA [ 4 ] | 0 | Normal |
|  | 1 | BCLK clock stop detect |

Clock stop flag clear (Write Only)

| Select Address | Explanation of operation |
| :---: | :--- |
| \&hOA [ 2 ] | When "1" is written, the XI stop flag is cleared. |
| \&h0A [ 1 ] | When "1" is written, the LRCK stop flag is cleared. |
| \&h0A [ 0 ] | When "1" is written, the BCLK stop flag is cleared. |

*When the clock stop automatic return function (Chapter 16-3) is used, these flags are cleared by the automatic operation.

## 16-2 Synchronous blank detection

As for synchronous blank detecting function, it detects as synchronous blank error when it counts between the rising edges of LRCK with internal clock ( 49.152 MHz ), and it shifts more than the definite value, and whether PLL is normally locked is judged.

| Input sampling frequency | 8 kHz | 12 kHz | 16 kHz | 24 kHz | 32 kHz | 48 kHz | 96 kHz | 192 kHz |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Count value <br> (Start of counting from 0) | 6143 | 4095 | 3071 | 2047 | 1535 | 1023 | 511 | 255 |

As for the detection result, reading from the register is possible. As a result of the judgment as synchronous blank once, it is not cleared until a clear command is transmitted even if the state of the clock returns normally. Moreover, the setting of the detection approval frequency is also possible, and if the error more than the predetermined number is detected, the flag (\&h07 [1]) becomes "1" by the command.

Synchronous blank flag reading register (Read Only)

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&h07 [ 1] | 0 | Normal |
|  | 1 | Synchronous blank detect |

Synchronous blank flag clear register (Write Only)

| Select Address | Explanation of operation |
| :---: | :--- |
| \&h07 [ 0 ] | When "1" is written, the synchronous blank flag is cleared. |

*When the clock stop automatic return function (Chapter 16-3) is used, these flags are cleared by the automatic operation.

Synchronous blank count setting
Default $=1 \mathrm{~h}$

| Select Address | Explanation of operation |
| :---: | :--- |
| $\& h 07[6: 4]$ | 1 or more is set. (It should be set from 1 to 7 ) <br> If synchronous blank more than the set number of count is detected, \& h07 [1] <br> becomes "1". |

## 16-3 Clock stop automatic return function

When the clock stop, the synchronous blank, and the frame error are detected, DSP stops the PWM output. Moreover, the serial audio output outputs the no signal data to SDATAO and does the free run. When the clock returns, the function to restart the DSP processing by the automatic operation is built into. The automatic return function is effective to initial value. Each error flag (\&h0A [5:4], \&h07 [1], and \&h04 [2]) returns to 0 when returning automatically. Moreover, the register to confirm whether the error occurred separately is prepared, and the state of the error can be monitored in that.

Clock stop automatic return function selection register
Default $=2 \mathrm{~h}$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hOE [ 1 ] | 0 | It decides it with \&hA1 [3:2]. (manual change) |
|  | 1 | It changes automatically by input fs. |
| \&hOE [0] | 0 | Automatic return function ON |
|  | 1 | Automatic return function OFF |

Clock stop, frame, and synchronous error detection monitor register
Default = Oh

| Select Address | Value | Explanation of operation |
| :---: | :---: | :---: |
| \&h0F [ 7 ] | 0 | Normal. When 0 is written, the flag of this bit is cleared. |
|  | 1 | Flame error flag detection monitor. |
| \&h0F [ 6] | 0 | Normal. When 0 is written, the flag of this bit is cleared. |
|  | 1 | Synchronous error flag detection monitor. |
| \&h0F [5] | 0 | Normal. When 0 is written, the flag of this bit is cleared. |
|  | 1 | XI clock stop flag detection monitor. |
| \& hOF [ 4 ] | 0 | Normal. When 0 is written, the flag of this bit is cleared. |
|  | 1 | LRCK clock stop flag detection monitor. |
| \& hOF [ 3 ] | 0 | Normal. When 0 is written, the flag of this bit is cleared. |
|  | 1 | BCLK clock stop flag detection monitor. |
| \& hOF [ 2:0] | - | Monitor for IC test, Read Only |

When the automatic return function is made effective, the limitation is generated in the usage of coefficient RAM used with the parametric equalizer and coefficient RAM and used with the FIR filter.

The coefficient for the parametric equalizer stores the coefficient for 48 kHz in BANK1, and stores the coefficient for 44.1 kHz in BANK2. BANK3 and BANK4 cannot be used (It is disregarded even if it sets it).

The method of the setting to each BANK according to the operation mode changes into the coefficient for the FIR filter. Store the coefficient for 48 kHz in BANK1 when using it by MODE I and III, and store the coefficient for 44.1 kHz in BANK2. Store the coefficient for 48 kHz in BANK1 when using it with MODE II, and store the coefficient for 44.1 kHz in BANK2. BANK3 and BANK4 cannot be used (It is disregarded even if it sets it).

About the restriction matter of the automatic return function from the clock error

Arrangement specification of coefficient RAM for parametric equalizer.


Arrangement specification of coefficient RAM for FIR filter

(2) When using it on MODE II


## 17. Software reset function

In this IC, the software reset by the command setting can be done. Execute the software reset after effectively setting the software reset. \&hFB 0 shows " 1 " while executing the software reset. When the reset processing is completed, it is cleared automatically.

Software reset effective setting
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hFA [7] | 0 | Software reset is invalid. |
|  | 1 | Software reset is valid. |

Software reset execution setting
Default $=0$

| Select Address | Value | Explanation of operation |
| :---: | :---: | :--- |
| \&hFB [0] | 0 | Release software reset. |
|  | 1 | Execute software reset. <br> (After the softreset is completed, it is cleared automatically.) |

*When the softreset is executed, it is not executed if \&FA 7 is not set to " 1 ".

Application Example (Stereo BTL output, RL=8 )


Figure 33. Application Example (Stereo BTL output, RL=8 )

- Application Example (Monaural PBTL output, RL=4 )


Figure 34. Application Example (Monaural PBTL output, RL=4 $)$

- Application Example (2.2ch application, $\mathrm{RL}=8 \Omega$ )


Figure 35. Application Example (2.2ch application, $\mathrm{RL}=8 \Omega$ )

## Selection of Components Externally Connected

## (1)Output LC Filter Circuit

An output filter is required to eliminate radio-frequency components exceeding the audio-frequency region supplied to a load (speaker). Because this IC uses sampling clock frequencies from 256 kHz to 384 kHz in the output PWM signals, the high-frequency components must be appropriately removed.
This section takes an example of an LC type LPF shown in Figure 12., in which coil L and capacitor $C$ compose a differential filter with an attenuation property of $-12 \mathrm{~dB} /$ oct. A large part of switching currents flow to capacitor C , and only a small part of the currents flow to speaker $\mathrm{R}_{\mathrm{L}}$. This filter reduces unwanted emission this way. In addition, coil L and capacitor Cg compose a filter against in-phase components, reducing unwanted emission further.


Following presents output LC filter constants with typical load impedances.

| $R_{L}$ | L | Cg | $\mathrm{C}_{\text {BTL }}$ |
| :---: | :---: | :---: | :---: |
| $4 \Omega$ | $10 \mu \mathrm{H}$ | $0.15 \mu \mathrm{~F}$ | $0.68 \mu \mathrm{~F}$ |
| $6 \Omega$ | $15 \mu \mathrm{H}$ | $0.1 \mu \mathrm{~F}$ | $0.47 \mu \mathrm{~F}$ |
| $8 \Omega$ | $22 \mu \mathrm{H}$ | $0.068 \mu \mathrm{~F}$ | $0.33 \mu \mathrm{~F}$ |

Use coils with a low direct-current resistance and with a sufficient margin of allowable currents. A high direct-current resistance causes power losses. In addition, select a closed magnetic circuit type product in normal cases to prevent unwanted emission.
Use capacitors with a low equivalent series resistance, and good impedance characteristics at high frequency ranges ( 100 kHz or higher). Also, select an item with sufficient withstand voltage because flowing massive amount of high-frequency currents is expected.
(2)BOM list (Stereo BTL output, $R_{L}=8 \Omega$ )

| Parts | Parts No. | Value | Company | Product No. | Rated Voltage | Tolerance |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IC | U1 | - | ROHM | BM5449MWV | - | - |
| Inductor | L29, L34, L36, L42 | $22 \mu \mathrm{H}$ | TOKO | B1047AS-220M | - | ( $\pm 20 \%$ ) |
| Resistor | R9 | 1.5 k ohm | ROHM | MCR03EZPJ152 | 1/10W | $\mathrm{J}( \pm 5 \%)$ |
|  | R8 | 1M ohm |  | MCR03EZPJ105 | 1/10W | $\mathrm{J}( \pm 5 \%)$ |
|  | R11 | 1.5k ohm |  | MCR03EZPF1501 | 1/16W | $\mathrm{F}( \pm 1 \%)$ |
|  | R52, R53 | 100k ohm |  | MCR03EZPJ104 | 1/10W | $\mathrm{J}( \pm 5 \%)$ |
| Capacitor | C25, C45 | 10رF | MURATA | GRM31CB11H106KA75L | 50 V | $\mathrm{B}( \pm 10 \%)$ |
|  | C29B, C36B | $0.33 \mu \mathrm{~F}$ |  | GRM219B31H334KA87 | 50 V | $\mathrm{B}( \pm 10 \%)$ |
|  | $\begin{aligned} & \text { C29A, C34A, } \\ & \text { C36A, C42A } \end{aligned}$ | $0.068 \mu \mathrm{~F}$ |  | GRM21BB11H683KA01 | 50 V | $B( \pm 10 \%)$ |
|  | $\begin{gathered} \text { C12, C14, C22 } \\ \text { C23, C24 } \end{gathered}$ | $1 \mu \mathrm{~F}$ |  | GRM185B31C105KE43 | 16V | $B( \pm 10 \%)$ |
|  | C11B | $0.027 \mu \mathrm{~F}$ |  | GRM033B10J273KE01 | 6.3 V | $\mathrm{B}( \pm 10 \%)$ |
|  | C11A | 2700pF |  | GRM033B10J272KA01 | 6.3 V | $\mathrm{B}( \pm 10 \%)$ |
|  | C8, C9 | 10pF |  | GRM188B11E100KA01 | 25 V | $\mathrm{B}( \pm 10 \%)$ |
| Oscillation unit | X8 | 12.288MHz | NIHON DENPA KOGYO | NX5032GA | - | - |

The CERALOCK can be used instead of the X'tal. The constant is as follows.
However, the frequency accuracy worsens compared with the crystal oscillation. The gap might be caused in the sampling frequency detection result.

| Parts | Parts No. | Value | Company | Product No. | Rated <br> Voltage | Tolerance |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Resistor | R9 | 220 ohm | ROHM | MCR03EZPJ221 | $1 / 10 \mathrm{~W}$ | $\mathrm{~J}( \pm 5 \%)$ |
|  | R8 | 1 M ohm | ROHM | MCR03EZPJ105 | $1 / 10 \mathrm{~W}$ | $\mathrm{~J}( \pm 5 \%)$ |
| Capacitor | C8, C9 | 33 pF | ROHM | It is built into the oscillation <br> unit ( CSTCE12M2G55-R0) | - | - |
| Oscillation <br> unit | X8 | 12.288 MHz | MURATA | CSTCE12M2G55-R0 | - | - |


#### Abstract

As return of current regenerated by back EMF of output coil happens, take steps such as putting capacitor between power supply and GND as an electric pathway for the regenerated current. Be sure that there is no problem with each property such as emptied capacity at lower temperature regarding electrolytic capacitor to decide capacity value. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.


(3) The settlement of the snubber

When over/undershoot of the output PWM exceeds rating, it must insert the snubber circuit shown below.
(1) Measure the spike resonance frequency f 1 of the PWM output wave shape (When it stands up.) by using FET probe in the OUT terminal. (Figure 79) The FET probe is to monitor very near pin and shorten ground lead at the time of that.
(2) Measure resonance frequency f2 of the spike as a snubber circuit fixed number $\mathrm{R}=0 \Omega$ (Only with the condenser C, to connect GND) At this time, the value of the condenser C is adjusted until it becomes half of the frequency
(2f2=f1) of the resonance frequency f 1 of $(1$. The value of C which it could get here is three times of the parasitic capacity Cp that a spike is formed. ( $\mathrm{C}=3 \mathrm{Cp}$ )
(3) Parasitic inductance Lp is looked for at the next formula.

$$
\mathrm{L}_{\mathrm{p}}=\frac{1}{\left(2 \pi f_{1}\right)^{2} C_{p}}
$$

(4) The character impedance Z of resonance is looked for from the parasitic capacity Cp and the parasitism inductance Lp at the next formula.

$$
\mathrm{Z}=\sqrt{\frac{L_{p}}{C_{p}}}
$$

(5) A snubber circuit fixed number $R$ is set up in the value which is the same as the character impedance $Z$. A snubber circuit fixed number $C$ is set up in the value of $4-10$ times of the parasitic capacity Cp . ( $\mathrm{C}=4 \mathrm{Cp} \sim$ 10 Cp ) Decide it with trade-off with the character because switching electric currents increase when the value of C is enlarged too much.


Figure 36. PWM Output waveform
(measure of spike resonance frequency


Figure 37.Snubber schematic

## - About circuit board layout

Be careful of the following order of priority, and design a circuit board layout.
(1)C25 • C45(10uF) • C12(1uF) put shortest compared with VCC and GND.
(2) The thermal pattern on the back connected with the GND.
(3)C14 • C22 • C23 • C24(1uF) put shortest compared with each pin and GND.
(4)Each GND line connected by one point without common impedance.
(5)Each power supply and each GND are divided
(6)GND pattern of both side connected with the a lot of VIA electric contacts to lower the impedance of GND.
(7)GND area of the heat radiation area widen to improve the heat radiation ability.

Reference: ROHM designed 4 layer board


Figure 38. ROHM designed 4layer board

参考: ROHM designed 4 layer board SilkScreen


Figure 39. Top Layer Silk Screen (Top View)


Figure 40. Bottom Layer Silk Screen (Top View)

ROHM designed 4-layer board Copper Layer


Figure 41. Top Copper Layer (Top View)


Figure 43. Mid Copper Layer2 (lop View)


Figure 42. Mid Copper Layer1 (Top View)


Figure 44. Bottom Copper Layer (Top View)


Measuring instrument:TH-156(Shibukawa Kuwano Electrical Instruments Co., Ltd.)
Measuring conditions: Installation on ROHM's board
Board size : $74.2 \mathrm{~mm} \times 74.2 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ (with thermal via on board)
Material : FR4

- The board and exposed heat sink on the back of package are connected by soldering.

PCB(1):4-layer board (Top and bottom layer back copper foil size:34.09mm²
2nd, 3rd layer back copper foil size: $5505 \mathrm{~mm}^{2}$ ), $\quad \theta$ ja $=29.1^{\circ} \mathrm{C} / \mathrm{W}$
PCB(2):4-layer board (back copper foil size: $5505 \mathrm{~mm}^{2}$ ), $\quad \theta$ ja $=25.9^{\circ} \mathrm{C} / \mathrm{W}$

OI/O equivalence circuit (Provided pin voltages are typ. Values)

| Pin No. | Pin name | Pin voltage | Pin explanation | Internal equivalence circuit |
| :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} 55 \\ 56 \\ 1 \\ 2 \\ 3 \end{gathered}$ | SDATAO2 <br> SDATAO1 <br> LRCKO <br> BCLKO <br> MCLKO | $V_{\text {D }}$ to 0 V | Digital Audio signal output pin |  |
| $\begin{aligned} & 4 \\ & 5 \\ & 6 \\ & 7 \end{aligned}$ | SDATA1 <br> SDATA2 <br> LRCK <br> BCLK | 3.3 V | Digital Audio signal input pin | (12) (4.5.6.7) |
| 8 | XI | - | X'tal input pin | (12) (8) ? ? ? ? ? ? |
| 9 | XO |  | X'tal output pin |  |
| 10 | VSS | OV | GND pin for Digital block | - |
| 11 | PLL |  | PLL's filter pin |  |
| 12 | DVDD | 3.3 V | Power supply pin for Digital I/O Please connect the capacitor | - |
| $\begin{aligned} & 13 \\ & 15 \end{aligned}$ | $\begin{aligned} & \text { TEST1 } \\ & \text { TEST2 } \end{aligned}$ | - | $\begin{aligned} & \text { Test pin } \\ & \text { Please connect to VSS. } \end{aligned}$ |  |
| 14 | REG15 | 1.5 V | Internal power supply pin for Digital circuit Please connect the capacitor |  |
| $\begin{aligned} & 16 \\ & 17 \\ & 18 \\ & 19 \end{aligned}$ | SW2N <br> SW2P <br> SW1N <br> SW1P | V DD to 0V | PWM Ouput for Subwoofer |  |

OI/O equivalence circuit (Provided pin voltages are typ. Values)

| Pin No. | Pin name | Pin voltage | Pin explanation | Internal equivalence circuit |
| :---: | :---: | :---: | :---: | :---: |
| 20 | GNDA | OV | GND pin for analog signal |  |
| 21 | IN_ERR | 5 V | Error flag input pin <br> H: Normal state <br> L: Error detect |  |
| 22 | FILP |  | Standard pin for power stage Please connect the capacitor | (22) (20) ? |
| 23 | REG5 | 5 V | Internal power supply pin for Power Stage Please connect the capacitor |  |
| 24 | REGG | 5 V | Internal power supply pin for Gate Driver Please connect the capacitor |  |
| 25 | VCCA | Vcc | Power supply pin for analog block Please connect the capacitor | - |
| 26,27 | VCCP2 | Vcc | Power supply pin for ch2 PWM signal Please connect the capacitor | $26,27 \longrightarrow$ |
| 28,29 | OUT2P | Vcc to 0V | Output pin of ch2 positive PWM Please connect to Output LPF. |  |
| 31,32 | GNDP2 | OV | GND pin for ch2 PWM signal | $\begin{aligned} & 2,8,59 \\ & \hline 8,9 \end{aligned}$ |
| 34,35 | OUT2N | Vcc to 0V | Output pin of ch2 negative PWM Please connect to Output LPF. | (31,32) |
| 36,37 | OUT1N | Vcc to 0V | Output pin of ch1 negative PWM <br> Please connect to Output LPF. | 45.4 |
| 39,40 | GNDP1 | OV | GND pin for ch1 PWM signal | $\therefore \quad 7^{p}$ |
| 42,43 | OUT1P | Vcc to 0V | Output pin of ch1 positive PWM <br> Please connect to Output LPF. |  |
| 45,46 | VCCP1 | - | Power supply pin for ch1 PWM signal Please connect the capacitor | (39.40) |

OI/O equivalence circuit (Provided pin voltages are typ. Values)

| NO. | Pin Name | Pin voltage | Pin explanation |
| :---: | :---: | :--- | :--- | :--- |
| 30,33 |  |  |  |
| 44 |  |  |  |$\quad$ N.C.

## Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.
2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

## 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.
6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.
7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.
8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

## 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

## 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## Operational Notes - continued

## 12. Regarding the Input Pin of the IC

This monolithic IC contains $\mathrm{P}+$ isolation and P substrate layers between adjacent elements in order to keep them isolated. $\mathrm{P}-\mathrm{N}$ junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):
When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the $P$ substrate) should be avoided.


Figure xx. Example of monolithic IC structure
13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.
14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).
15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature ( Tj ) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.
16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.
17. Power supply on/off (Pin 25, 26, 27, 45, 46)

In case power supply is started up, RSTX (Pin 51), PDX (Pin 50) and MUTEX (Pin 49) always should be set Low. And in case power supply is shut down, it should be set Low likewise. Then it is possible to eliminate pop noise when power supply is turned on/off. And also, all power supply terminals should start up and shut down together.
18. ERROR terminal (Pin 48), WARNING terminal(Pin 47)

The ERROR flag is outputted when Output short protection or DC voltage protection. And the WARNING flag is outputted when high temperature protection, under voltage protection or over voltage protection. This flag is the function which the condition of this product is shown in.
19. N.C.terminal (Pin 30, 33, 38, 41, 44)
N.C. terminal (Non Connection Pin) does not connect to the inside circuit. Therefore, possible to use open.
20. TESTterminal(Pin 13, 15)

TEST terminal connects with ground to prevent the malfunction by external noise.

## Operational Notes - continued

21. Precautions for Speaker-setting

If the impedance characteristics of the speakers at high-frequency range while increase rapidly, the IC might not have stable-operation in the resonance frequency range of the LC-filter. Therefore, consider adding damping-circuit, etc., depending on the impedance of the speaker.

## - Ordering Information

| B | M | 5 | 4 | 4 | 9 | M | Package <br> MWV: <br> UQFN056V7070 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |



Packaging and forming specification
E2: Embossed tape and reel

## - Marking Diagram



(UNIT: mm)
PKG: UQFN056V7070
Drawing No: EX465-5001-1
-Physical Dimensions Tape and Reel Information
UQFN056V7070


- Revision History

| Date | Revision | Changes |
| :---: | :---: | :--- |
| 18.Sep. 2012 | 001 | New Release |
| 15.Oct. 2012 | 002 | P102,103 Add PWM setting. <br> P129 pin47,48 1.Change equivalence circuit. 2.Change Pin explanation. |
| 7.FEB.2013 | 003 | P30 revise BM5443 to BM5449 |
| 5.JAN.2015 | 004 | Modify P118-P120 application circuit <br> Modify Operation notes |

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## Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ${ }^{(\text {Note } 1)}$, transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.
(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
| :---: | :---: | :---: | :---: |
| CLASSIII | CLASSIII | CLASS II b | CLASSIII |
|  |  | CLASSIII |  |

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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[b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
[c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl 2 , $\mathrm{H}_{2} \mathrm{~S}, \mathrm{NH}_{3}, \mathrm{SO}_{2}$, and $\mathrm{NO}_{2}$
[d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
[e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
[f] Sealing or coating our Products with resin or other coating materials
[g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
[h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

## Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of lonizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
[a] the Products are exposed to sea winds or corrosive gases, including $\mathrm{Cl} 2, \mathrm{H} 2 \mathrm{~S}, \mathrm{NH} 3, \mathrm{SO} 2$, and NO 2
[b] the temperature or humidity exceeds those recommended by ROHM
[c] the Products are exposed to direct sunshine or condensation
[d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

## Precaution for Product Label

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## Precaution for Disposition

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[^0]:    *7 These items show the typical performance of device and depend on board layout, parts, and power supply.
    The standard value is in mounting device and parts on surface of ROHM's board directly.

[^1]:    Continued on next page.

[^2]:    (*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

[^3]:    (*1) The GAIN1 pin can be changed the WARNING flag by command, and the GAIN2 pin can be changed the ERROR flag by command.

[^4]:    *1 This standard value has specified that the edge of LRCK and the rising edge of BCLK do not overlap

[^5]:    * This register cannot read-out.

