

## Description

The 9FGL0841 / 9FGL0851 devices are 8-output clock generators in IDT's 3.3V Full-Featured PCIe family. Each output has a dedicated OE# pin for clock management. Two different spread spectrum levels in addition to spread off are supported. The 9FGL0841 / 9FGL0851 supports PCIe Gen1–4 Common Clocked architectures (CC) and PCIe Separate Reference no-Spread (SRnS) and Separate Reference Independent Spread (SRIS) clocking architectures.

## Typical Applications

- Servers/High-Performance Computing/Accelerators
- Storage
- Embedded systems/Industrial control

## Output Features

- 8 100MHz Low-Power HCSL (LP-HCSL) DIF pairs:
  - 9FGL0841 default  $Z_o = 100\Omega$
  - 9FGL0851 default  $Z_o = 85\Omega$
- 1 3.3V LVCMOS REF output; Wake-On-LAN (WOL) support
- See [AN-891](#) for easy AC-coupling to other logic families

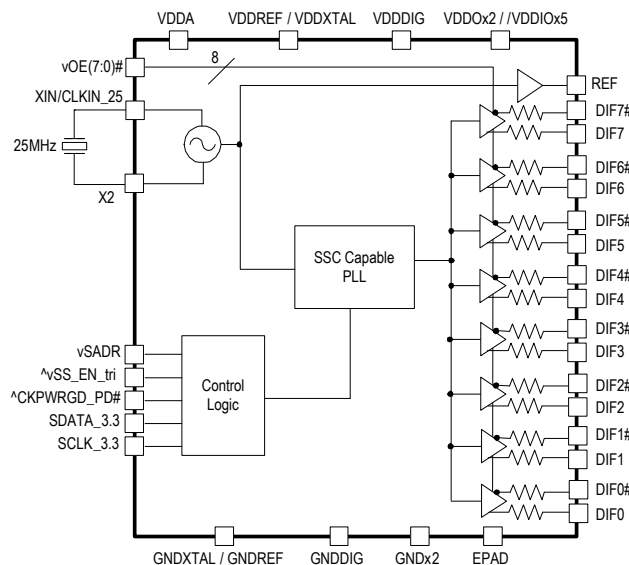
## Key Specifications

- PCIe Gen1–4 CC compliant; Gen2–3 SRIS compliant
- DIF cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 50ps
- DIF 12kHz–20MHz phase jitter is < 2ps rms when SSC is off
- REF phase jitter < 300fs rms; SSC off and < 1.9ps rms; SSC on
- $\pm 100$ ppm frequency accuracy on all clocks

## Features

- Direct connection to loads saves 32 resistors compared to standard PCIe devices
- 206mW typical power consumption (at 3.3V); eliminates thermal concerns
- $V_{DDIO}$  rail allows 35% power savings at optional 1.05V; maximum power savings
- SMBus-selectable features allows optimization to customer requirements:
  - Control input polarity
  - Control input pull-ups/pull-downs
  - Slew rate for each output
  - Differential output amplitude
  - 33 $\Omega$ , 85 $\Omega$  or 100 $\Omega$  output impedance for each output
- Devices contain default configuration; SMBus not required
- Contact factory for customized versions
- 25MHz input frequency
- OE# pins; support DIF power management
- Pin-selectable SRnS, CC 0% and CC/SRIS -0.5% spread
- SMBus-selectable CC/SRIS -0.25% spread
- Clean switching between the CC/SRIS spread settings
- DIF outputs blocked until PLL is locked; clean system start-up
- 2 selectable SMBus addresses
- Space saving 6 × 6 mm 48-VFQFPN package

## Block Diagram

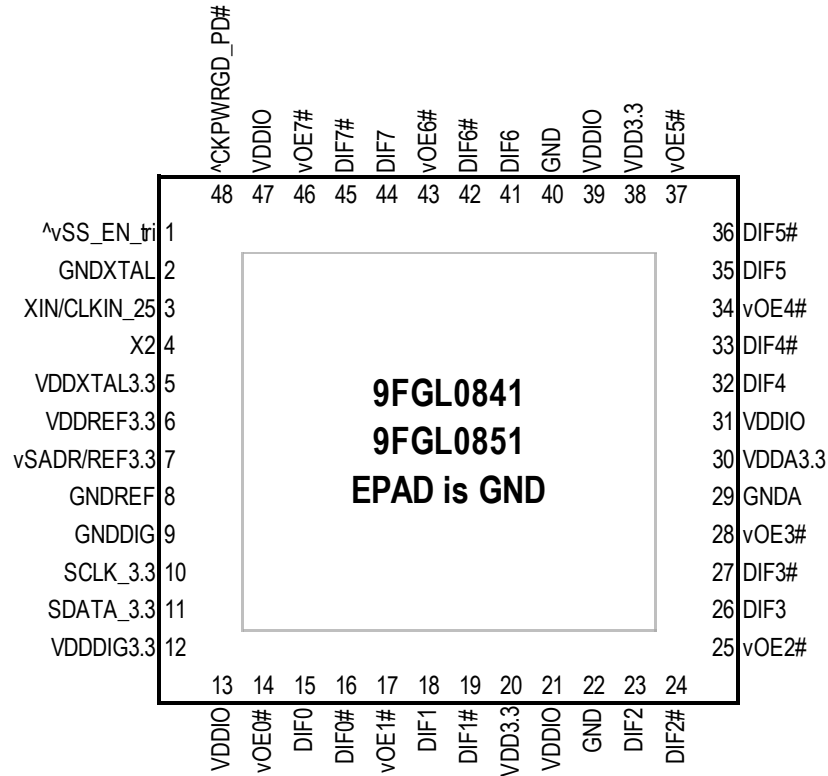


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## Pin Assignment

Figure 1. Pin Assignments for 6 x 6 mm 48-VFQFPN Package – Top View



**48-VFQFPN, 6 x 6 mm, 0.4mm pitch**

v prefix indicates internal pull-down resistor

^ prefix indicates internal pull-up resistor

^v prefix indicates internal pull-up and pull-down resistors

## Pin Descriptions

Table 1. Pin Descriptions

| Number | Name         | Type        | Description  |
|--------|--------------|-------------|--|
| 1      | ^vSS_EN_tri  | Latched In  | Latched select input to select spread spectrum amount at initial power up. See <a href="#">Spread Selection</a> table. |
| 2      | GNDXTAL      | GND         | GND for XTAL.  |
| 3      | XIN/CLKIN_25 | Input       | Crystal input or reference clock input. Nominally 25MHz.   |
| 4      | X2           | Output      | Crystal output.  |
| 5      | VDDXTAL3.3   | Power       | Power supply for XTAL. Nominally 3.3V.   |
| 6      | VDDREF3.3    | Power       | Power supply for REF output. Nominally 3.3V.   |
| 7      | vSADR/REF3.3 | Latched I/O | Latch to select SMBus address/3.3V LVCMOS copy of X1/REFIN pin.  |
| 8      | GNDREF       | GND         | Ground pin for the REF outputs.  |
| 9      | GNDDIG       | GND         | Ground pin for digital circuitry.  |

Table 1. Pin Descriptions (Cont.)

| Number | Name      | Type   | Description   |
|--------|-----------|--------|---|
| 10     | SCLK_3.3  | Input  | Clock pin of SMBus circuitry, 3.3V tolerant.  |
| 11     | SDATA_3.3 | I/O    | Data pin for SMBus circuitry, 3.3V tolerant.  |
| 12     | VDDDIG3.3 | Power  | 3.3V digital power (dirty power).   |
| 13     | VDDIO     | Power  | Power supply for differential outputs.  |
| 14     | vOE0#     | Input  | Active low input for enabling output 0. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 15     | DIF0      | Output | Differential true clock output.   |
| 16     | DIF0#     | Output | Differential complementary clock output.  |
| 17     | vOE1#     | Power  | Active low input for enabling output 1. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 18     | DIF1      | Input  | Differential true clock output.   |
| 19     | DIF1#     | Output | Differential complementary clock output.  |
| 20     | VDD3.3    | Power  | Power supply, nominally 3.3V.   |
| 21     | VDDIO     | Power  | Power supply for differential outputs.  |
| 22     | GND       | GND    | Ground pin.   |
| 23     | DIF2      | Output | Differential true clock output.   |
| 24     | DIF2#     | Output | Differential complementary clock output.  |
| 52     | vOE2#     | Power  | Active low input for enabling output 2. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 26     | DIF3      | Input  | Differential true clock output.   |
| 27     | DIF3#     | Output | Differential complementary clock output.  |
| 28     | vOE3#     | Power  | Active low input for enabling output 3. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 29     | GND A     | Input  | Ground pin for the PLL core.  |
| 30     | VDDA3.3   | Power  | 3.3V power for the PLL core.  |
| 31     | VDDIO     | Power  | Power supply for differential outputs.  |
| 32     | DIF4      | Output | Differential true clock output.   |
| 33     | DIF4#     | Output | Differential complementary clock output.  |
| 34     | vOE4#     | Power  | Active low input for enabling output 4. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 35     | DIF5      | Input  | Differential true clock output.   |
| 36     | DIF5#     | Output | Differential complementary clock output.  |
| 37     | vOE5#     | Input  | Active low input for enabling output 5. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 38     | VDD3.3    | Power  | Power supply. Nominally 3.3V.   |
| 39     | VDDIO     | Power  | Power supply for differential outputs.  |
| 40     | GND       | GND    | Ground pin.   |

Table 1. Pin Descriptions (Cont.)

| Number | Name         | Type   | Description   |
|--------|--------------|--------|---|
| 41     | DIF6         | Output | Differential true clock output.   |
| 42     | DIF6#        | Output | Differential complementary clock output.  |
| 43     | vOE6#        | Input  | Active low input for enabling output 6. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output.   |
| 44     | DIF7         | Output | Differential true clock output.   |
| 45     | DIF7#        | Output | Differential complementary clock output.  |
| 46     | vOE7#        | Input  | Active low input for enabling output 7. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output.   |
| 47     | VDDIO        | Power  | Power supply for differential outputs.  |
| 48     | ^CKPWRGD_PD# | Input  | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power-down mode, subsequent high assertions exit Power-down mode. This pin has internal pull-up resistor. |
| 49     | EPAD         | GND    | Connect to ground.  |

Table 2. Spread Selection

| ^vSS_EN_tri Pin | B1[4:3] | Spread% | Note                            |
|-----------------|---------|---------|---------------------------------|
| 0               | 00      | 0       | PCIe SRNS mode.                 |
| -               | 01      | -0.25   | PCIe Common Clock or SRIS mode. |
| M (VDD/2)       | 10      | 0       | PCIe Common Clock or SRIS mode. |
| 1               | 11      | -0.50   | PCIe Common Clock or SRIS mode. |

If SRnS mode is desired, power up with ^vSS\_EN\_tri = '0'. Do not attempt to switch to the other modes via SMBus control in Byte 1 or a system reset will be required. If Common Clock (CC) or SRIS mode is desired, power up with ^vSS\_EN\_tri at either 'M' or '1'. The desired spread spectrum amount can then be selected via Byte 1 without a requiring a system reset. Once 'M' or '1' is latched at power up, do not attempt to enter SRnS mode or a system reset will be required.

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9FGL0841 / 9FGL0851 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute Maximum Ratings

| Parameter                 | Symbol      | Conditions                 | Minimum | Maximum        | Units | Notes |
|---------------------------|-------------|----------------------------|---------|----------------|-------|-------|
| Supply Voltage            | $V_{DDx}$   |                            | -0.5    | 4.6            | V     | 1,2   |
| Input Voltage             | $V_{IN}$    |                            | -0.5    | $V_{DD} + 0.5$ | V     | 1,3   |
| Input High Voltage, SMBus | $V_{IHSMB}$ | SMBus clock and data pins. |         | 3.9            | V     | 1     |
| Storage Temperature       | $T_s$       |                            | -65     | 150            | °C    | 1     |
| Junction Temperature      | $T_j$       |                            |         | 125            | °C    | 1     |
| Input ESD Protection      | ESD prot    | Human Body Model.          | 2500    |                | V     | 1     |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Operation under these conditions is neither implied nor guaranteed.

<sup>3</sup> Not to exceed 4.6V.

## Thermal Characteristics

Table 4. Thermal Characteristics

| Symbol         | Parameter                        | Package | Typical Values | Units | Notes |
|----------------|----------------------------------|---------|----------------|-------|-------|
| $\theta_{JC}$  | Junction to case.                | NDG48   | 33             | °C/W  | 1     |
| $\theta_{Jb}$  | Junction to base.                |         | 2.1            | °C/W  | 1     |
| $\theta_{JA0}$ | Junction to air, still air.      |         | 37             | °C/W  | 1     |
| $\theta_{JA1}$ | Junction to air, 1 m/s air flow. |         | 30             | °C/W  | 1     |
| $\theta_{JA3}$ | Junction to air, 3 m/s air flow. |         | 27             | °C/W  | 1     |
| $\theta_{JA5}$ | Junction to air, 5 m/s air flow. |         | 26             | °C/W  | 1     |

<sup>1</sup> EPAD soldered to board.

## Electrical Characteristics

$T_A = T_{AMB}$ . Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

Table 5. SMBus Parameters

| Parameter                 | Symbol       | Conditions  | Minimum | Typical | Maximum | Units | Notes |
|---------------------------|--------------|---|---------|---------|---------|-------|-------|
| SMBus Input Low Voltage   | $V_{ILSMB}$  | $V_{DDSMB} = 3.3V$ .                                  |         |         | 0.8     | V     |       |
| SMBus Input High Voltage  | $V_{IHSMB}$  | $V_{DDSMB} = 3.3V$ .                                  | 2.1     |         | 3.6     | V     |       |
| SMBus Output Low Voltage  | $V_{OLSMB}$  | At $I_{PULLUP}$ .                                     |         |         | 0.4     | V     |       |
| SMBus Sink Current        | $I_{PULLUP}$ | At $V_{OL}$ .   | 4       |         |         | mA    |       |
| Nominal Bus Voltage       | $V_{DDSMB}$  |   | 2.7     |         | 3.6     | V     |       |
| SCLK/SDATA Rise Time      | $t_{RSMB}$   | (Max. $V_{IL} - 0.15V$ ) to (Min. $V_{IH} + 0.15V$ ). |         |         | 1000    | ns    | 1     |
| SCLK/SDATA Fall Time      | $t_{FSMB}$   | (Min. $V_{IH} + 0.15V$ ) to (Max. $V_{IL} - 0.15V$ ). |         |         | 300     | ns    | 1     |
| SMBus Operating Frequency | $f_{SMB}$    | SMBus operating frequency.                            |         |         | 500     | kHz   | 2     |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> The device must be powered up for the SMBus to function.

Table 6. Input/Supply/Common Parameters – Normal Operating Conditions

| Parameter                     | Symbol      | Conditions   | Minimum               | Typical              | Maximum               | Units | Notes |
|-------------------------------|-------------|--|-----------------------|----------------------|-----------------------|-------|-------|
| Supply Voltage                | $V_{DDxxx}$ | Supply voltage for core, analog and single-ended LVC MOS outputs.  | 3.135                 | 3.3                  | 3.465                 | V     |       |
| IO Supply Voltage             | $V_{DDIO}$  | Supply voltage for differential low power outputs.   | 0.9975                | 1.05–3.3             | 3.465                 | V     |       |
| Ambient Operating Temperature | $T_{AMB}$   | Industrial range.  | -40                   | 25                   | 85                    | °C    |       |
| Input High Voltage            | $V_{IH}$    | Single-ended inputs, except SMBus.   | $0.75 \times V_{DDx}$ |                      | $V_{DDx} + 0.3$       | V     |       |
| Input Low Voltage             | $V_{IL}$    |  | -0.3                  |                      | $0.25 \times V_{DDx}$ | V     |       |
| Input High Voltage            | $V_{IHtri}$ | Single-ended tri-level inputs ('_tri' suffix).   | $0.8 \times V_{DDx}$  |                      | $V_{DDx} + 0.3$       | V     |       |
| Input Mid Voltage             | $V_{IMtri}$ |  | $0.4 \times V_{DDx}$  | $0.5 \times V_{DDx}$ | $0.6 \times V_{DDx}$  | V     |       |
| Input Low Voltage             | $V_{ILtri}$ |  | -0.3                  |                      | $0.20 \times V_{DDx}$ | V     | 6     |
| Input Current                 | $I_{IN}$    | Single-ended inputs, $V_{IN} = GND$ , $V_{IN} = V_{DD}$ .  | -5                    |                      | 5                     | μA    |       |
|                               | $I_{INP}$   | Single-ended inputs.<br>$V_{IN} = 0V$ ; inputs with internal pull-up resistors.<br>$V_{IN} = V_{DD}$ ; inputs with internal pull-down resistors. | -50                   |                      | 50                    | μA    |       |
| Input Frequency               | $F_{IN}$    | XTAL or X1 input.  |                       | 25                   |                       | MHz   | 4     |
| Pin Inductance                | $L_{pin}$   |  |                       |                      | 7                     | nH    | 1     |
| Capacitance                   | $C_{IN}$    | Logic inputs, except DIF_IN.   | 1.5                   |                      | 5                     | pF    | 1     |
|                               | $C_{OUT}$   | Output pin capacitance.  |                       |                      | 6                     | pF    | 1     |

Table 6. Input/Supply/Common Parameters – Normal Operating Conditions (Cont.)

| Parameter               | Symbol               | Conditions  | Minimum | Typical | Maximum | Units         | Notes |
|-------------------------|----------------------|---|---------|---------|---------|---------------|-------|
| CLK Stabilization       | $t_{\text{STAB}}$    | From $V_{\text{DD}}$ power-up and after input clock stabilization or deassertion of PD# to 1st clock. |         | 0.3     | 1.8     | ms            | 1,2   |
| SS Modulation Frequency | $f_{\text{MOD}}$     | Triangular modulation.  | 30      | 31.6    | 33      | kHz           | 1     |
| OE# Latency             | $t_{\text{LATOE\#}}$ | DIF start after OE# assertion.<br>DIF stop after OE# deassertion.                                     | 1       | 2       | 3       | clocks        | 1,3   |
| Tdrive_PD#              | $t_{\text{DRVPD}}$   | DIF output enable after PD# de-assertion.   |         |         | 300     | $\mu\text{s}$ | 1,3   |
| Fall Time               | $t_{\text{F}}$       | Fall time of single-ended control inputs.   |         |         | 5       | ns            | 1,2   |
| Rise Time               | $t_{\text{R}}$       | Rise time of single-ended control inputs.   |         |         | 5       | ns            | 1,2   |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup> Time from deassertion until outputs are > 200mV.

<sup>4</sup> Contact the factory for other frequencies.

Table 7. DIF Low-Power HCSL Outputs

| Parameter                  | Symbol                   | Conditions  | Minimum | Typical | Maximum | Units | Notes      |
|----------------------------|--------------------------|---|---------|---------|---------|-------|------------|
| Slew Rate                  | Trf                      | Scope averaging on, fast setting.   | 2       | 2.7     | 4       | V/ns  | 2,3        |
|                            |                          | Scope averaging, slow setting.  | 1       | 1.9     | 3       | V/ns  | 2,3        |
| Crossing Voltage (abs)     | Vcross_abs               | Scope averaging off.  | 250     | 409     | 550     | mV    | 1,4,5      |
| Crossing Voltage (var)     | $\Delta\text{-Vcross}$   | Scope averaging off.  |         | 14      | 140     | mV    | 1,4,9      |
| Avg. Clock Period Accuracy | $T_{\text{PERIOD\_AVG}}$ |   | -100    | 0       | +2600   | ppm   | 2,10,12,13 |
| Absolute Period            | $T_{\text{PERIOD\_ABS}}$ | Includes jitter and spread spectrum modulation.   | 9.94906 | 10      | 10.1011 | ns    | 2,6        |
| Jitter, Cycle to Cycle     | $t_{\text{jyc-cyc}}$     |   |         | 16      | 50      | ps    | 2          |
| Voltage High               | $V_{\text{HIGH}}$        | Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on). | 660     | 761     | 850     | mV    | 1          |
| Voltage Low                | $V_{\text{LOW}}$         |   | -150    | -7      | 150     | mV    | 1          |
| Absolute Maximum Voltage   | $V_{\text{MIN}}$         | Measurement on single-ended signal using absolute value (scope averaging off).                        |         | 819     | 1150    | mV    | 1,7,15     |
| Absolute Minimum Voltage   | $V_{\text{MAX}}$         |   | -300    | -46     |         |       | 1,8,15     |
| Duty Cycle                 | $t_{\text{DC}}$          |   | 45      | 49      | 55      | %     | 2          |
| Slew Rate Matching         | $\Delta\text{Trf}$       | Single-ended measurement.   |         | 6       | 20      | %     | 1,14       |
| Skew, Output to Output     | $t_{\text{sk3}}$         | Averaging on, $V_{\text{T}} = 50\%$ .   |         | 12      | 50      | ps    | 2          |

<sup>1</sup> Measured from single-ended waveform.

<sup>2</sup> Measured from differential waveform.

<sup>3</sup> Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

<sup>4</sup> Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.



- <sup>5</sup> Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
- <sup>6</sup> Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation.
- <sup>7</sup> Defined as the maximum instantaneous voltage including overshoot.
- <sup>8</sup> Defined as the minimum instantaneous voltage including undershoot.
- <sup>9</sup> Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in  $V_{CROSS}$  for any particular system.
- <sup>10</sup> Refer to Section 8.6.2 of the PCI Express Base Specification, Revision 4.0 for information regarding PPM considerations.
- <sup>11</sup> System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors  $C_L$ . Single-ended probes must be used for measurements requiring single ended measurements. Either single-ended probes with math or differential probe can be used for differential measurements. Test load  $C_L = 2pF$ .
- <sup>12</sup> PCIe Gen1 through Gen4 specify  $\pm 300ppm$  frequency tolerances. The 9FGL0xxx devices already meet the tighter  $\pm 100ppm$  frequency tolerances proposed for PCIe Gen5 and required by most servers.
- <sup>13</sup> "ppm" refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100ppm, then we have an error budget of  $100Hz/ppm \times 100ppm = 10kHz$ . The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The  $\pm 100ppm$  applies to systems that do not employ Spread Spectrum clocking, or that use common clock source. For systems employing Spread Spectrum clocking, there is an additional 2,500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600ppm for Common Clock architectures. Separate Reference Clock architectures may have a lower allowed spread percentage.
- <sup>14</sup> Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a  $\pm 75$  mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.
- <sup>15</sup> At default SMBus amplitude settings.

Table 8. DIF LP-HCSL Output Unfiltered Phase Jitter Parameters

| Parameter                 | Symbol          | Conditions                                       | Minimum | Typical | Maximum | Units    |
|---------------------------|-----------------|--|---------|---------|---------|----------|
| Phase Jitter, 12kHz–20MHz | $t_{jph12k20M}$ | 100MHz outputs with REF output enabled, SSC off. |         | 1.9     | 2       | ps (rms) |

Table 9. Current Consumption

| Parameter   | Symbol       | Conditions  | Minimum | Typical | Maximum | Units | Notes |
|---|--------------|---|---------|---------|---------|-------|-------|
| Operating Supply Current  | $I_{DDAOP}$  | $V_{DDA}$ , all outputs active at 100MHz.   |         | 14      | 19      | mA    |       |
|   | $I_{DDOP}$   | All other $V_{DD}$ , except $V_{DDA}$ and $V_{DDIO}$ , all outputs active at 100MHz.        |         | 18      | 24      | mA    |       |
|   | $I_{DDIOOP}$ | $V_{DDIO}$ , all outputs active at 100MHz.  |         | 30      | 37      | mA    |       |
| Wake-on-LAN Current<br>(Power down state and Byte 3, bit 5 = '1') | $I_{DDAPD}$  | $V_{DDA}$ , DIF outputs off, REF output running.  |         | 0.9     | 1.5     | mA    | 1     |
|   | $I_{DDPD}$   | All other $V_{DD}$ , except $V_{DDA}$ and $V_{DDIO}$ , DIF outputs off, REF output running. |         | 5.2     | 8       | mA    | 1     |
|   | $I_{DDIOOP}$ | $V_{DDIO}$ , DIF outputs off, REF output running.   |         | 0.04    | 0.1     | mA    | 1     |
| Power Down Current<br>(Power down state and Byte 3, bit 5 = '0')  | $I_{DDAPD}$  | $V_{DDA}$ , all outputs off.  |         | 0.9     | 1.5     | mA    |       |
|   | $I_{DDPD}$   | All other $V_{DD}$ , except $V_{DDA}$ and $V_{DDIO}$ , all outputs off.                     |         | 1.7     | 2.3     | mA    |       |
|   | $I_{DDIOOP}$ | $V_{DDIO}$ , all outputs off.   |         | 0.04    | 0.1     | mA    |       |

<sup>1</sup> This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

Table 10. Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

 $T_{AMB}$  = over the specified operating range. Supply Voltages per normal operation conditions, See [Test Loads](#) for loading conditions.

| Parameter                                  | Symbol             | Conditions   | Minimum | Typical | Maximum | Industry Limits | Units    | Notes |
|--|--------------------|--|---------|---------|---------|-----------------|----------|-------|
| Phase Jitter Spread off or -0.25% or -0.5% | $t_{jphPCIeG1-CC}$ | PCIe Gen1.   |         | 17      | 29      | 86              | ps (p-p) | 1,2,3 |
|  | $t_{jphPCIeG2-CC}$ | PCIe Gen2 Low Band<br>10kHz < f < 1.5MHz<br>(PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).            |         | 0.4     | 0.58    | 3               | ps (rms) | 1,2   |
|  |                    | PCIe Gen2 High Band<br>1.5MHz < f < Nyquist (50MHz)<br>(PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz). |         | 1.1     | 1.6     | 3.1             | ps (rms) | 1,2   |
|  | $t_{jphPCIeG3-CC}$ | PCIe Gen3<br>(PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).  |         | 0.26    | 0.36    | 1               | ps (rms) | 1,2   |
|  | $t_{jphPCIeG4-CC}$ | PCIe Gen4<br>(PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).  |         | 0.26    | 0.36    | 0.5             | ps (rms) | 1,2   |

Table 11. Filtered Phase Jitter Parameters - PCIe Separate Reference Independent Spread (SRIS) Architectures

 $T_{AMB}$  = over the specified operating range. Supply Voltages per normal operation conditions, See [Test Loads](#) for loading conditions.

| Parameter                   | Symbol               | Conditions   | Minimum | Typical | Maximum | Industry Limits | Units    | Notes |
|-----------------------------|----------------------|--|---------|---------|---------|-----------------|----------|-------|
| Phase Jitter, -0.25% Spread | $t_{jphPCIeG2-SRIS}$ | PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz).             |         | 0.7     | 0.73    | 2               | ps (rms) | 1,4,5 |
|                             | $t_{jphPCIeG3-SRIS}$ | PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz). |         | 0.4     | 0.42    | 0.7             | ps (rms) | 1,4,5 |
| Phase Jitter, -0.5% Spread  | $t_{jphPCIeG2-SRIS}$ | PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz).             |         | 0.7     | 0.73    | 2               | ps (rms) | 1,4,5 |
|                             | $t_{jphPCIeG3-SRIS}$ | PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz). |         | 0.6     | 0.63    | 0.7             | ps (rms) | 1,4,5 |

**Notes on PCIe Filtered Phase Jitter tables:**

<sup>1</sup> Applies to all outputs, guaranteed by design and characterization.

<sup>2</sup> Based on PCIe Base Specification Rev 4.0 version 1.0. See <http://www.pcisig.com> for latest specifications.

<sup>3</sup> Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of  $1^{-12}$ .

<sup>4</sup> IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRnS) PCIe clock architectures

<sup>5</sup> According to the PCIe Base Specification Rev4.0 version 1.0, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. The PCIe Base Specification Rev5.0 is expected to resolve this.

Table 12. REF Output

| Parameter              | Symbol                           | Conditions  | Minimum                  | Typical | Maximum                  | Units       | Notes |
|------------------------|----------------------------------|---|--------------------------|---------|--------------------------|-------------|-------|
| Long Accuracy          | ppm                              | See T <sub>period</sub> min-max values.   | 0                        |         |                          | ppm         | 1,2   |
| Clock Period           | T <sub>period</sub>              | REF output.   | 40                       |         |                          | ns          | 2     |
| High Output Voltage    | V <sub>HIGH</sub>                | I <sub>OH</sub> = -2mA.   | 0.8 x V <sub>DDREF</sub> |         |                          | V           |       |
| Low Output Voltage     | V <sub>LOW</sub>                 | I <sub>OL</sub> = 2mA.  |                          |         | 0.2 x V <sub>DDREF</sub> | V           |       |
| Rise/Fall Slew Rate    | t <sub>rf1</sub>                 | Byte 3 = 1F, V <sub>OH</sub> = 0.8 x V <sub>DD</sub> ,<br>V <sub>OL</sub> = 0.2 x V <sub>DD</sub> . | 0.5                      | 0.9     | 1.5                      | V/ns        | 1     |
|                        | t <sub>rf1</sub>                 | Byte 3 = 5F, V <sub>OH</sub> = 0.8 x V <sub>DD</sub> ,<br>V <sub>OL</sub> = 0.2 x V <sub>DD</sub> . | 1.0                      | 1.5     | 2.5                      | V/ns        | 1,3   |
|                        | t <sub>rf1</sub>                 | Byte 3 = 9F, V <sub>OH</sub> = 0.8 x V <sub>DD</sub> ,<br>V <sub>OL</sub> = 0.2 x V <sub>DD</sub> . | 1.5                      | 2.1     | 3.1                      | V/ns        | 1     |
|                        | t <sub>rf1</sub>                 | Byte 3 = DF, V <sub>OH</sub> = 0.8 x V <sub>DD</sub> ,<br>V <sub>OL</sub> = 0.2 x V <sub>DD</sub> . | 2.0                      | 2.7     | 3.8                      | V/ns        | 1     |
| Duty Cycle             | d <sub>t1X</sub>                 | V <sub>T</sub> = V <sub>DD</sub> /2 V.  | 45                       | 49.7    | 55                       | %           | 1,4   |
| Duty Cycle Distortion  | d <sub>tcd</sub>                 | V <sub>T</sub> = V <sub>DD</sub> /2 V.  | -1                       | 0       | 0                        | %           | 1,5   |
| Jitter, Cycle to Cycle | t <sub>j<sub>cyc-cyc</sub></sub> | V <sub>T</sub> = V <sub>DD</sub> /2 V.  |                          | 35      | 125                      | ps          | 1,4   |
| Noise Floor            | t <sub>dBc1k</sub>               | 1kHz offset.  |                          | -145    | -135                     | dBc         | 1,4   |
|                        | t <sub>dBc10k</sub>              | 10kHz offset to Nyquist.  |                          | -150    | -140                     | dBc         | 1,4   |
| Jitter, Phase          | t <sub>j<sub>phREF</sub></sub>   | 12kHz to 5MHz, DIF SSC off.   |                          | 0.13    | 0.3                      | ps<br>(rms) | 1,4   |
|                        |                                  | 12kHz to 5MHz, DIF SSC on.  |                          | 1.4     | 1.5                      | ps<br>(rms) | 1,4   |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00MHz.

<sup>3</sup> Default SMBus value.

<sup>4</sup> When driven by a crystal.

<sup>5</sup> When driven by an external oscillator via the X1 pin, X2 should be floating.

## Power Management

 Table 13. Power Management <sup>3</sup>

| CKPWRGD_PD# | SMBus OE bit | OEx# Pin | DIF                   |                       | REF                   |
|-------------|--------------|----------|-----------------------|-----------------------|-----------------------|
|             |              |          | True O/P              | Comp. O/P             |                       |
| 0           | X            | X        | Low <sup>1</sup>      | Low <sup>1</sup>      | Hi-Z <sup>2</sup>     |
| 1           | 1            | 0        | Running               | Running               | Running               |
| 1           | 1            | 1        | Disabled <sup>1</sup> | Disabled <sup>1</sup> | Running               |
| 1           | 0            | X        | Disabled <sup>1</sup> | Disabled <sup>1</sup> | Disabled <sup>4</sup> |

<sup>1</sup> The output state is set by B11[1:0] (Low/Low default).

<sup>2</sup> REF is Hi-Z until the 1st assertion of CKPWRGD\_PD# high. After this, when CKPWRGD\_PD# is low, REF is disabled unless Byte3[5] = 1, in which case REF is running.

<sup>3</sup> Input polarities defined at default values for 9FGL0841 / 9FGL0851.

<sup>4</sup> See SMBus description for Byte 3, bit 4.

Table 14. SMBus Address Selection

|   | SADR | Address | + Read/Write Bit |
|---|------|---------|------------------|
| State of SADR on first application of CKPWRGD_PD# | 0    | 1101000 | X                |
|   | 1    | 1101010 | X                |

Table 15. Power Connections

| Pin Number      |                    |                | Description            |
|-----------------|--------------------|----------------|------------------------|
| V <sub>DD</sub> | V <sub>DDIO</sub>  | GND            |                        |
| 5               |                    | 2              | XTAL OSC.              |
| 6               |                    | 8              | REF power.             |
| 12              |                    | 9              | Digital (dirty) power. |
| 20,38           | 13, 21, 31, 39, 47 | 22, 29, 40, 49 | DIF outputs.           |
| 30              |                    | 29             | PLL analog.            |

## Test Loads

Figure 2. Single-ended Output Test Load

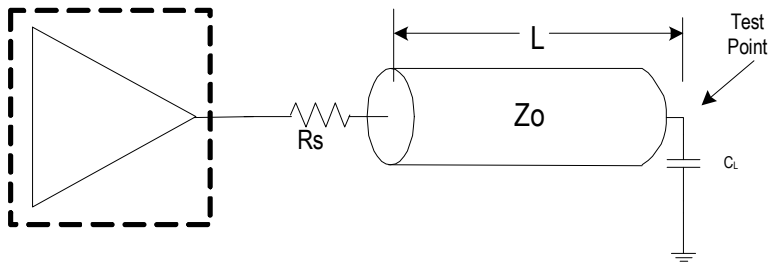


Figure 3. Low-Power HCSL Output Test Load (standard PCIe source-terminated test load)

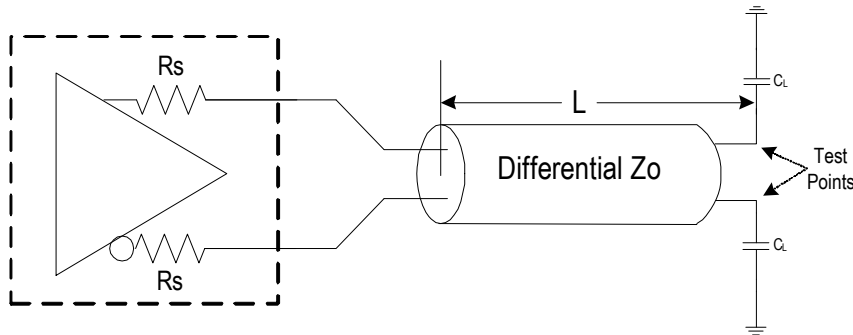


Figure 4. Test Setup for PCIe Jitter Measurements

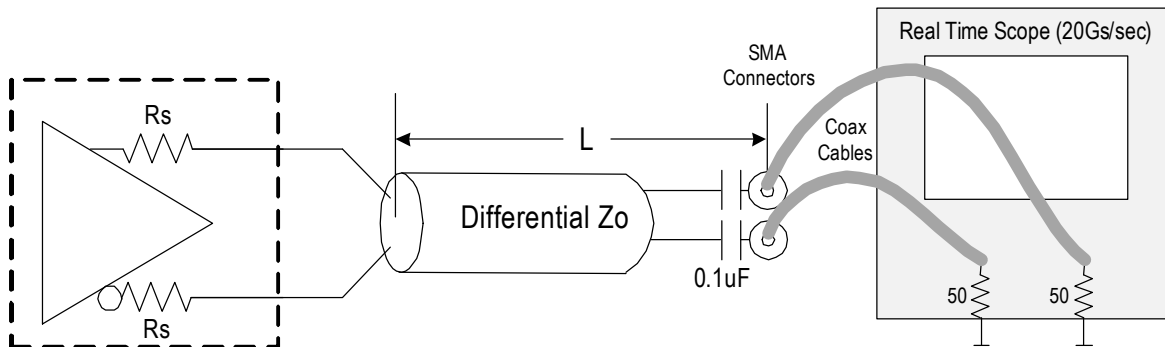


Table 16. Terminations

| Device   | L (inches) | Zo ( $\Omega$ ) | Rs ( $\Omega$ ) | REF C <sub>L</sub> (pF) | DIF C <sub>L</sub> (pF) |
|----------|------------|-----------------|-----------------|-------------------------|-------------------------|
| 9FGL0841 | 5          | 100             | None needed     | 4.7                     | 2                       |
| 9FGL0851 | 5          | 100             | 7.5             |                         |                         |
| 9FGL0841 | 5          | 85              | N/A             |                         |                         |
| 9FGL0851 | 5          | 85              | None needed     |                         |                         |

## Alternate Terminations

The 9FGL family can easily drive LVPECL, LVDS, and CML logic. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with IDT’s “Universal” Low-Power HCSL Outputs”](#) for details.

## Crystal Characteristics

Table 17. Recommended Crystal Characteristics

| Parameter   | Value       | Units       |
|---|-------------|-------------|
| Frequency   | 25          | MHz         |
| Resonance Mode  | Fundamental | —           |
| Frequency Tolerance @ 25°C  | ±20         | ppm maximum |
| Frequency Stability, reference at 25°C over operating temperature range | ±20         | ppm maximum |
| Temperature Range (industrial)  | -40 to +85  | °C          |
| Temperature Range (commercial)  | 0 to +70    | °C          |
| Equivalent Series Resistance (ESR)                                      | 50          | Ω maximum   |
| Shunt Capacitance ( $C_0$ )   | 7           | pF maximum  |
| Load Capacitance ( $C_L$ )  | 8           | pF maximum  |
| Drive Level   | 0.1         | mW maximum  |
| Aging per year  | ±5          | ppm maximum |

## General SMBus Serial Interface Information

### How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

| Index Block Write Operation |           |                      |
|-----------------------------|-----------|----------------------|
| Controller (Host)           |           | IDT (Slave/Receiver) |
| T                           | starT bit |                      |
| Slave Address               |           |                      |
| WR                          | WRite     |                      |
| Beginning Byte = N          |           | ACK                  |
| Data Byte Count = X         |           | ACK                  |
| Beginning Byte N            |           | ACK                  |
| O                           | X Byte    | O                    |
| O                           |           | O                    |
| O                           |           | O                    |
| Byte N + X - 1              |           | O                    |
| ACK                         |           |                      |
| P                           | stoP bit  |                      |

**Note:** Unless otherwise indicated, default values are for the 0841, and 0851. Address is latched on SADR pin.

### How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation |                 |                      |
|----------------------------|-----------------|----------------------|
| Controller (Host)          |                 | IDT (Slave/Receiver) |
| T                          | starT bit       |                      |
| Slave Address              |                 |                      |
| WR                         | WRite           |                      |
| Beginning Byte = N         |                 | ACK                  |
| RT Repeat starT            |                 | ACK                  |
| Slave Address              |                 |                      |
| RD                         | ReaD            |                      |
| ACK                        |                 | ACK                  |
| ACK                        |                 | Data Byte Count=X    |
| ACK                        |                 | Beginning Byte N     |
| O                          | X Byte          | O                    |
| O                          |                 | O                    |
| O                          |                 | O                    |
| O                          |                 | O                    |
| ACK                        |                 | Byte N + X - 1       |
| N                          | Not acknowledge |                      |
| P                          | stoP bit        |                      |

**SMBus Table: Output Enable Register <sup>1</sup>**

| Byte 0 | Name    | Control Function | Type | 0            | 1           | Default |
|--------|---------|------------------|------|--------------|-------------|---------|
| Bit 7  | DIF OE7 | Output Enable    | RW   | See B11[1:0] | Pin Control | 1       |
| Bit 6  | DIF OE6 | Output Enable    | RW   |              | Pin Control | 1       |
| Bit 5  | DIF OE5 | Output Enable    | RW   |              | Pin Control | 1       |
| Bit 4  | DIF OE4 | Output Enable    | RW   |              | Pin Control | 1       |
| Bit 3  | DIF OE3 | Output Enable    | RW   |              | Pin Control | 1       |
| Bit 2  | DIF OE2 | Output Enable    | RW   |              | Pin Control | 1       |
| Bit 1  | DIF OE1 | Output Enable    | RW   |              | Pin Control | 1       |
| Bit 0  | DIF OE0 | Output Enable    | RW   |              | Pin Control | 1       |

<sup>1</sup> A low on these bits will override the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default).

**SMBus Table: Spread Spectrum and V<sub>HIGH</sub> Control Register**

| Byte 1 | Name         | Control Function            | Type            | 0   | 1                                    | Default |
|--------|--------------|-----------------------------|-----------------|---|--------------------------------------|---------|
| Bit 7  | SSEN RB1     | SS Enable Readback Bit1     | R               | See <a href="#">Spread Selection</a> table. |                                      | Latch   |
| Bit 6  | SSEN RB0     | SS Enable Readback Bit0     | R               |   |                                      | Latch   |
| Bit 5  | SSEN_SWCNTRL | Enable SW control of SS     | RW              | SS controlled by latch (B1[7:6]).           | Values in B1[4:3] control SS amount. | 0       |
| Bit 4  | SSENSW1      | SS Enable Software Ctl Bit1 | RW <sup>1</sup> | See <a href="#">Spread Selection</a> table. |                                      | 0       |
| Bit 3  | SSENSW0      | SS Enable Software Ctl Bit0 | RW <sup>1</sup> |   |                                      | 0       |
| Bit 2  | Reserved     |                             |                 |   |                                      | X       |
| Bit 1  | AMPLITUDE 1  | Controls Output Amplitude   | RW              | 00 = 0.6V                                   | 01 = 0.68V                           | 1       |
| Bit 0  | AMPLITUDE 0  |                             | RW              | 10 = 0.75V                                  | 11 = 0.85V                           | 0       |

<sup>1</sup> See notes on [Spread Selection](#) table. B1[5] must be set to a 1 in order to use B1[4:3].

**SMBus Table: DIF Slew Rate Control Register**

| Byte 2 | Name             | Control Function         | Type | 0            | 1            | Default |
|--------|------------------|--------------------------|------|--------------|--------------|---------|
| Bit 7  | SLEWRATESEL DIF7 | Adjust Slew Rate of DIF7 | RW   | Slow Setting | Fast Setting | 1       |
| Bit 6  | SLEWRATESEL DIF6 | Adjust Slew Rate of DIF6 | RW   | Slow Setting | Fast Setting | 1       |
| Bit 5  | SLEWRATESEL DIF5 | Adjust Slew Rate of DIF5 | RW   | Slow Setting | Fast Setting | 1       |
| Bit 4  | SLEWRATESEL DIF4 | Adjust Slew Rate of DIF4 | RW   | Slow Setting | Fast Setting | 1       |
| Bit 3  | SLEWRATESEL DIF3 | Adjust Slew Rate of DIF3 | RW   | Slow Setting | Fast Setting | 1       |
| Bit 2  | SLEWRATESEL DIF2 | Adjust Slew Rate of DIF2 | RW   | Slow Setting | Fast Setting | 1       |
| Bit 1  | SLEWRATESEL DIF1 | Adjust Slew Rate of DIF1 | RW   | Slow Setting | Fast Setting | 1       |
| Bit 0  | SLEWRATESEL DIF0 | Adjust Slew Rate of DIF0 | RW   | Slow Setting | Fast Setting | 1       |

**Note:** See [DIF Low-Power HCSL Outputs](#) table for slew rates.



**SMBus Table: Nominal  $V_{HIGH}$  Amplitude Control / REF Control Register**

| Byte 3 | Name                    | Control Function           | Type | 0                          | 1                      | Default |
|--------|-------------------------|----------------------------|------|----------------------------|------------------------|---------|
| Bit 7  | REF                     | Slew Rate Control          | RW   | 00 = Slowest               | 01 = Slow              | 0       |
| Bit 6  |                         |                            | RW   | 10 = Fast                  | 11 = Fastest           | 1       |
| Bit 5  | REF Power Down Function | Wake-on-Lan Enable for REF | RW   | REF disabled in Power Down | REF runs in Power Down | 0       |
| Bit 4  | REF OE                  | REF Output Enable          | RW   | Disabled <sup>1</sup>      | Enabled                | 1       |
| Bit 3  | Reserved                |                            |      |                            |                        | X       |
| Bit 2  | Reserved                |                            |      |                            |                        | X       |
| Bit 1  | Reserved                |                            |      |                            |                        | X       |
| Bit 0  | Reserved                |                            |      |                            |                        | X       |

<sup>1</sup> The disabled state depends on Byte11[1:0]. '00' = Low, '01' = Hi-Z, '10' = Low, '11' = High.

**Byte 4 is Reserved.**

**SMBus Table: Revision and Vendor ID Register**

| Byte 5 | Name | Control Function | Type | 0            | 1 | Default |
|--------|------|------------------|------|--------------|---|---------|
| Bit 7  | RID3 | Revision ID      | R    | C rev = 0010 |   | 0       |
| Bit 6  | RID2 |                  | R    |              |   | 0       |
| Bit 5  | RID1 |                  | R    |              |   | 1       |
| Bit 4  | RID0 |                  | R    |              |   | 0       |
| Bit 3  | VID3 | VENDOR ID        | R    | 0001 = IDT   |   | 0       |
| Bit 2  | VID2 |                  | R    |              |   | 0       |
| Bit 1  | VID1 |                  | R    |              |   | 0       |
| Bit 0  | VID0 |                  | R    |              |   | 1       |

**SMBus Table: Device Type/Device ID**

| Byte 6 | Name         | Control Function | Type | 0  | 1 | Default |
|--------|--------------|------------------|------|--|---|---------|
| Bit 7  | Device Type1 | Device Type      | R    | 00 = FGx, 01 = DBx,<br>10 = DMx, 11 = DBx w/oPLL |   | 0       |
| Bit 6  | Device Type0 |                  | R    |  |   | 0       |
| Bit 5  | Device ID5   | Device ID        | R    | 0001000 binary or 08 hex                         |   | 0       |
| Bit 4  | Device ID4   |                  | R    |  |   | 0       |
| Bit 3  | Device ID3   |                  | R    |  |   | 1       |
| Bit 2  | Device ID2   |                  | R    |  |   | 0       |
| Bit 1  | Device ID1   |                  | R    |  |   | 0       |
| Bit 0  | Device ID0   |                  | R    |  |   | 0       |
|        |              |                  | R    |  |   | 0       |

**SMBus Table: Byte Count Register**

| Byte 7 | Name     | Control Function       | Type | 0   | 1 | Default |
|--------|----------|------------------------|------|---|---|---------|
| Bit 7  | Reserved |                        |      |   |   | X       |
| Bit 6  | Reserved |                        |      |   |   | X       |
| Bit 5  | Reserved |                        |      |   |   | X       |
| Bit 4  | BC4      | Byte count programming | RW   | Writing to this register will configure how many bytes will be read back, default is = 8 bytes. |   | 0       |
| Bit 3  | BC3      |                        | RW   |   |   | 1       |
| Bit 2  | BC2      |                        | RW   |   |   | 0       |
| Bit 1  | BC1      |                        | RW   |   |   | 0       |
| Bit 0  | BC0      |                        | RW   |   |   | 0       |

Bytes 8 and 9 are Reserved.

**SMBus Table: PLL MN Enable, PD\_Restore**

| Byte 10 | Name                    | Control Function             | Type | 0                  | 1                 | Default |
|---------|-------------------------|------------------------------|------|--------------------|-------------------|---------|
| Bit 7   | PLL M/N En <sup>1</sup> | M/N Programming Enable       | RW   | M/N Prog. Disabled | M/N Prog. Enabled | 0       |
| Bit 6   | Power-Down (PD) Restore | Restore Default Config in PD | RW   | Clear Config in PD | Keep Config in PD | 1       |
| Bit 5   | Reserved                |                              |      |                    |                   | X       |
| Bit 4   | Reserved                |                              |      |                    |                   | X       |
| Bit 3   | Reserved                |                              |      |                    |                   | X       |
| Bit 2   | Reserved                |                              |      |                    |                   | X       |
| Bit 1   | Reserved                |                              |      |                    |                   | X       |
| Bit 0   | Reserved                |                              |      |                    |                   | X       |

<sup>1</sup> This bit is a '1' on 9FGL0xP1 devices.

**SMBus Table: Stop State Control**

| Byte 11 | Name     | Control Function                         | Type | 0            | 1             | Default |
|---------|----------|--|------|--------------|---------------|---------|
| Bit 7   | Reserved |  |      |              |               | X       |
| Bit 6   | Reserved |  |      |              |               | X       |
| Bit 5   | Reserved |  |      |              |               | X       |
| Bit 4   | Reserved |  |      |              |               | X       |
| Bit 3   | Reserved |  |      |              |               | X       |
| Bit 2   | Reserved |  |      |              |               | X       |
| Bit 1   | STP[1]   | True/Complement DIF Output Disable State | RW   | 00 = Low/Low | 10 = High/Low | 0       |
| Bit 0   | STP[0]   |  | RW   | 01 = HiZ/HiZ | 11 = Low/High | 0       |

**SMBus Table: Impedance Control <sup>1</sup>**

| Byte 12 | Name        | Control Function | Type | 0   | 1 | Default  |
|---------|-------------|------------------|------|---|---|----------|
| Bit 7   | DIF3_imp[1] | DIF3 Zout        | RW   | 00 = 33Ω DIF Zout<br>01 = 85Ω DIF Zout<br>10 = 100Ω DIF Zout<br>11 = Reserved |   | See Note |
| Bit 6   | DIF3_imp[0] | DIF3 Zout        | RW   |   |   |          |
| Bit 5   | DIF2_imp[1] | DIF2 Zout        | RW   |   |   |          |
| Bit 4   | DIF2_imp[0] | DIF2 Zout        | RW   |   |   |          |
| Bit 3   | DIF1_imp[1] | DIF1 Zout        | RW   |   |   |          |
| Bit 2   | DIF1_imp[0] | DIF1 Zout        | RW   |   |   |          |
| Bit 1   | DIF0_imp[1] | DIF0 Zout        | RW   |   |   |          |
| Bit 0   | DIF0_imp[0] | DIF0 Zout        | RW   |   |   |          |

<sup>1</sup> Each output defaults to '10' for 9FGLxx41 and '01' for 9FGLxx51. Defaults for 9FGLxxP1 parts are programmable.

**SMBus Table: Impedance Control <sup>1</sup>**

| Byte 13 | Name        | Control Function | Type | 0   | 1 | Default  |
|---------|-------------|------------------|------|---|---|----------|
| Bit 7   | DIF7_imp[1] | DIF7 Zout        | RW   | 00 = 33Ω DIF Zout<br>01 = 85Ω DIF Zout<br>10 = 100Ω DIF Zout<br>11 = Reserved |   | See Note |
| Bit 6   | DIF7_imp[0] | DIF7 Zout        | RW   |   |   |          |
| Bit 5   | DIF6_imp[1] | DIF6 Zout        | RW   |   |   |          |
| Bit 4   | DIF6_imp[0] | DIF6 Zout        | RW   |   |   |          |
| Bit 3   | DIF5_imp[1] | DIF5 Zout        | RW   |   |   |          |
| Bit 2   | DIF5_imp[0] | DIF5 Zout        | RW   |   |   |          |
| Bit 1   | DIF4_imp[1] | DIF4 Zout        | RW   |   |   |          |
| Bit 0   | DIF4_imp[0] | DIF4 Zout        | RW   |   |   |          |

<sup>1</sup> Each output defaults to '10' for 9FGLxx41, and '01' for 9FGLxx51. Defaults for 9FGLxxP1 parts are programmable.

**SMBus Table: Pull-up Pull-down Control**

| Byte 14 | Name         | Control Function                               | Type | 0         | 1               | Default |
|---------|--------------|--|------|-----------|-----------------|---------|
| Bit 7   | OE3_pu/pd[1] | OE3 Pull-up (PuP)/<br>Pull-down (Pdwn) control | RW   | 00 = None | 10 = Pup        | 0       |
| Bit 6   | OE3_pu/pd[0] |  | RW   | 01=Pdwn   | 11 = Pup + Pdwn | 1       |
| Bit 5   | OE2_pu/pd[1] | OE2 Pull-up (PuP)/<br>Pull-down (Pdwn) control | RW   | 00 = None | 10 = Pup        | 0       |
| Bit 4   | OE2_pu/pd[0] |  | RW   | 01=Pdwn   | 11 = Pup + Pdwn | 1       |
| Bit 3   | OE1_pu/pd[1] | OE1 Pull-up (PuP)/<br>Pull-down (Pdwn) control | RW   | 00 = None | 10 = Pup        | 0       |
| Bit 2   | OE1_pu/pd[0] |  | RW   | 01=Pdwn   | 11 = Pup + Pdwn | 1       |
| Bit 1   | OE0_pu/pd[1] | OE0 Pull-up (PuP)/<br>Pull-down (Pdwn) control | RW   | 00 = None | 10 = Pup        | 0       |
| Bit 0   | OE0_pu/pd[0] |  | RW   | 01 = Pdwn | 11 = Pup + Pdwn | 1       |

**SMBus Table: Pull-up Pull-down Control**

| Byte 15 | Name         | Control Function                                | Type | 0          | 1                | Default |
|---------|--------------|---|------|------------|------------------|---------|
| Bit 7   | OE7_pu/pd[1] | OE7 Pull-up (PuP)/<br>Pull-down (Pdown) control | RW   | 00 = None  | 10 = Pup         | 0       |
| Bit 6   | OE7_pu/pd[0] |   | RW   | 01=Pdown   | 11 = Pup + Pdown | 1       |
| Bit 5   | OE6_pu/pd[1] | OE6 Pull-up (PuP)/<br>Pull-down (Pdown) control | RW   | 00 = None  | 10 = Pup         | 0       |
| Bit 4   | OE6_pu/pd[0] |   | RW   | 01=Pdown   | 11 = Pup + Pdown | 1       |
| Bit 3   | OE5_pu/pd[1] | OE5 Pull-up (PuP)/<br>Pull-down (Pdown) control | RW   | 00 = None  | 10 = Pup         | 0       |
| Bit 2   | OE5_pu/pd[0] |   | RW   | 01=Pdown   | 11 = Pup + Pdown | 1       |
| Bit 1   | OE4_pu/pd[1] | OE4 Pull-up (PuP)/<br>Pull-down (Pdown) control | RW   | 00 = None  | 10 = Pup         | 0       |
| Bit 0   | OE4_pu/pd[0] |   | RW   | 01 = Pdown | 11 = Pup + Pdown | 1       |

**SMBus Table: Pull-up Pull-down Control**

| Byte 16 | Name                | Control Function                                       | Type | 0          | 1                | Default |
|---------|---------------------|--|------|------------|------------------|---------|
| Bit 7   | Reserved            |  |      |            |                  | X       |
| Bit 6   | Reserved            |  |      |            |                  | X       |
| Bit 5   | Reserved            |  |      |            |                  | X       |
| Bit 4   | Reserved            |  |      |            |                  | X       |
| Bit 3   | Reserved            |  |      |            |                  | X       |
| Bit 2   | Reserved            |  |      |            |                  | X       |
| Bit 1   | CKPWRGD_PD_pu/pd[1] | CKPWRGD_PD Pull-up (PuP)/<br>Pull-down (Pdown) control | RW   | 00 = None  | 10 = Pup         | 1       |
| Bit 0   | CKPWRGD_PD_pu/pd[0] |  | RW   | 01 = Pdown | 11 = Pup + Pdown | 0       |

Byte 17 is Reserved.

**SMBus Table: Polarity Control**

| Byte 18 | Name         | Control Function  | Type | 0                | 1                 | Default |
|---------|--------------|-------------------|------|------------------|-------------------|---------|
| Bit 7   | OE7_polarity | Sets OE7 polarity | RW   | Enabled when Low | Enabled when High | 0       |
| Bit 6   | OE6_polarity | Sets OE6 polarity | RW   | Enabled when Low | Enabled when High | 0       |
| Bit 5   | OE5_polarity | Sets OE5 polarity | RW   | Enabled when Low | Enabled when High | 0       |
| Bit 4   | OE4_polarity | Sets OE4 polarity | RW   | Enabled when Low | Enabled when High | 0       |
| Bit 3   | OE3_polarity | Sets OE3 polarity | RW   | Enabled when Low | Enabled when High | 0       |
| Bit 2   | OE2_polarity | Sets OE2 polarity | RW   | Enabled when Low | Enabled when High | 0       |
| Bit 1   | OE1_polarity | Sets OE1 polarity | RW   | Enabled when Low | Enabled when High | 0       |
| Bit 0   | OE0_polarity | Sets OE0 polarity | RW   | Enabled when Low | Enabled when High | 0       |

**SMBus Table: Polarity Control**

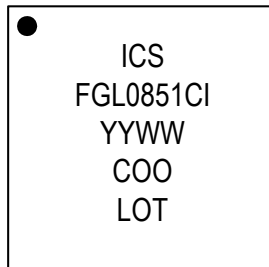
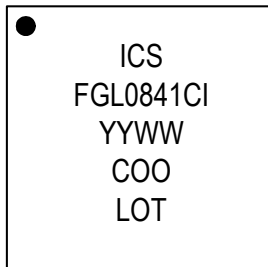
| Byte 19 | Name       | Control Function               | Type | 0                   | 1                    | Default |
|---------|------------|--------------------------------|------|---------------------|----------------------|---------|
| Bit 7   | Reserved   |                                |      |                     |                      | X       |
| Bit 6   | Reserved   |                                |      |                     |                      | X       |
| Bit 5   | Reserved   |                                |      |                     |                      | X       |
| Bit 4   | Reserved   |                                |      |                     |                      | X       |
| Bit 3   | Reserved   |                                |      |                     |                      | X       |
| Bit 2   | Reserved   |                                |      |                     |                      | X       |
| Bit 1   | Reserved   |                                |      |                     |                      | X       |
| Bit 0   | CKPWRGD_PD | Determines CKPWRGD_PD polarity | RW   | Power-down when Low | Power-down when High | 0       |

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

[www.idt.com/document/psc/48-vfqfpn-package-outline-drawing-60-x-60-x-090-mm-body-epad-42-x-42-mm-040mm-pitch-ndg48p2](http://www.idt.com/document/psc/48-vfqfpn-package-outline-drawing-60-x-60-x-090-mm-body-epad-42-x-42-mm-040mm-pitch-ndg48p2)

## Marking Diagrams



1. Lines 1 and 2: truncated part number
2. "I" denotes industrial temperature range.
3. "YYWW" is the last two digits of the year and the week the part was assembled.
4. "COO" denotes country of origin.
5. "LOT" denotes the lot number.

## Ordering Information

Table 18. Ordering Information

| Orderable Part Number | Package                         | Carrier Type | Temperature   | Output Impedance |
|-----------------------|---------------------------------|--------------|---------------|------------------|
| 9FGL0841CKILF         | 6 × 6 mm, 0.4mm pitch 48-VFQFPN | Trays        | -40° to +85°C | 100Ω             |
| 9FGL0841CKILFT        | 6 × 6 mm, 0.4mm pitch 48-VFQFPN | Reel         | -40° to +85°C |                  |
| 9FGL0851CKILF         | 6 × 6 mm, 0.4mm pitch 48-VFQFPN | Trays        | -40° to +85°C | 85Ω              |
| 9FGL0851CKILFT        | 6 × 6 mm, 0.4mm pitch 48-VFQFPN | Reel         | -40° to +85°C |                  |

"LF" denotes Pb-free configuration, RoHS compliant.

"C" is the device revision designator (will not correlate with the datasheet revision)

## Revision History

| Revision Date      | Description of Change  |
|--------------------|--|
| September 17, 2018 | Updated typical and maximum values for Phase Jitter, -0.5% spread. |
| August 31, 2018    | Initial release.   |



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