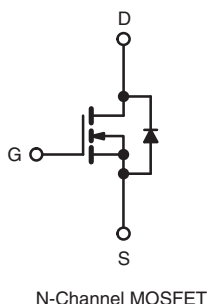
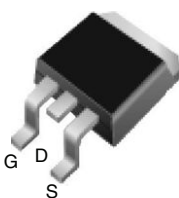


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	200	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	1.5
Q_g (Max.) (nC)	8.2	
Q_{gs} (nC)	1.8	
Q_{gd} (nC)	4.5	
Configuration	Single	

D²PAK (TO-263)



FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF610S-GE3	SiHF610STRL-GE3 ^a	SiHF610STRR-GE3 ^a
Lead (Pb)-free	IRF610SPbF	IRF610STRLPbF ^a	IRF610STRRPbF ^a
	SiHF610S-E3	SiHF610STL-E3 ^a	SiHF610STR-E3 ^a

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	200	V
Gate-Source Voltage			V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	3.3	A
		T _C = 100 °C		2.1	
Pulsed Drain Current ^a			I _{DM}	10	W/°C
Linear Derating Factor				0.29	
Linear Derating Factor (PCB Mount) ^e				0.025	
Single Pulse Avalanche Energy ^b			E _{AS}	64	mJ
Repetitive Avalanche Current ^a			I _{AR}	3.3	A
Repetitive Avalanche Energy ^a			E _{AR}	3.6	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	36	W
Maximum Power Dissipation (PCB Mount) ^e	T _A = 25 °C			3.0	
Peak Diode Recovery dV/dt ^c			dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50$ V, starting $T_J = 25^\circ\text{C}$, $L = 8.8$ mH, $R_g = 25\ \Omega$, $I_{AS} = 3.3$ A (see fig. 12).
- $I_{SD} \leq 3.3$ A, $dI/dt \leq 70$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) ^c	R_{thJA}	-	-	40	°C/W
Maximum Junction-to-Ambient	R_{thJA}	-	-	62	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	3.5	

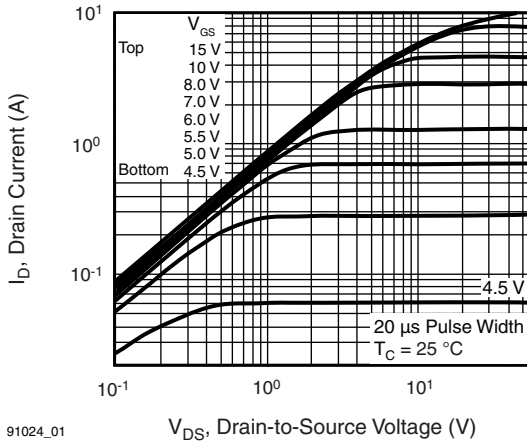
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		200	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.30	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 160V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 2.0 A ^b	-	-	1.5	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 2.0 A ^b		0.80	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	140	-	pF
Output Capacitance	C _{oss}			-	53	-	
Reverse Transfer Capacitance	C _{rss}			-	15	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 3.3 A, V _{DS} = 160 V see fig. 6 and 13 ^b	-	-	8.2	nC
Gate-Source Charge	Q _{gs}			-	-	1.8	
Gate-Drain Charge	Q _{gd}			-	-	4.5	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 100 V, I _D = 3.3 A, R _g = 24 Ω, R _D = 30 Ω, see fig. 10 ^b		-	8.2	-	ns
Rise Time	t _r			-	17	-	
Turn-Off Delay Time	t _{d(off)}			-	14	-	
Fall Time	t _f			-	8.9	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	3.3	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	10	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 3.3 A, V _{GS} = 0 V ^b		-	-	2.0	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 3.3 A, di/dt = 100 A/μs ^b		-	150	310	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.60	1.4	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

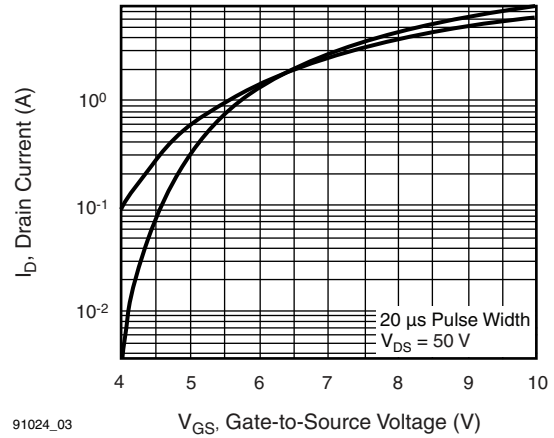
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
c. When mounted on 1" square PCB (FR-4 or G-10 material).

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



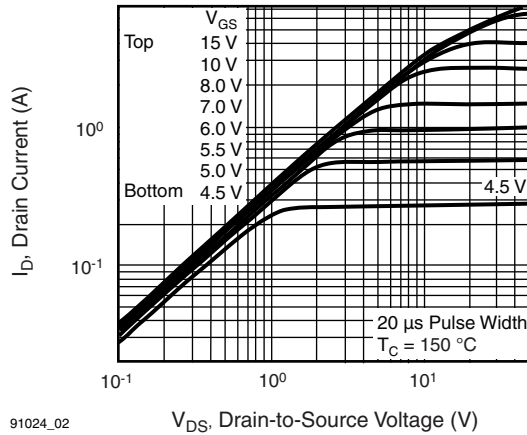
91024_01

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$



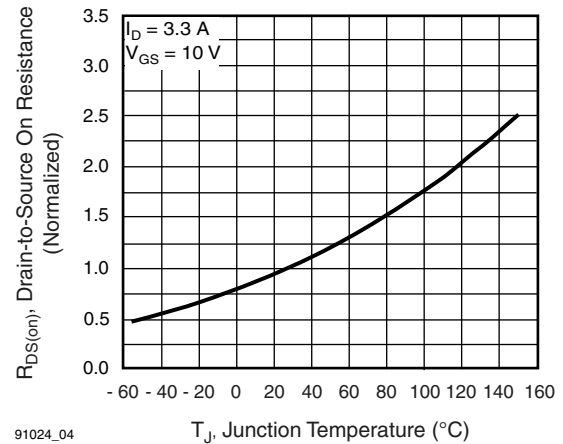
91024_03

Fig. 3 - Typical Transfer Characteristics



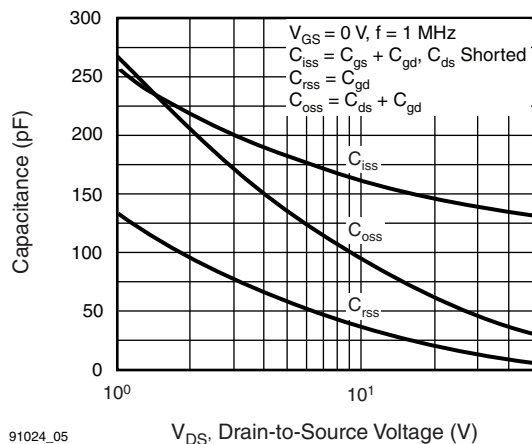
91024_02

Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

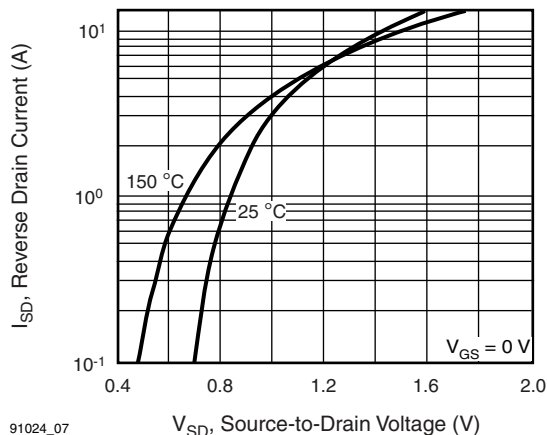


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Fig. 4 - Normalized On-Resistance vs. Temperature



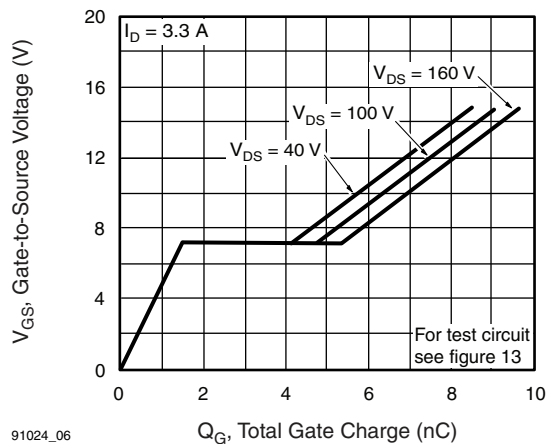
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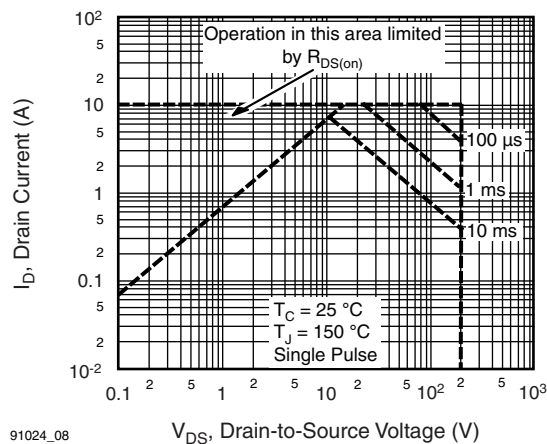
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage



91024_06



91024_08

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area

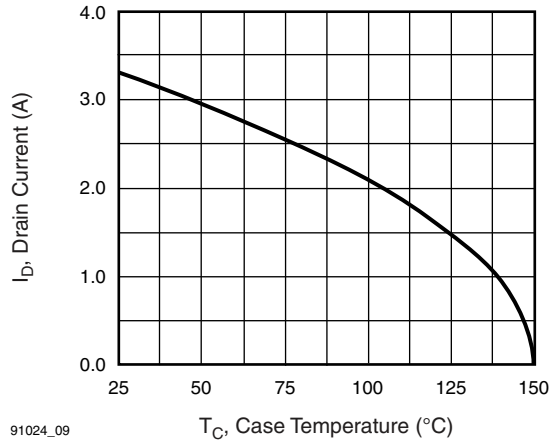


Fig. 9 - Maximum Drain Current vs. Case Temperature

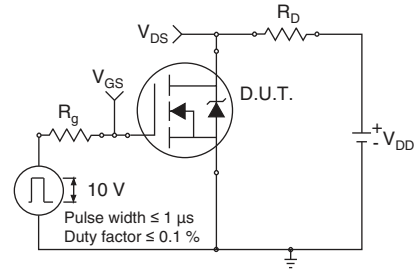


Fig. 10a - Switching Time Test Circuit

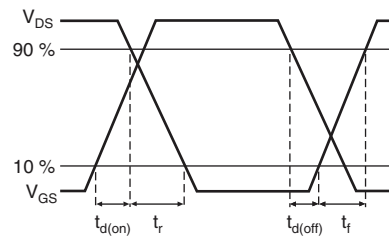


Fig. 10b - Switching Time Waveforms

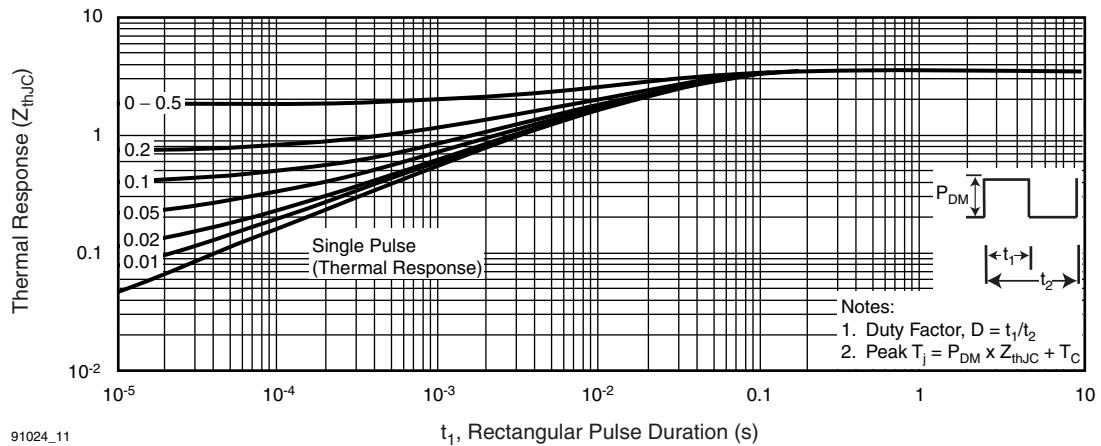


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

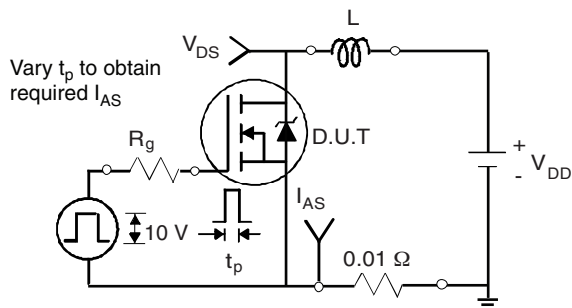


Fig. 12a - Unclamped Inductive Test Circuit

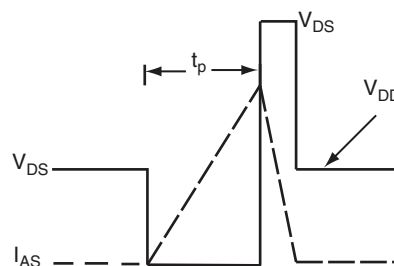


Fig. 12b - Unclamped Inductive Waveforms

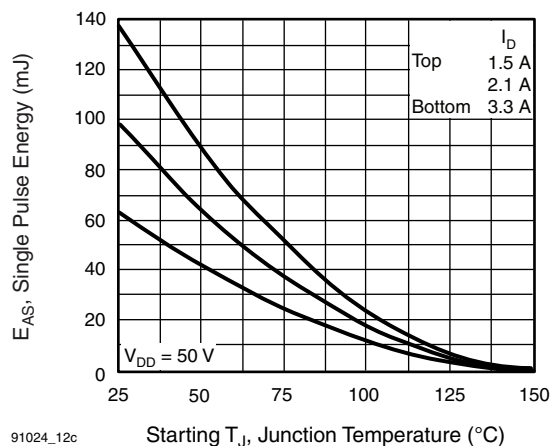


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

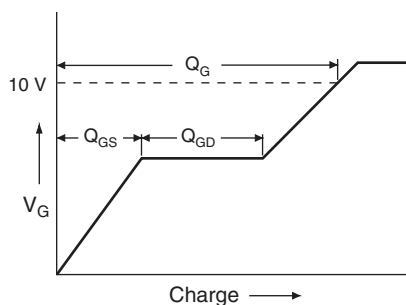


Fig. 13a - Basic Gate Charge Waveform

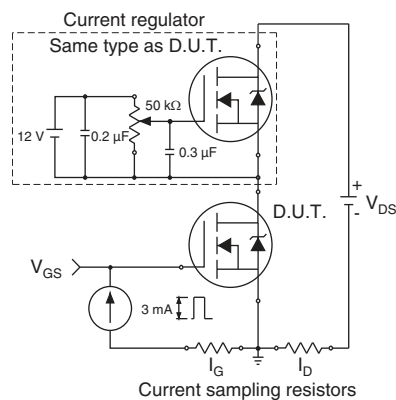
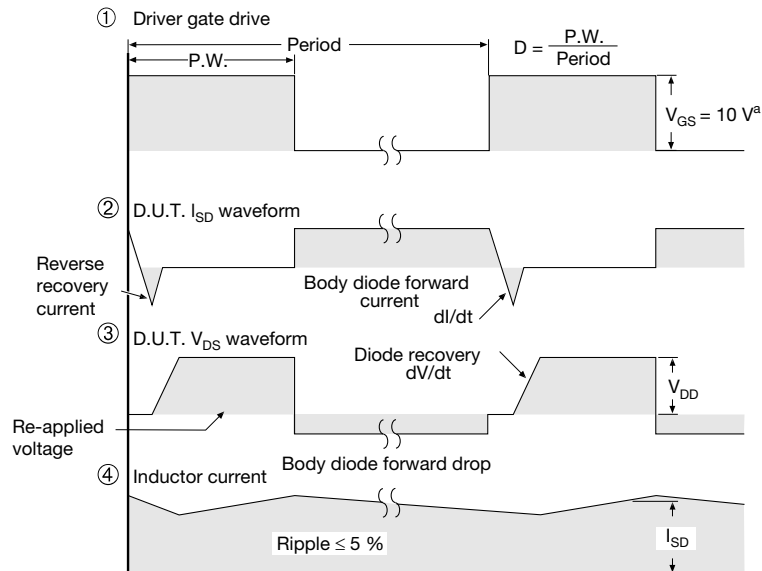
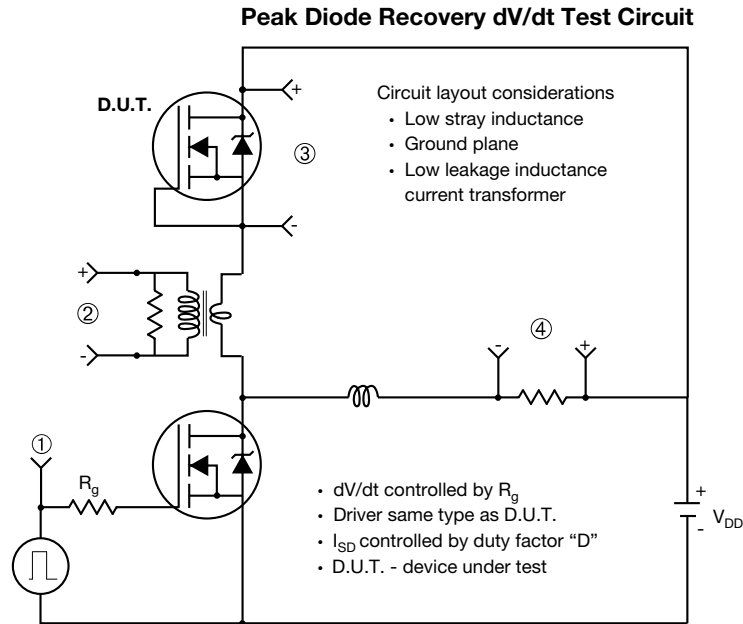


Fig. 13b - Gate Charge Test Circuit



Note

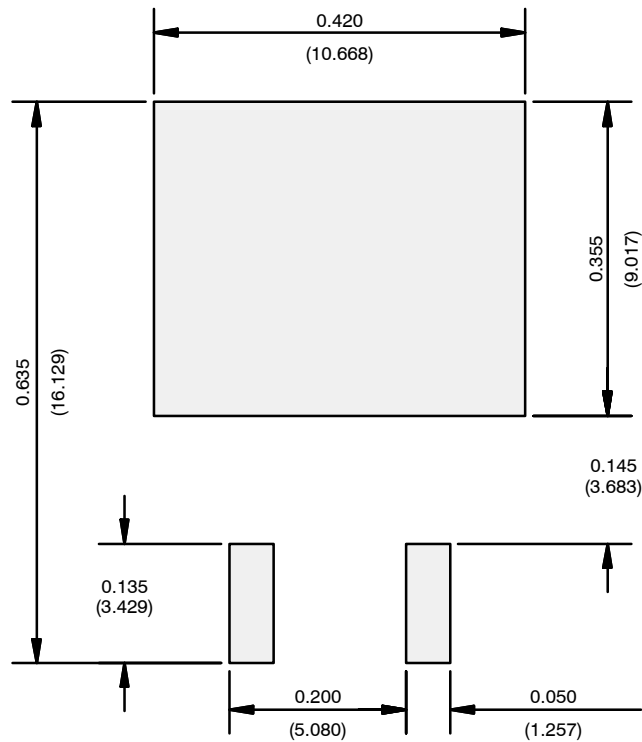
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А