ISL78302A

Dual LDO with Low Noise, Very High PSRR and Low IQ

FN7932
Rev 2.00
December 22, 2015

ISL78302A is a high-performance dual LDO capable of sourcing 300mA current from each output. It has a low standby current and very high PSRR and is stable with output capacitance of 1µF to 10µF with ESR of up to 200mΩ.

The device integrates an individual Power-On Reset (POR) function for each output. The POR delay for VO2 can be externally programmed by connecting a timing capacitor to the CPOR pin. The POR delay for VO1 is internally fixed at approximately 2ms. A reference bypass pin is also provided for connecting a noise-filtering capacitor for low noise and high-PSRR applications.

The quiescent current is typically only 47µA with both LDOs enabled and active. Separate Enable pins control each individual LDO output. When both Enable pins are low, the device is in shutdown, typically drawing less than 0.3µA.

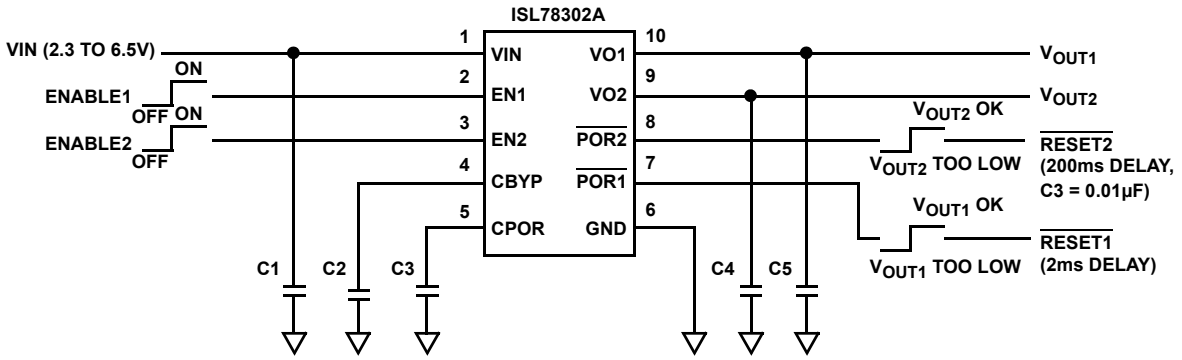
The ISL78302A is AEC-Q100 qualified. The ISL78302A is rated for the automotive temperature range (-40°C to +105°C).

Features

- Integrates Two 300mA High-performance LDOs
- Excellent Transient Response to Large Current Steps
- ±1.8% Accuracy Over All Operating Conditions
- Excellent Load Regulation: < 0.1% Voltage Change Across Full Range of Load Current
- Low Output Noise: Typically 30µV_{RMS} at 100µA (1.5V)
- Very High PSRR: 90dB at 1kHz
- Extremely Low Quiescent Current: 47µA (Both LDOs Active)
- Wide Input Voltage Capability: 2.3V to 6.5V
- Low Dropout Voltage: Typically 230mV at 300mA
- Stable with 1µF to 10µF Ceramic Capacitors
- Separate Enable and POR Pins for Each LDO
- Soft-start and Staged Turn-on to Limit Input Current Surge During Enable
- Current Limit and Overheat Protection
- Tiny 10 Ld 3mmx3mm DFN Package
- -40°C to +105°C Operating Temperature Range
- Pb-free (RoHS Compliant)
- AEC-Q100 Qualified

Applications

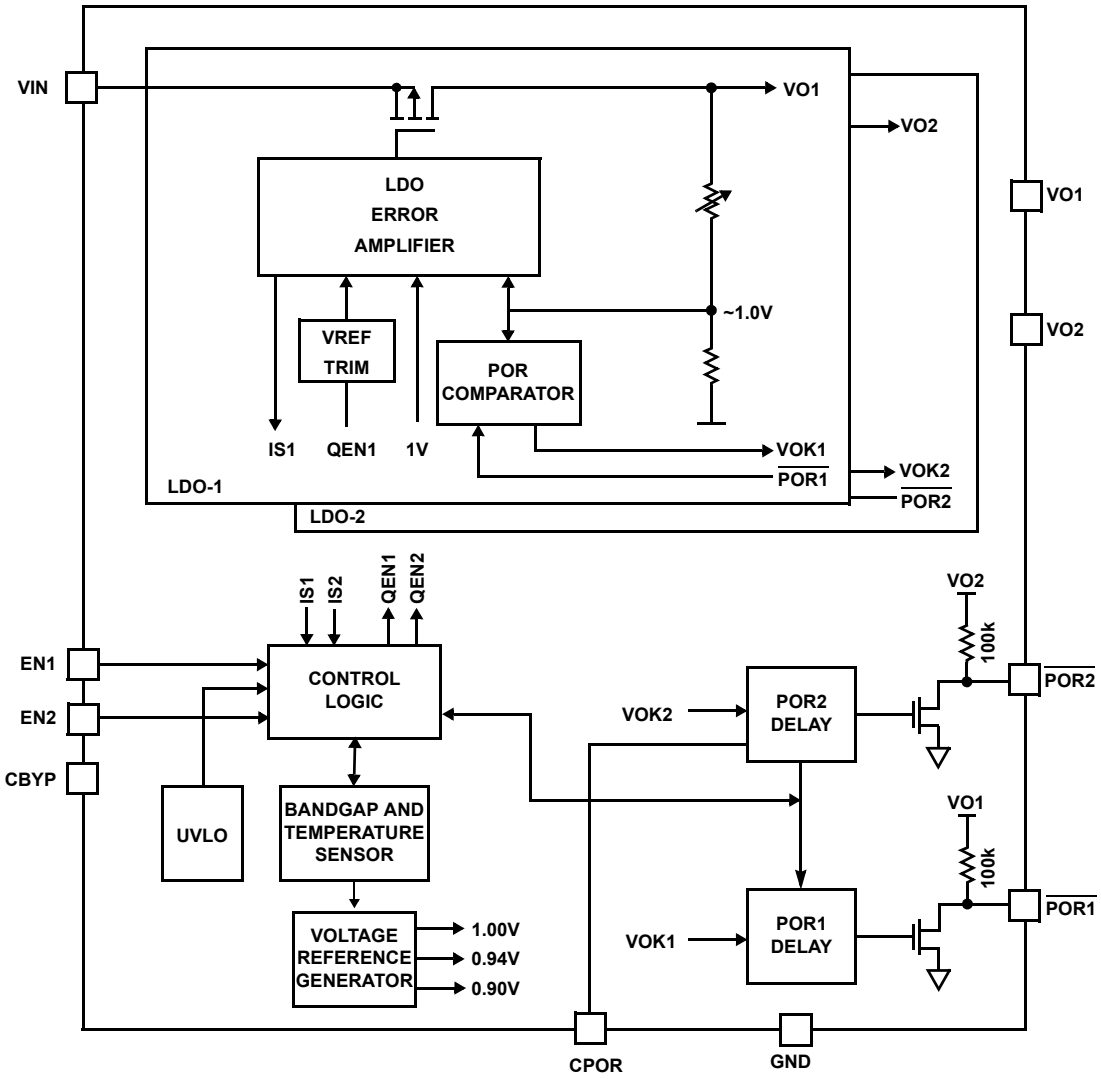
- Radio Receivers
- Camera Modules
- GPS/Navigation
- Infotainment Systems



C1, C4, C5: 1µF X5R CERAMIC CAPACITOR
C2: 0.1µF X7R CERAMIC CAPACITOR
C3: 0.01µF X7R CERAMIC CAPACITOR

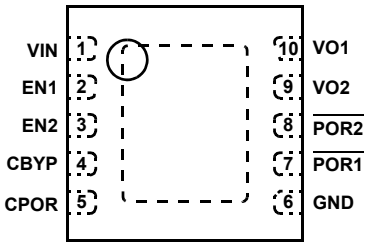
FIGURE 1. TYPICAL APPLICATION

Block Diagram



Pin Configuration

ISL78302A
(10 LD 3X3 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VIN	Analog I/O	Supply Voltage/LDO Input. Connect a 1µF capacitor to GND.
2	EN1	Low Voltage Compatible CMOS Input	LDO-1 Enable
3	EN2	Low Voltage Compatible CMOS Input	LDO-2 Enable
4	CBYP	Analog I/O	Reference Bypass Capacitor Pin. Optionally connect capacitor of value 0.01µF to 1µF between this pin and GND to tune in the desired noise and PSRR performance.
5	CPOR	Analog I/O	POR2 Delay Setting Capacitor Pin. Connect a capacitor between this pin and GND to delay the $\overline{POR2}$ output release after LDO-2 output reaches 94% of its specified voltage level (200ms delay per 0.01µF).
6	GND	Ground	Connection to system ground. Connect to PCB Ground plane.
7	$\overline{POR1}$	Open Drain Output (1mA)	Open-drain POR Output for LDO-1 (active-low). Internally connected to VO1 through 100kΩ resistor.
8	$\overline{POR2}$	Open Drain Output (1mA)	Open-drain POR Output for LDO-2 (active-low). Internally connected to VO2 through 100kΩ resistor.
9	VO2	Analog I/O	LDO-2 Output. Connect capacitor of value 1µF to 10µF to GND (1µF recommended).
10	VO1	Analog I/O	LDO-1 Output. Connect capacitor of value 1µF to 10µF to GND (1µF recommended).

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	VO1 VOLTAGE (V)	VO2 VOLTAGE (V)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG DWG. #
ISL78302AARMMZ	DNAL	3.0	3.0	-40 to +105	10 Ld 3x3 DFN	L10.3x3C
ISL78302AARLLZ	DNAM	2.9	2.9	-40 to +105	10 Ld 3x3 DFN	L10.3x3C
ISL78302AARJMZ	DNAN	2.8	3.0	-40 to +105	10 Ld 3x3 DFN	L10.3x3C
ISL78302AARJRZ	DNAP	2.8	2.6	-40 to +105	10 Ld 3x3 DFN	L10.3x3C
ISL78302AARJCZ	DNAK	2.8	1.8	-40 to +105	10 Ld 3x3 DFN	L10.3x3C
ISL78302AARGCZ	DNAR	2.7	1.8	-40 to +105	10 Ld 3x3 DFN	L10.3x3C
ISL78302AARPLZ	DNAS	1.85	2.9	-40 to +105	10 Ld 3x3 DFN	L10.3x3C
ISL78302AARBJZ	DNAT	1.5	2.8	-40 to +105	10 Ld 3x3 DFN	L10.3x3C

NOTES:

1. Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78302A. For more information on MSL, please see Tech Brief TB363.

Absolute Maximum Ratings

Supply Voltage (V_{IN}) . . . . . +7.1V
V_O1, V_O2 Pins . . . . . +3.6V
All Other Pins . . . . . -0.3 to (V_{IN} + 0.3)V

ESD Ratings

Human Body Model (Tested per JESD22-A114E) 3000V
Machine Model (Tested per JESD-A115-A) 200V
Charge Device Model (Tested per AEC-Q100-011) 1500V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package (Notes 4, 5)	59	18.5

Junction Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -40°C to +105°C
Operating Temperature Range . . . . . -40°C to +105°C
Supply Voltage (VIN) . . . . . 2.3V to 6.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: T_A = -40°C to 105°C; V_{IN} = (V_O + 0.5V) to 6.5V with a minimum V_{IN} of 2.3V; C_{IN} = 1µF; C_O = 1µF; C_{BYP} = 0.01µF; C_{POR} = 0.01µF. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
DC CHARACTERISTICS						
Supply Voltage	V_{IN}		**2.3**		**6.5**	V
Ground Current		Quiescent condition: I_{O1} = 0µA; I_{O2} = 0µA				
	I_{DD1}	One LDO active		30	**36**	µA
	I_{DD2}	Both LDO active		47	**55**	µA
Shutdown Current	I_{DDS}			0.3	**2.1**	µA
UVLO Threshold	V_{UV+}		**1.9**	2.1	**2.3**	V
	V_{UV-}		**1.6**	1.8	**2.0**	V
Regulation Voltage Accuracy		V_{IN} = V_O + 0.5V to 5.5V, I_O = 10µA to 300mA, T_J = +25°C	**-0.8**		**+0.8**	%
		V_{IN} = V_O + 0.5V to 5.5V, I_O = 10µA to 300mA, T_J = -40°C to +125°C	**-1.8**		**+1.8**	%
Maximum Output Current	I_{MAX}	Continuous	**300**			mA
Internal Current Limit	I_{LIM}		**320**	475	**650**	mA
Dropout Voltage (Note 7)	V_{DO1}	I_O = 300mA; V_O < 2.5V		450		mV
		I_O = 150mA; V_O < 2.5V		225	**250**	
	V_{DO2}	I_O = 300mA; 2.5V ≤ V_O ≤ 2.8V		250		mV
		I_O = 150mA; 2.5V ≤ V_O ≤ 2.8V		125	**160**	mV
	V_{DO3}	I_O = 300mA; V_O > 2.8V		230		mV
		I_O = 150mA; V_O > 2.8V		115	**145**	mV
Thermal Shutdown Temperature	T_{SD+}			145		°C
	T_{SD-}			110		°C
AC CHARACTERISTICS						
Ripple Rejection		I_O = 10mA, V_{IN} = 2.8V(min), V_O = 1.8V, C_{BYP} = 0.1µF				
		@ 1kHz		90		dB
		@ 10kHz		70		dB
		@ 100kHz		50		dB

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: T_A = -40°C to 105°C; V_{IN} = (V_O + 0.5V) to 6.5V with a minimum V_{IN} of 2.3V; C_{IN} = 1µF; C_O = 1µF; C_{BYP} = 0.01µF; C_{POR} = 0.01µF. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued) (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Output Noise Voltage		I_O = 100µA, V_O = 1.5V, T_A = +25°C, C_{BYP} = 0.1µF BW = 10Hz to 100kHz		30		$µV_{RMS}$
DEVICE START-UP CHARACTERISTICS						
Device Enable Time	t_{EN}	Time from assertion of the ENx pin to when the output voltage reaches 95% of the VO (nom)		250	**500**	µs
LDO Soft-Start Ramp Rate	t_{SSR}	Slope of linear portion of LDO output voltage ramp during start-up		30	**60**	µs/V
EN1, EN2 PIN CHARACTERISTICS						
Input Low Voltage	V_{IL}		**-0.3**		**0.5**	V
Input High Voltage	V_{IH}		**1.35**		**V_{IN} + 0.3**	V
Input Leakage Current	I_{IL}, I_{IH}				**0.1**	µA
Pin Capacitance	C_{PIN}	Informative		5		pF
$\overline{POR1}$, $\overline{POR2}$ PIN CHARACTERISTICS						
$\overline{POR1}$, $\overline{POR2}$ Thresholds	V_{POR+}	As a percentage of nominal output voltage	**91**	94	**97**	%
	V_{POR-}		**87**	90	**93**	%
$\overline{POR1}$ Delay	t_{P1LH}		**0.5**	2.0	**3.2**	ms
	t_{P1HL}			25		µs
$\overline{POR2}$ Delay	t_{P2LH}	C_{POR} = 0.01µF	**100**	200	**300**	ms
	t_{P2HL}			25		µs
$\overline{POR1}$, $\overline{POR2}$ Pin Output Low Voltage	V_{OL}	@ I_{OL} = 1.0mA			**0.2**	V
$\overline{POR1}$, $\overline{POR2}$ Pin Internal Pull-Up Resistance	R_{POR}		**78**	100	**180**	kΩ

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. VOx = 0.98*VOx(NOM); valid for VOx greater than 1.85V.

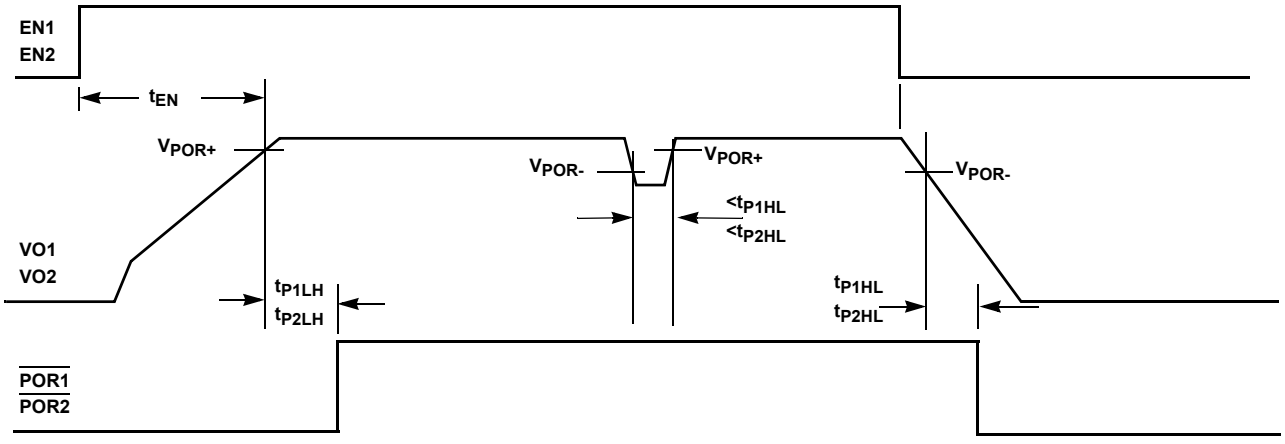


FIGURE 2. TIMING PARAMETER DEFINITION

Typical Performance Curves

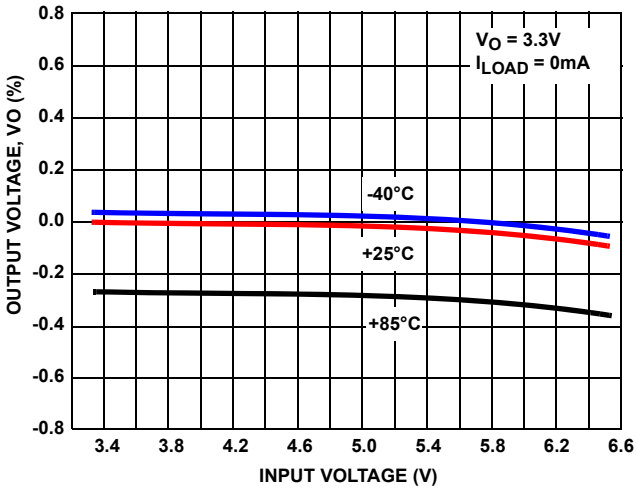


FIGURE 3. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

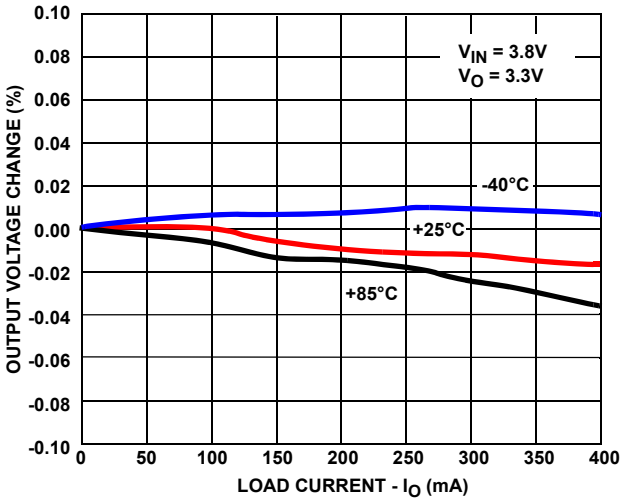


FIGURE 4. OUTPUT VOLTAGE CHANGE vs LOAD CURRENT

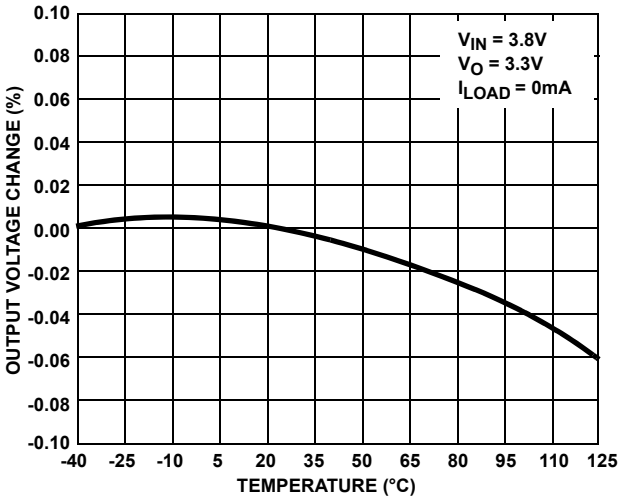


FIGURE 5. OUTPUT VOLTAGE CHANGE vs TEMPERATURE

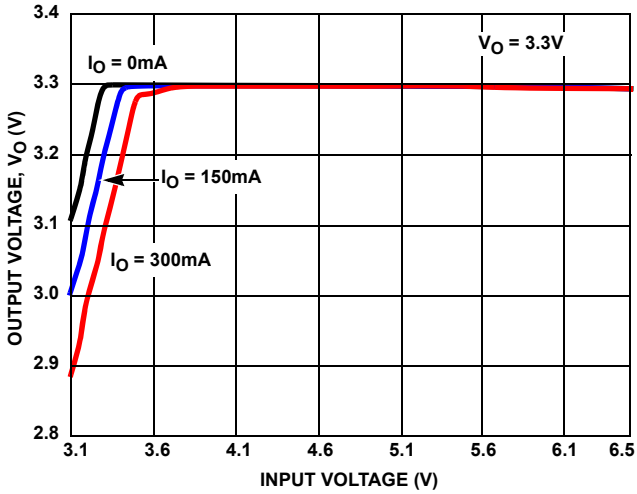


FIGURE 6. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

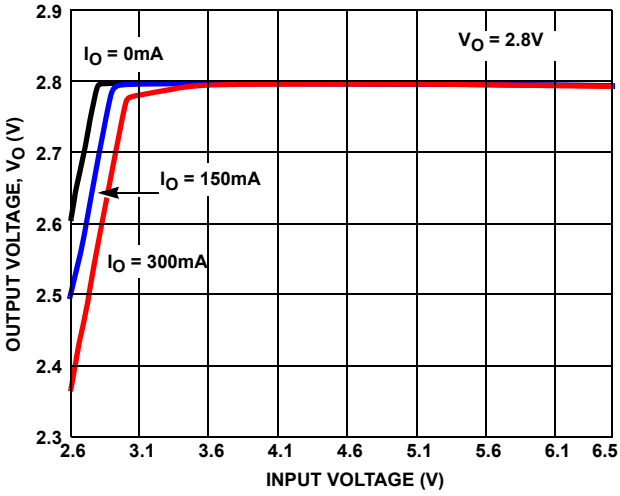


FIGURE 7. OUTPUT VOLTAGE vs INPUT VOLTAGE (2.8V OUTPUT)

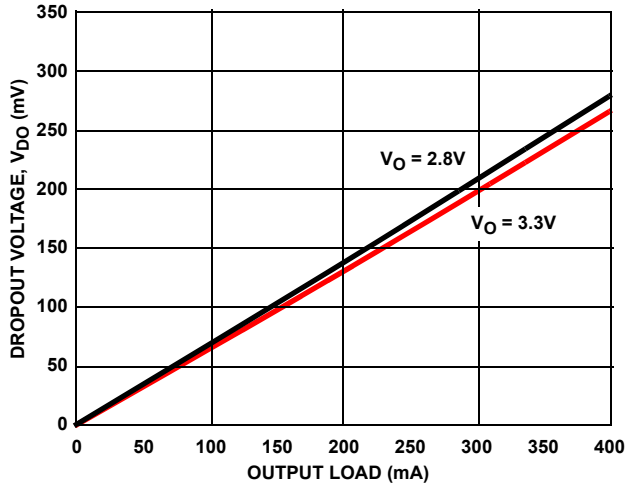


FIGURE 8. DROPOUT VOLTAGE vs LOAD CURRENT

Typical Performance Curves (Continued)

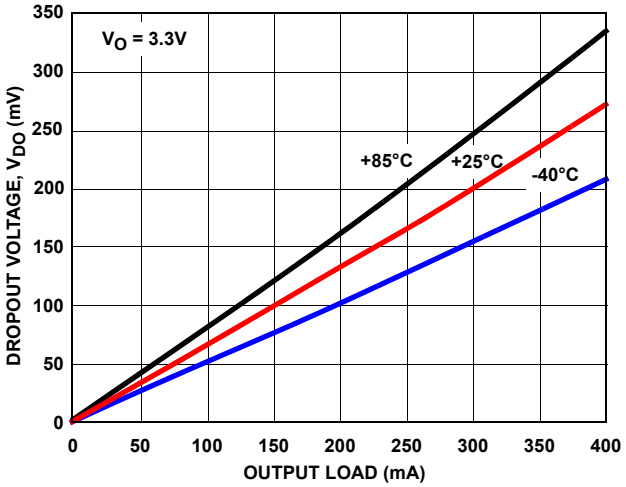


FIGURE 9. DROPOUT VOLTAGE vs LOAD CURRENT

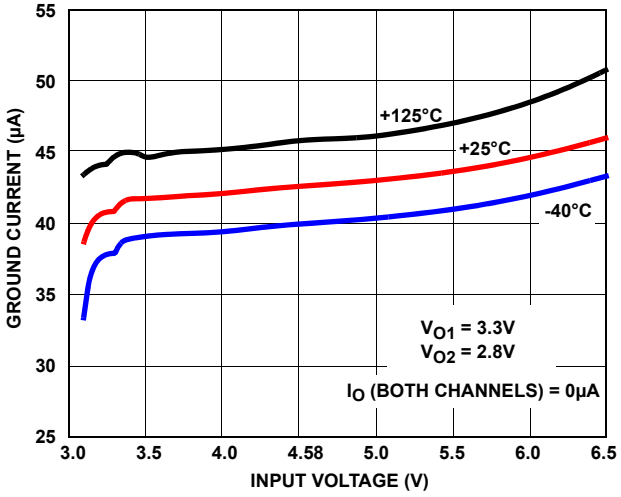


FIGURE 10. GROUND CURRENT vs INPUT VOLTAGE

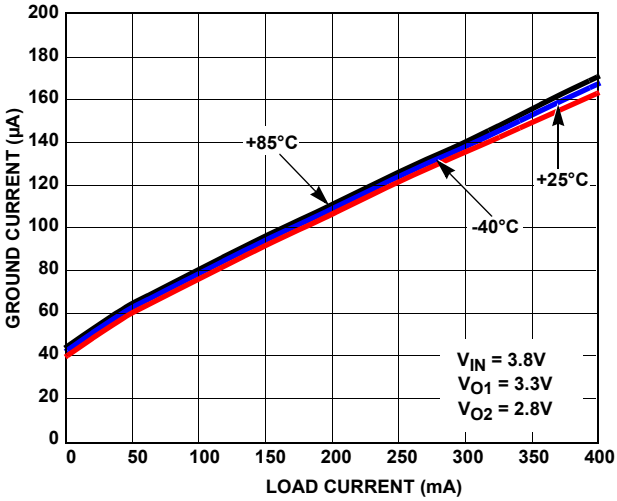


FIGURE 11. GROUND CURRENT vs LOAD

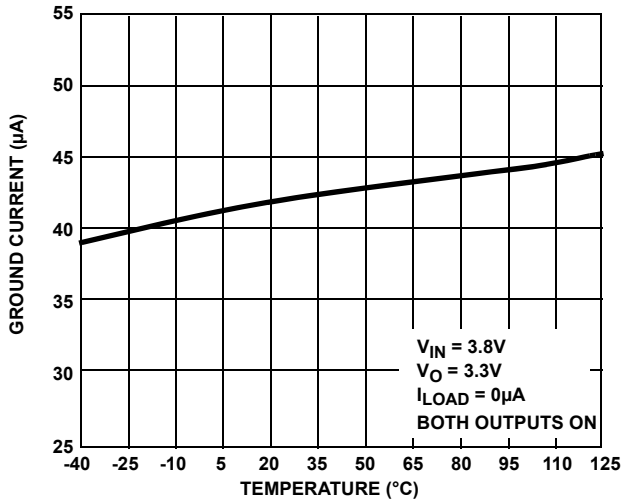


FIGURE 12. GROUND CURRENT vs TEMPERATURE

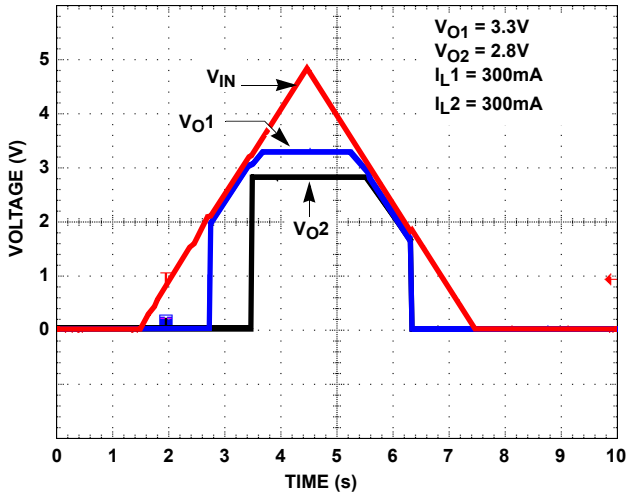


FIGURE 13. POWER-UP/POWER-DOWN

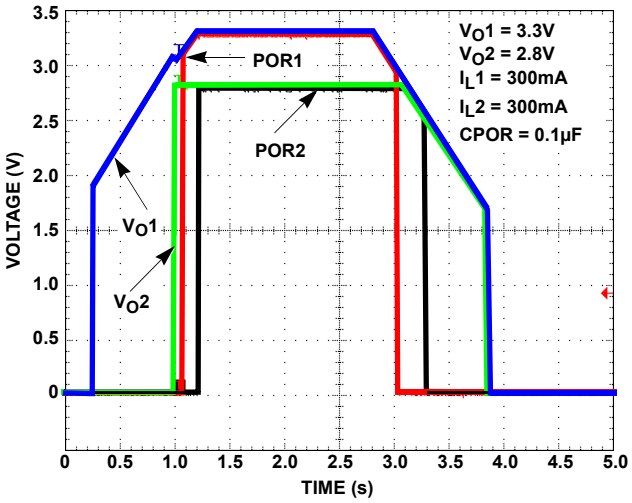


FIGURE 14. POWER-UP/POWER-DOWN WITH POR SIGNALS

Typical Performance Curves (Continued)

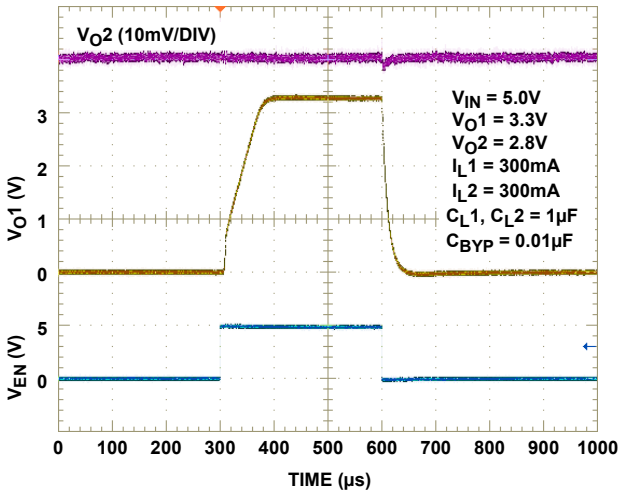


FIGURE 15. TURN-ON/TURN-OFF RESPONSE

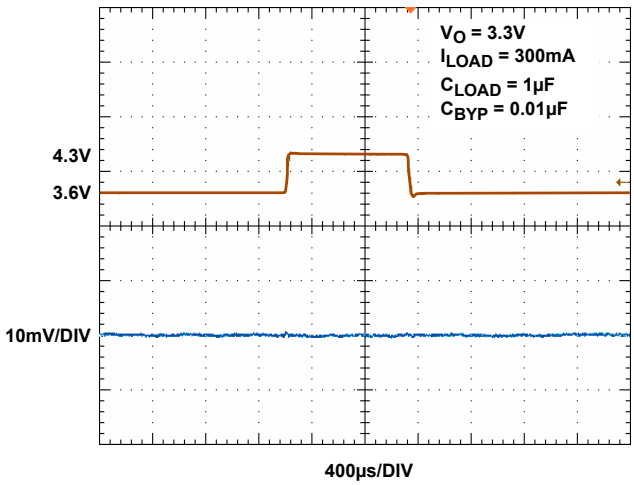


FIGURE 16. LINE TRANSIENT RESPONSE (3.3V OUTPUT)

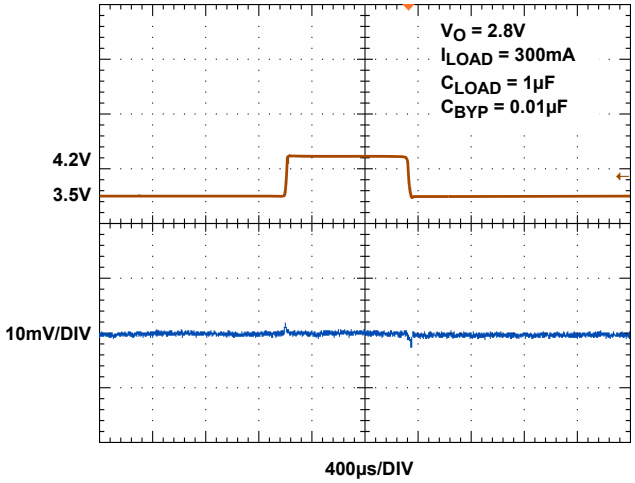


FIGURE 17. LINE TRANSIENT RESPONSE (2.8V OUTPUT)

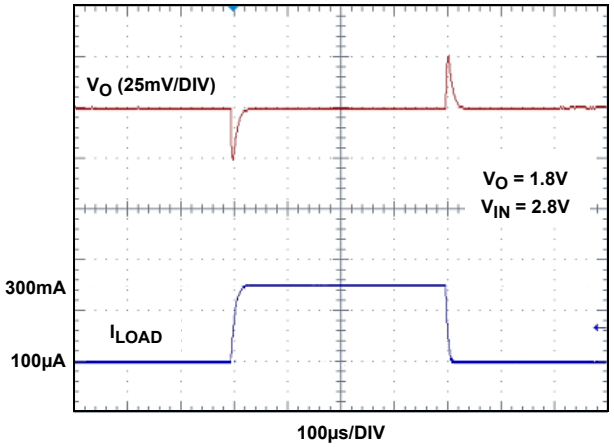


FIGURE 18. LOAD TRANSIENT RESPONSE

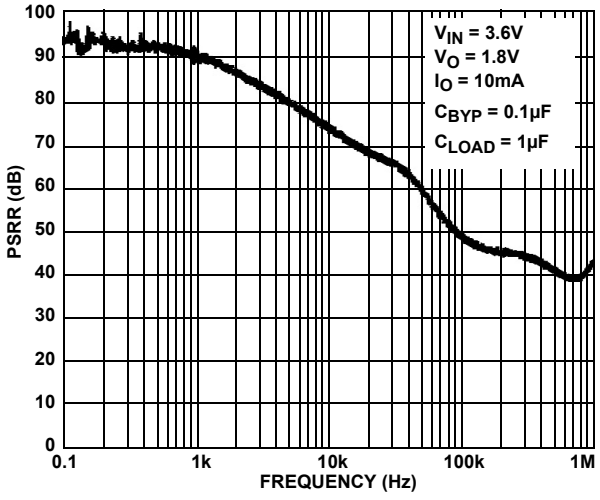


FIGURE 19. PSRR vs FREQUENCY

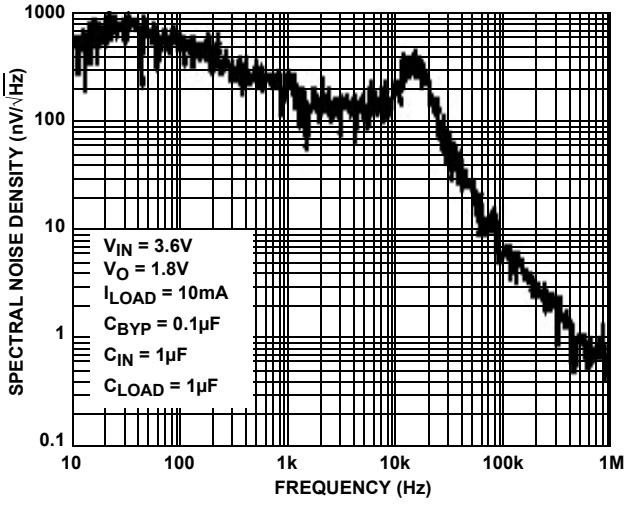


FIGURE 20. SPECTRAL NOISE DENSITY vs FREQUENCY

Functional Description

The ISL78302A contains two high-performance LDOs. High performance is achieved through a circuit that delivers fast transient response to varying load conditions. In a quiescent condition, the ISL78302A adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, smart thermal shutdown protection, staged turn-on, and soft-start. Smart thermal shutdown protects the device against overheating. Staged turn-on and soft-start minimize start-up input current surges without causing excessive device turn-on time.

Power Control

The ISL78302A has two separate enable pins (EN1 and EN2) to individually control power to each of the LDO outputs. When both EN1 and EN2 are low, the device is in shutdown mode. During this condition, all on-chip circuits are off, and the device draws minimum current, typically less than 0.3µA.

When one or both of the enable pins are asserted, the device first polls the output of the UVLO detector to ensure that VIN voltage is at least about 2.1V. Once verified, the device initiates a start-up sequence. During the start-up sequence, trim settings are first read and latched. Then, sequentially, the bandgap, reference voltage, and current generation circuitry power up. Once the references are stable, a fast-start circuit quickly charges the external reference bypass capacitor (connected to the CBYP pin) to the proper operating voltage. After the bypass capacitor has been charged, the LDOs power up in their specified sequence.

Soft-start circuitry integrated into each LDO limits the initial ramp-up rate to about 30µs/V to minimize current surge.

If EN1 is brought high, and EN2 goes high before the VO1 output stabilizes, the ISL78302A delays the VO2 turn-on until the VO1 output reaches its target level.

If EN2 is brought high, and EN1 goes high before VO2 starts its output ramp, then VO1 turns on first, and the ISL78302A delays the VO2 turn-on until the VO1 output reaches its target level.

If EN2 is brought high, and EN1 goes high after VO2 starts its output ramp, then the ISL78302A immediately starts to ramp up the VO1 output.

If both EN1 and EN2 are brought high at the same time, the VO1 output has priority, and is always powered up first.

During operation, whenever the VIN voltage drops below about 1.8V, the ISL78302A immediately disables both LDO outputs. When VIN rises back above 2.1V, the device re-initiates its start-up sequence, and LDO operation resumes automatically.

Reference Generation

The reference generation circuitry includes a trimmed bandgap, a trimmed voltage reference divider, a trimmed current reference generator, and an RC noise filter. The filter includes the external capacitor connected to the CBYP pin. A 0.01µF capacitor connected to CBYP implements a 100Hz lowpass filter and is recommended for most high-performance applications. For the lowest noise application, a 0.1µF or greater CBYP capacitor should be used. This filters the reference noise below the 10Hz to 1kHz frequency band, which is crucial in many noise-sensitive applications.

The bandgap generates a zero temperature coefficient (TC) voltage for the reference divider. The reference divider provides the regulation reference, POR detection thresholds, and other voltage references required for current generation and over-temperature detection.

The current generator provides the references required for adaptive biasing as well as references for LDO output current limit and thermal shutdown determination.

LDO Regulation and Programmable Output Divider

The LDO regulator is implemented with a high-gain operational amplifier driving a PMOS pass transistor. The design of the ISL78302A provides a regulator that has low quiescent current, fast transient response, and overall stability across all operating and load current conditions. LDO stability is guaranteed for a 1µF to 10µF output capacitor that has a tolerance better than 20% and ESR less than 200mΩ. The design is performance-optimized for a 1µF capacitor. Unless limited by the application, use of an output capacitor value above 4.7µF is not normally needed as LDO performance improvement is minimal.

Each LDO uses an independently trimmed 1V reference. An internal resistor divider drops the LDO output voltage down to 1V. This is compared to the 1V reference for regulation.

Power-On Reset Generation

Each LDO has a separate power-on reset (POR) signal generation circuit that outputs to the respective $\overline{\text{POR}}$ pins. The POR signal is generated as follows.

A POR comparator continuously monitors the output of each LDO. The LDO enters a power-good state when the output voltage is above 94% of the expected output voltage for a period exceeding the LDO PGOOD entry delay time. In the power-good state, the open-drain $\overline{\text{PORx}}$ output is in a high-impedance state. An internal 100kΩ pull-up resistor pulls the pin up to the respective LDO output voltage. An external resistor can be added between the $\overline{\text{PORx}}$ output and the LDO output for a faster rise time; however, the $\overline{\text{PORx}}$ output should not connect through an external resistor to a supply greater than the associated LDO voltage.

For the 1.5V regulated output option, it has been found that the internal pull-ups on POR output does not always function correctly above V_{IN} = 6V. For this reason, it is recommended to use an external 100kΩ pull-up resistor for the POR pin that is associated to the 1.5V output. For outputs higher than 1.5V, no external resistor is required over the full input range from 2.3V to 6.5V.

The power-good state is exited when the LDO output falls below 90% of the expected output voltage for a period longer than the PGOOD exit delay time. While power-good is false, the ISL78302A pulls the respective $\overline{\text{POR}}$ pin low.

For LDO-1, the PGOOD entry delay time is fixed at about 2ms while the PGOOD exit delay is about 25µs. For LDO-2, the PGOOD entry and exit delays are determined by the value of the external capacitor connected to the CPOR pin. For a 0.01µF capacitor, the

entry and exit delays are 200ms and 25µs, respectively. Larger or smaller capacitor values yield proportionately longer or shorter delay times. The POR exit delay should never be allowed to be less than 10µs to ensure sufficient immunity against transient induced false POR triggering.

Overheat Detection

The bandgap provides a proportional-to-temperature current that is indicative of the temperature of the silicon. This current is compared with references to determine if the device is in danger of damage due to overheating. When the die temperature reaches about +145°C, one or both of the LDOs momentarily shuts down until the die cools sufficiently. In the overheat condition, only the LDO sourcing more than 50mA is shut off. This does not affect the operation of the other LDO. If both LDOs source more than 50mA and an overheat condition occurs, both LDO outputs are disabled. Once the die temperature falls back below about +110°C, the disabled LDOs are re-enabled, and soft-start automatically takes place.

The ISL78302A provides short-circuit protection by limiting the output current to about 475mA. If short circuited, an output current of 475mA will cause die heating. If the short circuit lasts long enough, the overheat detection circuit will turn off the output.

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 22, 2015	FN7932.2	On page 4, updated Charged Device Model test method from “JESD22-C101C” to “AEC-Q100-011”. Updated POD L10.3x3C to current version with changes as follows: Removed package outline and included center to center distance between lands on recommended land pattern. Removed Note 4 “Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.” since it is not applicable to this package. Renumbered notes accordingly. Tiebar Note 4 updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
December 23, 2013	FN7932.1	Page 10 - 2nd line of the disclaimer changed from: "Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted" to: "Intersil Automotive Qualified products are manufactured, assembled and tested utilizing TS16949 quality systems as noted"
May 21, 2012	FN7932.0	Initial Release

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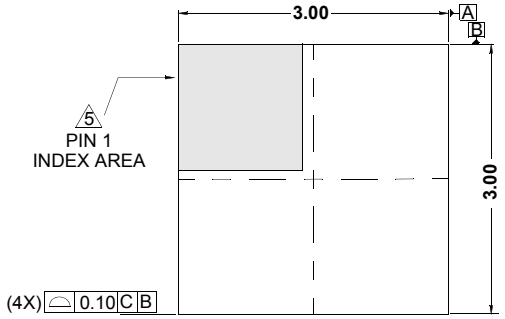
Package Outline Drawing

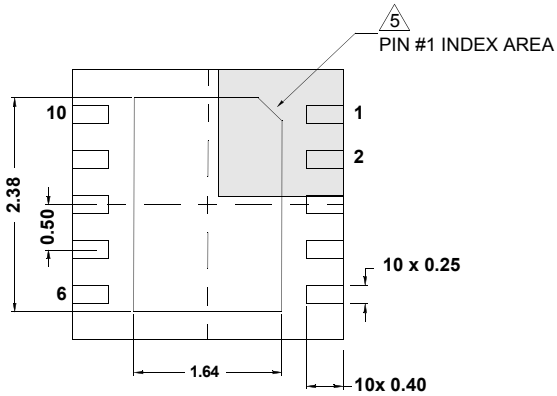
L10.3x3C

10 LEAD DUAL FLAT PACKAGE (DFN)

Rev 4, 3/15

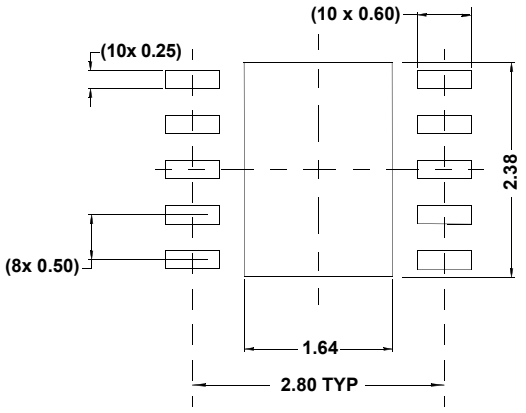


TOP VIEW

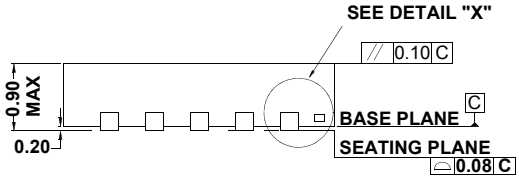


BOTTOM VIEW

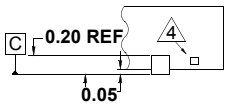
(4X) 0.10 M C B



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Compliant to JEDEC MO-229-WEED-3 except for E-PAD dimensions.

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