80960SA
EMBEDDED 32-BIT MICROPROCESSOR WITH 16-BIT BURST DATA BUS

- **High-Performance Embedded Architecture**
  - **— 20 MIPS* Burst Execution at 20 MHz**
  - **— 7.5 MIPS Sustained Execution at 20 MHz**
- **512-Byte On-Chip Instruction Cache**
  - **— Direct Mapped**
  - **— Parallel Load/Decode for Uncached Instructions**
- **Multiple Register Sets**
  - **— Sixteen Global 32-Bit Registers**
  - **— Sixteen Local 32-Bit Registers**
  - **— Four Local Register Sets Stored On-Chip**
  - **— Register Scoreboarding**
- **Pin Compatible with 80960SB**
- **Built-in Interrupt Controller**
  - **— 4 Direct Interrupt Pins**
  - **— 31 Priority Levels, 256 Vectors**
- **Easy to Use, High Bandwidth 16-Bit Bus**
  - **— 32 Mbytes/s Burst**
  - **— Up to 16 Bytes Transferred per Burst**
- **32-Bit Address Space, 4 Gigabytes**
- **80-Lead Quad Flat Pack (EIAJ QFP)**
  - **— 84-Lead Plastic Leaded Chip Carrier (PLCC)**
- **Software Compatible with 80960KA/KB/CA/CF Processors**

The 80960SA is a member of Intel's i960® 32-bit processor family, which is designed especially for low cost embedded applications. It includes a 512-byte instruction cache and a built-in interrupt controller. The 80960SA has a large register set, multiple parallel execution units and a 16-bit burst bus. Using advanced RISC technology, this high performance processor is capable of execution rates in excess of 7.5 million instructions per second*. The 80960SA is well-suited for a wide range of cost sensitive embedded applications including non-impact printers, network adapters and I/O controllers.

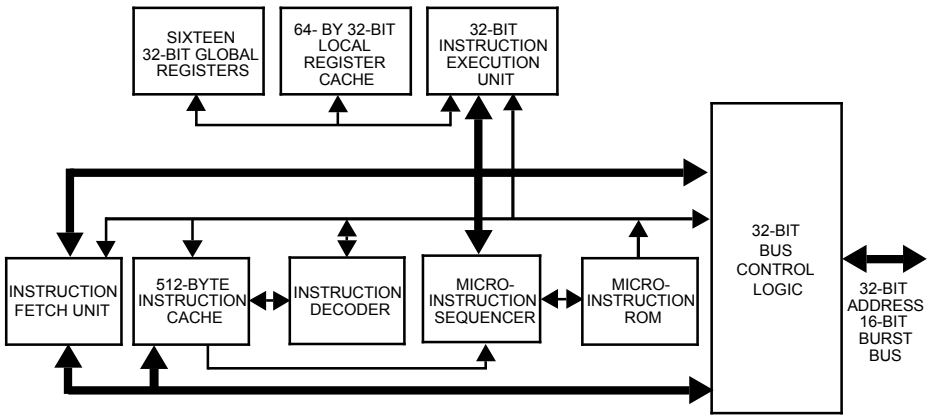


Figure 1. The 80960SA Processor's Highly Parallel Architecture

* Relative to Digital Equipment Corporation's VAX-11/780 at 1 MIPS (VAX-11™ is a trademark of Digital Equipment Corporation)

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1.0 THE i960® PROCESSOR

The 80960SA is a member of the 32-bit architecture from Intel known as the i960 processor family. These microprocessors were especially designed to serve the needs of embedded applications. The embedded market includes applications as diverse as industrial automation, avionics, image processing, graphics and networking. These types of applications require high integration, low power consumption, quick interrupt response times and high performance. Since time to market is critical, embedded microprocessors need to be easy to use in both hardware and software designs.

All members of the i960 processor family share a common core architecture which utilizes RISC technology so that, except for special functions, the family members are object-code compatible. Each new processor in the family adds its own special set of functions to the core to satisfy the needs of a specific application or range of applications in the embedded market.

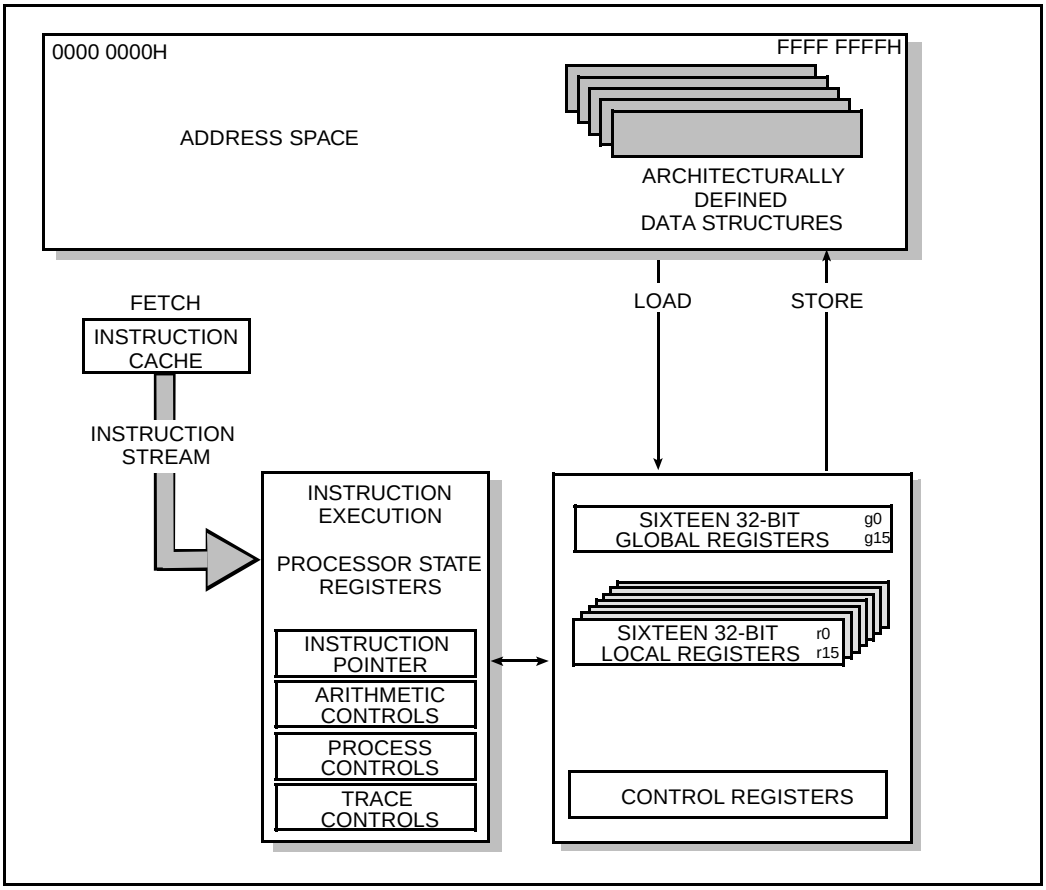


Figure 2. 80960SA Programming Environment

1.1 Key Performance Features

The 80960SA architecture is based on the most recent advances in microprocessor technology and is grounded in Intel's long experience in the design and manufacture of embedded microprocessors. Many features contribute to the 80960SA's exceptional performance:

1. **Large Register Set.** Having a large number of registers reduces the number of times that a processor needs to access memory. Modern compilers can take advantage of this feature to optimize execution speed. For maximum flexibility, the 80960SA provides thirty-two 32-bit registers. (See Figure 2.)
2. **Fast Instruction Execution.** Simple functions make up the bulk of instructions in most programs so that execution speed can be improved by ensuring that these core instructions are executed as quickly as possible. The most frequently executed instructions — such as register-register moves, add/subtract, logical operations and shifts — execute in one to two cycles. (Table 1 contains a list of instructions.)
3. **Load/Store Architecture.** One way to improve execution speed is to reduce the number of times that the processor must access memory to perform an operation. As with other processors based on RISC technology, the 80960SA has a Load/Store architecture. As such, only the LOAD and STORE instructions reference memory; all other instructions operate on registers. This type of architecture simplifies instruction decoding and is used in combination with other techniques to increase parallelism.
4. **Simple Instruction Formats.** All instructions in the 80960SA are 32 bits long and must be aligned on word boundaries. This alignment makes it possible to eliminate the instruction alignment stage in the pipeline. To simplify the instruction decoder, there are only five instruction formats; each instruction uses only one format. (See Figure 3.)
5. **Overlapped Instruction Execution.** Load operations allow execution of subsequent instructions to continue before the data has been returned from memory, so that these instructions can overlap the load. The 80960SA manages this process transparently to software through the use of a register scoreboard. Conditional instructions also make use of a scoreboard so that subsequent unrelated instructions may be executed while the conditional instruction is pending.
6. **Integer Execution Optimization.** When the result of an arithmetic execution is used as an operand in a subsequent calculation, the value is sent immediately to its destination register. At the same time, the value is put on a bypass path to the ALU, thereby saving the time that otherwise would be required to retrieve the value for the next operation.
7. **Bandwidth Optimizations.** The 80960SA gets optimal use of its memory bus bandwidth because the bus is tuned for use with the on-chip instruction cache: instruction cache line size matches the maximum burst size for instruction fetches. The 80960SA automatically fetches four words in a burst and stores them directly in the cache. Due to the size of the cache and the fact that it is continually filled in anticipation of needed instructions in the program flow, the 80960SA is relatively insensitive to memory wait states. The benefit is that the 80960SA delivers outstanding performance even with a low cost memory system.
8. **Cache Bypass.** If a cache miss occurs, the processor fetches the needed instruction then sends it on to the instruction decoder at the same time it updates the cache. Thus, no extra time is spent to load and read the cache.

Table 1. 80960SA Instruction Set

Data Movement	Arithmetic	Logical	Bit and Bit Field
Load	Add	And	Set Bit
Store	Subtract	Not And	Clear Bit
Move	Multiply	And Not	Not Bit
Load Address	Divide	Or	Check Bit
	Remainder	Exclusive Or	Alter Bit
	Modulo	Not Or	Scan For Bit
	Shift	Or Not	Scan Over Bit
	Extended Multiply	Nor	Extract
	Extended Divide	Exclusive Nor	Modify
		Not	
		Nand	
		Rotate	
Comparison	**Branch**	**Call/Return**	**Fault**
Compare	Unconditional Branch	Call	Conditional Fault
Conditional Compare	Conditional Branch	Call Extended	Synchronize Faults
Compare and Increment	Compare and Branch	Call System	
Compare and Decrement		Return	
		Branch and Link	
Debug	**Miscellaneous**	**Decimal**	
Modify Trace Controls	Atomic Add	Move	
Mark	Atomic Modify	Add with Carry	
Force Mark	Flush Local Registers	Subtract with Carry	
	Modify Arithmetic Controls		
	Scan Byte for Equal		
	Test Condition Code		
Synchronous			
Synchronous Load			
Synchronous Move			

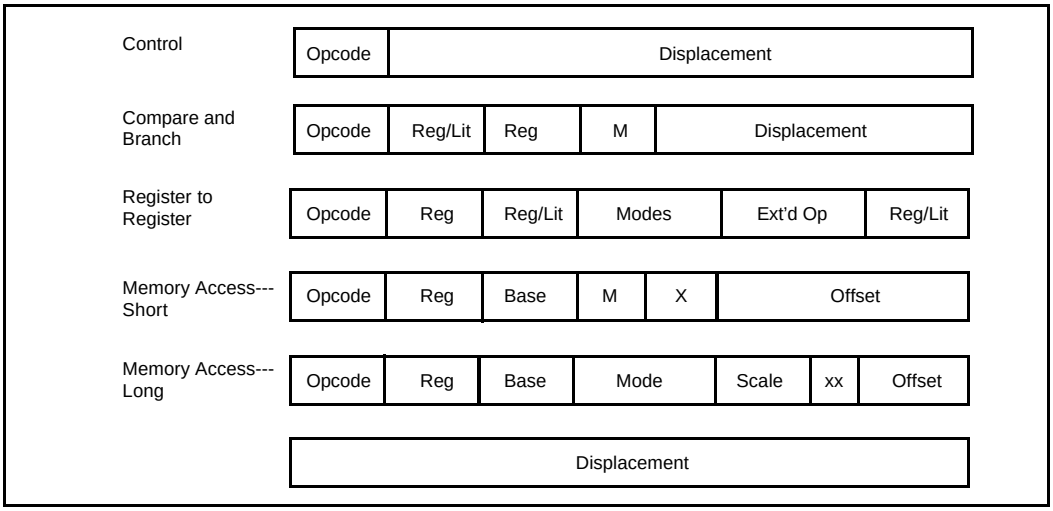


Figure 3. Instruction Formats

1.1.1 Memory Space And Addressing Modes

The 80960SA offers a linear programming environment so that all programs running on the processor are contained in a single address space. Maximum address space size is 4 Gigabytes (2^{32} bytes).

For ease of use the 80960SA has a small number of addressing modes, but includes all those necessary to ensure efficient execution of high-level languages such as C. Table 2 lists the memory addressing modes.

Table 2. Memory Addressing Modes

- 12-Bit Offset
- 32-Bit Offset
- Register-Indirect
- Register + 12-Bit Offset
- Register + 32-Bit Offset
- Register + (Index-Register x Scale-Factor)
- Register x Scale Factor + 32-Bit Displacement
- Register + (Index-Register x Scale-Factor) + 32-Bit Displacement

Scale-Factor is 1, 2, 4, 8 or 16

1.1.2 Data Types

The 80960SA recognizes the following data types:

Numeric:

- 8-, 16-, 32- and 64-bit ordinals
- 8-, 16-, 32- and 64-bit integers

Non-Numeric:

- Bit
- Bit Field
- Triple Word (96 bits)
- Quad-Word (128 bits)

1.1.3 Large Register Set

The 80960SA programming environment includes a large number of registers. In fact, 32 registers are available at any time. The availability of this many registers greatly reduces the number of memory accesses required to perform algorithms, which leads to greater instruction processing speed.

There are two types of general-purpose register: local and global. The global registers consist of sixteen 32-bit registers (g0 though g15). These registers perform the same function as the general-

purpose registers provided in other popular microprocessors. The term global refers to the fact that these registers retain their contents across procedure calls.

The local registers, on the other hand, are procedure specific. For each procedure call, the 80960SA allocates 16 local registers (r0 through r15). Each local register is 32 bits wide.

1.1.4 Multiple Register Sets

To further increase the efficiency of the register set, multiple sets of local registers are stored on-chip (See Figure 4). This cache holds up to four local register frames, which means that up to three procedure calls can be made without having to access the procedure stack resident in memory.

Although programs may have procedure calls nested many calls deep, a program typically oscillates back and forth between only two to three levels. As a result, with four stack frames in the cache, the probability of having a free frame available on the cache when a call is made is very high. In fact, runs of representative C-language programs show that 80% of the calls are handled without needing to access memory.

If four or more procedures are active and a new procedure is called, the 80960SA moves the oldest local register set in the stack-frame cache to a procedure stack in memory to make room for a new set of registers. Global register g15 is the frame pointer (FP) to the procedure stack.

Global registers are not exchanged on a procedure call, but retain their contents, making them available to all procedures for fast parameter passing.

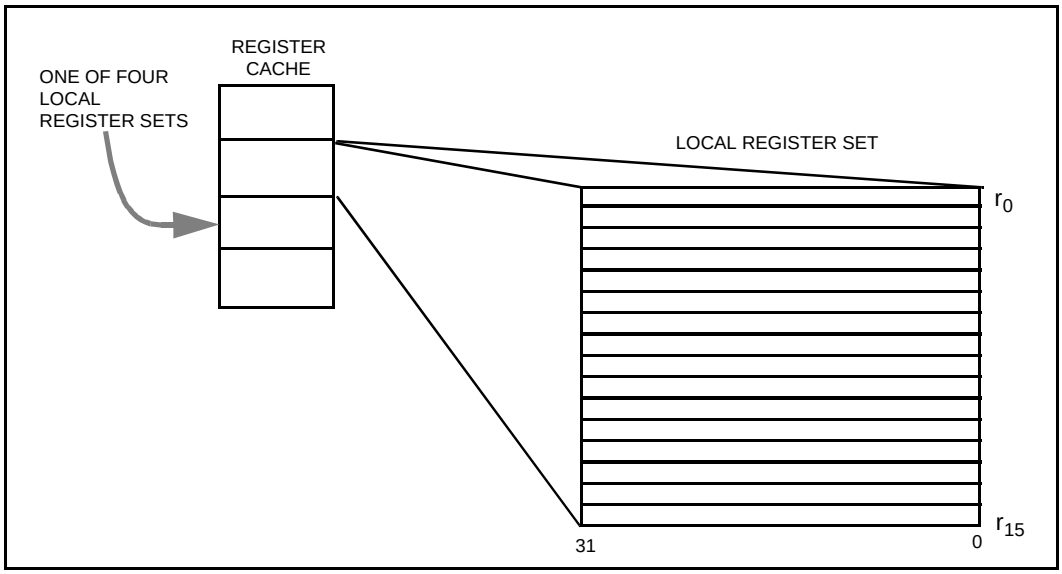


Figure 4. Multiple Register Sets Are Stored On-Chip

1.1.5 Instruction Cache

To further reduce memory accesses, the 80960SA includes a 512-byte on-chip instruction cache. The instruction cache is based on the concept of locality of reference; most programs are not usually executed in a steady stream but consist of many branches, loops and procedure calls that lead to jumping back and forth in the same small section of code. Thus, by maintaining a block of instructions in cache, the number of memory references required to read instructions into the processor is greatly reduced.

To load the instruction cache, instructions are fetched in 16-byte blocks; up to four instructions can be fetched at one time. An efficient prefetch algorithm increases the probability that an instruction will already be in the cache when it is needed.

Code for small loops often fits entirely within the cache, leading to a great increase in processing speed since further memory references might not be necessary until the program exits the loop. Similarly, when calling short procedures, the code for the calling procedure is likely to remain in the cache so it will be there on the procedure's return.

1.1.6 Register Scoreboarding

The instruction decoder is optimized in several ways. One optimization method is the ability to overlap instructions by using register scoreboarding.

Register scoreboarding occurs when a LOAD moves a variable from memory into a register. When the instruction initiates, a scoreboard bit on the target register is set. Once the register is loaded, the bit is reset. In between, any reference to the register contents is accompanied by a test of the scoreboard bit to ensure that the load has completed before processing continues. Since the processor does not need to wait for the LOAD to complete, it can execute additional instructions placed between the LOAD and the instruction that uses the register contents, as shown in the following example:

```
ld data_2, r4
ld data_2, r5
Unrelated instruction
Unrelated instruction
add r4, r5, r6
```

In essence, the two unrelated instructions between LOAD and ADD are executed "for free" (i.e., take no apparent time to execute) because they are executed while the register is being loaded. Up to three load instructions can be pending at one time with three corresponding scoreboard bits set. By exploiting this feature, system programmers and compiler writers have a useful tool for optimizing execution speed.

1.1.7 High Bandwidth Bus

The 80960SA CPU resides on a high-bandwidth address/data bus. The bus provides a direct communication path between the processor and the memory and I/O subsystem interfaces. The processor uses the bus to fetch instructions, manipulate memory and respond to interrupts. Bus features include:

- 16-bit data path multiplexed onto the lower bits of the 32-bit address path
- Eight 16-bit half-word burst capability which allows transfers from 1 to 16 bytes at a time
- High bandwidth reads and writes with 32 Mbytes/s burst (at 20 MHz)

Table 3 defines bus signal names and functions; Table 4 defines other component-support signals such as interrupt lines.

1.1.8 Interrupt Handling

The 80960SA can be interrupted in one of two ways: by the activation of one of four interrupt pins or by sending a message on the processor's data bus.

The 80960SA is unusual in that it automatically handles interrupts on a priority basis and can keep track of pending interrupts through its on-chip interrupt controller. Two of the interrupt pins can be configured to provide 8259A-style handshaking for expansion beyond four interrupt lines.

1.1.9 Debug Features

The 80960SA has built-in debug capabilities. There are two types of breakpoints and six trace modes. Debug features are controlled by two internal 32-bit registers, the Process-Controls Word and the Trace-Controls Word. By setting bits in these control words, a software debug monitor can closely control how the processor responds during program execution.

The 80960SA provides two hardware breakpoint registers on-chip which, by using a special command, can be set to any value. When the instruction pointer matches either breakpoint register value, the breakpoint handling routine is automatically called.

The 80960SA also provides software breakpoints through the use of two instructions: MARK and FMARK. These can be placed at any point in a program and cause the processor to halt execution at that point and call the breakpoint handling routine. The breakpoint mechanism is easy to use and provides a powerful debugging tool.

Tracing is available for instructions (single step execution), calls and returns and branching. Each trace type may be enabled separately by a special debug instruction. In each case, the 80960SA executes the instruction first and then calls a trace handling routine (usually part of a software debug monitor). Further program execution is halted until the routine completes, at which time execution resumes at the next instruction. The 80960SA's tracing mechanisms, implemented completely in hardware, greatly simplify the task of software test and debug.

1.1.10 Fault Detection

The 80960SA has an automatic mechanism to handle faults. Fault types include trace and arithmetic faults. When the processor detects a fault, it automatically calls the appropriate fault handling routine and saves the current instruction pointer and necessary state information to make efficient recovery possible. Like interrupt handling routines, fault handling routines are usually written to meet the needs of specific applications and are often included as part of the operating system or kernel.

For each of the fault types, there are numerous subtypes that provide specific information about a fault. The fault handler can use this specific information to respond correctly to the fault.

1.1.11 Built-in Testability

Upon reset, the 80960SA automatically conducts an exhaustive internal test of its major blocks of logic. Then, before executing its first instruction, it does a zero check sum on the first eight words in memory to ensure that the memory image was programmed correctly. If a problem is discovered at any point during the self-test, the 80960SA asserts its $\overline{\text{FAIL}}$ pin and will not begin program execution. Self test takes approximately 24,000 cycles to complete.

System manufacturers can use the 80960SA's self-test feature during incoming parts inspection. No special diagnostic programs need to be written. The test is both thorough and fast. The self-test capability helps ensure that defective parts are discovered before systems are shipped and, once in the field, the self-test makes it easier to distinguish between problems caused by processor failure and problems resulting from other causes.

1.1.12 CHMOS

The 80960SA is fabricated using Intel's CHMOS IV (Complementary High Speed Metal Oxide Semiconductor) process. The 80960SA is available at 10 and 16 MHz in the QFP package and at 10, 16 and 20 MHz in the PLCC package.

Table 3. 80960SA Pin Description: Bus Signals (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
CLK2	**I**	**SYSTEM CLOCK** provides the fundamental timing for 80960SA systems. It is divided by two inside the 80960SA to generate the internal processor clock.
A31:16	**O** T.S.	**ADDRESS BUS** carries the upper 16 bits of the 32-bit physical address to memory. It is valid throughout the burst cycle; no latch is required.
AD15:1, D0	**I/O** T.S.	**ADDRESS/DATA BUS** carries the low order 32-bit addresses and 16-bit data to and from memory. AD15:4 must be latched since the cycle following the address cycle carries data on the bus.
A3:1	**O** T.S.	**ADDRESS BUS** carries the word addresses of the 32-bit address to memory. These three bits are incremented during a burst access indicating the next word address of the burst access. Note that A3:1 are duplicated with AD3:1 during the address cycle.
ALE	**O** T.S.	**ADDRESS LATCH ENABLE** indicates the transfer of a physical address. ALE is asserted during a T_a cycle and deasserted before the beginning of the T_d state. It is active HIGH and floats to a high impedance state during a hold cycle (T_h).
$\overline{AS}$	**O** T.S.	**ADDRESS STATUS** indicates an address state. $\overline{AS}$ is asserted every T_a state and deasserted during the following T_d state. $\overline{AS}$ is driven HIGH during reset.
W/$\overline{R}$	**O** T.S.	**WRITE/READ** specifies, during a T_a cycle, whether the operation is a write or read. It is latched on-chip and remains valid during T_d cycles.
$\overline{DEN}$	**O** T.S.	**DATA ENABLE** is asserted during T_d cycles and indicates transfer of data on the AD lines. The AD lines should not be driven by an external source unless $\overline{DEN}$ is asserted. When $\overline{DEN}$ is asserted, outputs from the previous cycle are guaranteed to be three-stated. In addition, $\overline{DEN}$ deasserted indicates inputs have been captured; therefore input hold times can be disregarded. $\overline{DEN}$ is driven HIGH during reset.
DT/$\overline{R}$	**O** T.S.	**DATA TRANSMIT / RECEIVE** indicates the direction of data transfer to and from the bus. It is low during T_a and T_d cycles for a read or interrupt acknowledgment; it is high during T_a and T_d cycles for a write. DT/$\overline{R}$ never changes state when $\overline{DEN}$ is asserted. DT/$\overline{R}$ is driven HIGH during reset.
$\overline{READY}$	**I**	**READY** indicates that data on AD lines can be sampled or removed. If $\overline{READY}$ is not asserted during a T_d cycle, the T_d cycle is extended to the next cycle by inserting a wait state (T_w).

I/O = Input/Output, O = Output, I = Input, O.D. = Open Drain, T.S. = Three-state

Table 3. 80960SA Pin Description: Bus Signals (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION
$\overline{\text{LOCK}}$	**I/O** O.D.	**BUS LOCK** prevents bus masters from gaining control of the bus during Read/Modify/Write (RMW) cycles. The processor or any bus agent may assert $\overline{\text{LOCK}}$. At the start of a RMW operation, the processor examines the $\overline{\text{LOCK}}$ pin. If the pin is already asserted, the processor waits until it is not asserted. If the pin is not asserted, the processor asserts $\overline{\text{LOCK}}$ during the T_a cycle of the read transaction. The processor deasserts $\overline{\text{LOCK}}$ in the T_a cycle of the write transaction. While $\overline{\text{LOCK}}$ is asserted, a bus agent can perform a normal read or write but not a RMW operation. The processor also asserts $\overline{\text{LOCK}}$ during interrupt-acknowledge transactions. Do not leave $\overline{\text{LOCK}}$ unconnected. It must be pulled high for the processor to function properly. **ONCE MODE**: The $\overline{\text{LOCK}}$ pin is sampled during reset. If it is asserted LOW at the end of reset, all outputs will be three-stated until the part is reset again. ONCE mode is used in conjunction with an in-circuit emulator.
$\overline{\text{BE1:0}}$	**O** T.S.	**BYTE ENABLE LINES** specify which data bytes (up to two) on the bus take part in the current bus cycle. $\overline{\text{BE1}}$ corresponds to AD15:8; $\overline{\text{BE0}}$ corresponds to AD7:1, D0. The byte enable lines are asserted appropriately during each data cycle. **INITIALIZATION FAILURE** indicates that the processor has failed to initialize correctly. The failure state is indicated by a combination of $\overline{\text{BLAST}}$ asserted and $\overline{\text{BE1:0}}$ not asserted. This condition occurs after $\overline{\text{RESET}}$ is deasserted and before the first bus transaction begins. $\overline{\text{FAIL}}$ is asserted while the processor performs a self-test. If the self-test completes successfully, $\overline{\text{FAIL}}$ is deasserted. The processor then performs a zero checksum on the first eight words of memory, If it fails, $\overline{\text{FAIL}}$ is asserted for a second time and remains asserted; if it passes, system initialization continues and $\overline{\text{FAIL}}$ remains deasserted.
HOLD	**I**	**HOLD** indicates a request from an external bus master to acquire the bus. When the processor receives HOLD and grants bus control to another master, it floats its three-state bus lines, then asserts HLDA and enters the T_h state. When HOLD is deasserted, the processor deasserts HLDA and enters the T_i or T_a state.
HLDA	**O** T.S.	**HOLD ACKNOWLEDGE** notifies an external bus master that the processor has relinquished control of the bus. This signal is always driven. At reset it is driven LOW.
$\overline{\text{BLAST}}$/$\overline{\text{FAIL}}$	**O** T.S.	**BURST LAST** indicates the last data cycle (T_d) of a burst access. It is asserted low during the last T_d and associated with T_w cycles in a burst access. **INITIALIZATION FAILURE** indicates that the processor has failed to initialize correctly. The failure state is indicated by a combination of $\overline{\text{BLAST}}$ asserted and $\overline{\text{BE1:0}}$ not asserted. This condition occurs after $\overline{\text{RESET}}$ is deasserted and before the first bus transaction begins. $\overline{\text{FAIL}}$ is asserted while the processor performs a self-test. If the self-test completes successfully, $\overline{\text{FAIL}}$ is deasserted. The processor then performs a zero checksum on the first eight words of memory, If it fails, $\overline{\text{FAIL}}$ is asserted for a second time and remains asserted; if it passes, system initialization continues and $\overline{\text{FAIL}}$ remains deasserted.

I/O = Input/Output, O = Output, I = Input, O.D. = Open Drain, T.S. = Three-state

Table 4. 80960SA Pin Description: Support Signals

NAME	TYPE	DESCRIPTION
RESET	I	**RESET** clears the processor's internal logic and causes it to reinitialize. During RESET assertion, the input pins are ignored (except for INT0, INT1, INT3, LOCK), the three-state output pins are placed in a HIGH impedance state (except for DT/R, DEN, and AS) and other output pins are placed in their non-asserted states. RESET must be asserted for at least 41 CLK2 cycles for a predictable reset. Optionally, for a synchronous reset, the LOW and HIGH transition of RESET should occur after the rising edge of both CLK2 and the external bus CLK and before the next rising edge of CLK2. The interrupt pins indicate the initialization sequence executed. Typical initialization requires driving only INT0 and INT3 to a HIGH state. The reset conditions follow:

INT0	INT1	INT3	LOCK	Action Taken
1	x	1	1	Run self test (core initialization)
0	0	1	1	Disable self-test
0	1	x	x	Reserved
x	x	0	x	Reserved
x	x	x	0	ONCE mode (see LOCK pin)

INT0	I	**INTERRUPT 0** indicates a pending interrupt. To signal an interrupt in a synchronous system, this pin — as well as the other interrupt pins — must be enabled by being deasserted for at least one bus cycle and then asserted for at least one additional bus cycle. In an asynchronous system, the pin must remain deasserted for at least two system clock cycles and then asserted for at least two more system clock cycles. The interrupt control register must be programmed with an interrupt vector before using this pin. INT0 is sampled during reset to determine if the self-test sequence is to be executed.
INT1	I	**INTERRUPT 1**, like INT0, provides direct interrupt signaling. INT1 is sampled during reset to determine if the self-test sequence is to be executed.
INT2/INTR	I	**INTERRUPT2/INTERRUPT REQUEST**: The interrupt control register determines how this pin is interpreted. If INT2, it has the same interpretation as the INT0 and INT1 pins. If INTR, it is used to receive an interrupt request from an external interrupt controller.
INT3/INTA	**I/O** T.S.	**INTERRUPT3/INTERRUPT ACKNOWLEDGE**: The interrupt control register determines how this pin is interpreted. If INT3, it has the same interpretation as the INT0 and INT1 pins. If INTA, it is used as an output to control interrupt acknowledge transactions. The INTA output is latched on-chip and remains valid during T_d cycles; as an output, it is open-drain. INT3 must be pulled HIGH during reset.
NC	N/A	**NOT CONNECTED** indicates pins should not be connected. Never connect any pin marked NC; these pins may be reserved for factory use.

I/O = Input/Output, O = Output, I = Input, O.D. = Open Drain, T.S. = Three-state

2.0 ELECTRICAL SPECIFICATIONS

2.1 Power and Grounding

The 80960SA is implemented in CHMOS IV technology and therefore has modest power requirements. Its high clock frequency and numerous output buffers (address/data, control, error and arbitration signals) can cause power surges as multiple output buffers simultaneously drive new signal levels. For clean on-chip power distribution, V_{CC} and V_{SS} pins separately feed the device's functional units. Power and ground connections must be made to all 80960SA power and ground pins. On the circuit board, all V_{CC} pins must be strapped closely together, preferably on a power plane; all V_{SS} pins should be strapped together, preferably on a ground plane.

2.2 Power Decoupling Recommendations

Place a liberal amount of decoupling capacitance near the 80960SA. When driving the bus the processor can cause transient power surges, particularly when connected to a large capacitive load.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance is reduced by shortening board traces between the processor and decoupling capacitors as much as possible.

2.3 Connection Recommendations

For reliable operation, always connect unused inputs to an appropriate signal level. In particular, if one or more interrupt lines are not used, they should be pulled up. No inputs should ever be left floating.

The $\overline{\text{LOCK}}$ open-drain pin requires a pullup resistor whether or not the pin is used as an output. Figure 5 shows the recommended resistor value.

Do not connect external logic to pins marked NC.

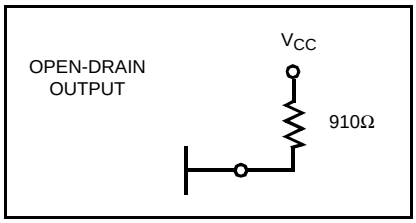


Figure 5. Connection Recommendation for $\overline{\text{LOCK}}$

2.4 Characteristic Curves

Figure 6 shows typical supply current requirements over the operating temperature range of the processor at supply voltage (V_{CC}) of 5V. Figure 7 shows the typical power supply current (I_{CC}) that the 80960SA requires at various operating frequencies when measured at three input voltage (V_{CC}) levels.

For a given output current (I_{OL}) the curve in Figure 8 shows the worst case output low voltage (V_{OL}). Figure 9 shows the typical capacitive derating curve for the 80960SA measured from 1.5V on the system clock (CLK) to 0.8V on the falling edge and 2.0V on the rising edge of the bus address/data (AD) signals.

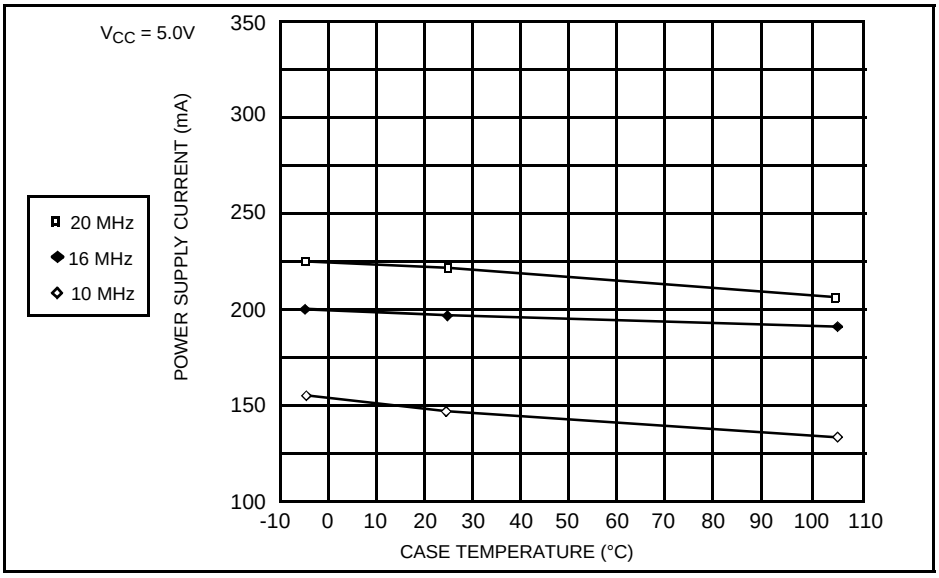


Figure 6. Typical Supply Current vs. Case Temperature

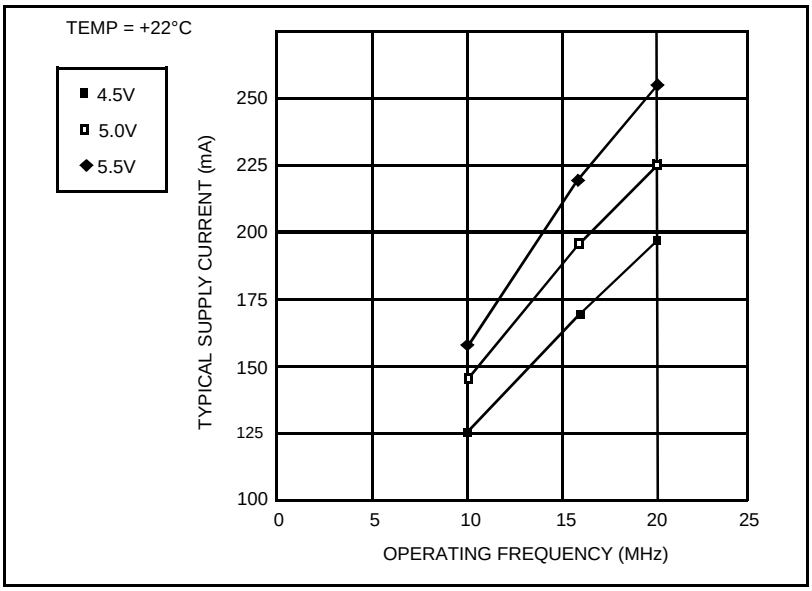


Figure 7. Typical Current vs. Frequency (Room Temp)

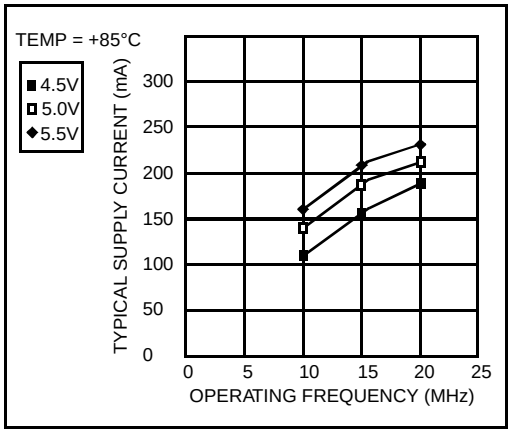


Figure 8. Typical Current vs. Frequency (Hot Temp)

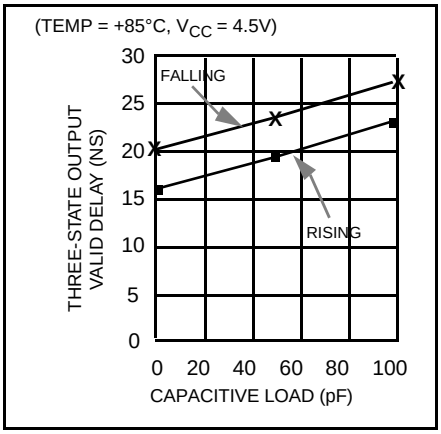


Figure 9. Capacitive Derating Curve

2.5 Test Load Circuit

Figure 10 illustrates the load circuit used to test the 80960SA's output pins.

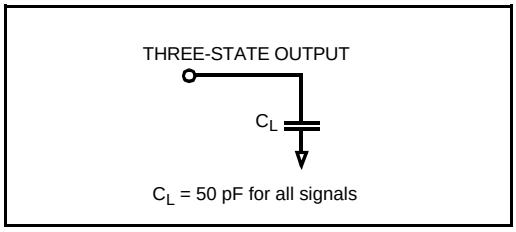


Figure 10. Test Load Circuit for Three-State Output Pins

2.6 ABSOLUTE MAXIMUM RATINGS*

Parameter	Maximum Rating
Operating Temperature (PLCC)	0°C to +85°C Case
Operating Temperature (QFP)	0°C to +100°C Case
Storage Temperature	–65°C to +150°C
Voltage on Any Pin (PLCC)	–0.5V to VCC +0.5V
Voltage on Any Pin (QFP)	–0.25V to VCC +0.25V
Power Dissipation	1.9W (20 MHz)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

2.7 DC Characteristics

80960SA (10 and 16 MHz QFP) T_{CASE} = 0°C to +100°C, V_{CC} = 5V ± 5%
80960SA (10 and 16 MHz PLCC) T_{CASE} = 0°C to +85°C, V_{CC} = 5V ± 10%
80960SA (20 MHz PLCC) T_{CASE} = 0°C to +85°C, V_{CC} = 5V ± 5%

Table 5. DC Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	–0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{CL}	CLK2 Input Low Voltage	–0.3	+0.8	V	
V_{CH}	CLK2 Input High Voltage	0.7 V_{CC}	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45 0.45	V V	I_{OL} = 4.0 mA I_{OL} = 6 mA, $\overline{LOCK}$ Pin
V_{OH}	Output High Voltage	2.4		V	All TS, -2.5 mA (1)
I_{CC}	Power Supply Current: 10 MHz-QFP 10 MHz-PLCC 16 MHz-PLCC 20 MHz-PLCC		 240 240 300 340	 mA mA mA mA	 T_{CASE} = 0°C T_{CASE} = 0°C T_{CASE} = 0°C T_{CASE} = 0°C
I_{LI1}	Input Leakage Current, Except $\overline{INT0}$, $\overline{LOCK}$		±15	µA	$0 \le V_{IN} \le V_{CC}$
I_{LI2}	Input Leakage Current, $\overline{INT0}$, $\overline{LOCK}$		–300	µA	V_{IN} = 0.45V (2)
I_{OL}	Output Leakage Current		±15	µA	
C_{IN}	Input Capacitance		10	pF	f_C = 1 MHz (3)
C_O	Output Capacitance		12	pF	f_C = 1 MHz (3)
C_{CLK}	Clock Capacitance		10	pF	f_C = 1 MHz (3)

NOTES:
1. Not measured for open-drain output.
2. $\overline{INT0}$ and $\overline{LOCK}$ have internal pullup devices.
3. Input, output and clock capacitance are not tested.

2.8 AC Specifications

This section describes the AC specifications for the 80960SA pins. All input and output timings are specified relative to the 1.5V level of the rising edge of CLK2 and refer to the time at which the signal crosses 1.5V (for output delay and input setup). All AC testing should be done with input voltages of 0.4V and 2.4V, except for the clock (CLK2) which should be tested with input voltages of 0.45V and 0.7 x V_{CC}. See Figure 11 and Tables 6, 7 and 8 for timing relationships for the 80960SA signals.

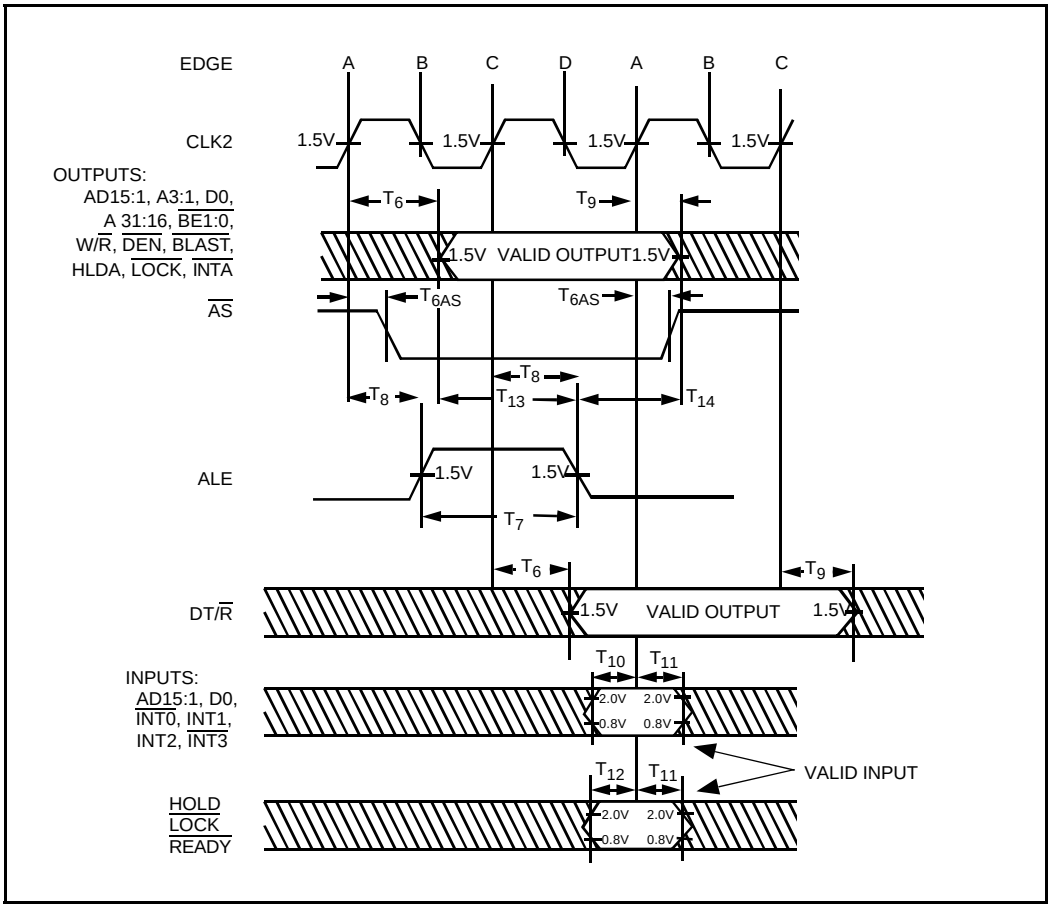


Figure 11. Drive Levels and Timing Relationships for 80960SA Signals

Table 6. 80960SA AC Characteristics (10 MHz)

Symbol	Parameter	Min	Max	Units	Notes
Input Clock					
T_1	Processor Clock Period (CLK2)	50	125	ns	V_{IN} = 1.5V
T_2	Processor Clock Low Time (CLK2)	8		ns	V_T = 10% Point = $V_{CL} + (V_{CH} - V_{CL}) \times 0.1$
T_3	Processor Clock High Time (CLK2)	8		ns	V_T = 90% Point = $V_{CL} + (V_{CH} - V_{CL}) \times 0.9$
T_4	Processor Clock Fall Time (CLK2)		10	ns	V_T = 90% to 10% Point (1)
T_5	Processor Clock Rise Time (CLK2)		10	ns	V_T = 10% to 90% Point (1)
Synchronous Outputs					
T_6	Output Valid Delay	2	31	ns	
T_{6AS}	$\overline{AS}$ Output Valid Delay	2	25	ns	
T_7	ALE Width	T_1 - 11		ns	
T_8	ALE Output Valid Delay	4	33	ns	
T_9	Output Float Delay	2	20	ns	(2)
Synchronous Inputs					
T_{10}	Input Setup 1	10		ns	
T_{11}	Input Hold	2		ns	
T_{12}	Input Setup 2	13		ns	
T_{13}	Setup to ALE Inactive	10		ns	
T_{14}	Hold after ALE Inactive	8		ns	
T_{15}	$\overline{RESET}$ Hold	3		ns	(3)
T_{16}	$\overline{RESET}$ Setup	5		ns	(3)
T_{17}	$\overline{RESET}$ Width	2050		ns	41 CLK2 Periods Minimum

NOTES:

1. Processor clock (CLK2) rise time and fall time are not tested.
2. A float condition occurs when the maximum output current becomes less than I_{LO}. Float delay is not tested, but should be no longer than the valid delay.
3. Meeting $\overline{RESET}$ setup and hold times is an optional method of synchronizing your clocks. If you decide to use an asynchronous reset, synchronizing the clock can be accomplished by using $\overline{AS}$.

Table 7. 80960SA AC Characteristics (16 MHz)

Symbol	Parameter	Min	Max	Units	Notes
Input Clock					
T_1	Processor Clock Period (CLK2)	31.25	125	ns	V_{IN} = 1.5V
T_2	Processor Clock Low Time (CLK2)	8		ns	V_T = 10% Point = $V_{CL} + (V_{CH} - V_{CL}) \times 0.1$
T_3	Processor Clock High Time (CLK2)	8		ns	V_T = 90% Point = $V_{CL} + (V_{CH} - V_{CL}) \times 0.9$
T_4	Processor Clock Fall Time (CLK2)		10	ns	V_T = 90% to 10% Point (1)
T_5	Processor Clock Rise Time (CLK2)		10	ns	V_T = 10% to 90% Point (1)
Synchronous Outputs					
T_6	Output Valid Delay	2	25	ns	
T_{6AS}	$\overline{AS}$ Output Valid Delay	2	21	ns	
T_7	ALE Width	T_1 - 11		ns	
T_8	ALE Output Valid Delay	2	22	ns	
T_9	Output Float Delay	2	20	ns	(2)
Synchronous Inputs					
T_{10}	Input Setup 1	10		ns	
T_{11}	Input Hold	2		ns	
T_{12}	Input Setup 2	13		ns	
T_{13}	Setup to ALE Inactive	10		ns	
T_{14}	Hold after ALE Inactive	8		ns	
T_{15}	$\overline{RESET}$ Hold	3		ns	(3)
T_{16}	$\overline{RESET}$ Setup	5		ns	(3)
T_{17}	$\overline{RESET}$ Width	1281		ns	41 CLK2 Periods Minimum

NOTES:

1. Processor clock (CLK2) rise time and fall time are not tested.
2. A float condition occurs when the maximum output current becomes less than I_{LO}. Float delay is not tested, but should be no longer than the valid delay.
3. Meeting $\overline{RESET}$ setup and hold times is an optional method of synchronizing your clocks. If you decide to use an asynchronous reset, synchronizing the clock can be accomplished by using $\overline{AS}$.

Table 8. 80960SA AC Characteristics (20 MHz)

Symbol	Parameter	Min	Max	Units	Notes
Input Clock					
T_1	Processor Clock Period (CLK2)	25	125	ns	V_{IN} = 1.5V
T_2	Processor Clock Low Time (CLK2)	6		ns	V_T = 10% Point = $V_{CL} + (V_{CH} - V_{CL}) \times 0.1$
T_3	Processor Clock High Time (CLK2)	6		ns	V_T = 90% Point = $V_{CL} + (V_{CH} - V_{CL}) \times 0.9$
T_4	Processor Clock Fall Time (CLK2)		10	ns	V_T = 90% to 10% Point (1)
T_5	Processor Clock Rise Time (CLK2)		10	ns	V_T = 10% to 90% Point (1)
Synchronous Outputs					
T_6	Output Valid Delay	2	20	ns	
T_{6AS}	$\overline{AS}$ Output Valid Delay	2	20	ns	
T_7	ALE Width	T_1 - 11		ns	
T_8	ALE Output Valid Delay	2	18	ns	
T_9	Output Float Delay	2	17	ns	(2)
Synchronous Inputs					
T_{10}	Input Setup 1	7		ns	
T_{11}	Input Hold	2		ns	
T_{12}	Input Setup 2	13		ns	
T_{13}	Setup to ALE Inactive	10		ns	
T_{14}	Hold after ALE Inactive	8		ns	
T_{15}	$\overline{RESET}$ Hold	3		ns	(3)
T_{16}	$\overline{RESET}$ Setup	5		ns	(3)
T_{17}	$\overline{RESET}$ Width	1025		ns	41 CLK2 Periods Minimum

NOTES:

1. Processor clock (CLK2) rise time and fall time are not tested.
2. A float condition occurs when the maximum output current becomes less than I_{LO}. Float delay is not tested, but should be no longer than the valid delay.
3. Meeting $\overline{RESET}$ setup and hold times is an optional method of synchronizing your clocks. If you decide to use an asynchronous reset, synchronizing the clock can be accomplished by using $\overline{AS}$.

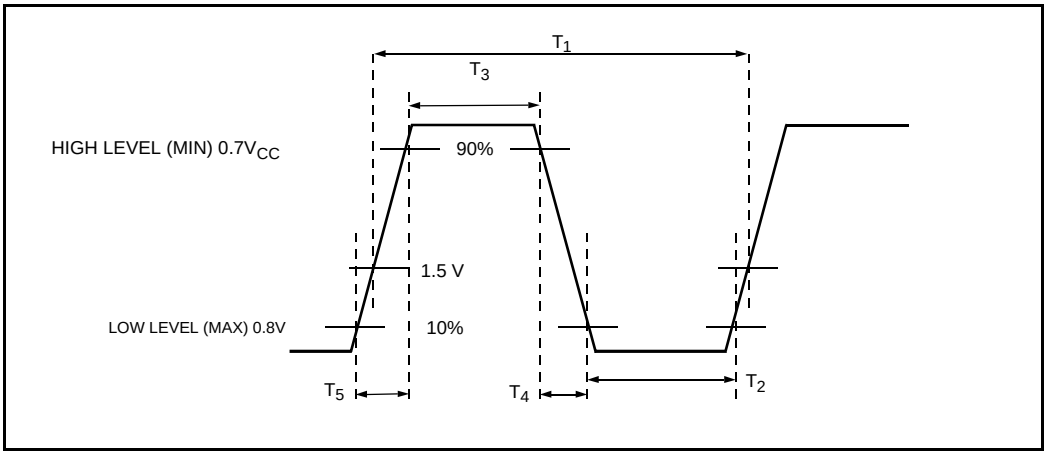
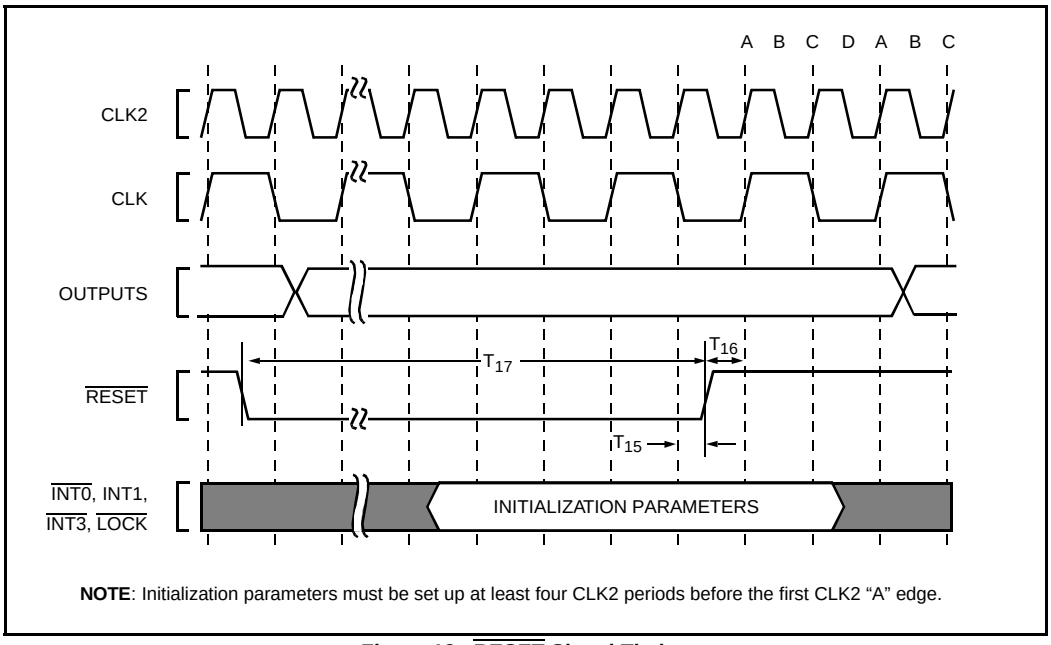


Figure 12. Processor Clock Pulse (CLK2)



NOTE: Initialization parameters must be set up at least four CLK2 periods before the first CLK2 “A” edge.

Figure 13. $\overline{\text{RESET}}$ Signal Timing

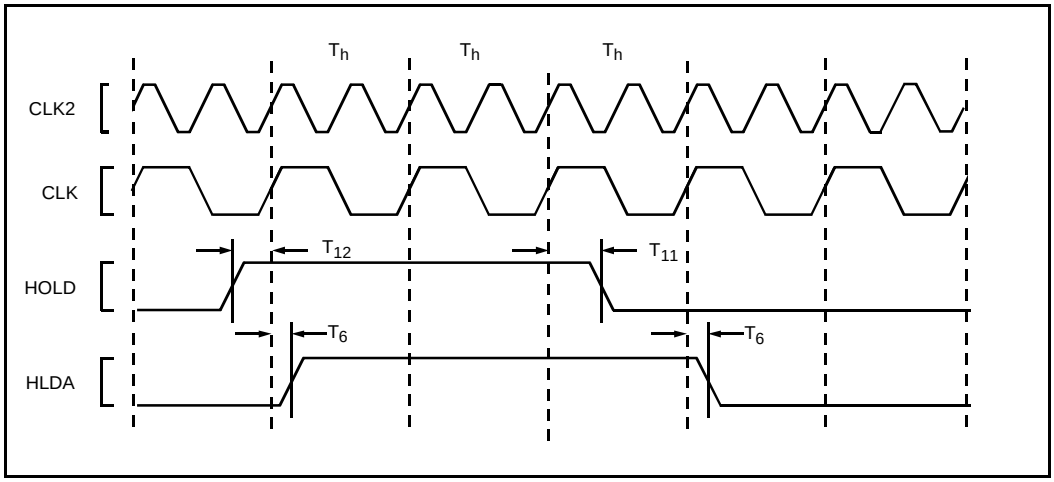


Figure 14. HOLD Timing

3.0 MECHANICAL DATA

3.1 Packaging

The 80960SA is available in two package types:

- 80-lead quad flat pack (EIAJ QFP). Shown in Figure 15.
- 84-lead plastic leaded chip carrier (PLCC). Shown in Figure 16.

Dimensions for both package types are given in the Intel *Packaging* handbook (Order #240800).

3.2 Pin Assignment

The QFP and PLCC have different pin assignments. The QFP pins are numbered in order from 1 to 80 around the package perimeter. The PLCC pins are numbered in order from 1 to 84 around the package perimeter. Tables 9 and 10 list the function of each QFP pin; Tables 11 and 12 list the function of each PLCC pin.

V_{CC} and GND connections must be made to multiple V_{CC} and GND pins. Each V_{CC} and GND pin must be connected to the appropriate voltage or ground and externally strapped close to the package. It is recommended that you include separate power and ground planes in your circuit board for power distribution.

Pins identified as NC (No Connect) should never be connected.

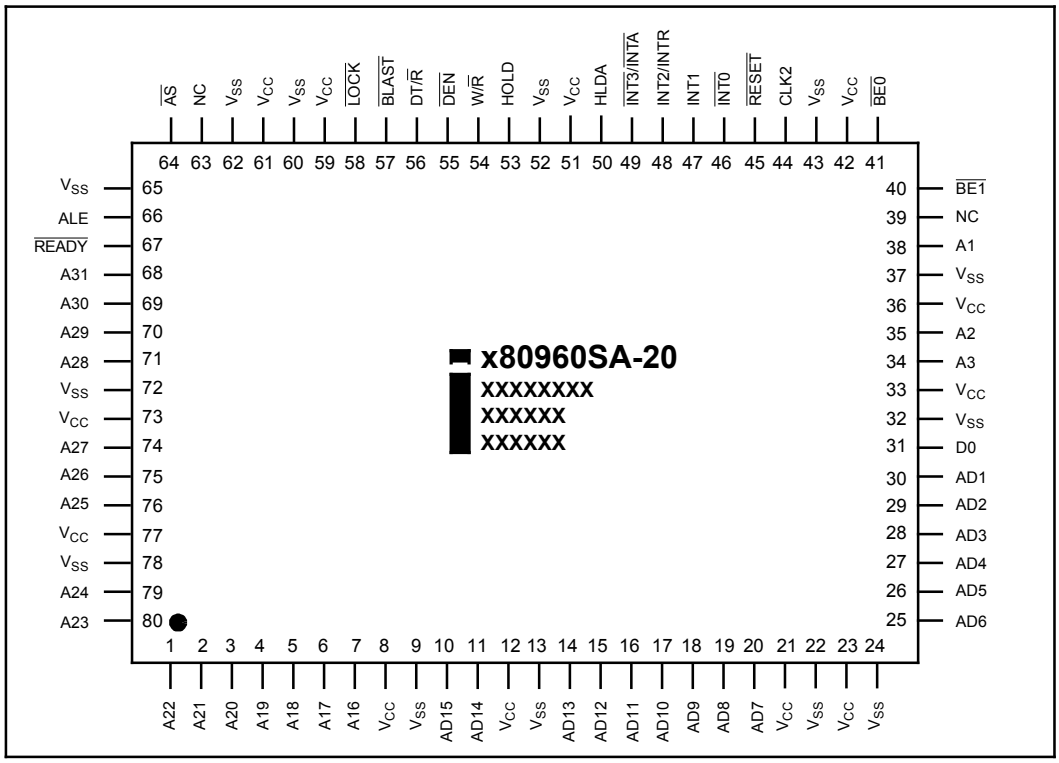


Figure 15. 80-Lead EIAJ Quad Flat Pack (QFP) Package

NOTE: To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

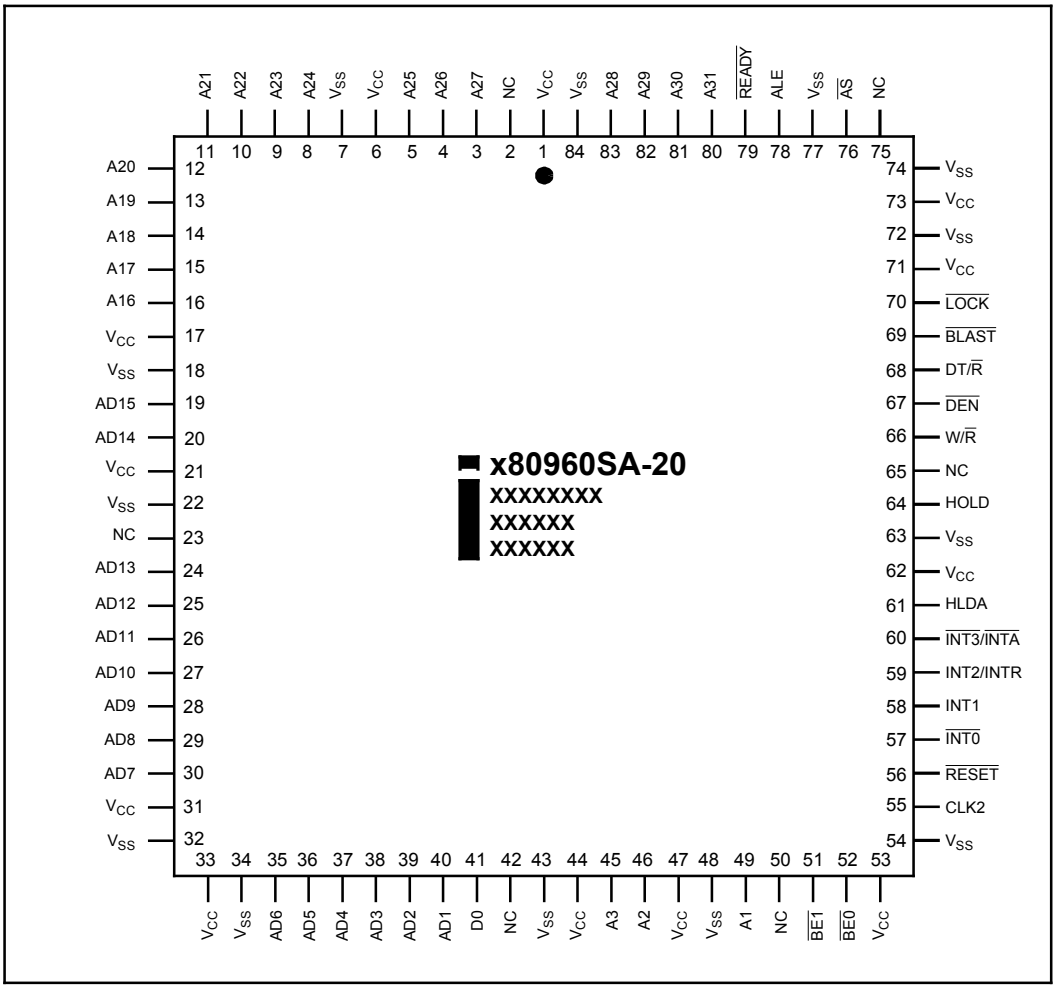


Figure 16. 84-Lead Plastic Leaded Chip Carrier (PLCC) Package

NOTE: To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

3.3 Pinout

Table 9. 80960SA QFP Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	A22	21	V_{CC}	41	$\overline{BE0}$	61	V_{CC}
2	A21	22	V_{SS}	42	V_{CC}	62	V_{SS}
3	A20	23	V_{CC}	43	V_{SS}	63	NC
4	A19	24	V_{SS}	44	CLK2	64	$\overline{AS}$
5	A18	25	AD6	45	$\overline{RESET}$	65	V_{SS}
6	A17	26	AD5	46	$\overline{INT0}$	66	ALE
7	A16	27	AD4	47	INT1	67	$\overline{READY}$
8	V_{CC}	28	AD3	48	INT2/INTR	68	A31
9	V_{SS}	29	AD2	49	$\overline{INT3}/\overline{INTA}$	69	A30
10	AD15	30	AD1	50	HLDA	70	A29
11	AD14	31	D0	51	V_{CC}	71	A28
12	V_{CC}	32	V_{SS}	52	V_{SS}	72	V_{SS}
13	V_{SS}	33	V_{CC}	53	HOLD	73	V_{CC}
14	AD13	34	A3	54	W/$\overline{R}$	74	A27
15	AD12	35	A2	55	$\overline{DEN}$	75	A26
16	AD11	36	V_{CC}	56	DT/$\overline{R}$	76	A25
17	AD10	37	V_{SS}	57	$\overline{BLAST}$	77	V_{CC}
18	AD9	38	A1	58	$\overline{LOCK}$	78	V_{SS}
19	AD8	39	NC	59	V_{CC}	79	A24
20	AD7	40	$\overline{BE1}$	60	V_{SS}	80	A23

NOTES:
Do not connect any external logic to any pins marked NC.

Table 10. 80960SA QFP Pinout — In Signal Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A1	38	A18	5	D0	31	V_{CC}	51
A2	35	A19	4	$\overline{DEN}$	55	V_{CC}	59
A3	34	A20	3	DT/$\overline{R}$	56	V_{CC}	61
AD1	30	A21	2	HLDA	50	V_{CC}	73
AD2	29	A22	1	HOLD	53	V_{CC}	77
AD3	28	A23	80	$\overline{INT0}$	46	V_{CC}	8
AD4	27	A24	79	INT1	47	V_{SS}	13
AD5	26	A25	76	INT2/INTR	48	V_{SS}	22
AD6	25	A26	75	$\overline{INT3}$/$\overline{INTA}$	49	V_{SS}	24
AD7	20	A27	74	LOCK	58	V_{SS}	32
AD8	19	A28	71	NC	39	V_{SS}	37
AD9	18	A29	70	NC	63	V_{SS}	43
AD10	17	A30	69	$\overline{READY}$	67	V_{SS}	52
AD11	16	A31	68	$\overline{RESET}$	45	V_{SS}	60
AD12	15	ALE	66	V_{CC}	12	V_{SS}	62
AD13	14	$\overline{AS}$	64	V_{CC}	21	V_{SS}	72
AD14	11	$\overline{BE0}$	41	V_{CC}	23	V_{SS}	78
AD15	10	$\overline{BE1}$	40	V_{CC}	33	V_{SS}	9
A16	7	$\overline{BLAST}$	57	V_{CC}	36	V_{SS}	65
A17	6	CLK2	44	V_{CC}	42	W/$\overline{R}$	54

NOTES:
Do not connect any external logic to any pins marked N.C.

Table 11. 80960SA PLCC Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	V_{CC}	22	V_{SS}	43	V_{SS}	64	HOLD
2	NC	23	NC	44	V_{CC}	65	NC
3	A27	24	AD13	45	A3	66	W/$\overline{R}$
4	A26	25	AD12	46	A2	67	$\overline{DEN}$
5	A25	26	AD11	47	V_{CC}	68	DT/$\overline{R}$
6	V_{CC}	27	AD10	48	V_{SS}	69	$\overline{BLAST}$
7	V_{SS}	28	AD9	49	A1	70	$\overline{LOCK}$
8	A24	29	AD8	50	NC	71	V_{CC}
9	A23	30	AD7	51	$\overline{BE1}$	72	V_{SS}
10	A22	31	V_{CC}	52	$\overline{BE0}$	73	V_{CC}
11	A21	32	V_{SS}	53	V_{CC}	74	V_{SS}
12	A20	33	V_{CC}	54	V_{SS}	75	NC
13	A19	34	V_{SS}	55	CLK2	76	$\overline{AS}$
14	A18	35	AD6	56	$\overline{RESET}$	77	V_{SS}
15	A17	36	AD5	57	$\overline{INT0}$	78	ALE
16	A16	37	AD4	58	INT1	79	$\overline{READY}$
17	V_{CC}	38	AD3	59	INT2/INTR	80	A31
18	V_{SS}	39	D2	60	$\overline{INT3}$/$\overline{INTA}$	81	A30
19	AD15	40	D1	61	HLDA	82	A29
20	AD14	41	D0	62	V_{CC}	83	A28
21	V_{CC}	42	NC	63	V_{SS}	84	V_{SS}

NOTES:
Do not connect any external logic to any pins marked NC.

Table 12. 80960SA PLCC Pinout — In Signal Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A1	49	A18	14	DT/$\overline{R}$	68	V_{CC}	44
A2	46	A19	13	HLDA	61	V_{CC}	47
A3	45	A20	12	HOLD	64	V_{CC}	53
D0	41	A21	11	$\overline{INT0}$	57	V_{CC}	6
AD1	40	A22	10	INT1	58	V_{CC}	62
AD2	39	A23	9	INT2/INTR	59	V_{CC}	71
AD3	38	A24	8	$\overline{INT3}$/$\overline{INTA}$	60	V_{CC}	73
AD4	37	A25	5	$\overline{LOCK}$	70	V_{SS}	18
AD5	36	A26	4	NC	2	V_{SS}	22
AD6	35	A27	3	NC	23	V_{SS}	32
AD7	30	A28	83	NC	42	V_{SS}	34
AD8	29	A29	82	NC	50	V_{SS}	43
AD9	28	A30	81	NC	65	V_{SS}	48
AD10	27	A31	80	NC	75	V_{SS}	54
AD11	26	ALE	78	$\overline{READY}$	79	V_{SS}	63
AD12	25	$\overline{AS}$	76	$\overline{RESET}$	56	V_{SS}	7
AD13	24	$\overline{BE0}$	52	V_{CC}	1	V_{SS}	72
AD14	20	$\overline{BE1}$	51	V_{CC}	17	V_{SS}	74
AD15	19	$\overline{BLAST}$	69	V_{CC}	21	V_{SS}	77
AD16	16	CLK2	55	V_{CC}	31	V_{SS}	84
A17	15	$\overline{DEN}$	67	V_{CC}	33	W/$\overline{R}$	66

NOTES:
Do not connect any external logic to any pins marked NC.

3.4 Package Thermal Specifications

The 80960SA is specified for operation when case temperature is within the range 0°C to +85°C (PLCC) or 0°C to 100°C (QFP). Measure case temperature at the top center of the package. Ambient temperature can be calculated from:

$T_J = T_C + P*\theta_{JC}$
$T_A = T_J - P*\theta_{JA}$
$T_C = T_A + P*[\theta_{JA}–\theta_{JC}]$

Compute P by multiplying the maximum voltage by the typical current at maximum temperature. Values for θ_{JA} and θ_{JC} for various airflows are given in Table 13 for the QFP package and in Table 14 for the PLCC package. I_{CC} at maximum temperature is typically 80 percent of specified I_{CC} maximum (cold).

Table 13. 80960SA QFP Package Thermal Characteristics

Thermal Resistance — °C/Watt							
Parameter	**Airflow — ft./min (m/sec)**						
	0	**50**	**100**	**200**	**400**	**600**	**800**
θ Junction-to-Ambient (Case measured in the middle of the top of the package) (No Heatsink)	59	57	54	50	44	40	38
θ Junction-to-Case	11	11	11	11	11	11	11

NOTES:
This table applies to 80960SA QFP soldered directly to board.

Table 14. 80960SA PLCC Package Thermal Characteristics

Thermal Resistance — °C/Watt								
Parameter	**Airflow — ft./min (m/sec)**							
	0	**50**	**100**	**200**	**400**	**600**	**800**	**1000**
θ Junction-to-Ambient (No Heatsink)	34	32	29.5	28	25	23	21	20.5
θ Junction-to-Case	12	12	12	12	12	12	12	12

NOTES:
This table applies to 80960SA PLCC soldered directly to board.

3.5 Stepping Register Information

Upon reset, register g0 contains die stepping information. Table 15 shows the relationship between the number in g0 and the current die stepping

Table 15. Die Stepping Cross Reference

Register g0	Die Stepping
01010101H	C-1

The current numbering pattern in g0 may not be consistent with past or future steppings of this product.

4.0 WAVEFORMS

Figures 17, 18, 19, 20 and 21 show waveforms for various transactions on the 80960SA's bus. Figure 22 shows a cold reset functional waveform.

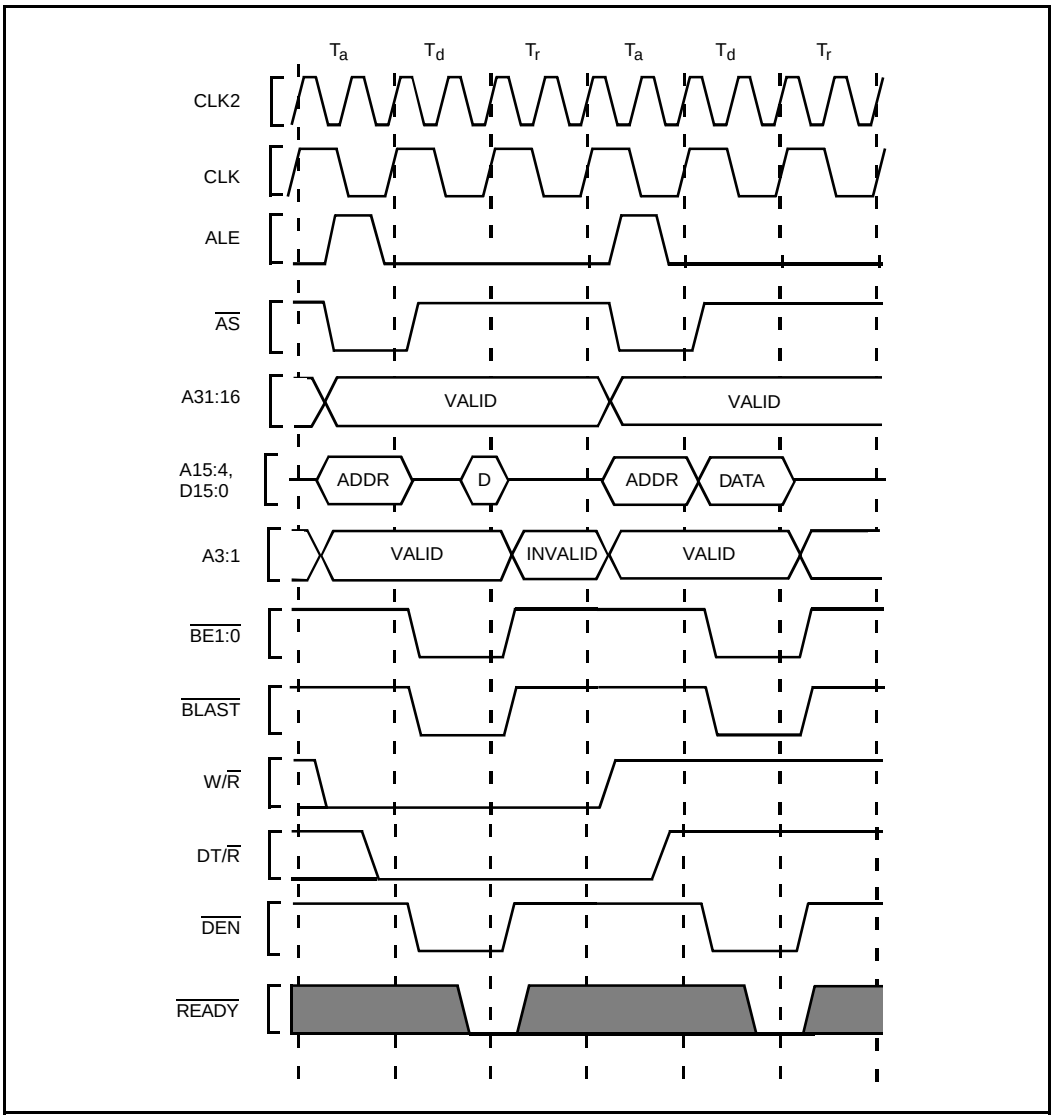


Figure 17. Non-Burst Read and Write Transactions Without Wait States

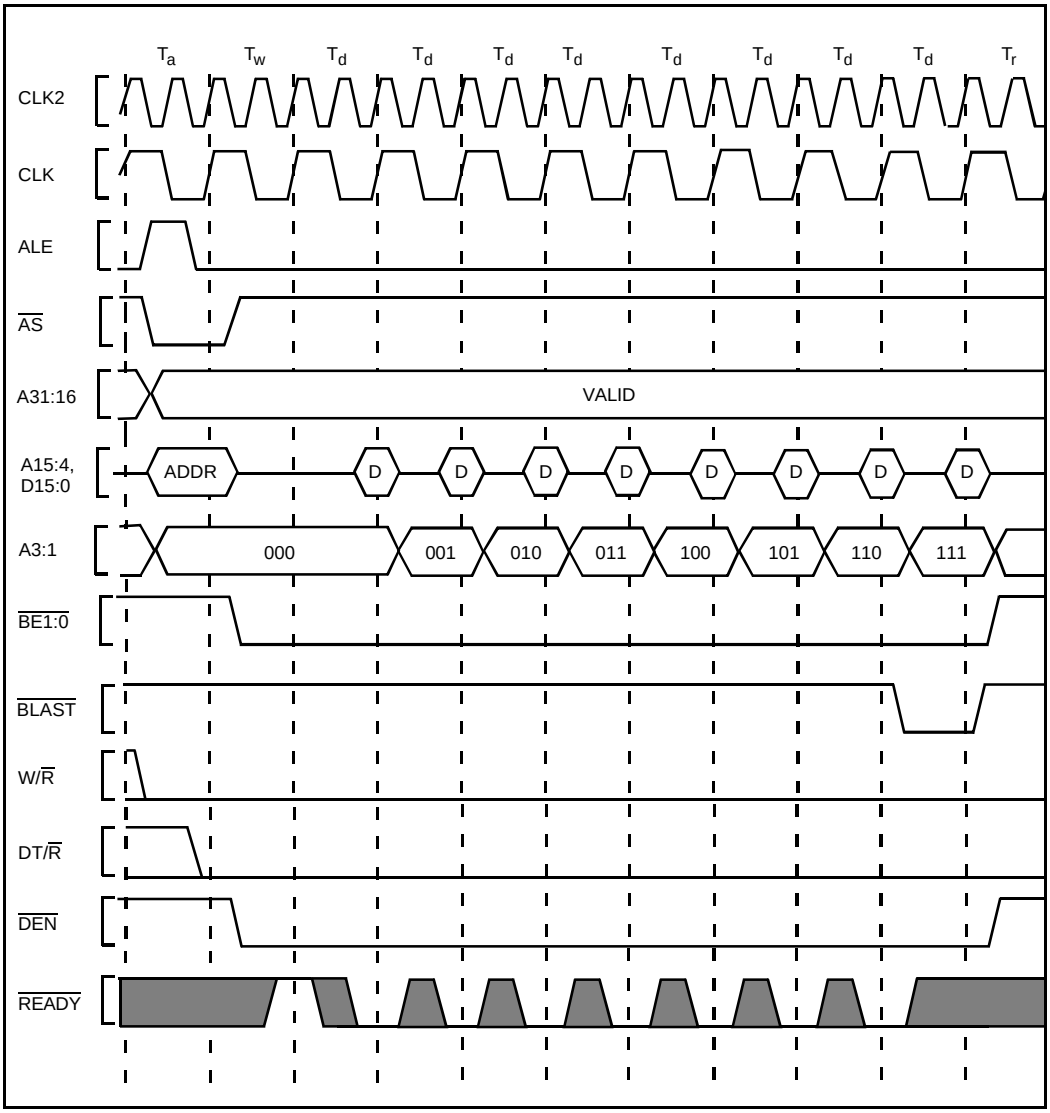


Figure 18. Quad Word Burst Read Transaction With 1, 0, 0, 0, 0, 0, 0, 0 Wait States

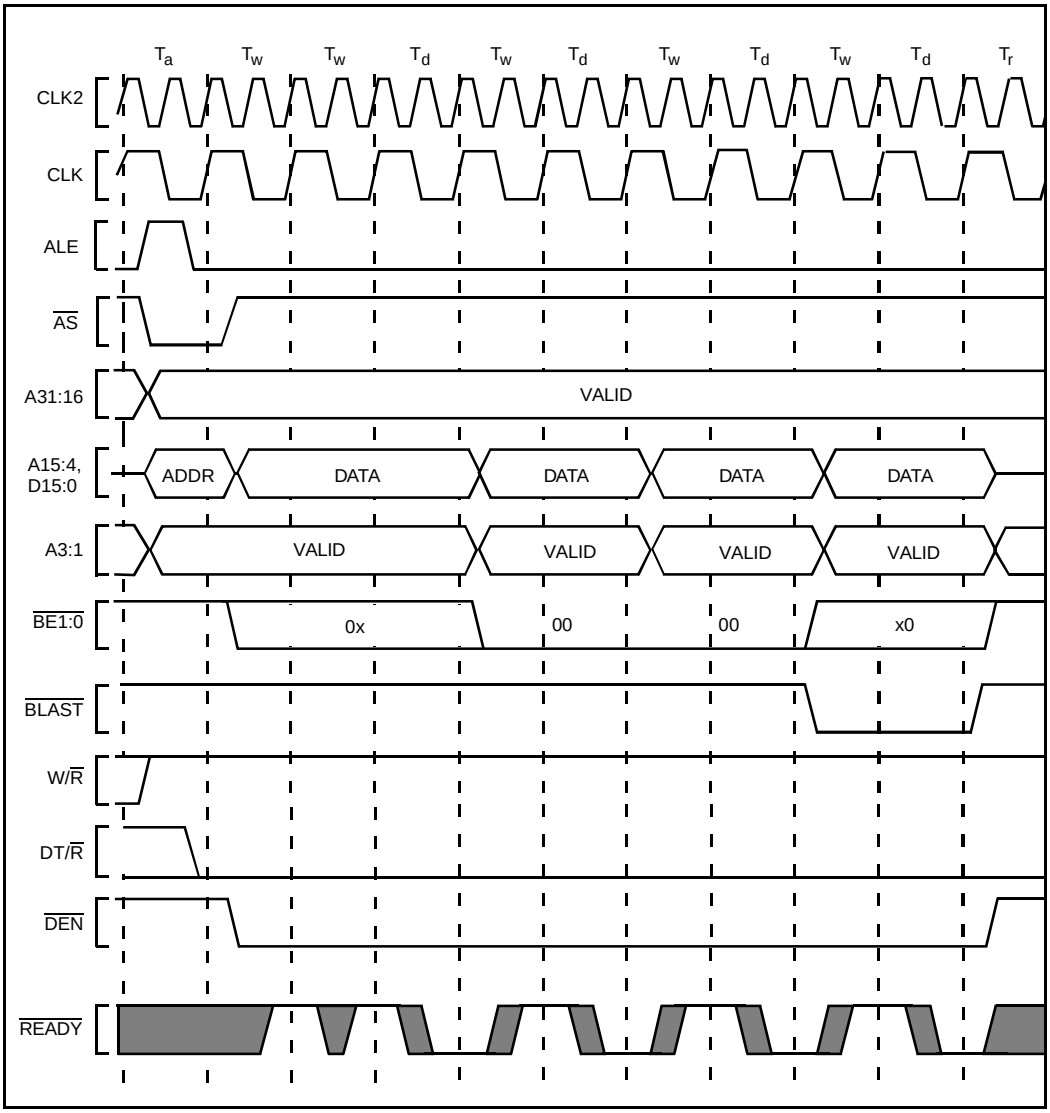


Figure 19. Burst Write Transaction With 2, 1, 1, 1 Wait States (6-8 Bytes Transferred)

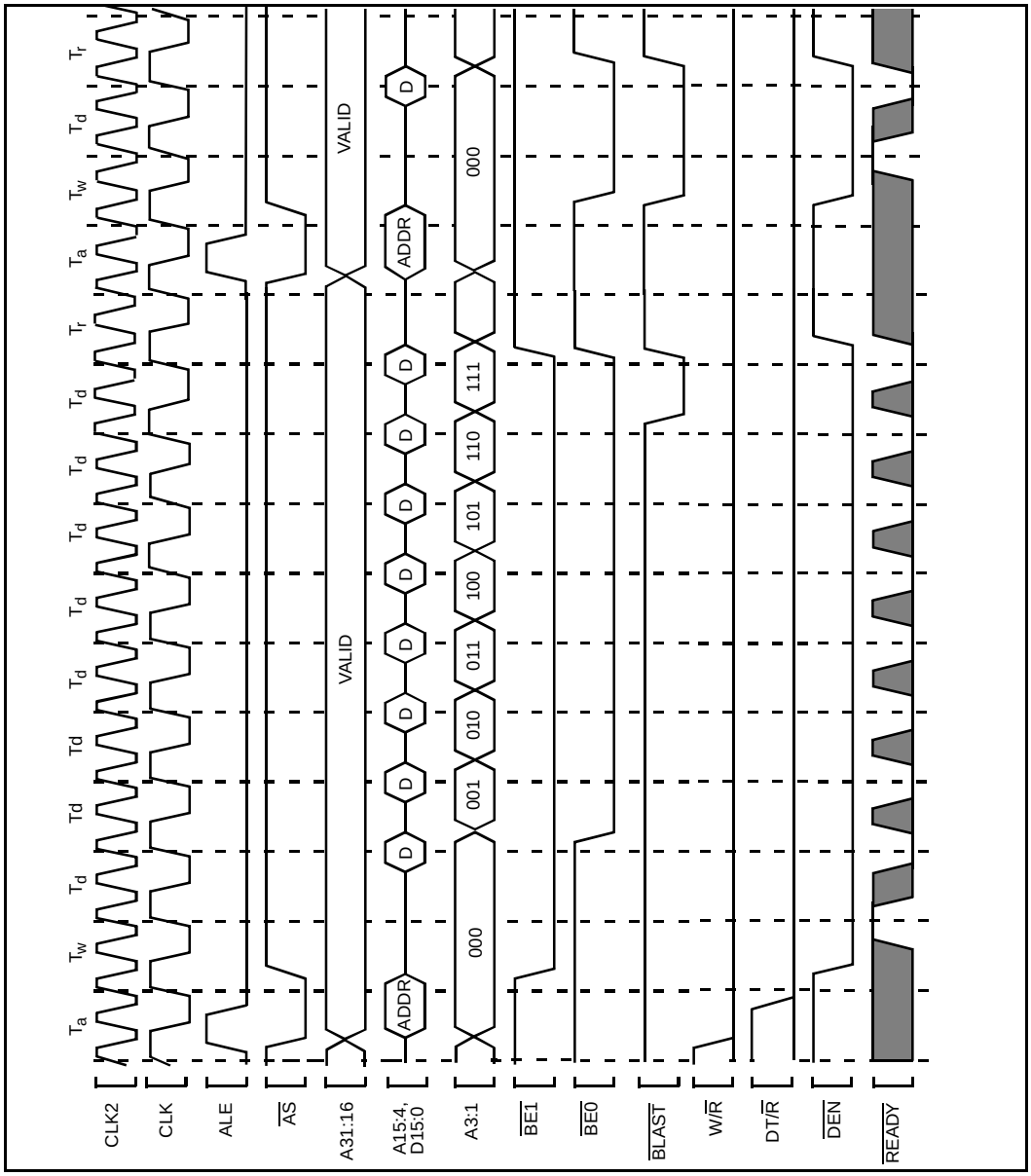


Figure 20. Accesses Generated by Quad Word Read Bus Request, Misaligned One Byte from Quad Word Boundary 1, 0, 0, 0, 0, 0, 0, 0 Wait States

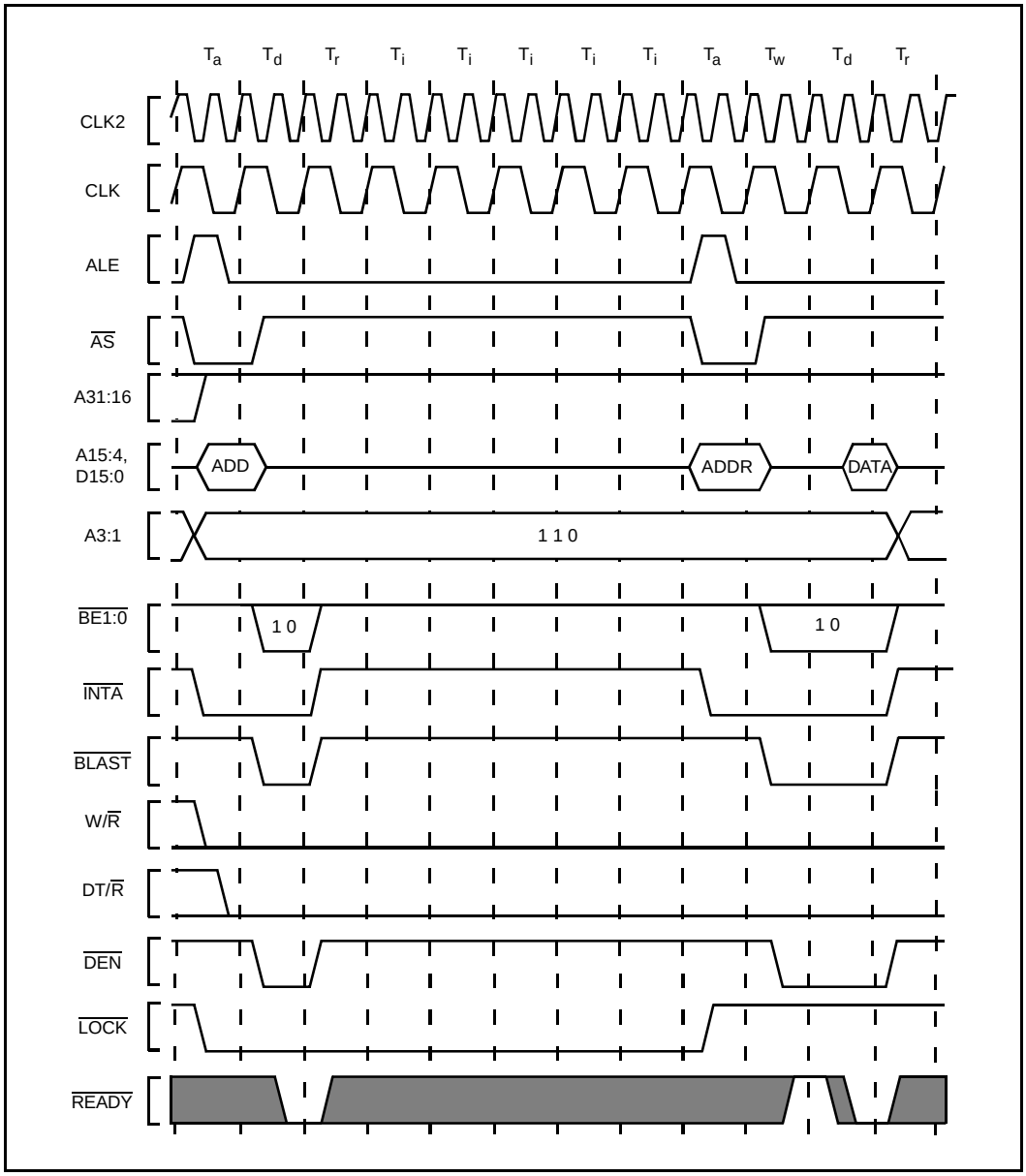


Figure 21. Interrupt Acknowledge Cycle

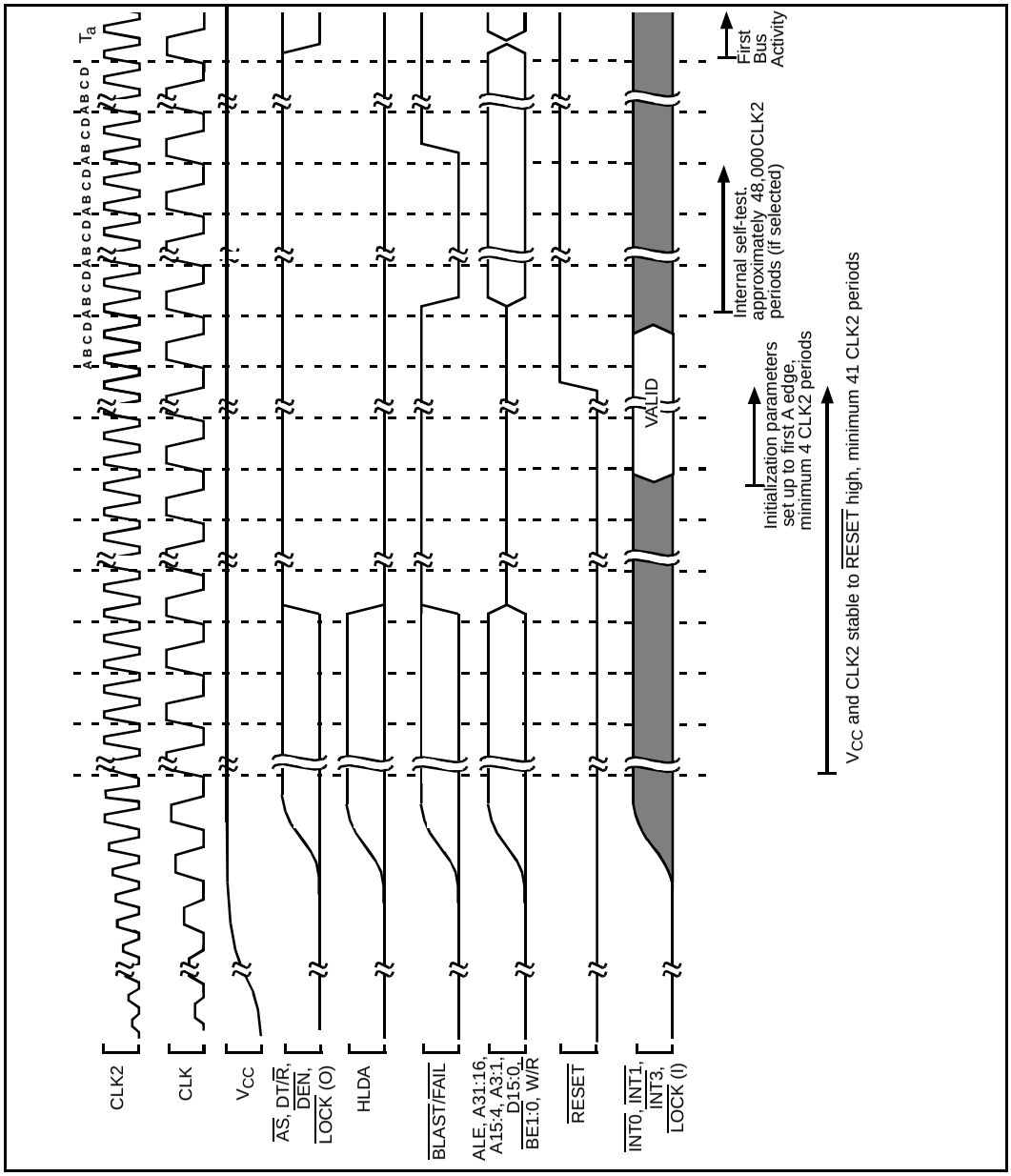


Figure 22. Cold Reset Waveform

5.0 REVISION HISTORY

This data sheet supersedes data sheet 272206-001 and applies only to those devices identified as the current stepping in section 3.5. The sections significantly changed since the previous revision are:

Section	Last Rev.	Description
Overall	-003	To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".
2.3 Connection Recommendations (pg. 11)	-001	Removed two $\overline{LOCK}$ pin Connection Recommendation figures and added Figure 5 to reflect the new $\overline{LOCK}$ pin connection recommendation of a single 910Ω pullup resistor.
2.5 Test Load Circuit (pg. 13)	-001	Obsolete figure (Test Load Circuit for Open-Drain Output Pins) removed to reflect current test conditions.
2.7 DC Characteristics (pg. 14)	-001	I_{OL} value at 0.45V improved. WAS: 2.5 mA IS: 4.0 mA $\overline{LOCK}$ pin I_{OL} value at 0.45V relaxed. WAS: 12 mA IS: 6 mA $\overline{LOCK}$ pin I_{OL} value at 0.60V deleted. 80960SA 16 MHz QFP added to product list.
3.5 Stepping Register Information (pg. 27)	-001	New section added.

Data sheet 270917-004 applied to both the 80960SA and the 80960SB. The 80960SA was then documented alone in data sheet 272206-001. The sections significantly changed between revisions -004 of the SA/SB data sheet and 272206-001 of the SA data sheet were:

Section	Last Rev.	Description
2.3 Connection Recommendations (pg. 11)	-004	Deleted corresponding graph of open drain voltage vs. output current.
Figure 6. Typical Supply Current vs. Case Temperature (pg. 11) Figure 7. Typical Current vs. Frequency (Room Temp) (pg. 12) Figure 8. Typical Current vs. Frequency (Hot Temp) (pg. 12)	-004	Regraphed new data in three graphs instead of two.
Table 5. DC Characteristics (pg. 15)	-004	Input Leakage Current (I_{LI2}) Specification added to accurately describe leakage of $\overline{INT0}$ and $\overline{LOCK}$ as inputs. I_{CC} max reduced: Power Supply Current: Was: Is: 10 MHz 280 240 16 MHz 350 300

NOTES:
Page numbers refer to 80960SA data sheet number 272206-001.

Section	Last Rev.	Description
Table 6. 80960SA AC Characteristics (10 MHz) (pg. 17) Table 7. 80960SA AC Characteristics (16 MHz) (pg. 18).	-004	T_7 minimum specification improved: Power Supply Current: Was: Is: 10 MHz 24 ns T_1 - 11 ns 16 MHZ 15 ns T_1 - 11 ns
Table 8. 80960SA AC Characteristics (20 MHz) (pg. 19)	-004	New 20 MHz specification table added for 80960SA C-step.
Table 11. 80960SA PLCC Pinout — In Pin Order (pg. 26)	-004	θ_{JA} increased to reflect smaller die size and lower I_{CC}.
Table 11. 80960SA PLCC Pinout — In Pin Order (pg. 26)	-004	θ_{JA} and θ_{JC} increased to reflect smaller die size and lower I_{CC}.

NOTES:
Page numbers refer to 80960SA data sheet number 272206-001.

The sections significantly changed between revisions -003 and -004 of the 80960SA/SB Data Sheet were:

Section	Last Rev.	Description
DC Characteristics	-003	Operating temperature for PLCC package changed: WAS: T_{CASE} = 0°C to +100°C IS: T_{CASE} = 0°C to +85°C The test program has not changed.
Table 9. 80960SA and 80960SB QFP Pinout — In Pin Order	-003	Signal A12 incorrectly shown as Pin 28; is now correctly shown as Pin 38. Note added to clarify No Connect Pins.

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Телефон: 8 (812) 309-75-97 (многоканальный)
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Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А