PM6680A

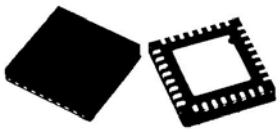
Dual synchronous step-down controller with adjustable output voltages plus LDO

Features

- 6 V to 36 V input voltage range
- Adjustable output voltages
- 5V LDO delivers 100 mA peak current
- 1.237 V ± 1 % reference voltage available externally
- Current sensing using low side MOSFETs $R_{DS(on)}$
- Valley current sensing
- Soft-start internally fixed at 2ms
- Soft output discharge
- Latched OVP and UVP
- Selectable pulse skipping at light loads
- Selectable minimum frequency (33 kHz) in pulse skip mode
- 5mW maximum quiescent power
- Independent power good signals
- Output voltage ripple compensation
- Thermal shutdown

Applications

- Embedded computer system
- FPGA system power
- Industrial applications on 24 V
- High performance and high density DC/DC modules



VFQFPN-32 5X5

Description

PM6680A is a dual step-down controller specifically designed to provide extremely high efficiency conversion, with loss less current sensing technique. The constant on-time architecture assures fast load transient response and the embedded voltage feed-forward provides nearly constant switching frequency operation. An embedded integrator control loop compensates the DC voltage error due to the output ripple. Pulse skipping technique increases efficiency at very light load. Moreover a minimum switching frequency of 33 kHz is selectable to avoid audio noise issues. The PM6680A provides a selectable switching frequency, allowing three different values of switching frequencies for the two switching sections. The output voltages OUT1 and OUT2 can be adjusted from 0.9 V to 5 V and from 0.9 V to 3.3 V respectively.

Table 1. Device summary

Order codes	Package	Packaging
PM6680A	VFQFPN-32 5X5 (exposed pad)	Tube
PM6680ATR		Tape and reel

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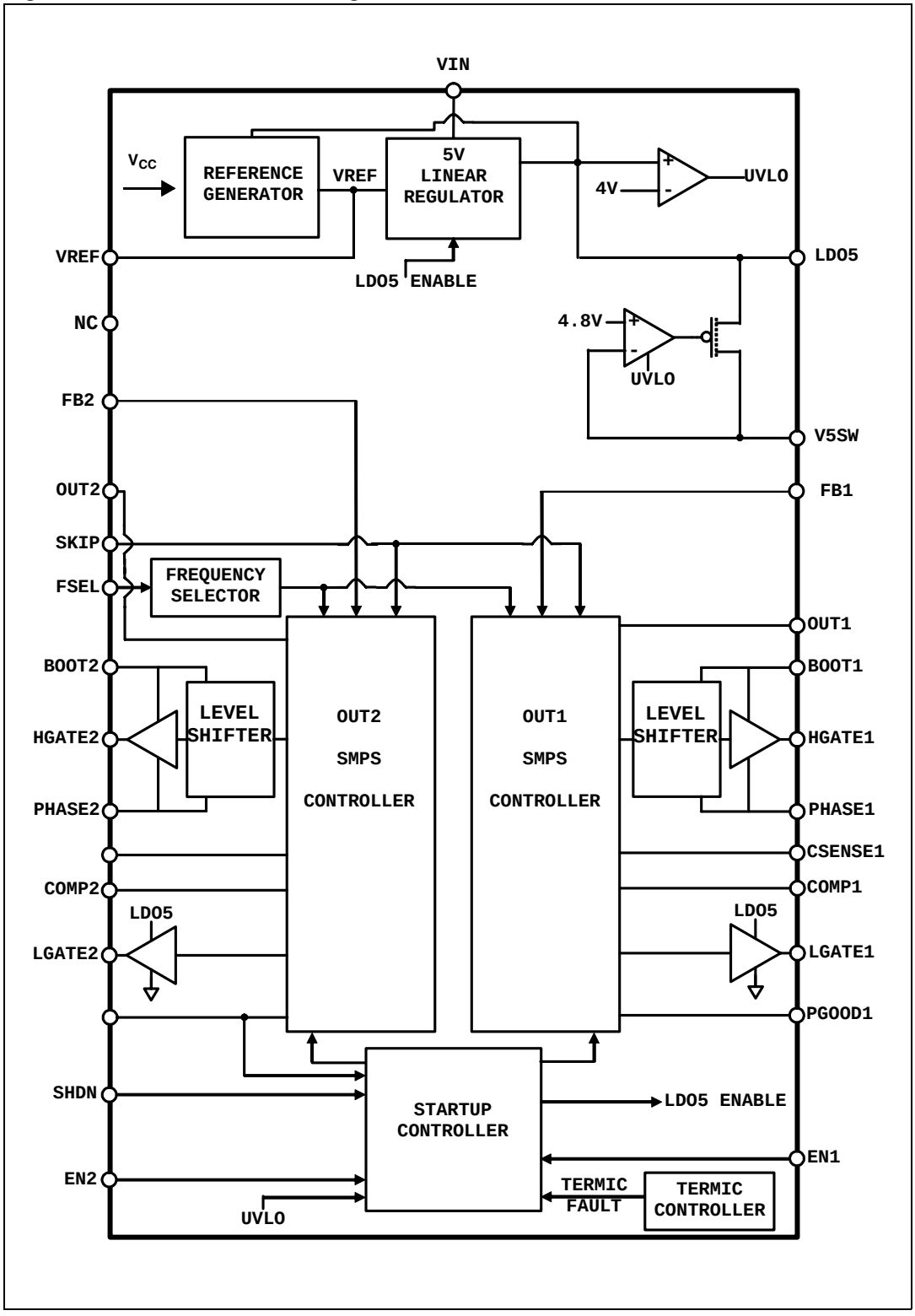
1 Block diagram

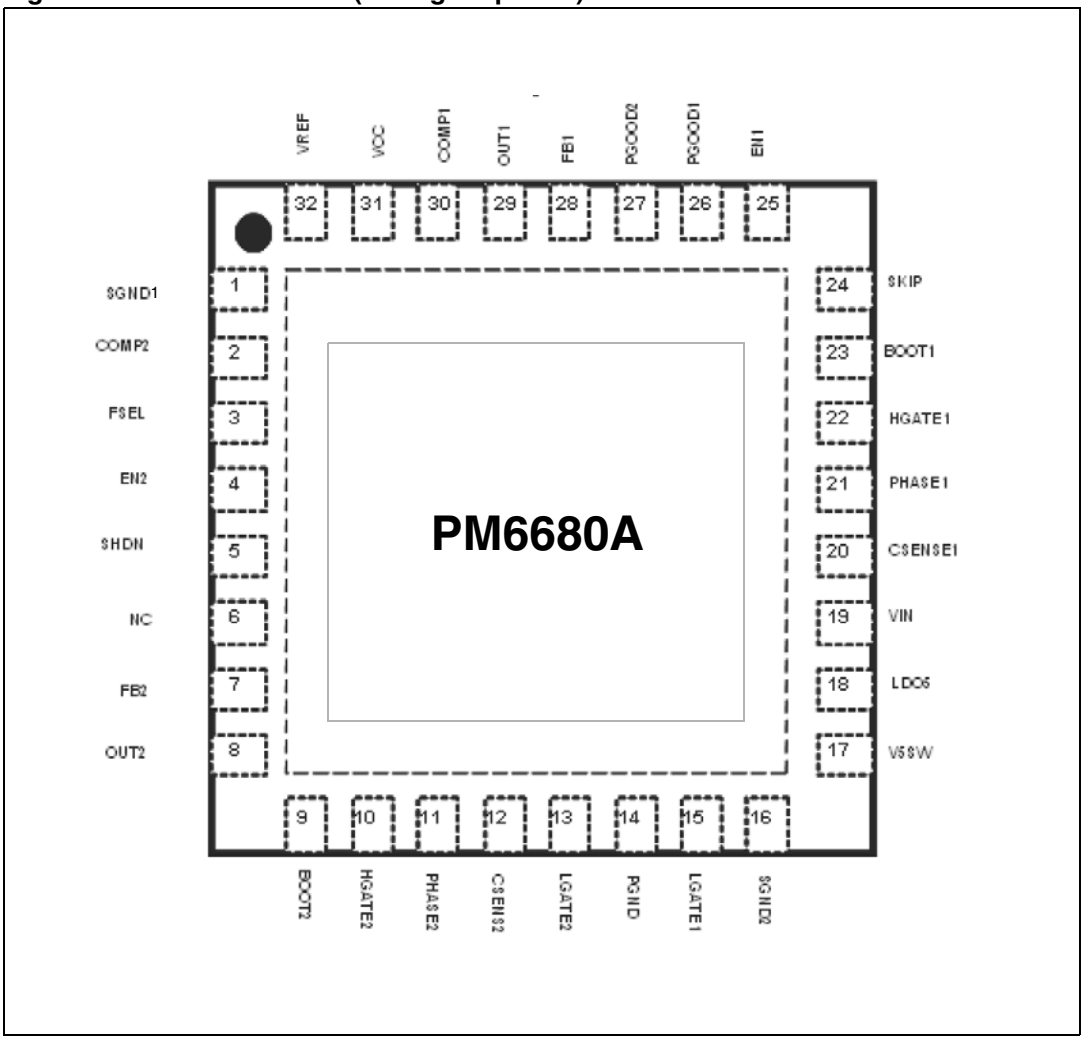
Figure 1. Functional block diagram



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Functions

Table 2. Pin functions

N°	Pin	Function
1	SGND1	Signal ground. Reference for internal logic circuitry. It must be connected to the signal ground plan of the power supply. The signal ground plan and the power ground plan must be connected together in one point near the PGND pin.
2	COMP2	DC voltage error compensation pin for the switching section 2
3	FSEL	Frequency selection pin. It provides a selectable switching frequency, allowing three different values of switching frequencies for the switching sections.
4	EN2	Enable input for the switching section 2. • The section 2 is enabled applying a voltage greater than 2.4 V to this pin. • The section 2 is disabled applying a voltage lower than 0.8 V. When the section is disabled the High Side gate driver goes low and Low Side gate driver goes high. If both EN1 and EN2 pins are low and SHDN pin is high the device enters in standby mode.
5	SHDN	Shutdown control input. • The device switch off if the SHDN voltage is lower than the device off thershold (Shutdown mode) • The device switch on if the SHDN voltage is greater than the device on threshold. The SHDN pin can be connected to the battery through a voltage divider to program an undervoltage lockout. In shutdown mode, the gate drivers of the two switching sections are in high impedance (high-Z).
6	NC	Not connected.
7	FB2	Feedback input for the switching section 2 This pin is connected to a resistive voltage-divider from OUT2 to PGND to adjust the output voltage from 0.9 V to 3.3 V.
8	OUT2	Output voltage sense for the switching section 2.This pin must be directly connected to the output votage of the switching section.
9	BOOT2	Bootstrap capacitor connection for the switching section 2. It supplies the high-side gate driver.
10	HGATE2	High-side gate driver ouput for section 2. This is the floating gate driver output.
11	PHASE2	Switch node connection and return path for the high side driver for the section 2.It is also used as negative current sense input.
12	CSENSE2	Positive current sense input for the switching section 2. This pin must be connected through a resistor to the drain of the synchronous rectifier (R_{DSON} sensing) to obtain a positive current limit threshold for the power supply controller.
13	LGATE2	Low-side gate driver output for the section 2.
14	PGND	Power ground. This pin must be connected to the power ground plan of the power supply.
15	LGATE1	Low-side gate driver output for the section 1.
16	SGND2	Signal ground for analog circuitry. It must be connected to the signal ground plan of the power supply.

Table 2. Pin functions (continued)

N°	Pin	Function
17	V5SW	Internal 5 V regulator bypass connection. • If V5SW is connected to OUT5 (or to an external 5 V supply) and V5SW is greater than 4.9 V, the LDO5 regulator shuts down and the LDO5 pin is directly connected to OUT5 through a 3 Ω (max) switch. If V5SW is connected to GND, the LDO5 linear regulator is always on.
18	LDO5	5V internal regulator output. It can provide up to 100 mA peak current. LDO5 pin supplies embedded low side gate drivers and an external load.
19	VIN	Device supply voltage input and battery voltage sense. A bypass filter (4 Ω and 4.7 µF) between the battery and this pin is recommended.
20	CSENSE1	Positive current sense input for the switching section 1. This pin must be connected through a resistor to the drain of the synchronous rectifier (R_{DSON} sensing) to obtain a positive current limit threshold for the power supply controller.
21	PHASE1	Switch node connection and return path for the high side driver for the section 1.It is also used as negative current sense input.
22	HGATE1	High-side gate driver ouput for section 1. This is the floating gate driver output.
23	BOOT1	Bootstrap capacitor connection for the switching section 1. It supplies the high-side gate driver.
24	SKIP	Pulse skipping mode control input. • If the pin is connected to LDO5 the PWM mode is enabled. • If the pin is connected to GND, the pulse skip mode is enabled. • If the pin is connected to VREF the pulse skip mode is enabled but the switching frequency is kept higher than 33 kHz (No-audible puse skip mode).
25	EN1	Enable input for the switching section 1. • The section 1 is enabled applying a voltage greater than 2.4 V to this pin. • The section 1 is disabled applying a voltage lower than 0.8 V. When the section is disabled the High Side gate driver goes low and Low Side gate driver goes high.
26	PGOOD1	Power Good ouput signal for the section 1. This pin is an open drain ouput and when the ouput of the switching section 1 is out of +/- 10 % of its nominal value.It is pulled down.
27	PGOOD2	Power Good ouput signal for the section 2. This pin is an open drain ouput and when the ouput of the switching section 2 is out of +/- 10 % of its nominal value.It is pulled down.
28	FB1	Feedback input for the switching section 1. This pin is connected to a resistive voltage-divider from OUT1 to PGND to adjust the output voltage from 0.9 V to 5.5 V.
29	OUT1	Output voltage sense for the switching section 1.This pin must be directly connected to the output votage of the switching section.
30	COMP1	DC voltage error compensation pin for the switching section 1.
31	VCC	Device supply voltage pin. It supplies all the internal analog circuitry except the gate drivers (see LDO5). Connect this pin to LDO5.
32	VREF	Internal 1.237 V high accuracy voltage reference. It can deliver 50 µA. Bypass to SGND with a 100 nF capacitor to reduce noise.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings

Parameter		Value	Unit
V5SW, LDO5 to PGND		-0.3 to 6	V
VIN to PGND		-0.3 to 36	V
HGATEx and BOOTx, to PHASEx		-0.3 to 6	V
PHASEx to PGND		-0.6(1) to36	V
CSENSEx , to PGND		-0.6 to 42	V
CSENSEx to BOOTx		-6 to 0.3	V
LGATEx to PGND		-0.3 (2) to LDO5 +0.3	V
FBx, COMPx, SKIP, , FSEL,,VREF to SGND1,SGND2		-0.3 to Vcc+0.3	V
PGND to SGND1,SGND2		-0.3 to 0.3	V
SHDN,PGOODx, OUTx, VCC, ENx to SGND1,SGND2		-0.3 to 6	V
Power Dissipation at T_A = 25ºC		2.8	W
Maximum withstanding Voltage range test condition: CDF-AEC-Q100-002- “Human Body Model” acceptance criteria: “Normal Performance”	VIN	±1000	V
	Other pins	±2000	

1. PHASE to PGND up to -2.5 V for t < 10 ns
2. LGATEx to PGND up to -1 V for t < 40 ns

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	35	°C/W
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction operating temperature range	-40 to 125	°C

4 Electrical characteristics

Table 5. Electrical characteristics

T_A = -40 °C to 125 °C, unless otherwise specified. All parameters at operating temperature extremes are guaranteed by design and statistical analysis (not production tested).

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply section						
VIN	Input voltage range	Vout = Vref, LDO5 in regulation	5.5		36	V
V_{CC}	IC supply voltage		4.5		5.5	V
V_{V5SW}	Turn-ON voltage threshold			4.8	4.9	V
	Turn-OFF voltage threshold		4.6	4.75		V
	Hysteresis		20	50		mV
V_{V5SW}	Maximum operating range				5.5	V
$R_{DS(on)}$	LDO5 Internal bootstrap switch resistance	V5SW > 4.9 V		1.8	3	Ω
	OUTx,OUTx discharge-Mode On-resistance			18	25	Ω
	OUTx, OUTx discharge-Mode Synchronous rectifier Turn-on level		0.2	0.36	0.6	V
Pin	Operating power consumption	FBx > V_{REF}, Vref in regulation, V5WS to 5V			4	mW
Ish	Operating current sunk by V_{IN}	SHDN connected to GND,		20	30	µA
Isb	Operating current sunk by V_{IN}	ENx to GND, V5SW to GND		190	250	µA
Shutdown section						
V_{SHDN}	Device ON threshold		1.2	1.5	1.7	V
	Device OFF threshold		0.8	0.85	0.9	V
Soft start section						
	Soft start ramp time		2		3.5	ms
Current limit and zero crossing comparator						
I_{CSENSE}	Input bias current limit (1)		90	100	110	µA
	Comparator offset	V_{CSENSE} - V_{PGND}	-6		6	mV
	Zero crossing comparator offset	V_{PGND} - V_{PHASE}	-1		11	mV
	Fixed negative current limit threshold	V_{PGND} - V_{PHASE}		-120		mV

1. T_A = -25 °C to 125 °C

Table 5. Electrical characteristics (continued)
(T_A = -40 °C to 125 °C, unless otherwise specified. All parameters at operating temperature extremes are guaranteed by design and statistical analysis (not production tested).

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Minimum on time							
On time pulse width@Vin = 24 V		FSEL to GND	OUT1=3.3 V	595	700	805	ns
			OUT2=1.8 V	190	225	260	
		FSEL to VREF	OUT1=3.3 V	400	470	545	
			OUT2=1.8 V	145	170	200	
		FSEL to LDO5	OUT1=3.3 V	300	355	410	
			OUT2=1.8 V	105	125	145	
Minimum off time							
TOFFMIN @ Vin = 24 V					350	500	ns
Voltage reference							
VREF	Voltage accuracy	4V < VLDO5 < 5.5 V		1.224	1.236	1.249	V
	Load regulation	-100 µA < IREF < 100 µA		-4		4	mV
	Undervoltage lockout fault threshold	Falling edge of REF				0.95	mV
PWM comparator							
FB	Voltage accuracy			-909	900	909	mV
FB	Input bias current				0.1		µA
COMP	Over voltage clamp	Normal mode			250		mV
		Pulse skip mode			60		
COMP	Under voltage clamp				-150		
Line regulation							
		Both SMPS, 6V < V_{IN} < 36V (2)				1	%
LDO5 linear regulation							
VLDO5	LDO5 linear output voltage	6 V < V_{IN} < 36 V, 0 < ILDO5 < 50 mA		4.9	5.0	5.1	V
	LDO5 line regulation	6 V < V_{IN} < 36 V, ILDO5 = 20 mA ,				0.004	%/V
ILDO5	LDO5 current limit	VLDO5 > UVLO		270	330	400	mA
ULVO	Under voltage lockout of LDO5			3.94	4	4.13	V

2. By demoboard test

Table 5. Electrical characteristics (continued)
(T_A = -40 °C to 125 °C, unless otherwise specified. All parameters at operating temperature extremes are guaranteed by design and statistical analysis (not production tested).

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
High and low gate drivers						
	HGATE driver on-resistence	HGATEx high state (pullup)		2.0	3	Ω
		HGATEx low state (pulldown)		1.6	2.7	Ω
	LGATE driver on-resistance	LGATEx high state (pullup)		1.4	2.1	Ω
		LGATEx low state (pulldown)		0.8	1.2	Ω
PGOOD pins UVP/OVP protections						
OVP	Over voltage threshold	Both SMPS sections with respect to VREF	112	116	120	%
UVP	Under voltage threshold		65	68	71	%
PGOOD1,2	Upper threshold (VFB-VREF)		107	110	113	%
	Lower threshold (VFB-VREF)		88	91	94	%
IPGOOD1,2	PGOOD leakage current	VPGOOD1,2 forced to 5.5 V			1	µA
VPGOOD1,2	Output low voltage	ISink = 4 mA		150	250	mV
Thermal shutdown						
T_{SDN}	Shutdown temperature			150		°C
Power management pins						
EN1,2	SMPS disabled level				0.8	V
	SMPS enabled level		2.4			
FSEL	Frequency selection range	Low level (3)			0.5	V
		Middle level (3)	1.0		VLDO5-1.5	
		High level (3)	VLDO5-0.8			
SKIP	Pulse skip mode	(3)			0.5	V
	PWM mode	(3)	1.0		VLDO5-1.5	
	Ultrasonic mode	(3)	VLDO5-0.8			
	Input leakage current	VEN1,2 = 0 to 5 V			1	µA
		VSKIP = 0 to 5 V			1	
		VSHDN = 0 to 5 V			1	
		VFSEL = 0 to 5 V			1	

3. By design

5 Typical operating characteristics

FSEL=GND(200/300 kHz), SKIP=GND(skip mode), V5SW=EXT5V (external 5 V power supply connected), input voltage VIN = 24 V, SHDN, EN1 and EN2 high, OUT1 = 3.3 V, OUT2 = 1.8 V, no load unless specified)

Figure 3. OUT1 = 3.3 V efficiency

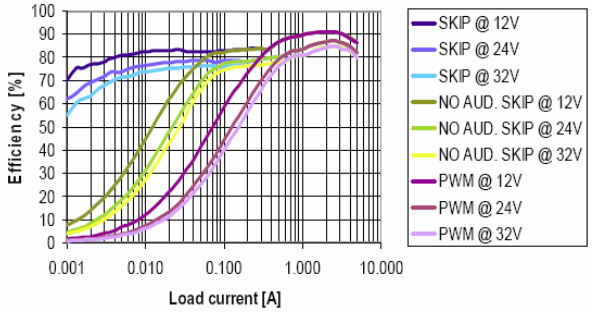


Figure 4. OUT2 = 1.8 V efficiency

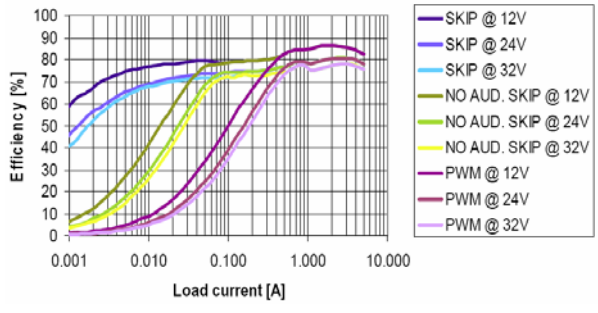


Figure 5. PWM no load battery current vs input voltage

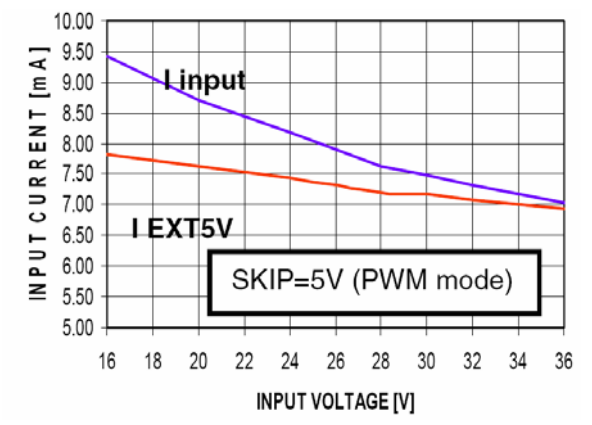


Figure 6. Skip no load battery current vs input voltage

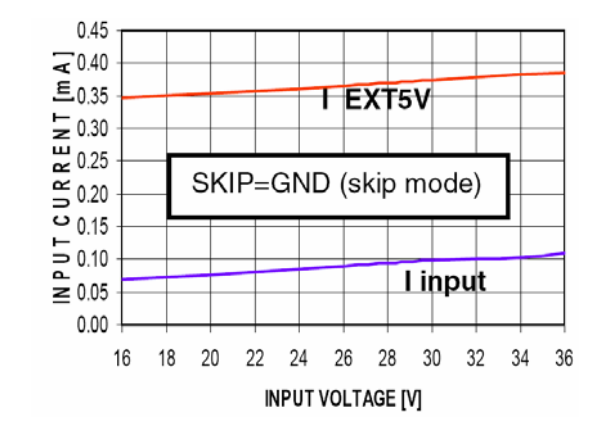


Figure 7. No-audible skip no load battery current vs input voltage

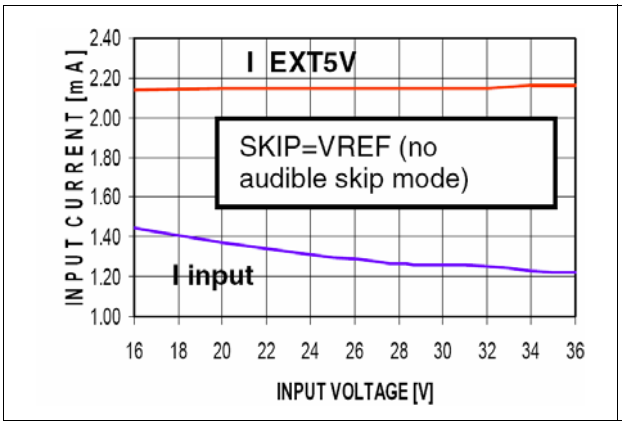


Figure 8. Standby mode input battery current vs input voltage

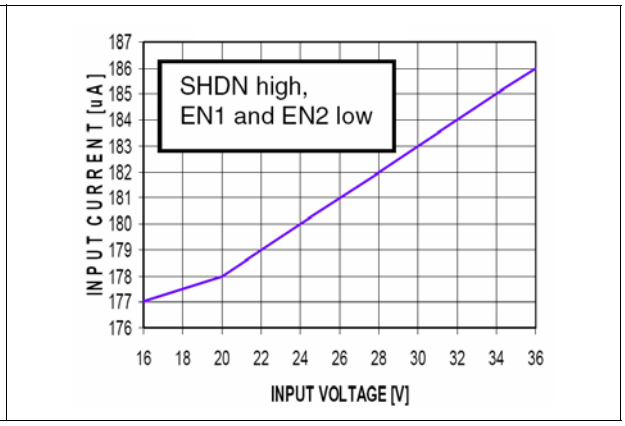


Figure 9. Shutdown mode input battery current vs input voltage

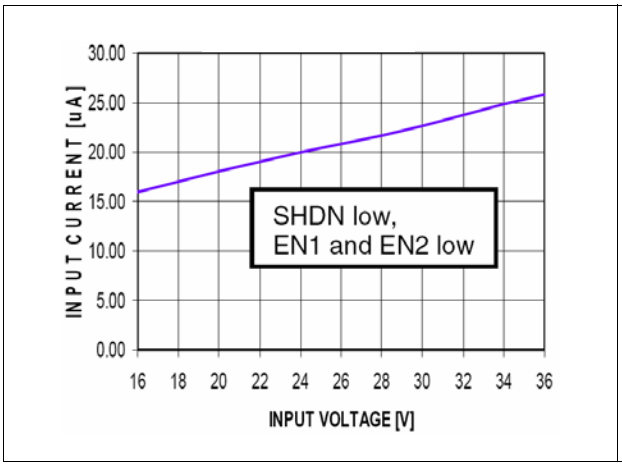


Figure 10. LDO5 vs output current

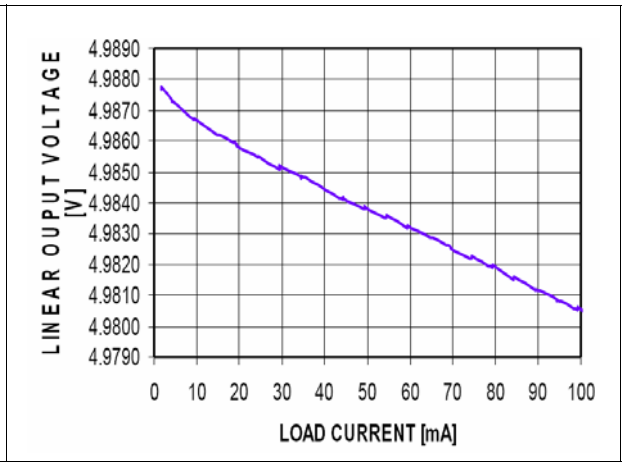


Figure 11. OUT1 = 3.3 V switching frequency

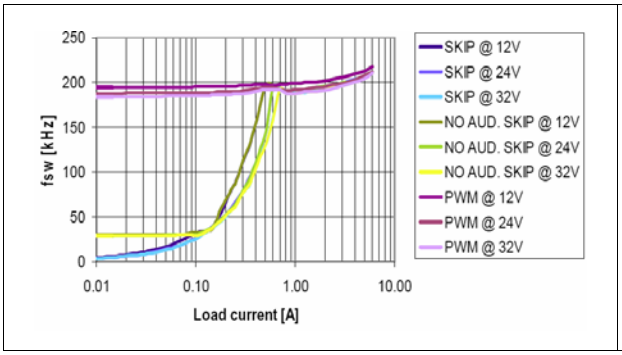


Figure 12. OUT2 = 1.8 V switching frequency

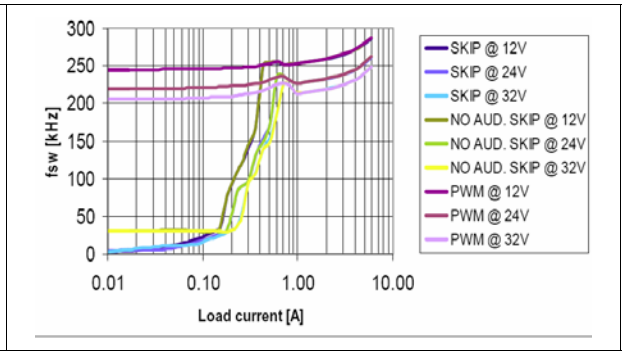


Figure 13. OUT1 = 3.3 V load regulation

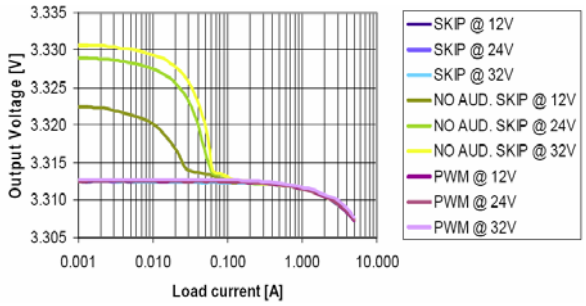


Figure 14. OUT2 = 1.8 V load regulation

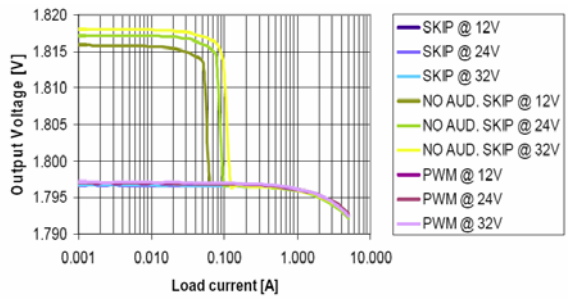


Figure 15. Voltage reference vs load current

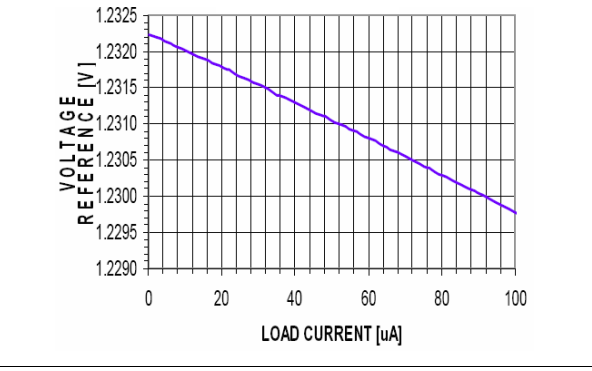


Figure 16. OUT1, OUT2 and LDO5 Power-Up

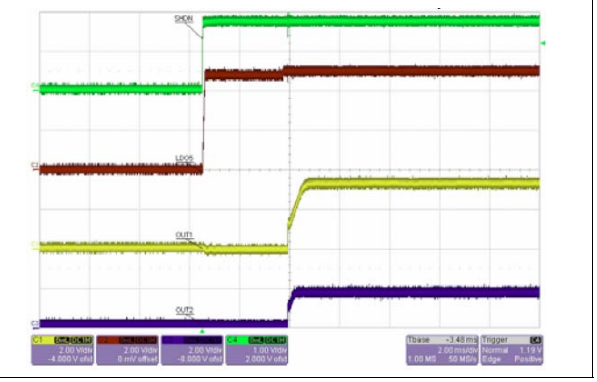


Figure 17. OUT1 = 3.3V load transient 0→2A

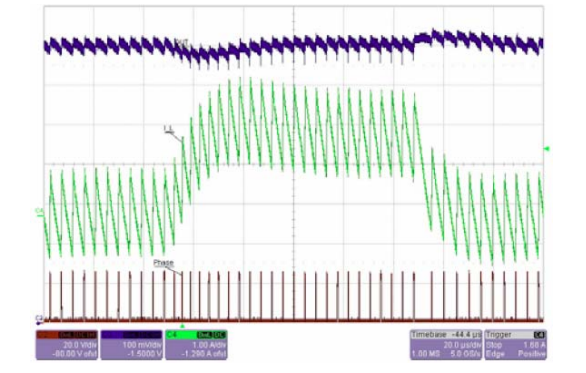


Figure 18. OUT2 = 1.8V load transient 0→2A

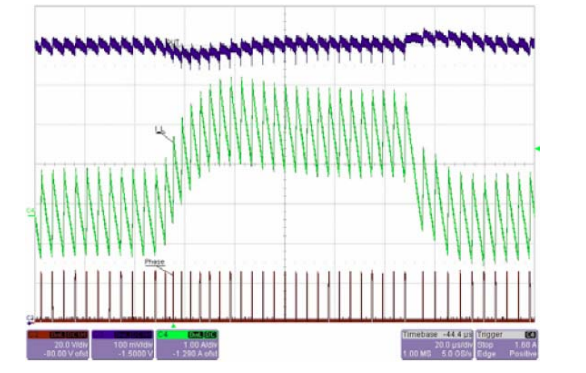


Figure 19. 3.3 V soft start (1Ω load)

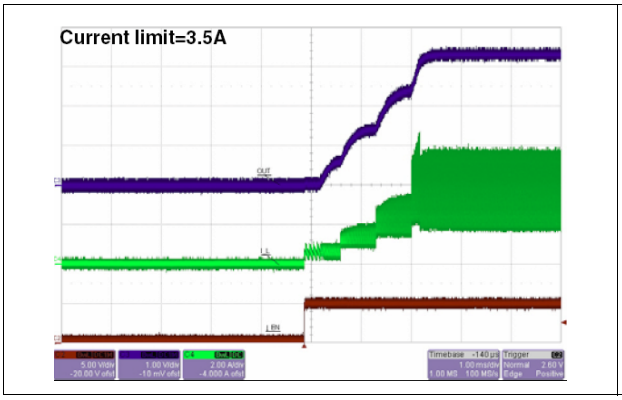


Figure 20. 1.8 V soft start (0.6Ω load)

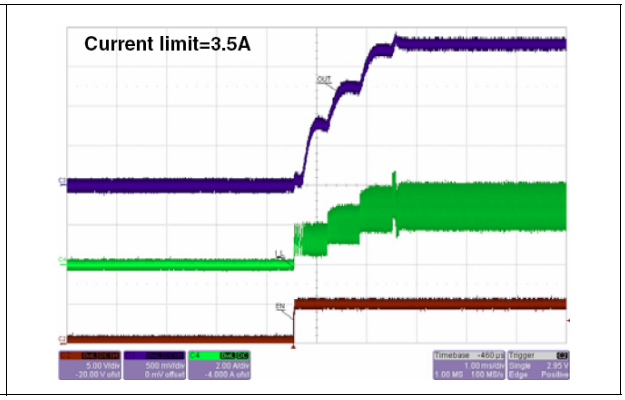


Figure 21. OUT1 = 3.3 V soft end (no load)

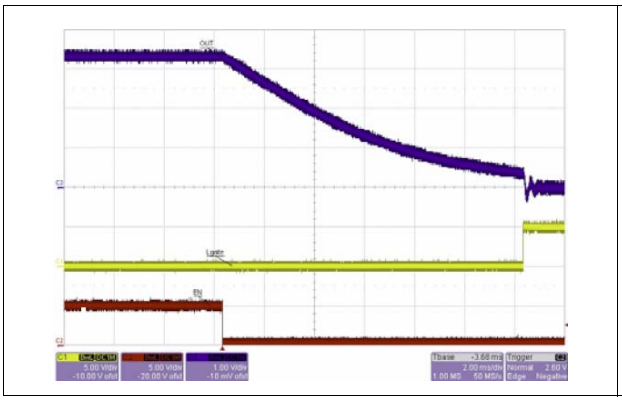


Figure 22. OUT2 = 1.8 V soft end (no load)

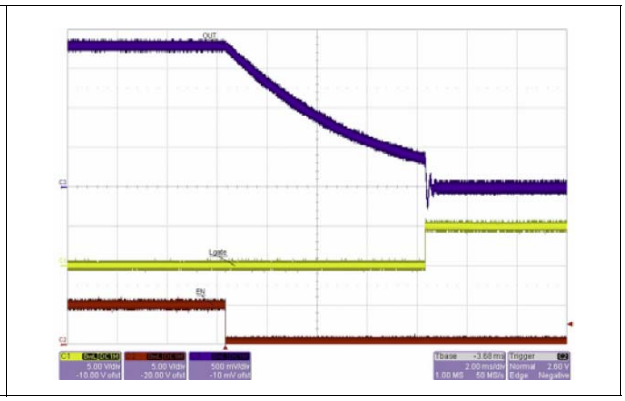


Figure 23. OUT1 = 3.3 V soft end (0.8 load)

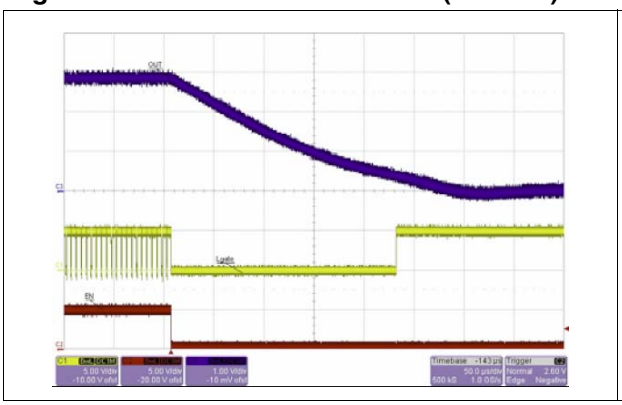


Figure 24. OUT2 = 1.8 V soft end (0.6 load)

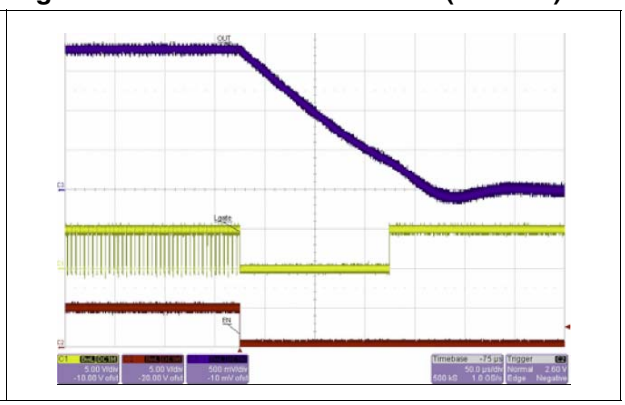


Figure 25. 3.3 V no-audible skip mode

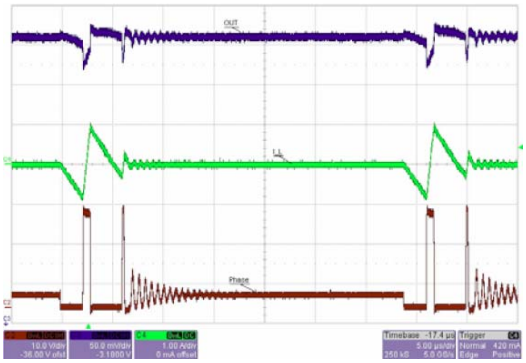
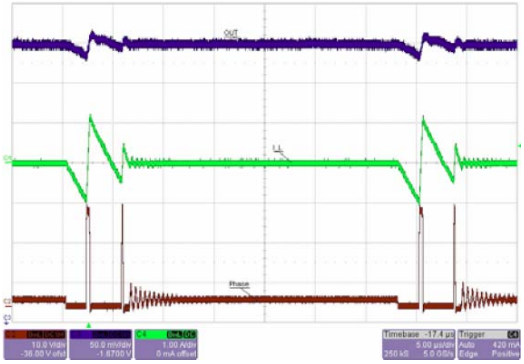
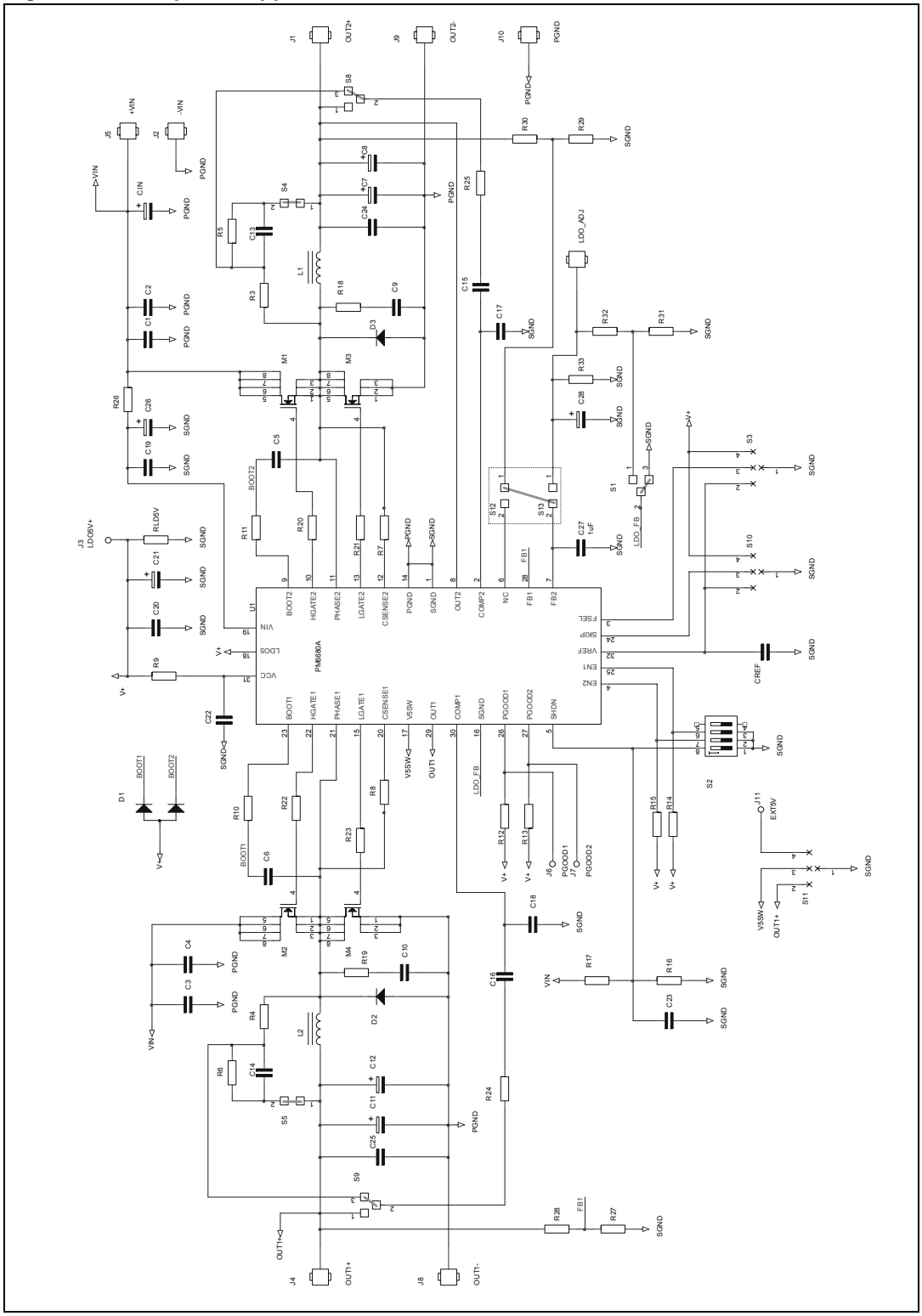


Figure 26. 1.8 V no-audible skip mode



6 Application schematic

Figure 27. Simplified application schematic



7 Device description

The PM6680A is a dual step-down controller dedicated to provide logic voltages for industrial automation applications.

It is based on a Constant On Time control architecture. This type of control offers a very fast load transient response with a minimum external component count. A typical application circuit is shown in Figure 3.

The PM6680A regulates two adjustable output voltages: OUT1 and OUT2. The switching frequency of the two sections can be adjusted to 200/300 kHz, 300/400 kHz or 400/500 kHz respectively. In order to maximize the efficiency at light load condition, a pulse skipping mode can be selected.

The PM6680A includes also a 5 V linear regulator (LDO5) that can power the switching drivers. If the output OUT1 regulates 5 V, in order to maximize the efficiency in higher consumption status, the linear regulator can be turned off and their outputs can be supplied directly from the switching outputs. The PM6680A provides protection versus overvoltage, undervoltage and over temperature as well as power good signals for monitoring purposes. An external 1.237 V reference is available.

7.1 Constant on time PWM control

If the SKIP pin is tied to 5 V, the device works in PWM mode. Each power section has an independent on time control.The PM6680A employees a pseudo-fixed switching frequency, Constant On Time (COT) controller as core of the switched mode section. Each power section has an independent COT control.

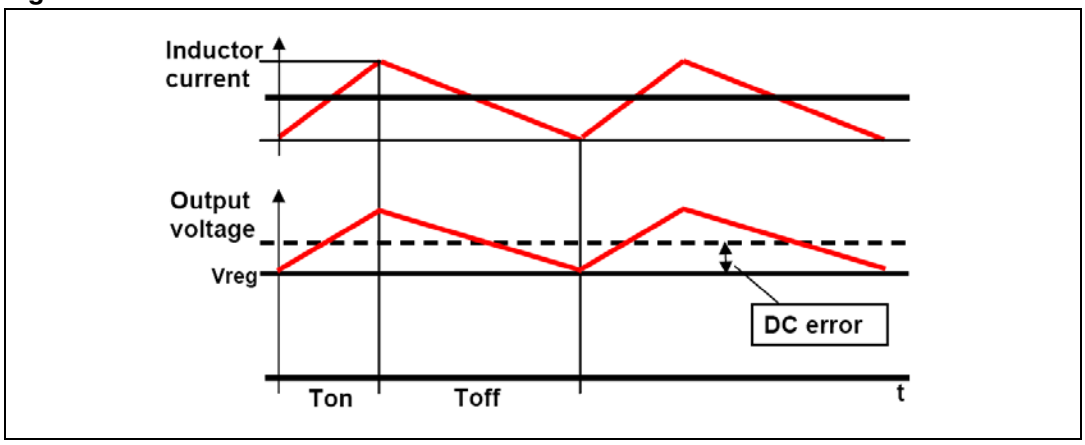
The COT controller is based on a relatively simple algorithm and uses the ripple voltage due to the output capacitor's ESR to trigger the fixed on-time one-shot generator. In this way, the output capacitor's ESR acts as a current sense resistor providing the appropriate ramp signal to the PWM comparator. On-time one-shot duration is directly proportional to the output voltage, sensed at the OUT1/OUT2 pins, and inversely proportional to the input voltage, sensed at the VIN pin, as follows:

Equation 1

$$T_{ON} = K \cdot \frac{V_{OUT}}{V_{IN}}$$

This leads to a nearly constant switching frequency, regardless of input and output voltages. When the output voltage goes lower than the regulated voltage Vreg, the on-time one shot generator directly drives the high side MOSFET for a fixed on time allowing the inductor current to increase; after the on time, an off time phase, in which the low side MOSFET is turned on, follows. *Figure 28* shows the inductor current and the output voltage waveforms in PWM mode.

Figure 28. Constant ON time PWM control



The duty cycle of the buck converter in steady state is:

Equation 2

$$D = \frac{V_{OUT}}{V_{IN}}$$

The PWM control works at a nearly fixed frequency f_{SW}:

Equation 3

$$f_{SW} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{on} \times \frac{V_{OUT}}{V_{IN}}} = 1/K_{on}$$

As mentioned the steady state switching frequency is theoretically independent from input voltage and from output voltage.

Actually the frequency depends on parasitic voltage drops that are present during the charging path(high side switch resistance, inductor resistance(DCR)) and discharging path(low side switch resistance, DCR).

As a result the switching frequency increases as a function of the load current.

Standard switching frequency values can be selected for both sections by pin FSEL as shown in the following table:

Table 6. FSEL pin selection: typical switching frequency

	Fsw@OUT1 = 3.3 V (kHz)	Fsw@OUT2 = 1.8 V (kHz)
FSEL = GND	195	335
FSEL = VREF	295	440
FSEL = LDO5	390	600

7.2 Constant on time architecture

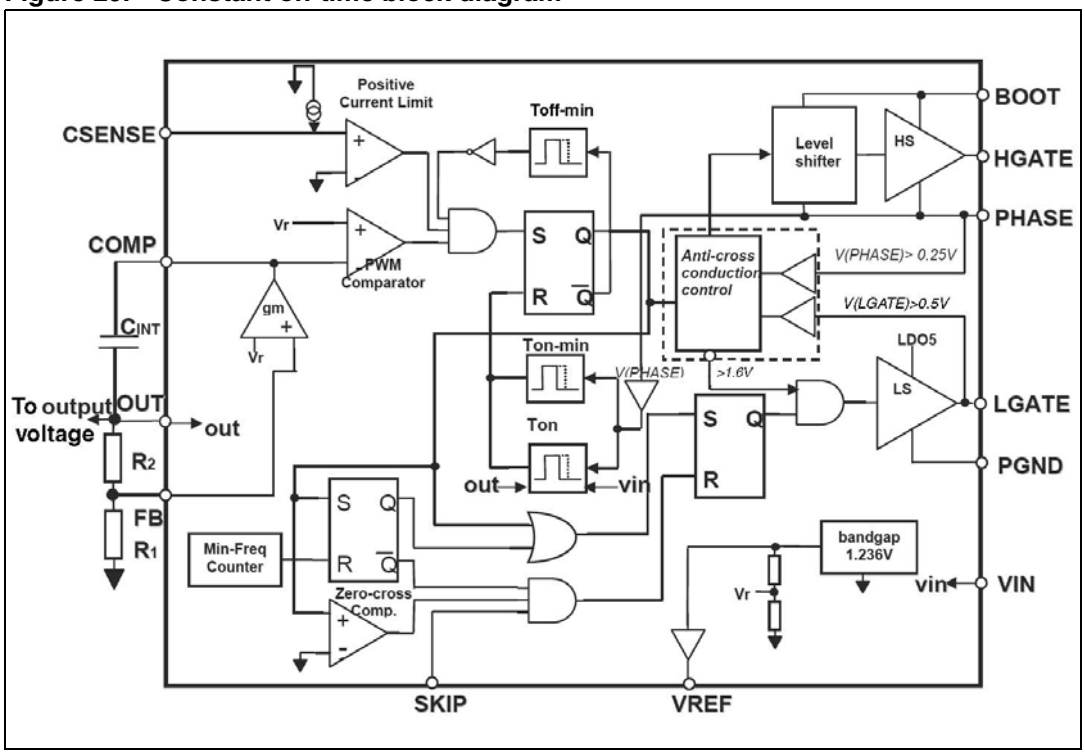
Figure 29 shows the simplified block diagram of a constant on time controller. A minimum off-time constrain (350 ns typ.) is introduced to allow inductor valley current sensing on synchronous switch. A minimum on-time (130 ns) is also introduced to assure the start-up switching sequence.

PM6680A has a one-shot generator for each power section that turns on the high side MOSFET when the following conditions are satisfied simultaneously: the PWM comparator is high, the synchronous rectifier current is below the current limit threshold, and the minimum off-time has timed out.

Once the on-time has timed out, the high side switch is turned off, while the synchronous switch is turned on according to the anti-cross conduction circuitry management.

When the negative input voltage at the PWM comparator (*Figure 29*), which is a scaled-down replica of the output voltage (see the external R1/R2 divider in *Figure 29*), reaches the valley limit (determined by internal reference Vr = 0.9 V), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

Figure 29. Constant on-time block diagram



In steady state the FB pin voltage is about Vr and the regulated output voltage depends on the external divider:

Equation 4

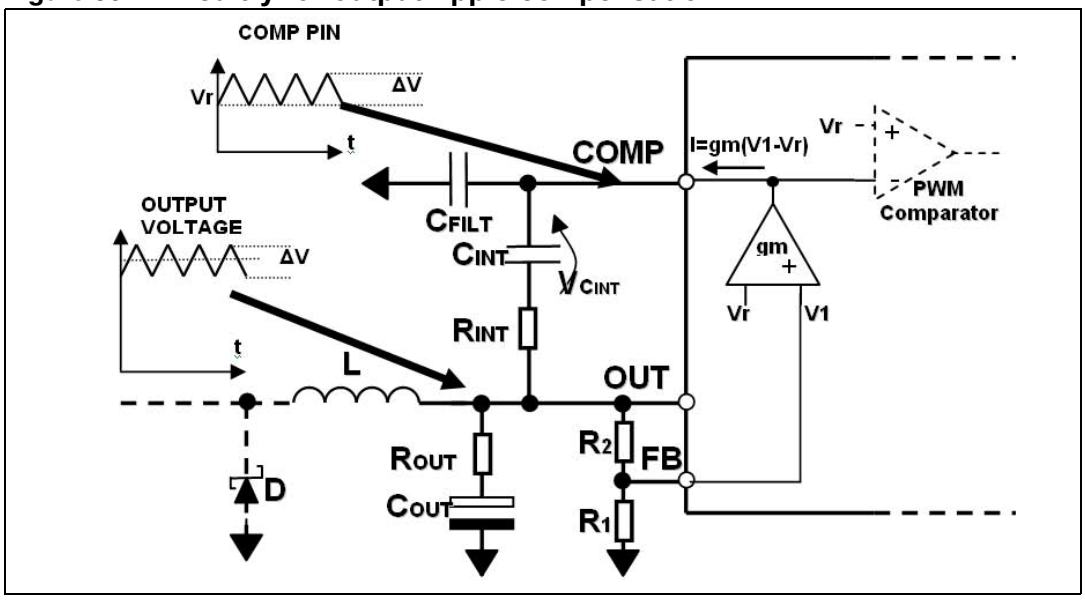
$$OUT = Vr \times \left(1 + \frac{R_2}{R_1}\right)$$

7.3 Output ripple compensation and loop stability

In a classic constant on time control, the system regulates the valley value of the output voltage and not the average value, as shown in *Figure 28* In this condition, the output voltage ripple is source of a DC static error.

To compensate this error, an integrator network can be introduced in the control loop, by connecting the output voltage to the COMP1/COMP2 (for the OUT1 and OUT2 sections respectively) pin through a capacitor C_{INT} as in *Figure 30*.

Figure 30. Circuitry for output ripple compensation



The integrator amplifier generates a current, proportional to the DC errors between the FB voltage and Vr, which decreases the output voltage in order to compensate the total static error, including the voltage drop on PCB traces. In addition, C_{INT} provides an AC path for the output ripple. In steady state, the voltage on COMP1/COMP2 pin is the sum of the reference voltage Vr and the output ripple (see *Figure 30*). In fact when the voltage on the COMP pin reaches Vr, a fixed Ton begins and the output increases.

For example, we consider Vout = 5 V with an output ripple of ΔV = 50 mV. Considering C_{INT} >> C_{FILT}, the C_{INT} DC voltage drop VC_{INT} is about 5 V -Vr + 25 mV = 4.125 V. C_{INT} assures an AC path for the output voltage ripple. Then the COMP pin ripple is a replica of the output ripple, with a DC value of Vr + 25 mV = 925 mV.

For more details about the output ripple compensation network, see the *Chapter 9.6: Closing the integrator loop on page 35* in the Design guidelines.

7.4 Pulse skip mode

If the SKIP pin is tied to ground, the device works in skip mode.

At light loads a zero-crossing comparator truncates the low-side switch on-time when the inductor current becomes negative. In this condition the section works in discontinuous conduction mode. The threshold between continuous and discontinuous conduction mode is:

Equation 5

$$ILOAD(SKIP) = \frac{V_{IN} - V_{OUT}}{2 \times L} \times T_{ON}$$

For higher loads the inductor current doesn't cross the zero and the device works in the same way as in PWM mode and the frequency is fixed to the nominal value.

Figure 31. PWM and pulse skip mode inductor current

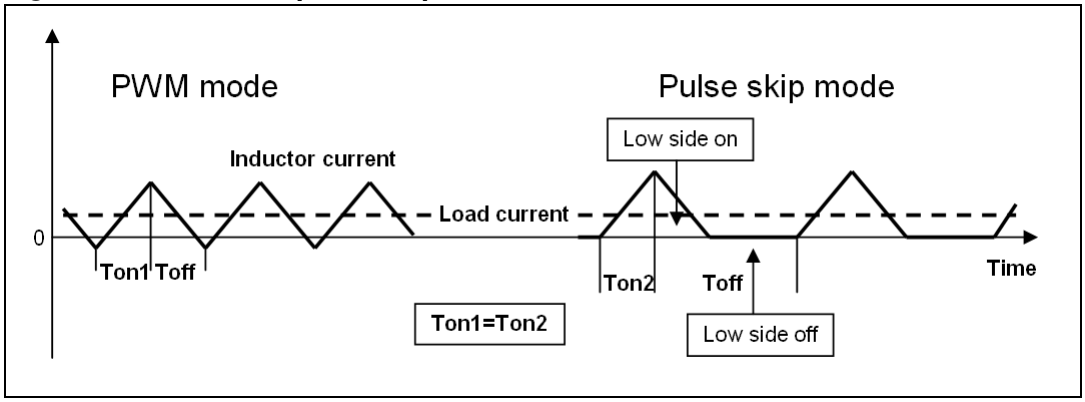


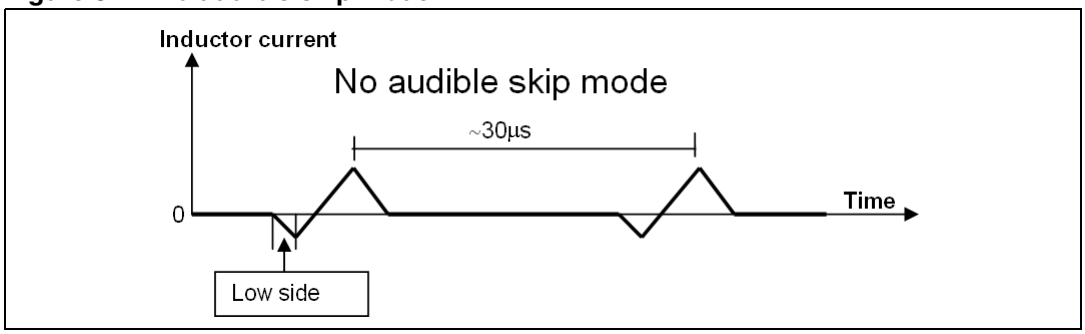
Figure 31 shows inductor current waveforms in PWM and SKIP mode. In order to keep average inductor current equal to load current, in SKIP mode some switching cycles are skipped. When the output ripple reaches the regulated voltage Vreg, a new cycle begins. The off cycle duration and the switching frequency depend on the load condition.

As a result of the control technique, losses are reduced at light loads, improving the system efficiency.

7.5 No-audible skip mode

If SKIP pin is tied to V_{REF}, a no-audible skip mode with a minimum switching frequency of 33 kHz is enabled. At light load condition, If there is not a new switching cycle within a 30 µs (typ.) period, a no-audible skip mode cycle begins.

Figure 32. No audible skip mode



The low side switch is turned on until the output voltage crosses about Vreg + 1 %. Then the high side MOSFET is turned on for a fixed on time period. Afterwards the low side switch is enabled until the inductor current reaches the zero-crossing threshold. This keeps the switching frequency higher than 33 kHz. As a consequence of the control, the regulated voltage can be slightly higher than Vreg (up to 1 %).

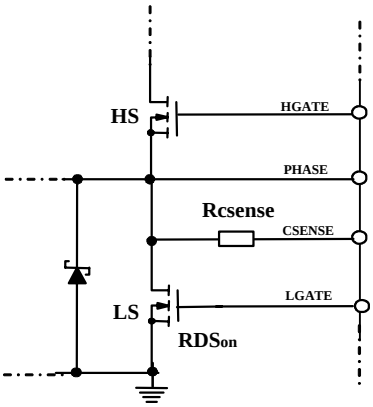
If, due to the load, the frequency is higher than 33 kHz, the device works like in skip mode.

No-audible skip mode reduces audio frequency noise that may occur in pulse skip mode at very light loads, keeping the efficiency higher than in PWM mode.

7.6 Current limit

The current-limit circuit employs a "valley" current-sensing algorithm. During the conduction time of the low side MOSFET the current flowing through it is sensed. The current-sensing element is the low side MOSFET on-resistance (*Figure 33*).

Figure 33. Rsense sensing technique



An internal 100 µA current source is connected to CSENSE pin and determines a voltage drop on RCSENSE. If the voltage across the sensing element is greater than this voltage drop, the controller doesn't initiate a new cycle. A new cycle starts only when the sensed current goes below the current limit.

Since the current limit circuit is a valley current limit, the actual peak current limit is greater than the current limit threshold by an amount equal to the inductor ripple current.

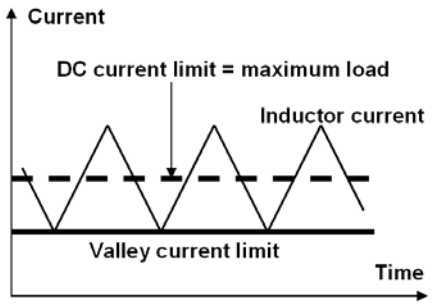
Moreover the maximum DC load is equal to the valley current limit plus half of the inductor ripple current:

Equation 6

$$I_{LOAD}(max) = I_{Lvalley} + \frac{\Delta I_L}{2}$$

The output current limit depends on the current ripple, as shown in *Figure 34*:

Figure 34. Current waveforms in current limit conditions



Being fixed the valley threshold, the greater the current ripple is, greater the DC output current is The valley current limit can be set with resistor RCSENSE:

Equation 7

$$R_{CSENSE} = \frac{R_{DS(on)} \times I_{Lvalley}}{Icsense}$$

Where I_{CSENSE} = 100 µA, RDSon is the drain-source on resistance of the low side switch. Consider the temperature effect and the worst case value in RDSon calculation.

The accuracy of the valley current threshold detection depends on the offset of the internal comparator (ΔV_{OFF}) and on the accuracy of the current generator (ΔI_{CSENSE})

Equation 8

$$\frac{\Delta I_{Lvalley}}{I_{Lvalley}} = \frac{\Delta I_{CSENSE}}{I_{CSENSE}} + \left[\frac{\Delta V_{OFF}}{R_{CSENSE} \times I_{CSENSE}} \times 100\right] + \frac{\Delta R_{CSENSE}}{R_{CSENSE}} + \frac{\Delta R_{SNS}}{R_{SNS}}$$

Where RSNS is the sensing element(RDSon)

PM6680A provides also a fixed negative peak current limit to prevent an excessive reverse inductor current when the switching section sinks current from the load in PWM mode. This negative current limit threshold is measured between PHASE and SGND pins, comparing the magnitude drop on the PHASE node during the conduction time of the low side MOSFET with an internal fixed voltage of 120 mV.

The negative valley-current limit I_{NEG} (if the device works in PWM mode) is given by:

Equation 9

$$I_{NEG} = \frac{120mV}{R_{DSon}}$$

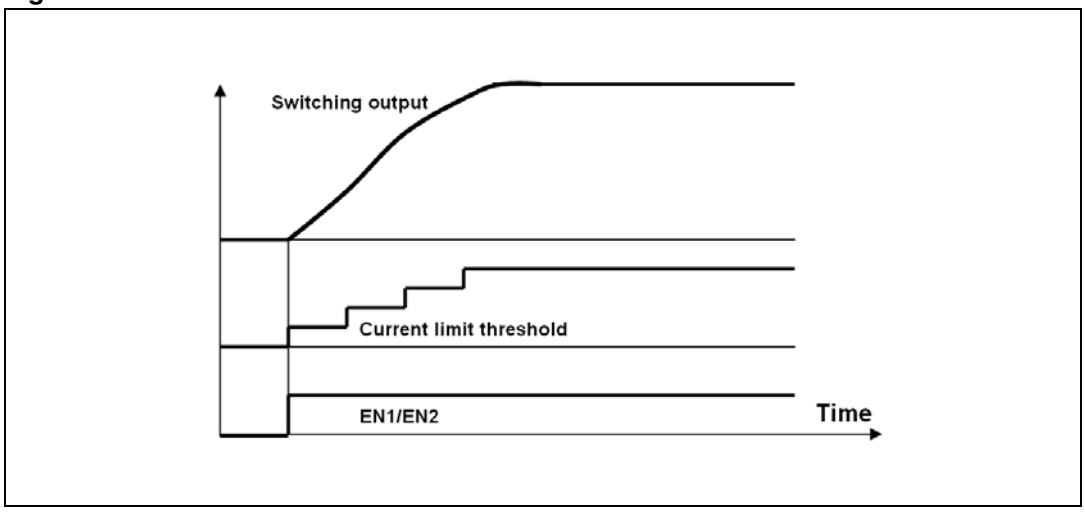
7.7 Soft start and soft end

Each switching section is enabled separately by asserting high EN1/EN2 pins respectively. In order to realize the soft start, at the startup the overcurrent threshold is set 25 % of the nominal value and the undervoltage protection (see related sections) is disabled. The controller starts charging the output capacitor working in current limit. The overcurrent threshold is increased from 25 % to 100 % of the nominal value with steps of 25 % every 700 µs (typ.). After 2.8 ms (typ.) the undervoltage protection is enabled. The soft start time is not programmable. A minimum capacitor C_{INT} is required to ensure a soft start without any overshoot on the output:

Equation 10

$$C_{INT} \geq \frac{6\mu A}{\frac{I_{Lvalley}}{4} + \frac{\Delta I_L}{2}} \times C_{out}$$

Figure 35. Soft start waveforms



When a switching section is turned off (EN1/EN2 pins low), the controller enters in soft end mode.The output capacitor is discharged through an internal 18 Ω p-MOSFET switch; when the output voltage reaches 0.3 V, the low-side MOSFET turns on, keeping the output to ground. The soft end time also depends on load condition.

7.8 Gate drivers

The integrated high-current drivers allow to use different power MOSFETs. The high side driver MOSFET uses a bootstrap circuit which is indirectly supplied by LDO5 output. The BOOT and PHASE pins work respectively as supply and return rails for the HS driver.

The low side driver uses the internal LDO5 output for the supply rail and PGND pin as return rail.

An important feature of the gate drivers is the adaptive anti-cross conduction protection, which prevents high side and low side MOSFETs from being on at the same time. When the high side MOSFET is turned off the voltage at the phase node begins to fall. The low side MOSFET is turned on when the voltage at the phase node reaches an internal threshold. When the low side MOSFET is turned off, the high side remains off until the LGATE pin voltage goes approximatively under 1 V.

The power dissipation of the drivers is a function of the total gate charge of the external power MOSFETs and the switching frequency, as shown in the following equation:

Equation 11

$$P_{driver} = V_{driver} \times Q_g \times f_{SW}$$

Where V_{driver} is the 5 V driver supply.

7.9 Reference voltage and bandgap

The 1.237 V (typ.) internal bandgap voltage is accurate to ±1 % over the temperature range. It is externally available (VREF pin) and can supply up to ± 100 µA and can be used as a voltage threshold for the multifunction pins FSEL and SKIP to select the appropriate working mode. Bypass VREF to ground with a 100 nF minimum capacitor.

If VREF goes below 0.87 V (typ.) , the system detects a fault condition and all the circuitry is turned off. A toggle on the input voltage (power on reset) or a toggle on SHDN pin is necessary to restart the device.

An internal divider of the bandgap provides a voltage reference Vr of 0.9 V. This voltage is used as reference for the linear and the switching regulators outputs. The overvoltage protection, the undervoltage protection and the power good signals are referred to Vr.

7.10 Internal linear regulator

The PM6680A has an internal linear regulator providing 5 V (LDO5) at ± 2 % accuracy. High side drivers, low side drivers and most of internal circuitry are supplied by LDO5 output through VCC pin (an external RC filter may be applied between LDO5 and VCC). The linear regulator can provide an average output current of 50 mA and a peak output current of 100 mA. Bypass LDO5 output with a minimum 1µF ceramic capacitor and a 4,7 µF tantalum capacitor (ESR $\geq$ 2 Ω). If the 5 V output goes below 4 V, the system detects a fault condition and all the circuitry is turned off. A power on reset or a toggle on SHDN pin is necessary to restart the device.

V5SW pin allows to keep the 5 V linear regulator always active or to enable the internal bootstrap-switchover function: if the 5 V switching output is connected to V5SW, when the voltage on V5SW pin is above 4.8 V, an internal 3.0 Ω max p-channel MOSFET switch connects V5SW pin to LDO5 pin and simultaneously LDO5 shuts down. This configuration allows to achieve higher efficiency. V5SW can be connected also to an external 5 V supply.

LDO5 regulator turns off and LDO5 is supplied externally. If V5SW is connected to ground, the internal 5 V regulator is always on and supplies LDO5 output

Table 7. V5SW multifunction pin

V5SW	Description
GND	The 5 V linear regulator is always turned on and supplies LDO5 output.
Switching 5 V output	The 5 V linear regulator is turned off when the voltage on V5SW is above 4.8 V and the LDO5 output is supplied by the switching 5 V output.
External 5 V supply	The 5 V linear regulator is turned off when the voltage on V5SW is above 4.8 V and LDO5 output is supplied by the external 5 V.

7.11 Power up sequencing and operative modes

Let us consider SHDN, EN1 and EN2 low at the beginning. An external voltage is applied as input voltage. The device is in shutdown mode.

When the SHDN pin voltage is above the shutdown device on threshold (1.5 V typ.), the controller begins the power-up sequence. All the latched faults are cleared. LDO5 undervoltage control is blanked for 4 ms and the internal regulator LDO5 turns on. If the LDO5 output is above the UVLO threshold after this time, the device enters in standby mode. The switching outputs are kept to ground by turning on the low side MOSFETs.

When EN1 and EN2 pins are forced high the switching sections begin their soft start sequence.

Table 8. Operatives modes

Mode	Conditions	Description
Run	SHDN is high, *EN1/EN2* pins are high	Switching regulators are enabled; internal linear regulators outputs are enabled.
Standby	Both *EN1/EN2* pins are low and *SHDN* pin is high	Internal Linear regulators active (LDO5 is always on). In Standby mode *LGATE1/LGATE2* pins are forced high while *HGATE1/HGATE2* pins are forced low.
Shutdown	*SHDN* is low	All circuits off.

8 Monitoring and protections

Power good signals

The PM6680A provides two independent power good signals: one for each switching section (PGOOD1/PGOOD2).

PGOOD1/PGOOD2 signals are low if the output voltage is out of ± 10 % of the designed set point or during the soft-start, standby and shutdown mode.

Thermal protection

The PM6680A has a thermal protection to preserve the device from overheating. The thermal shutdown occurs when the die temperature goes above +150 °C. In this case all internal circutry is turned off and the power sections are turned off after the discharge mode.

A power on reset or a toggle on the SHDN pin is necessary to restart the device.

Overvoltage protection

When the switching output voltage is about 115 % of its nominal value, a latched overvoltage protection occurs. In this case, the synchronous rectifier immediately turns on while the high-side MOSFET turns off. The output capacitor is rapidly discharged and the load is preserved from being damaged. The overvoltge protection is also active during the soft start. Once an overvoltage protection has been detected, a toggle on SHDN, EN1/EN2 pins or a power on reset is necessary to exit from the latched state.

Undervoltage protection

When the switching output voltage is below 70 % of its nominal value, a latched undervoltage protection occurs. In this case the switching section is immediately disabled and both switches are open. The controller enters in soft end mode and the output is eventually kept to ground, turning low side MOSFET on. The undervoltage circuit protection is enabled only at the end of the soft-start. Once an overvoltage protection has been detected, a toggle on SHDN, EN1/EN2 pin or a power on reset is necessary to clear the undervoltage fault and starts with a new soft-start phase.

Table 9. Protections and operatives modes

Mode	Conditions	Description
Overvoltage protection	OUT1/OUT2 > 115% of the nominal value	*LGATE*1/LGATE2 pin is forced high, LDO5 remains active. Exit by a power on reset or toggling *SHDN* or *EN1/EN2*
Undervoltage protection	OUT1/OUT2 < 70 % of the nominal value	*LGATE1/LGATE2* is forced high after the soft end mode, LDO5 remains active. Exit by a power on reset or toggling *SHDN* or *EN1/EN2*
Thermal shutdown	T_J> +150 °C	All circuitry off. Exit by a POR on *VIN* or toggling *SHDN.*

9 Design guidelines

The design of a switching section starts from two parameters:

- Input voltage range: in notebook applications it varies from the minimum battery voltage, VINmin to the AC adapter voltage, V_{INmax}.
- Maximum load current: it is the maximum required output current, $I_{LOAD(max)}$.

9.1 Switching frequency

It's possible to set 3 different working frequency ranges for the two sections with FSEL pin (*Table 6*).

Switching frequency mainly influences two parameters:

- Inductor size: for a given saturation current and RMS current, greater frequency allows to use lower inductor values, which means smaller size.
- Efficiency: switching losses are proportional to frequency. High frequency generally involves low efficiency.

9.2 Inductor selection

Once that switching frequency is defined, inductor selection depends on the desired inductor ripple current and load transient performance.

Low inductance means great ripple current and could generate great output noise. On the other hand, low inductor values involve fast load transient response.

A good compromise between the transient response time, the efficiency, the cost and the size is to choose the inductor value in order to maintain the inductor ripple current ΔI_L between 20 % and 50 % of the maximum output current $I_{LOAD(max)}$. The maximum ΔI_L occurs at the maximum input voltage. With this considerations, the inductor value can be calculated with the following relationship:

Equation 12

$$L = \frac{V_{IN} - V_{OUT}}{f_{sw} \times \Delta I_L} \times \frac{V_{OUT}}{V_{IN}}$$

where fsw is the switching frequency, V_{IN} is the input voltage, V_{OUT} is the output voltage and ΔI_L is the selected inductor ripple current.

In order to prevent overtemperature working conditions, inductor must be able to provide an RMS current greater than the maximum RMS inductor current I_{LRMS}:

Equation 13

$$I_{LRMS} = \sqrt{(I_{LOAD}(max))^2 + \frac{(\Delta I_L(max))^2}{12}}$$

Where $\Delta I_{L(max)}$ is the maximum ripple current:

Equation 14

$$\Delta I_L(max) = \frac{V_{INmax} - V_{OUT}}{f_{sw} \times L} \times \frac{V_{OUT}}{V_{INmax}}$$

If hard saturation inductors are used, the inductor saturation current should be much greater than the maximum inductor peak current Ipeak:

Equation 15

$$Ipeak = I_{LOAD}(max) + \frac{\Delta I_L(max)}{2}$$

Using soft saturation inductors it's possible to choose inductors with saturation current limit nearly to Ipeak.

Below there is a list of some inductor manufacturers.

Table 10. Inductor manufacturer

Manufacturer	Series	Inductor value (uH)	RMS current (A)	Saturation current (A)
COILCRAFT	MSS1038	1.5 to 22	2.85 to 7.85	2.9 to 8.30
COILCRAFT	MSS7341	3.3 to 22	1.7 to 3.95	1.3 to 3.5
WURTH	TPC	1 to 22 µH	2.7 to 8	2.6 to 9.5

9.3 Output capacitor

The selection of the output capacitor is based on the ESR value Rout and the voltage rating rather than on the capacitor value Cout.

The output capacitor has to satisfy the output voltage ripple requirements. Lower inductor value can reduce the size of the choke but increases the inductor current ripple ΔIL.

Since the voltage ripple $V_{RIPPLEout}$ is given by:

Equation 16

$$V_{RIPPLEout} = R_{out} \times \Delta I_L$$

A low ESR capacitor is required to reduce the output voltage ripple. Switching sections can work correctly even with 20 mV output ripple.

However, to reduce jitter noise between the two switching sections it's preferable to work with an output voltage ripple greater than 30 mV. If lower output ripple is required, a further compensation network is needed (see Closing the integrator loop paragraph).

Finally the output capacitor choice deeply impacts on the load transient response (see Load transient response paragraph). Below there is a list of some capacitor manufacturers.

Table 11. Output capacitor manufacturer

Manufacturer	Series	Capacitor value (uF)	Rated voltage (V)	ESR max (mΩ)
SANYO	POSCAP TPB, TPD, TPE	100 to 470	2.5 to 6.3	12 to 65
PANASONIC	SPCAP UD, UE	100 to 470	2 to 6.3	7 to 18

9.4 Input capacitors selection

In a buck topology converter the current that flows into the input capacitor is a pulsed current with zero average value. The input RMS current of the two switching sections can be roughly estimated as follows:

Equation 17

$$I_{CinRMS} = \sqrt{D_1 \times I_1^2 \times (1 - D_1) + D_2 \times I_2^2 \times (1 - D_2)}$$

Where D1, D2 are the duty cycles and I1, I2 are the maximum load currents of the two sections.

Input capacitor should be chosen with an RMS rated current higher than the maximum RMS current given by both sections.

Tantalum capacitors are good in term of low ESR and small size, but they occasionally can burn out if subjected to very high current during the charge. Ceramic capacitors have usually a higher RMS current rating with smaller size and they remain the best choice.

Below there is a list of some ceramic capacitor manufacturers.

Table 12. Input capacitor manufacturer

Manufacturer	Series	Capacitor value (uF)	Rated voltage (V)
TAYIO YUDEN	UMK325BJ106KM-T	10	50
TAYIO YUDEN	GMK325BJ106MN	10	35

9.5 Power MOSFETS

Logic-level MOSFETs are recommended, since low side and high side gate drivers are powered by LDO5. Their breakdown voltage VBR_{DSS} must be higher than V_{INmax}.

In notebook applications, power management efficiency is a high level requirement. The power dissipation on the power switches becomes an important factor in switching selections. Losses of high-side and low-side MOSFETs depend on their working conditions.

The power dissipation of the high-side MOSFET is given by:

Equation 18

$$P_{DHighSide} = P_{conduction} + P_{switching}$$

Maximum conduction losses are approximately:

Equation 19

$$P_{conduction} = R_{DSon} \times \frac{V_{OUT}}{V_{INmin}} \times I_{LOAD}(max)^2$$

where RDSon is the drain-source on resistance of the high side MOSFET.

Switching losses are approximately:

Equation 20

$$P_{switching} = \frac{V_{IN} \times (I_{LOAD}(max) - \frac{\Delta I_L}{2}) \times t_{on} \times f_{sw}}{2} + \frac{V_{IN} \times (I_{LOAD}(max) + \frac{\Delta I_L}{2}) \times t_{off} \times f_{sw}}{2}$$

where t_{on} and t_{off} are the switching times of the turn $_{on}$ and turn $_{off}$ phases of the MOSFET.

As general rule, high side MOSFETs with low gate charge are recommended, in order to minimize driver losses.

Below there is a list of possible choices for the high side MOSFET.

Table 13. High side MOSFET manufacturer

Manufacturer	Type	Gate charge (nC)	Rated reverse voltage (V)
ST	STS5NF60L	25	60

The power dissipation of the low side MOSFET is given by:

Equation 21

$$P_{DLowSide} = P_{conduction}$$

Maximum conduction losses occur at the maximum input voltage:

Equation 22

$$P_{conduction} = R_{DSon} \times \left(1 - \frac{V_{OUT}}{V_{INmax}}\right) \times I_{LOAD}(max)^2$$

Choose a synchronous rectifier with low R_{DSon}. When high side MOSFET turns on, the fast variation of the phase node voltage can bring up even the low side gate through its gate-drain capacitance C_{RSS}, causing cross-conduction problems. Choose a low side MOSFET that minimizes the ratio C_{RSS}/C_{GS} ($C_{GS} = C_{ISS} - C_{RSS}$).

Below there is a list of some possible low side MOSFETs.

Table 10. Low side MOSFET manufacturer

Manufacturer	Type	R_{DSon} (mΩ)	$\frac{C_{RSS}}{C_{GS}}$	Rated reverse voltage (V)
ST	STS7NF60L	[VC11] 19	0.0625	60

Dual n-channel MOSFETs can be used in applications with a maximum output current of about 3 A. Below there is a list of some MOSFET manufacturers.

Table 14. Dual MOSFET manufacturer

Manufacturer	Type	R_{DSon} (mΩ)	Gate charge (nC)	Rated reverse voltage (V)
ST	STS4DNF60L	50	15	60

A rectifier across the low side MOSFET is recommended. The rectifier works as a voltage clamp across the synchronous rectifier and reduces the negative inductor swing during the dead time between turning the high-side MOSFET off and the synchronous rectifier on. It can increase the efficiency of the switching section, since it reduces the low side switch losses. A shottky diode is suitable for its low forward voltage drop (0.3 V). The diode reverse voltage must be greater than the maximum input voltage V_{INmax}. A minimum recovery reverse charge is preferable. Below there is a list of some shottky diode manufacturers.

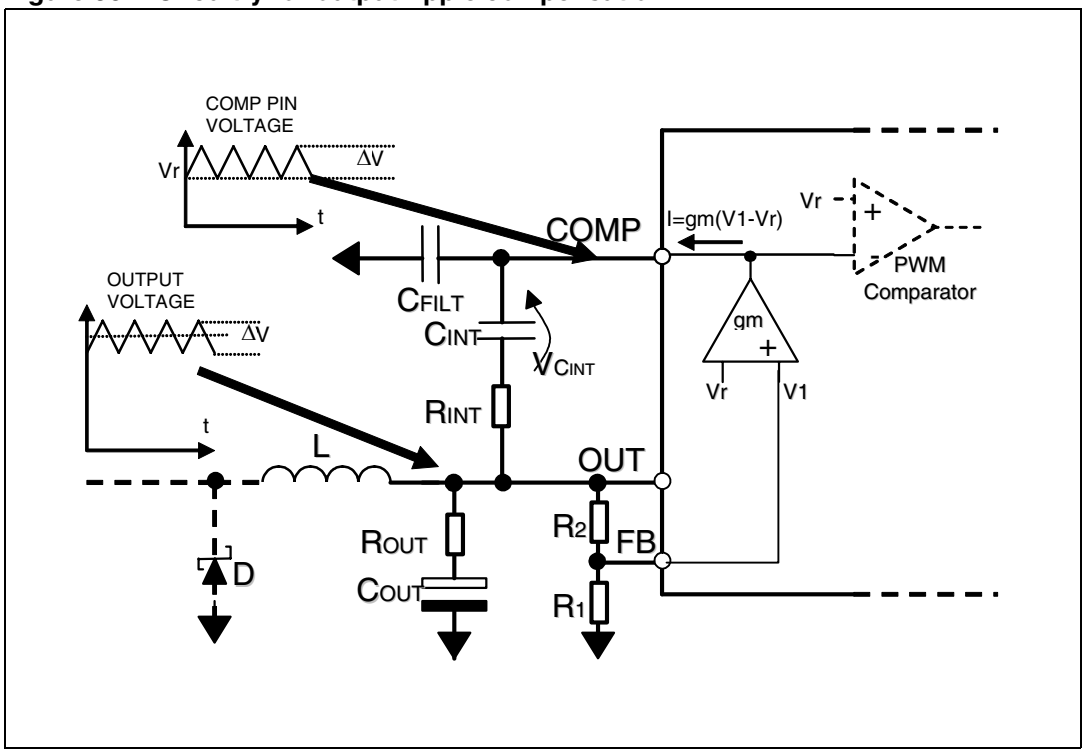
Table 15. Schottky diode manufacturer

Manufacturer	Series	Forward voltage (V)	Rated reverse voltage (V)	Reverse current (uA)
ST	STPS1L40M	0.5	40	21

9.6 Closing the integrator loop

The design of external feedback network depends on the output voltage ripple. If the ripple is higher than approximately 30 mV, the feedback network (*Figure 36*) is usually enough to keep the loop stable.

Figure 36. Circuitry for output ripple compensation



The stability of the system depends firstly on the output capacitor zero frequency.

The following condition should be satisfied:

Equation 23

$$f_{sw} > k \times f_{Zout} = \frac{k}{2\pi \times C_{out} \times R_{out}}$$

where k is a design parameter greater than 3 and Rout is the ESR of the output capacitor. It determinates the minimum integrator capacitor value C_{INT}:

Equation 24

$$C_{INT} > \frac{g_m}{2\pi \times \left(\frac{f_{sw}}{k} - f_{Zout}\right)} \times \frac{Vr}{V_{OUT}}$$

where gm = 50 µs is the integrator transconductance.

In order to ensure stability it must be also verified that:

Equation 25

$$C_{INT} > \frac{g_m}{2\pi \times f_{Zout}} \times \frac{Vr}{V_{OUT}}$$

In order to reduce ground noise due to load transient on the other section, it is recommended to add a resistor R_{INT} and a capacitor C_{filt} that, together with C_{INT}, realize a low pass filter (see figure 13). The cutoff frequency f_{CUT} must be much greater (10 or more times) than the switching frequency of the section:

Equation 26

$$R_{INT} = \frac{1}{2\pi \times f_{CUT} \times \frac{C_{INT} \times C_{filt}}{C_{INT} + C_{filt}}}$$

Due to the capacitive divider (C_{INT}, C_{filt}), the ripple voltage at the COMP pin is given by:

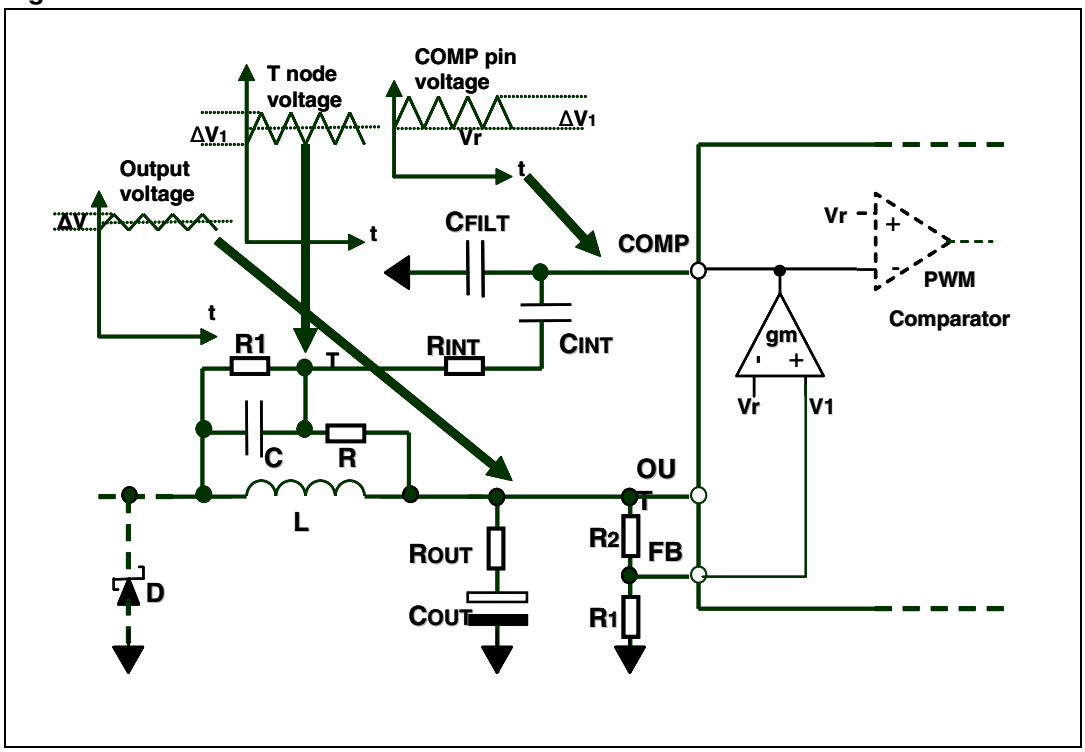
Equation 27

$$V_{RIPPLE_{INT}} = V_{RIPPLEout} \times \frac{C_{INT}}{C_{INT} + C_{filt}} = V_{RIPPLEout} \times q$$

Where $V_{RIPPLEout}$ is the output ripple and q is the attenuation factor of the output ripple.

If the ripple is very small (lower than approximately 30 mV), a further compensation network, named virtual ESR network, is needed. This additional part generates a triangular ripple that is added to the ESR output voltage ripple at the input of the integrator network. The complete control schematic is represented in *Figure 37*.

Figure 37. Virtual ESR network



The T node voltage is the sum of the output voltage and the triangular waveform generated by the virtual ESR network. In fact the virtual ESR network behaves like a further equivalent ESR.

A good trade-off is to design the network in order to achieve an R_{ESR} given by:

Equation 28

$$R_{ESR} = \frac{V_{RIPPLE}}{\Delta I_L} - R_{out}$$

where ΔIL is the inductor current ripple and V_{RIPPLE} is the overall ripple of the T node voltage. It should be chosen higher than approximately 30 mV.

The new closed loop gain depends on $C_{INT.}$ In order to ensure stability it must be verified that:

Equation 29

$$C_{INT} > \frac{g_m}{2\pi \times f_Z} \times \frac{Vr}{V_{OUT}}$$

Where:

Equation 30

$$f_Z = \frac{1}{2\pi \times C_{out} \times R_{TOT}}$$

where R_{TOT} is the sum of the ESR of the output capacitor R_{out} and the equivalent ESR given by the virtual ESR network RESR.

Moreover C_{INT} must meet the following condition:

Equation 31

$$f_{sw} > k \times f_Z = \frac{k}{2\pi \times C_{out} \times R_{TOT}}$$

Where k is a free design parameter greater than 3 and determines the minimum integrator capacitor value C_{INT}:

Equation 32

$$C_{INT} > \frac{g_m}{2\pi \times \left(\frac{f_{sw}}{k} - f_Z\right)} \times \frac{Vr}{V_{OUT}}$$

C must be selected as shown:

Equation 33

$$C > 5 \times C_{INT}$$

R must be chosen in order to have enough ripple voltage on integrator input:

Equation 34

$$R = \frac{L}{R_{ESR} \times C}$$

R1 can be selected as follows:

Equation 35

$$R1 = \frac{R \times \left(\frac{1}{C \times \pi \times f_Z}\right)}{R - \frac{1}{C \times \pi \times f_Z}}$$

Example:

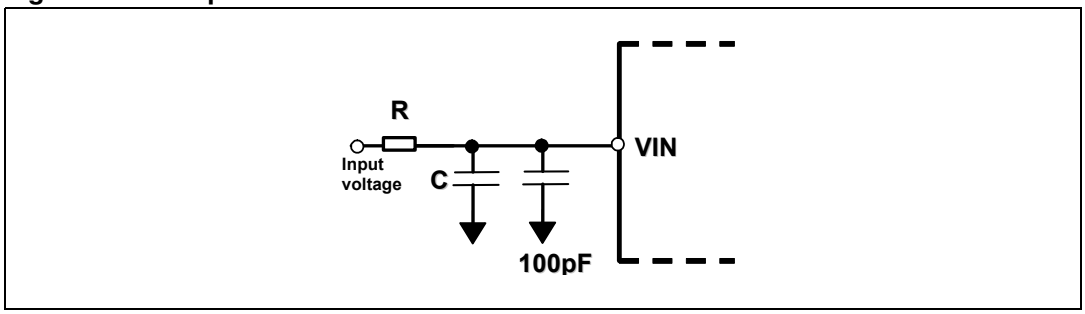
OUT1=1.5 V, f_{SW} = 290 kHz, L = 2.5 µH, Cout = 330 µF with Rout < 12 mΩ.
We design R_{ESR} = 12 mΩ. We choose C_{INT} = 1 nF by equations 30, 33 and Cfilt = 47 pF, R_{INT} = 1 kΩ by eq.27, 28. C = 5.6 nF by Eq.34. Then R = 36 kΩ (eq.34) and R1 = 3 kΩ (eq.35).

9.7 Other parts design

- VIN filter

  A VIN pin low pass filter is suggested to reduce switching noise. The low pass filter is shown in the next figure:

Figure 38. VIN pin filter

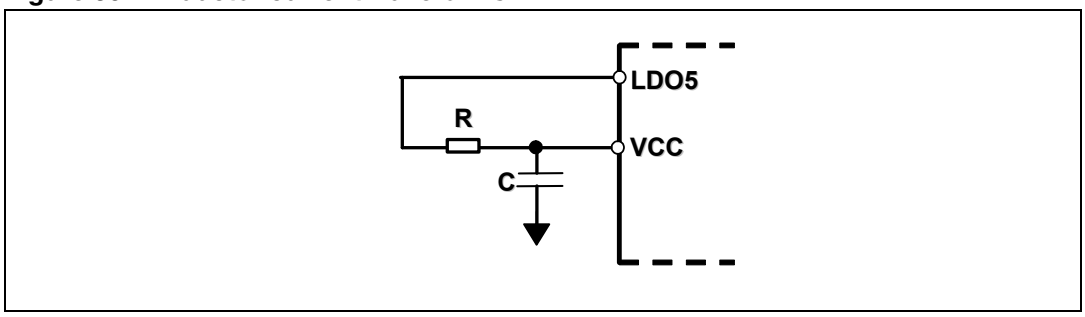


Typical components values are: R = 3.9 Ω and C = 4.7 µF.

- VCC filter

  A VCC low pass filter helps to reject switching commutations noise:

Figure 39. Inductor current waveforms



Typical components values are: R = 47 Ω and C = 1µF.

- VREF capacitor

  A 10nF to 100nF ceramic capacitor on VREF pin must be added to ensure noise rejection.

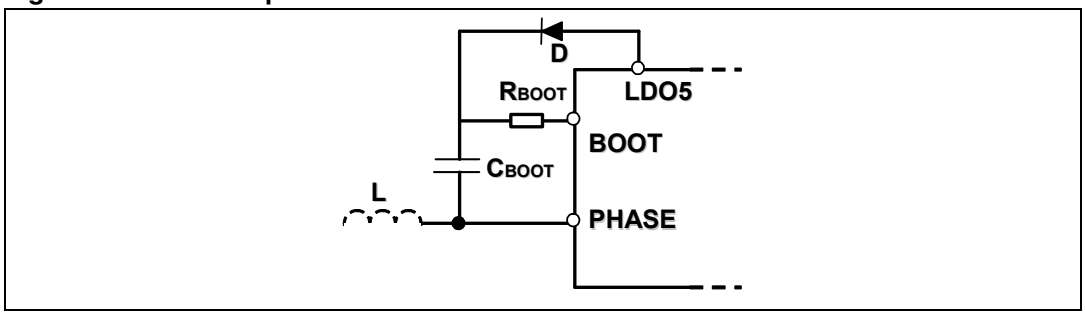
- LDO5 output capacitors

  Bypass the output of each linear regulator with 1 µF ceramic capacitor closer to the LDO pin and a 4.7µF tantalum capacitor (ESR = 2 Ω). In most applicative conditions a 4.7 µF ceramic output capacitor can be enough to ensure stability.

- Bootstrap circuit

  The external bootstrap circuit is represented in the next figure:

Figure 40. Bootstrap circuit



The bootstrap circuit capacitor value C_{BOOT} must provide the total gate charge to the high side MOSFET during turn on phase. A typical value is 100 nF.

The bootstrap diode D must charge the capacitor during the off time phases. The maximum rated voltage must be higher than V_{INmax}.

A resistor R_{BOOT} on the BOOT pin could be added in order to reduce noise when the phase node rises up, working like a gate resistor for the turn on phase of the high side MOSFET.

9.8 Design example

The following design example considers an input voltage from 16 V to 32 V(the typical value is 24 V). The two switching outputs are OUT1 = 3.3 V and OUT2 = 1.8 V and must deliver a maximum current of 2.5 A. The selected switching frequencies are about 290 kHz for OUT1 section and about 440 kHz for OUT2 section (see *Table 6*).

1. Inductor selection

OUT1: ILOAD = 2.5 A, 45 % ripple current.

Equation 36

$$L = \frac{3.3V \cdot (24V - 3.3V)}{290KHz \cdot 24V \cdot 0.45 \cdot 2.5} \approx 8.2\mu H$$

We choose standard value L= 8.2 µH.

$\Delta I_{L(max)}$ = 1.16 A @VIN = 24 V.

I_{LRMS} = 2.523 A

I_{peak} = 2.5 A + 0.58 A = 3.83 A

OUT2:ILOAD=2.5 A, 35 % ripple current.

Equation 37

$$L = \frac{1.8V \cdot (20V - 1.8V)}{425KHz \cdot 24V \cdot 0.35 \cdot 2.5} \approx 4.7\mu H$$

We choose standard value L=4.7 µH.

$\Delta I_{L(max)}$ = 0.886 A @VIN =24 V.

I_{LRMS} = 2.523 A

I_{peak} = 2.5 A + 0.58 A = 3.83 A

2. **Output capacitor selection**
   We would like to have an output ripple smaller than 25 mV.
   OUT1: POSCAP 4TPE150MI
   OUT2: POSCAP 6TPE220M
3. **Power MOSFETs**
   OUT1:High side: STS5NF60L
   Low side: STS7NF60L
   OUT2:High side: STS5NF60L
   Low side: STS7NF60L
4. **Current limit**
   OUT1:

Equation 38

$$I_{Ivalley}(\min) = I_{IOAD}(\max) - \frac{\Delta I_L(\min)}{2} = 2.2A$$

Equation 39

$$R_{CSENSE} \equiv \frac{2.2A}{100\mu A} \cdot 25m\Omega \approx 550\Omega$$

(Let's assume the maximum temperature Tmax = 75 °C in R_{DSon} calculation). We choose standard value R_{CSENSE} = 560 Ω.

OUT2:

Equation 40

$$I_{Ivalley}(\min) = I_{IOAD}(\max) - \frac{\Delta I_L(\min)}{2} = 2.057A$$

Equation 41

$$R_{CSENSE} \equiv \frac{2.057A}{100\mu A} \cdot 25m\Omega \approx 550\Omega$$

(Let's assume Tmax=75 °C in R_{DSon} calculation). We choose standard value R_{CSENSE} = 560 Ω.

5. **Input capacitor**

   Maximum input capacitor RMS current is about 1.084 A. Then I_{CINRMS} > 1.084 A

   We put two 10 µF ceramic capacitors with Irms = 1.5 A.

6. **Synchronous rectifier**

   OUT1: Shottky diode STPS1L40M

   OUT2: Shottky diode STPS1L40M

7. **Integrator loop**

   (Refer to figure 14)

   OUT1: The ripple is smaller than 40 mV, then the virtual ESR network is required.

   C_{INT} = 1.5 nF; C_{filt} = 47 pF; R_{INT} = 1.1 kΩ

   OUT2: The ripple is smaller than 40 mV, then the virtual ESR network is required.

   C_{INT} =1.5 nF; C_{filt} =47 pF; R_{INT} = 820 Ω

8. **Output feedback divider**

   (Refer to figure 6)

   OUT1: R1 = 10 kΩ; R2 = 27 kΩ

   OUT2: R1 = 10 kΩ; R2 = 10 kΩ

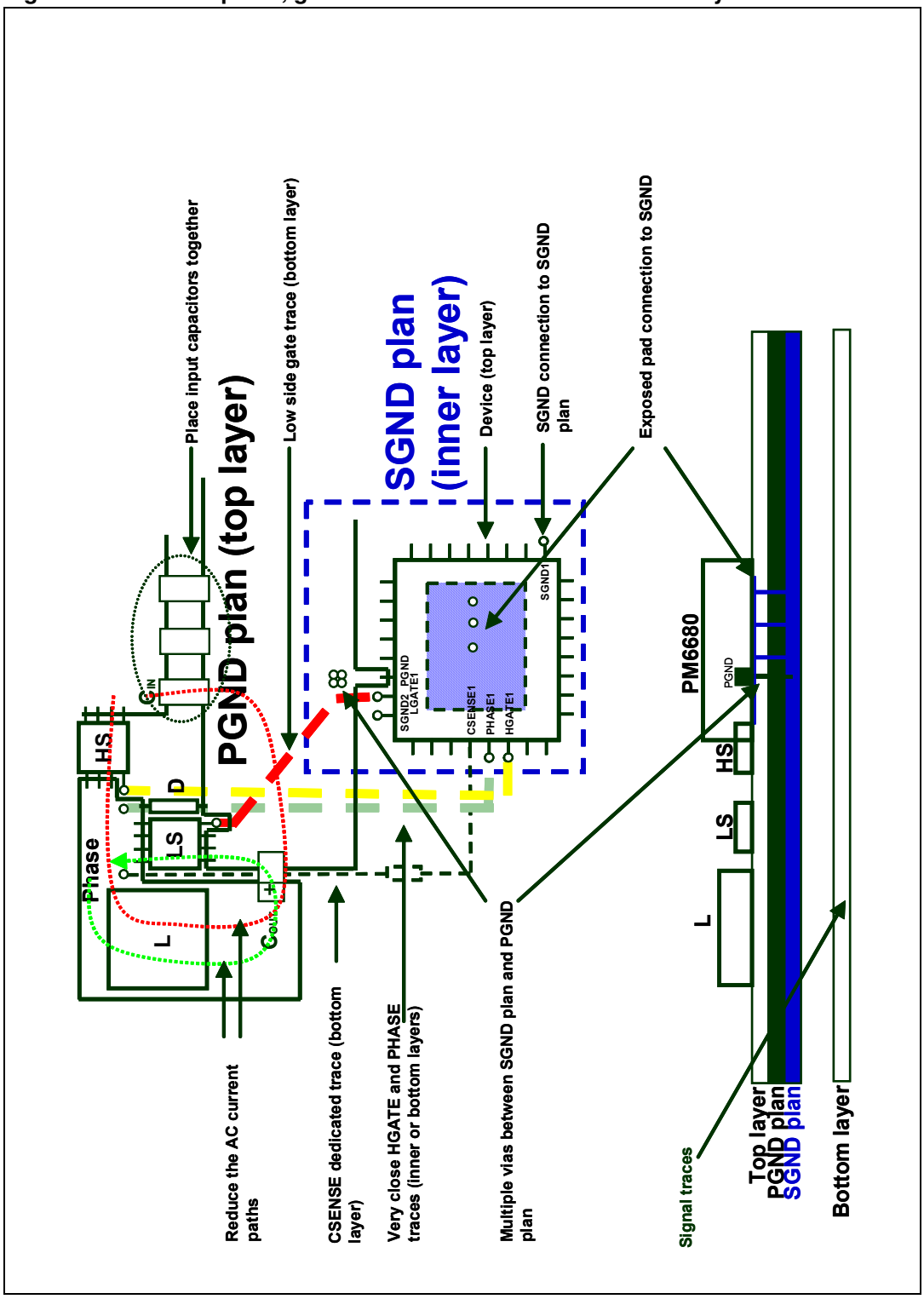
9. **Layout guidelines**

   The layout is very important in terms of efficiency, stability and noise of the system. It is possible to refer to the PM6680A demoboard for a complete layout example.

   For good PC board layout follows these guidelines:

- Place on the top side all the power components (inductors, input and output capacitors, MOSFETs and diodes). Refer them to a power ground plan, PGND. If possible, reserve a layer to PGND plan. The PGND plan is the same for both the switching sections.
- AC current paths layout is very critical (see*Figure 41*). The first priority is to minimize their length. Trace the LS MOSFET connection to PGND plan as short as possible. Place the synchronous diode D near the LS MOSFET. Connect the LS MOSFET drain to the switching node with a short trace.
- Place input capacitors near HS MOSFET drain. It is recommended to use the same input voltage plan for both the switching sections, in order to put together all input capacitors.
- Place all the sensitive analog signals (feedbacks, voltage reference, current sense paths) on the bottom side of the board or in an inner layer. Isolate them from the power top side with a signal ground layer, SGND. Connect the SGND and PGND plans only in one point (a multiple vias connection is preferable to a 0 ohm resistor connection) near the PGND device pin. Place the device on the top or on the bottom size and connect the exposed pad and the SGND pins to the SGND plan (see *Figure 41*).

Figure 41. Current paths, ground connection and driver traces layout



- As general rule, make the high side and low side drivers traces wide and short. The high side driver is powered by the bootstrap circuit. It's very important to place capacitor CBOOT and diode DBOOT as near as possible to the HGATE pin (for example on the layer opposite to the device). Route HGATE and PHASE traces as near as possible in order to minimize the area between them.
- The Low side gate driver is powered by the 5 V linear regulator output. Placing PGND and LGATE pins near the low side MOSFETs reduces the length of the traces and the crosstalk noise between the two sections.
- The linear regulator output LDO5 is referred to SGND as long as the reference voltage Vref. Place their output filtering capacitors as near as possible to the device.
- Place input filtering capacitors near VCC and VIN pins.
- It would be better if the feedback networks connected to COMP, FB and OUT pins are "referred" to SGND in the same point as reference voltage Vref. To avoid capacitive coupling place these traces as far as possible from the gate drivers and phase (switching) paths.
- Place the current sense traces on the bottom side. Using It is recommended to use a dedicated connection between the switching node and the current limit resistor R_{CSENSE}.

10 Package mechanical data

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Table 16. VFQFPN 5x5 mechanical data (mm)

Dim	Min	Typ	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	4.85	5.00	5.15
D2	See exposed pad variations (1)		
E	4.85	5.00	5.15
E2	See exposed pad variations (1)		
e		0.50	
L	0.30	0.40	0.50
ddd			0.05

1. Dimensions D2 & E2 are not in accordance with JEDEC.

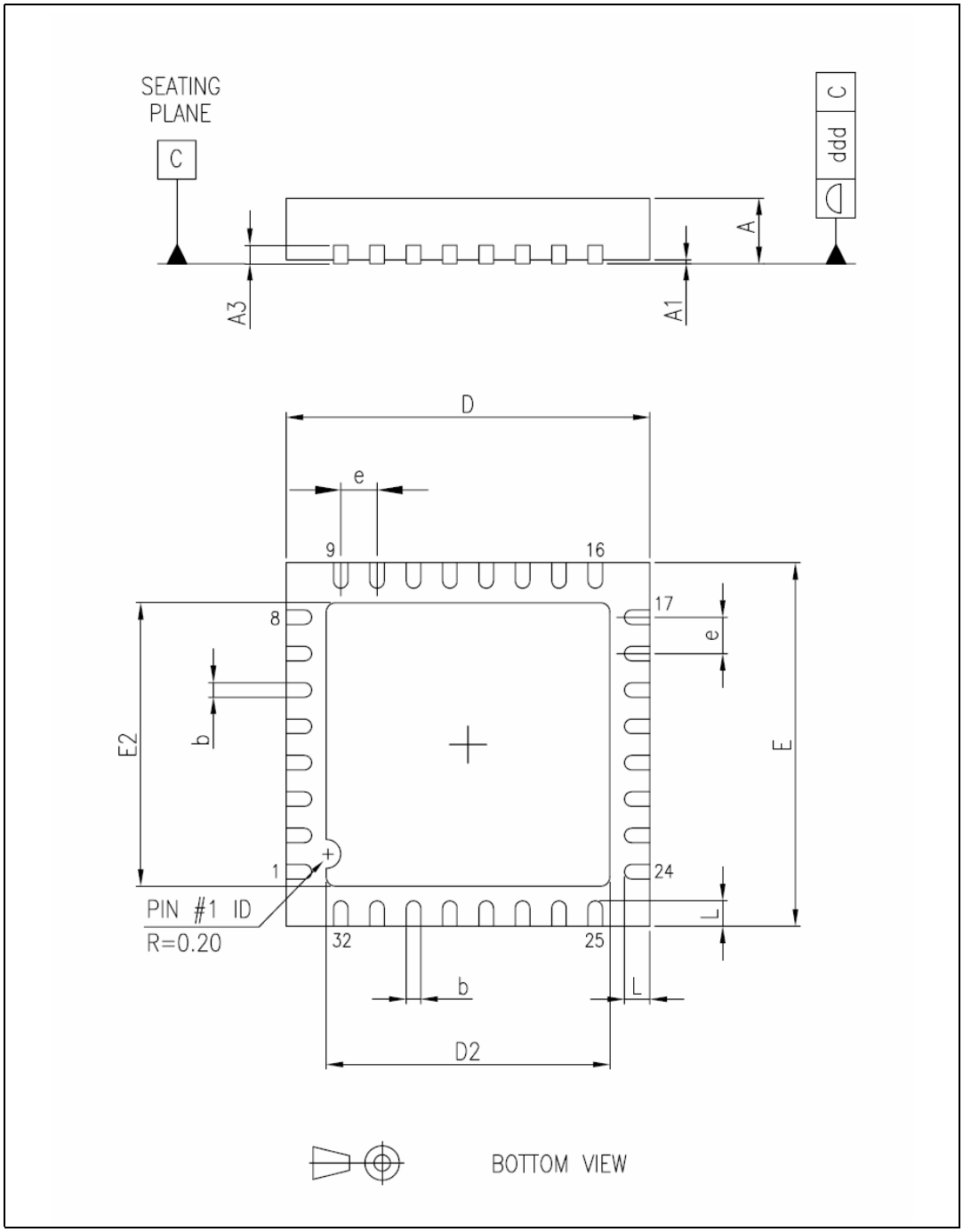
Table 17. Exposed pad variations

D2			E2		
Min	Typ	Max	Min	Typ	Max
2.90	3.10	3.20	2.90	3.10	3.20

Note: 1 VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Package No lead. Very thin: A=1.00 mm Max.

2 Dimensions D2 & E2 are not in accordance with JEDEC.

Figure 42. Package dimensions



11 Revision history

Table 18. Document revision history

Date	Revision	Changes
12-Oct-2006	1	Initial release.
17-Dec-2007	2	Added *Section 5: Typical operating characteristics on page 12* and *Section 9: Design guidelines on page 30*

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