

DESCRIPTION

Demonstration circuit 936A features the **LTC[®]2609** Quad 16-bit DAC. This device establishes a new board-density benchmark for 16-bit DACs and advances performance standards for output drive, crosstalk and load regulation in single supply, voltage-output multiple DACs.

DC936A has many features for evaluating the performance of the LTC2609. Onboard 5V, 4.096V, and 2.5V precision references are provided. The LTC2609 features separate reference inputs for each DAC, and any of the onboard references can be used for any of the reference inputs.

Another feature of this board is the onboard LTC2428 20-bit ADC for monitoring DAC output voltage. The 16ppm total error of this device is adequate for taking meaningful measurements of various LTC2609 parameters.

Design files for this circuit board are available at <http://www.linear.com/demo>

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PERFORMANCE SUMMARY Specifications are at T_A = 25°C

PARAMETER	CONDITION	VALUE
Resolution		16 Bits
Monotonicity	V _{CC} = 5V, V _{REF} = 4.096V	16 Bits
Differential Nonlinearity	V _{CC} = 5V, V _{REF} = 4.096V	±1LSB
Integral Nonlinearity	V _{CC} = 5V, V _{REF} = 4.096V	±18LSB Typical
Load Regulation	V _{CC} = V _{REF} = 5V, Mid-Scale I _{OUT} = ±15mA	2LSB/mA Max
DC Crosstalk	Due to Load Current Change on Any Other Channel	4µV/mA

QUICK START PROCEDURE

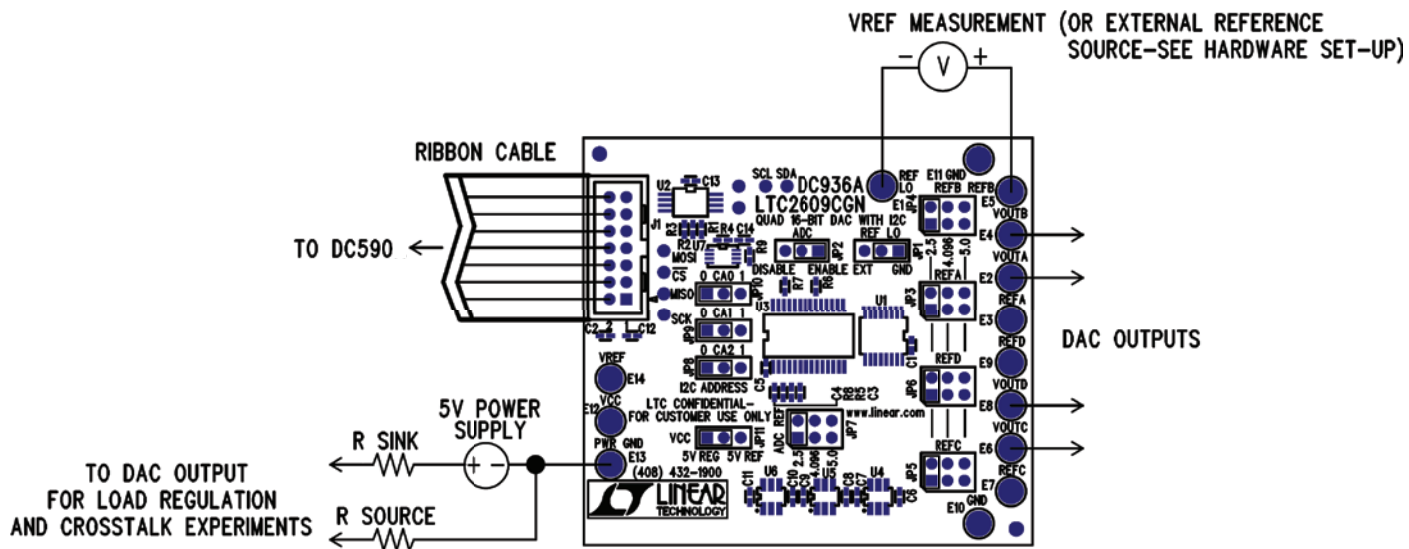


Figure 1. Proper Measurement Equipment Setup

QUICK START PROCEDURE

Connect DC936A to a DC590 USB serial controller using the supplied 14-conductor ribbon cable. Connect DC590 to a host PC with a standard USB A/B cable. Run the evaluation software supplied with DC590 or download it from www.linear.com/software. The correct control panel

will be loaded automatically. Click the COLLECT button to begin outputting codes to the DACs and reading back the resulting output voltage for each DAC.

Complete software documentation is available from the Help menu item, as features may be added periodically.

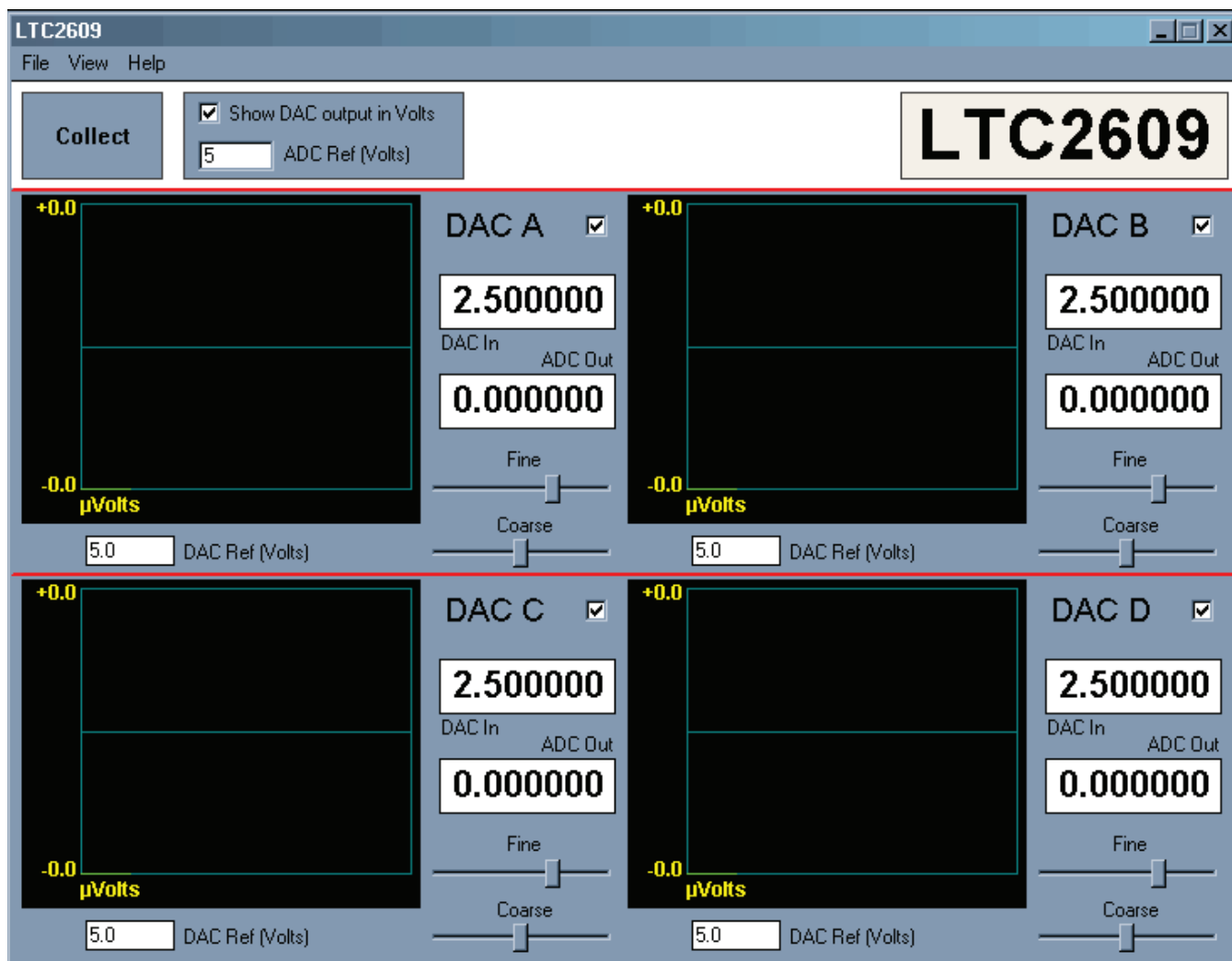


Figure 2. Evaluation Software

HARDWARE SETUP

Jumpers

JP1 – REFLO Selection. Either tied to ground or supplied externally to the REFLO turret post.

JP2 – ADC Disable. Set to ON for normal operation, with the onboard ADC enabled. For very sensitive noise measurements, the ADC may be disabled. The software will then display a positive full-scale reading.

JP7 – V_{REF} Select for ADC. This selects which onboard reference is used for the LTC2428 ADC. If all DAC references are set to the same voltage, set the ADC reference to the same voltage. If different DAC reference voltages are used, set the ADC reference to the highest DAC reference voltage.

JP3, JP4, JP5, JP6 – Select reference for DAC A, B, C, and D, respectively. Onboard references are 2.5V, 4.096V, and 5.0V. Remove jumper entirely to apply an external reference.

JP11 – V_{CC} select. V_{CC} is taken either from the onboard 5V reference or the 5V regulated supply from the controller board. Selecting the 5V reference for V_{CC} and V_{REF} allows characterization of rail to rail operation of the LTC2609.

JP8, JP9, JP10 – I^2C Address Selection. These are connected to the CA0, CA1, CA2 pins. The demo software uses the global I^2C address, so these pins have no effect when used with the QuikEval™ software. They can be used in prototyping to set the I^2C address of the LTC2607 – refer to the data sheet for the mapping of CA0, 1, 2 levels to I^2C addresses.

Analog Connections

DAC Outputs – The four DAC outputs from the LTC2609 are brought out to turrets labeled DAC A through DAC D. These may be connected to external instruments or other circuitry.

DAC outputs are not in alphabetical order on the circuit board.

DAC References – The REFA, REFB, REFC, and REFD turrets are connected directly to the reference terminals of the onboard references. When one of the onboard references is being used, the reference voltage may be monitored at this point. An external reference may also be applied to this turret after removing the associated reference selection jumper.

REFLO – This is connected to the LTC2609 REFLO pin and can be used to raise the zero-code output of all of the DACs above ground potential. This is normally set to ground, but may be raised up to 1V above ground. Refer to the LTC2609 data sheet for details.

Ground Connections

Grounding – Separate power and signal grounds are provided. Any large currents drawn from the DAC outputs should be returned to the power ground turret closest to Pin 1 on the 14-pin header. Signal ground is connected to the exposed ground planes at the top and bottom edges of the board, and to the two turrets labeled “GND.” Use signal ground as the reference point for measurements and connections to external circuits.

EXPERIMENTS

The following experiments are intended to demonstrate some of the outstanding features of the LTC2609. All can be performed using the onboard LTC2428 to monitor the DAC output voltage. The indicated output voltage will typically agree with an HP3458A voltmeter to 5 digits. If a DAC will be sinking or sourcing a significant current, then the output voltage should be measured as close to the DAC as possible.

Most of the data sheet specifications use a 4.096V reference, so this is the preferred reference to use for these experiments. Using the 5 volt reference has the limitation that V_{CC} may be slightly lower than V_{REF} , which may affect the full scale error.

Using an external power supply is highly recommended for these experiments, especially those that draw significant current. Refer to the DC590 quick start guide for details.

Resolution

The onboard LTC2428 ADC has an input resolution of $6\mu\text{V}$. This will easily resolve a 1LSB ($76\mu\text{V}$ for $V_{REF} = 5\text{V}$, $62.5\mu\text{V}$ for $V_{REF} = 4.096\text{V}$) change in the LTC2609 output. Set one of the DAC channels to a voltage close to mid-scale. Select the FINE slider on the control panel with the mouse and use the right and left arrow keys to step the output by single LSBs. The change should be clearly visible in the output graph. (It may be necessary to wait for the graph to clear if a large step has just occurred. This can be sped up by disabling all other DAC channels in the software by un-checking them.)

Integral Nonlinearity

A rough measurement of INL can be taken using the onboard ADC. Measure one of the LTC2609 outputs at code 256 and 65,535 and calculate the slope and intercept using a spreadsheet. Next, take several readings at intermediate points. The readings should not deviate from the calculated line by more than 64LSBs, and they will typically be within 12LSBs.

Load Regulation/DC Output Impedance

Select “Regulator” for V_{CC} source. Set one of the outputs to mid-scale (code 32768.) source or sink 15mA from one of the DAC outputs by pulling it to power ground or V_{CC} with an appropriate value resistor. The voltage change should be less than 2.25mV, corresponding to an output impedance of 0.15Ω . Output impedance is typically less than 0.030Ω . (measure DAC voltage at the output pin if using a voltmeter.)

Zero Scale Error

Set one of the DACs to code 0. The measured output should be less than 9mV and will typically be less than 1mV.

Offset Error

Set one of the DACs to code 256. The output voltage should be within 1mV of the correct value, or $V_{REF} \cdot 256/65535$.

Gain Error

Set one of the DACs to code 65,535. The output voltage should be within 0.7% of V_{REF} , and will typically be within 0.2%.

DC Crosstalk

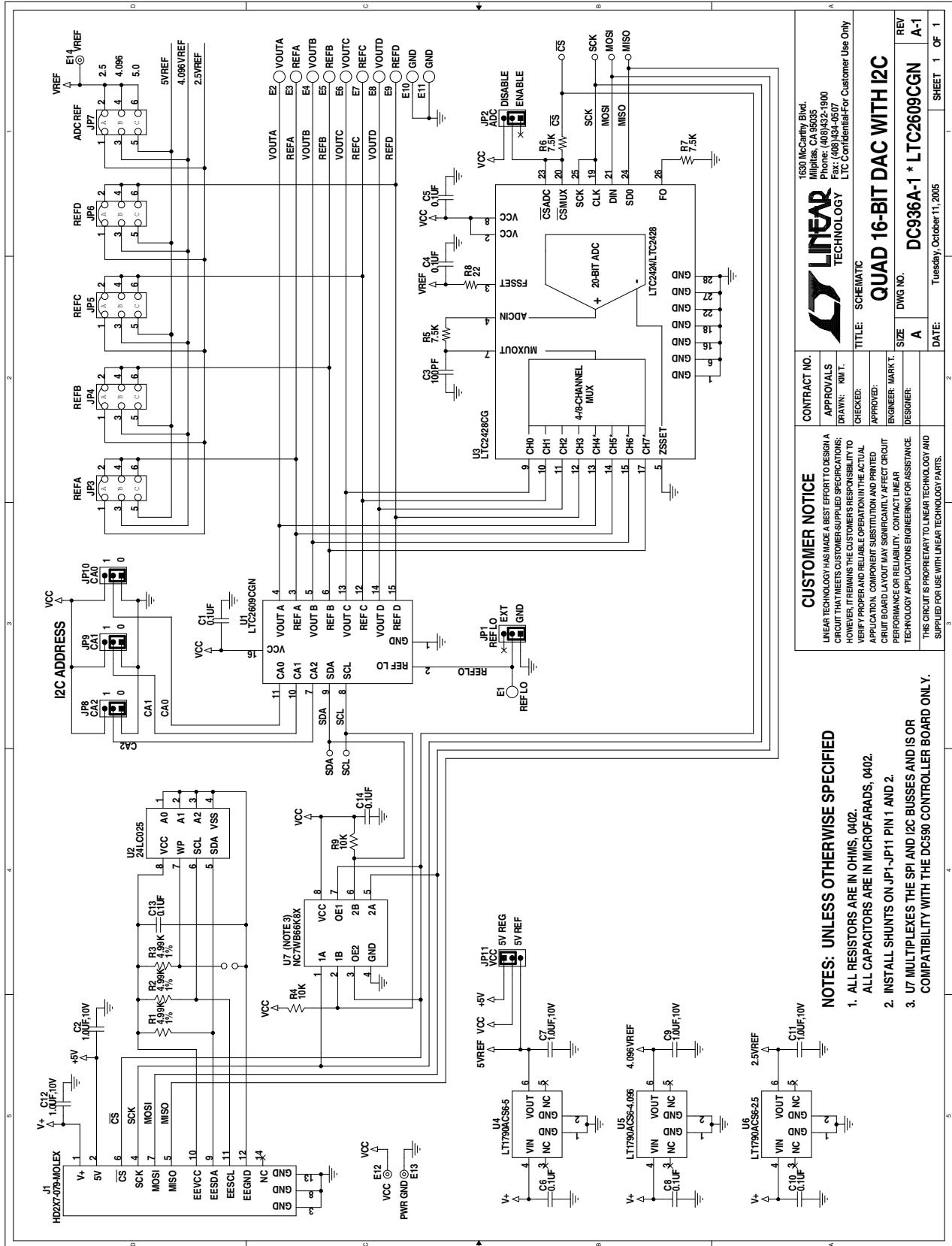
Set all DACs to mid-scale. Connect a 250Ω resistor from one output to V_{CC} or power ground (to sink or source 10mA, respectively, when the 5V reference is being used.) A given output should not change by more than $3.5\mu\text{V}$ per milliamp of output current in all other DACs combined.

DEMO MANUAL DC936A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	8	C1, C4, C5, C6, C8, C10, C13, C14	CAP., X7R, 0.1 μ F 16V,0402	TDK, C1005X7R1C104M
2	5	C2, C7, C9, C11, C12	CAP., X5R, 1.0 μ F 10V, 0402	TDK, C1005X5R1A105MT
3	1	C3	CAP., NPO, 100pF 50V, 0402	AVX, 04025A101MAT
4	14	E1-E14	TESTPOINT, TURRET, 0.064"	MILL-MAX, 2308-2
5	6	JP1, JP2, JP8, JP9, JP10, JP11	JMP, 3 PIN 1 ROW .079CC	SAMTEC TMM-103-02-L-S
6	5	JP3, JP4, JP5, JP6, JP7	HEADER, 2x3 PIN, 0.079CC	SAMTEC TMM-103-02-L-D
7	11	JP1-JP11 PIN 1 AND 2	SHUNT, .079" CENTER	SAMTEC 2SN-BK-G
8	1	J1	HEADER, 2x7 PIN, 0.079CC	MOLEX, 87831-1420
9	3	R1, R2, R3	RES., CHIP, 4.99k, 1%, 0402	AAC, CR05-4991FM
10	2	R4, R9	RES., CHIP 10k 1/16W 5%, 0402	PANASONIC, ERJ2GEJ103X
11	3	R5, R6, R7	RES., CHIP, 7.5k, 5%, 0402	AAC, CR05-752JM
12	1	R8	RES., CHIP, 22, 5%, 0402	AAC, CR05-220JM
13	1	U1	I.C., LTC2609CGN, SSOP16GN	LINEAR TECH., LTC2609CGN
14	1	U2	I.C., 24LC025, TSSOP8	MICROCHIP, 24LC025-I /ST
15	1	U3	I.C., LTC2428CG, SSOP28G	LINEAR TECH., LTC2428CG
16	1	U4	I.C., LT1790ACS6-5.0, SOT23-6	LINEAR TECH., LT1790ACS6-5
17	1	U5	I.C., LT1790ACS6-4.096, SOT23-6	LINEAR TECH., LT1790ACS6-4.096
18	1	U6	I.C., LT1790ACS6-2.5, SOT23-6	LINEAR TECH., LT1790ACS6-2.5
19	1	U7	I.C., NC7WB66K8X, US8	FAIRCHILD, NC7WB66K8X

SCHEMATIC DIAGRAM



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THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.		DRAWN: KMT	
		CHECKED:	
		APPROVED:	
		ENGINEER: MARK T.	
		DESIGNER:	
		TITLE: SCHEMATIC	
		1630 McCarthy Blvd. Milpitas, CA 95035 Phone: (408)432-1900 Fax: (408)434-0507 LTC Confidential-For Customer Use Only	
		TITLE: QUAD 16-BIT DAC WITH I2C	
		DWG NO. DC936A-1 * LTC2609CGN	
		SIZE A	
		DATE: Tuesday, October 11, 2005	
		SHEET 1 OF 1	

- NOTES: UNLESS OTHERWISE SPECIFIED**
1. ALL RESISTORS ARE IN OHMS, 0402.
 2. ALL CAPACITORS ARE IN MICROFARADS, 0402.
 3. INSTALL SHUNTS ON JP1-JP11 PIN 1 AND 2.
 4. U7 MULTIPLEXES THE SPI AND I2C BUSES AND IS OR COMPATIBILITY WITH THE DC590 CONTROLLER BOARD ONLY.



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DEMO MANUAL DC936A

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