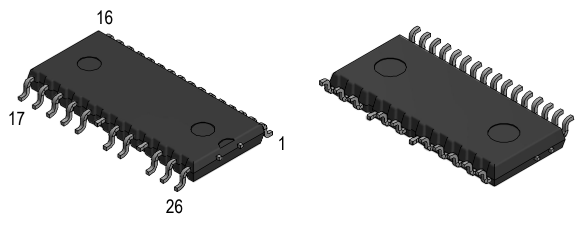
STIPNS1M50T-H

SLLIMM™-nano small low-loss intelligent molded module IPM, 3-phase inverter, 1 A, 3.6 Ω max., 500 V MOSFET

Datasheet - production data



NSDIP-26L

Features

- IPM 1 A, 500 V, $R_{DS(on)}$= 3.6 Ω, 3-phase MOSFET inverter bridge including control ICs for gate driving
- Optimized for low electromagnetic interference
- 3.3 V, 5 V, 15 V CMOS/TTL input comparators with hysteresis and pull-down/pull-up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Comparator for fault protection against overtemperature and overcurrent
- Op-amp for advanced current sensing
- Optimized pinout for easy board layout
- NTC for temperature control (UL 1434 CA 2 and 4)
- Moisture sensitive level (MSL) 3

Applications

- 3-phase inverters for small power motor drives
- Dish washers, refrigerator compressors, heating systems, air-conditioning fans, draining and recirculation pumps

Description

This SLLIMM (small low-loss intelligent molded module) nano provides a compact, high-performance AC motor drive in a simple, rugged design. It is composed of six MOSFETs and three half-bridge HVICs for gate driving, providing low electromagnetic interference (EMI) characteristics with optimized switching speed. The package is optimized for thermal performance and compactness in built-in motor applications, or other low power applications where assembly space is limited. This IPM includes an operational amplifier, completely uncommitted, and a comparator that can be used to design a fast and efficient protection circuit. SLLIMM™ is a trademark of STMicroelectronics.

Table 1: Device summary

Order code	Marking	Package	Packing
STIPNS1M50T-H	IPNS1M50T-H	NSDIP-26L	Tape and reel

This is information on a product in full production.

Contents

1 Internal schematic diagram and pin configuration

Figure 1: Internal schematic diagram

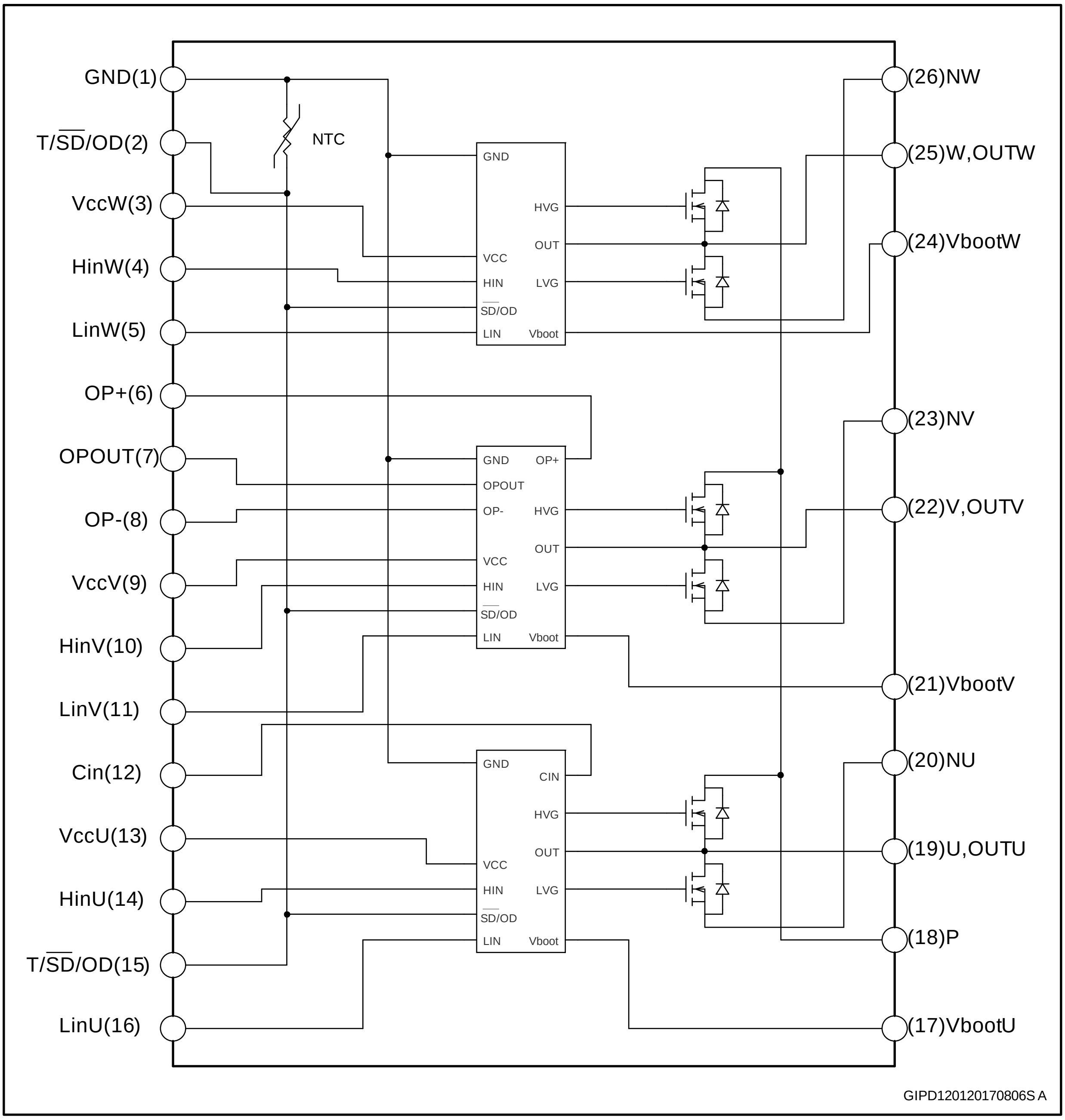
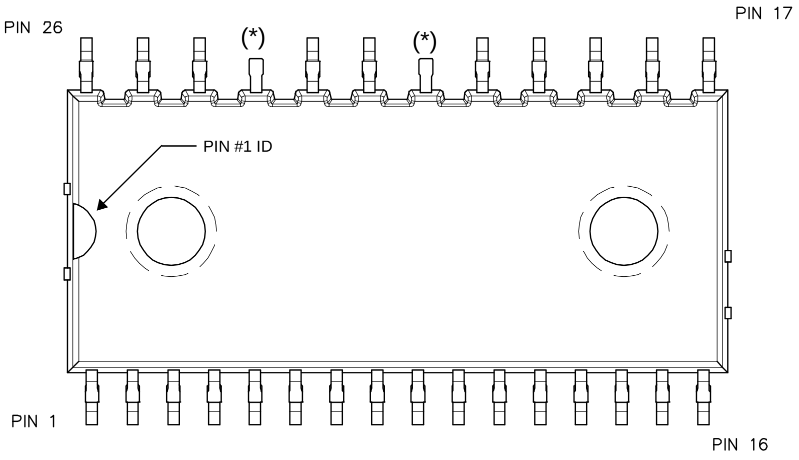


Table 2: Pin description

Pin	Symbol	Description
1	GND	Ground
2	T/$\overline{SD}$/OD	NTC thermistor terminal / shutdown logic input (active low) / open-drain (comparator output)
3	V_{CC} W	Low voltage power supply W phase
4	HIN W	High-side logic input for W phase
5	LIN W	Low-side logic input for W phase
6	OP+	Op-amp non inverting input
7	OP_{OUT}	Op-amp output
8	OP-	Op-amp inverting input
9	V_{CC} V	Low voltage power supply V phase
10	HIN V	High-side logic input for V phase
11	LIN V	Low-side logic input for V phase
12	CIN	Comparator input
13	V_{CC} U	Low voltage power supply for U phase
14	HIN U	High-side logic input for U phase
15	T/$\overline{SD}$/OD	NTC thermistor terminal / shutdown logic input (active low) / open-drain (comparator output)
16	LIN U	Low-side logic input for U phase
17	V_{BOOT} U	Bootstrap voltage for U phase
18	P	Positive DC input
19	U, OUT_U	U phase output
20	N_U	Negative DC input for U phase
21	V_{BOOT} V	Bootstrap voltage for V phase
22	V, OUT_V	V phase output
23	N_V	Negative DC input for V phase
24	V_{BOOT} W	Bootstrap voltage for W phase
25	W, OUT_W	W phase output
26	N_W	Negative DC input for W phase

Figure 2: Pin layout (top view)



(*) Dummy pin internally connected to P (positive DC input).

2 Electrical ratings

2.1 Absolute maximum ratings

Table 3: Inverter part

Symbol	Parameter	Value	Unit
V_{DSS}	MOSFET blocking voltage (or drain-source voltage) for each MOSFET (V_{IN}(1)= 0)	500	V
± I_D	Continuous current each MOSFET	1	A
± I_{DP}(2)	Peak drain current each MOSFET (less than 1 ms)	2	A
P_{TOT}	Each MOSFET total dissipation at T_C = 25 °C	10.8	W

Notes:

(1)Applied among HINi, LINi and GND for i = U, V, W.

(2)Pulse width limited by max. junction temperature.

Table 4: Control part

Symbol	Parameter	Min.	Max.	Unit
V_{OUT}	Output voltage applied among OUT_U, OUT_V, OUT_W - GND	V_{boot} - 21	V_{boot} + 0.3	V
V_{CC}	Low voltage power supply	- 0.3	21	V
V_{CIN}	Comparator input voltage	- 0.3	V_{CC} + 0.3	V
V_{op+}	Op-amp non-inverting input	- 0.3	V_{CC} + 0.3	V
V_{op-}	Op-amp inverting input	- 0.3	V_{CC} + 0.3	V
V_{boot}	Bootstrap voltage	- 0.3	620	V
V_{IN}	Logic input voltage applied among HIN, LIN and GND	- 0.3	15	V
$V_{T/\overline{SD}/OD}$	Open-drain voltage	- 0.3	15	V
$\Delta V_{OUT/dT}$	Allowed output slew rate		50	V/ns

Table 5: Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 s)	1000	V
T_j	Power chip operating junction temperature range	-40 to 150	°C
T_C	Module case operation temperature range	-40 to 125	°C

2.2 Thermal data

Table 6: Thermal data

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Thermal resistance junction-case	11.5	°C/W

3 Electrical characteristics

T_J = 25 °C unless otherwise specified.

3.1 Inverter part

Table 7: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero-gate voltage drain current	V_{DS} = 500 V, V_{CC} = 15 V, V_{Boot} = 15 V			1	mA
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{CC}= V_{boot} = 15 V, V_{IN}(1) = 0 V, I_D = 1 mA	500			V
$R_{DS(on)}$	Static drain source turn-on resistance	V_{CC} = V_{boot} = 15 V, V_{IN}(1)= 0 - 5 V, I_D = 0.5 A		3.2	3.6	Ω
V_{SD}	Drain-source diode forward voltage	V_{IN}(1) = 0 “logic state”, I_D = 1 A		0.9	1.6	V

Notes:

(1)Applied among HINx, LINx and GND for x=U,V,W.

Table 8: Inductive load switching time and energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{on}(1)	Turn-on time	V_{DD} = 300 V, V_{CC} = V_{boot} = 15 V, V_{IN}(2) = 0 - 5 V, I_C = 0.5 A (see *Figure 4: "Switching time definition"*)	-	226	-	ns
$t_{c(on)}$(1)	Crossover time (on)		-	130	-	
t_{off}(1)	Turn-off time		-	248	-	
$t_{c(off)}$(1)	Crossover time (off)		-	56	-	
t_{rr}	Reverse recovery time		-	155	-	
E_{on}	Turn-on switching energy		-	25	-	µJ
E_{off}	Turn-off switching energy		-	3.8	-	

Notes:

(1)t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of MOSFET itself under the internally given gate driving conditions.

(2)Applied among HINx, LINx and GND for x=U,V,W.

Figure 3: Switching time test circuit

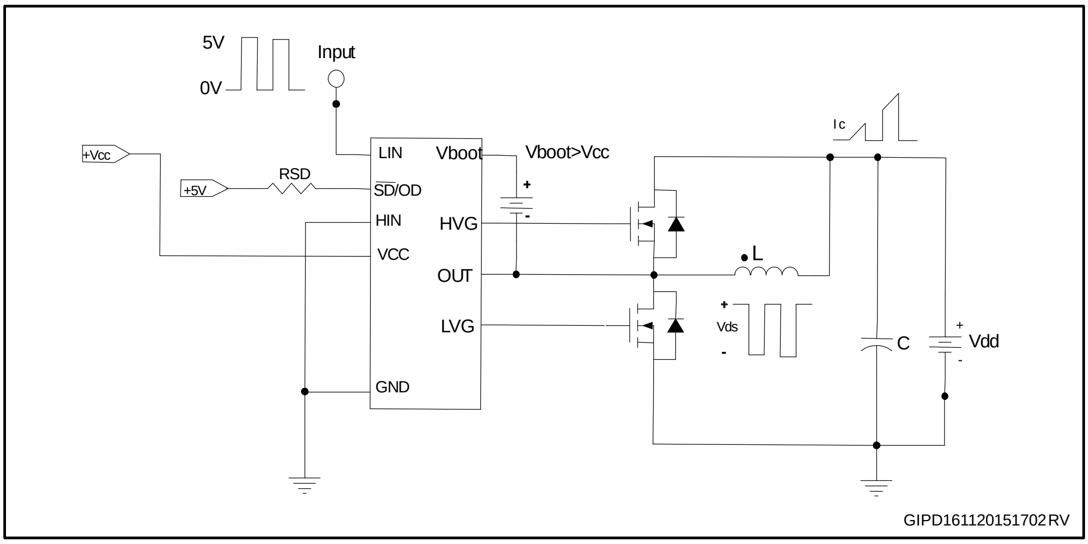


Figure 4: Switching time definition

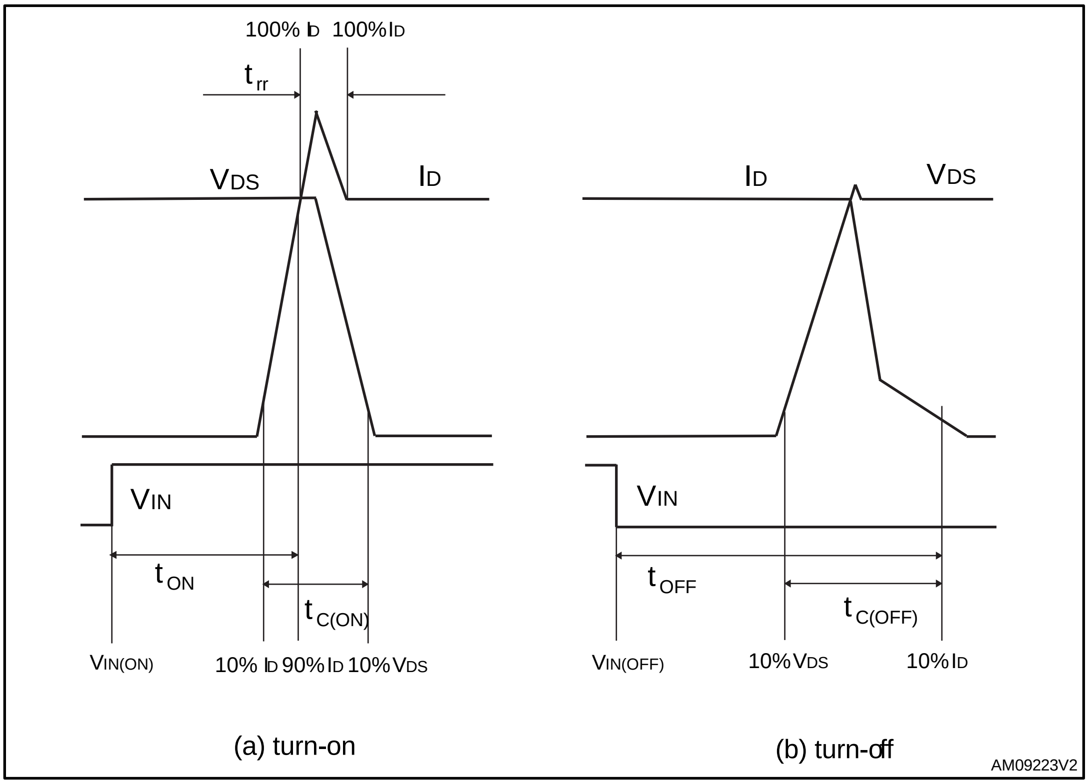


Figure 4: "Switching time definition" refers to HIN, LIN inputs (active high).

3.2 Control part

(V_{CC} = 15 V unless otherwise specified).

Table 9: Low voltage power supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.5	1.8	V
V_{CC_thON}	V_{CC} UV turn ON threshold		11.5	12	12.5	V
V_{CC_thOFF}	V_{CC} UV turn OFF threshold		10	10.5	11	V
I_{qccu}	Undervoltage quiescent supply current	V_{CC} = 10 V, T/$\overline{SD}$/OD = 5 V; LIN = 0 V; H_{IN} = 0, C_{IN} = 0			150	µA
I_{qcc}	Quiescent current	V_{cc} = 15 V, T/$\overline{SD}$/OD = 5 V; LIN = 0 V; H_{IN} = 0, C_{IN} = 0			1	mA
V_{ref}	Internal comparator (CIN) reference voltage		0.5	0.54	0.58	V

Table 10: Bootstrapped voltage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BS_hys}	V_{BS} UV hysteresis		1.2	1.5	1.8	V
V_{BS_thON}	V_{BS} UV turn-ON threshold		11.1	11.5	12.1	V
V_{BS_thOFF}	V_{BS} UV turn-OFF threshold		9.8	10	10.6	V
I_{QBSU}	Undervoltage V_{BS} quiescent current	V_{BS} < 9 V T/$\overline{SD}$/OD = 5 V; LIN = 0 V and HIN = 5 V; C_{IN} = 0		70	110	µA
I_{QBS}	V_{BS} quiescent current	V_{BS} = 15 V T/$\overline{SD}$/OD = 5 V; LIN = 0 V and HIN = 5 V; C_{IN} = 0		200	300	µA
$R_{DS(on)}$	Bootstrap driver on- resistance	LVG ON		120		Ω

Table 11: Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage				0.8	V
V_{ih}	High logic level voltage		2.25			V
I_{HINh}	HIN logic “1” input bias current	HIN = 15 V	20	40	100	µA
I_{HINl}	HIN logic “0” input bias current	HIN = 0 V			1	µA
I_{LINh}	LIN logic “1” input bias current	LIN = 15 V	20	40	100	µA
I_{LINl}	LIN logic “0” input bias current	LIN = 0 V			1	µA
I_{SDh}	$\overline{SD}$ logic “0” input bias current	$\overline{SD}$= 15 V	220	295	370	µA
I_{SDl}	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 0 V			3	µA
Dt	Dead time	see *Figure 9: "Dead time and interlocking waveform definitions"*		180		ns

Table 12: Op-amp characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	V_{ic} = 0 V, V_o = 7.5 V			6	mV
I_{io}	Input offset current	V_{ic} = 0 V, V_o = 7.5 V		4	40	nA
I_{ib}	Input bias current (1)			100	200	nA
V_{OL}	Low level output voltage	R_L = 10 kΩ to V_{CC}		75	150	mV
V_{OH}	High level output voltage	R_L = 10 kΩ to GND	14	14.7		V
I_o	Output short-circuit current	Source, V_{id} = +1 V; V_o = 0 V	16	30		mA
		Sink, V_{id} = -1 V; V_o = V_{CC}	50	80		mA
SR	Slew rate	V_i = 1 - 4 V; C_L = 100 pF; unity gain	2.5	3.8		V/µs
GBWP	Gain bandwidth product	V_o = 7.5 V	8	12		MHz
A_{vd}	Large signal voltage gain	R_L = 2 kΩ	70	85		dB
SVR	Supply voltage rejection ratio	vs. V_{CC}	60	75		dB
CMRR	Common mode rejection ratio		55	70		dB

Notes:

(1) The direction of input current is out of the IC.

Table 13: Sense comparator characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ib}	Input bias current	V_{CIN} = 1 V			1	µA
V_{od}	Open-drain low level output voltage	I_{od} = 3 mA			0.5	V
R_{ON_OD}	Open-drain low level output resistance	I_{od} = 3 mA		166		Ω
R_{PD_SD}	$\overline{SD}$ pull-down resistor (1)			125		kΩ
t_{d_comp}	Comparator delay	T/$\overline{SD}$/OD pulled to 5 V through 100 kΩ resistor		90	130	ns
SR	Slew rate	C_L = 180 pF; R_{pu} = 5 kΩ		60		V/µs
t_{sd}	Shutdown to high- / low-side driver propagation delay	V_{OUT} = 0, V_{boot} = V_{CC}, V_{IN} = 0 to 3.3 V	50	125	200	ns
t_{isd}	Comparator triggering to high- / low-side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CIN	50	200	250	

Notes:

(1) Equivalent values as a result of the resistances of three drivers in parallel.

Table 14: Truth table

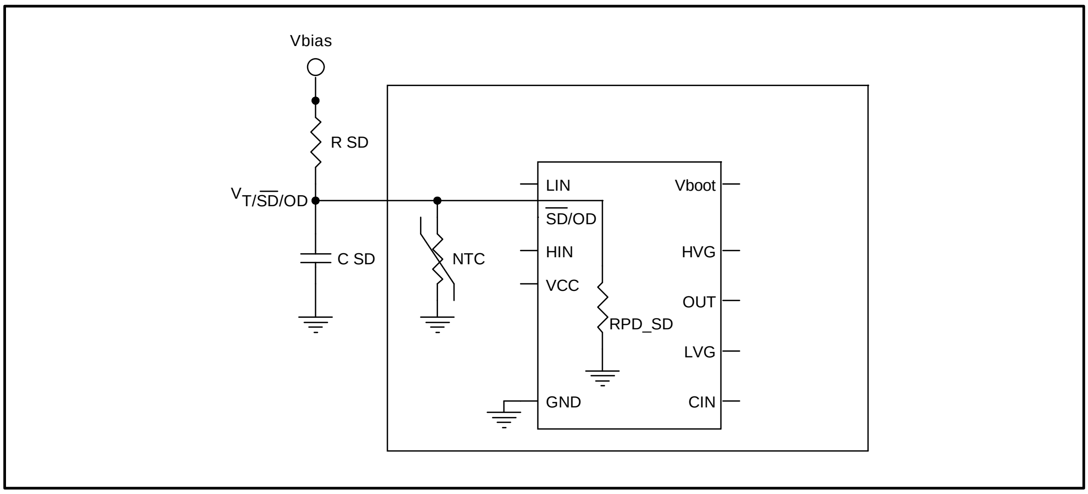
Condition	Logic input (V_I)			Output	
	T/$\overline{\text{SD}}$/OD	LIN	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X(1)	X(1)	L	L
Interlocking half-bridge tri-state	H	H	H	L	L
0 “logic state” half-bridge tri-state	H	L	L	L	L
1 “logic state” low-side direct driving	H	H	L	H	L
1 “logic state” high-side direct driving	H	L	H	L	H

Notes:

(1)X: don’t care.

3.2.1 NTC thermistor

Figure 5: Internal structure of $\overline{\text{SD}}$ and NTC



RPD_SD: equivalent value as result of resistances of three drivers in parallel.

Figure 6: Equivalent resistance (NTC//RPD_SD)

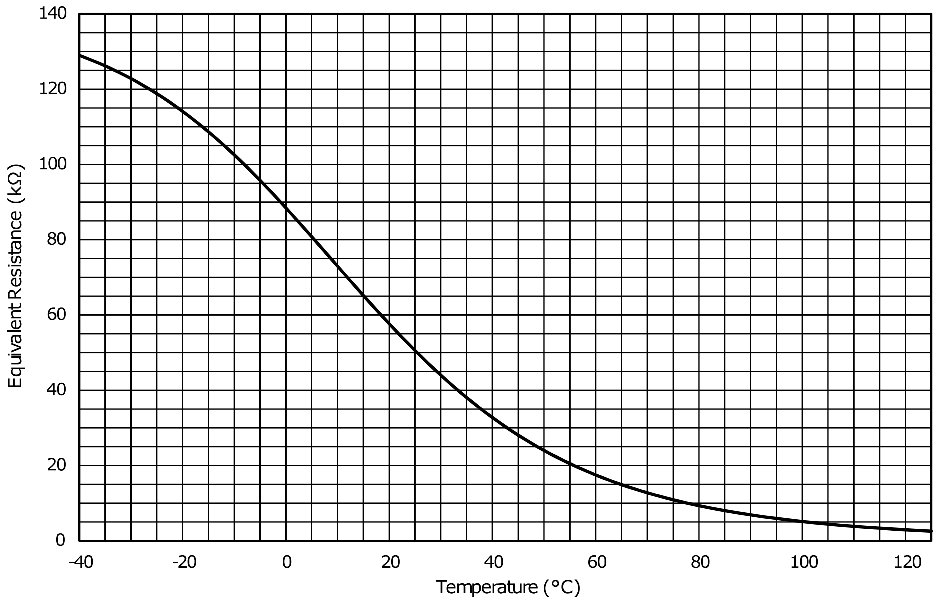


Figure 7: Equivalent resistance (NTC//RPD_SD) zoom

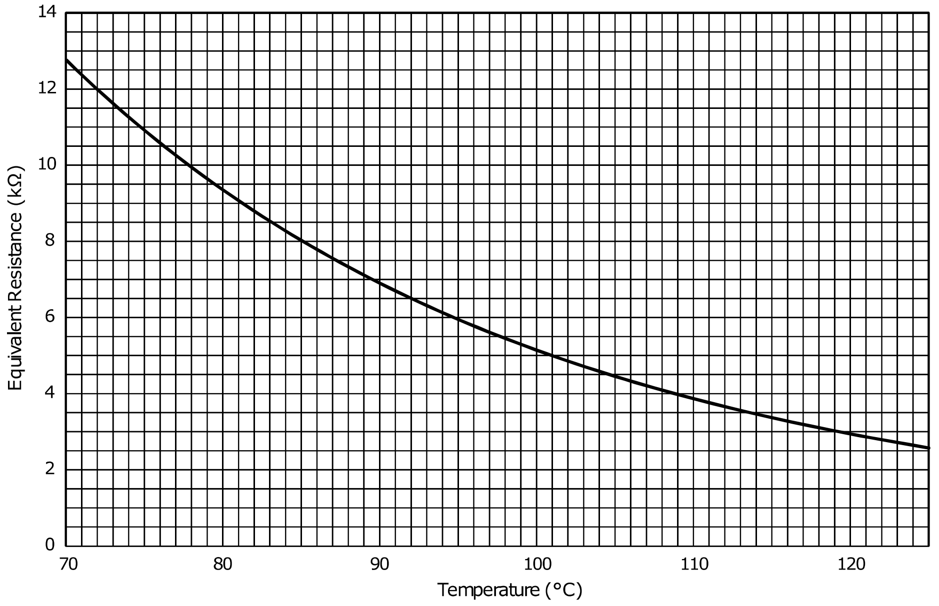
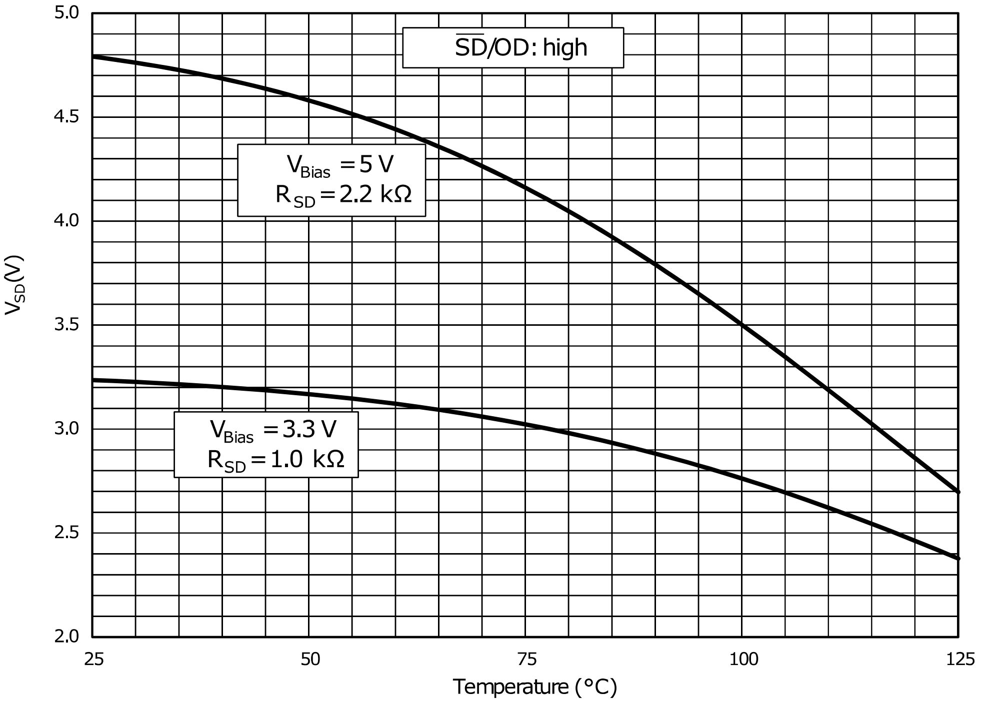
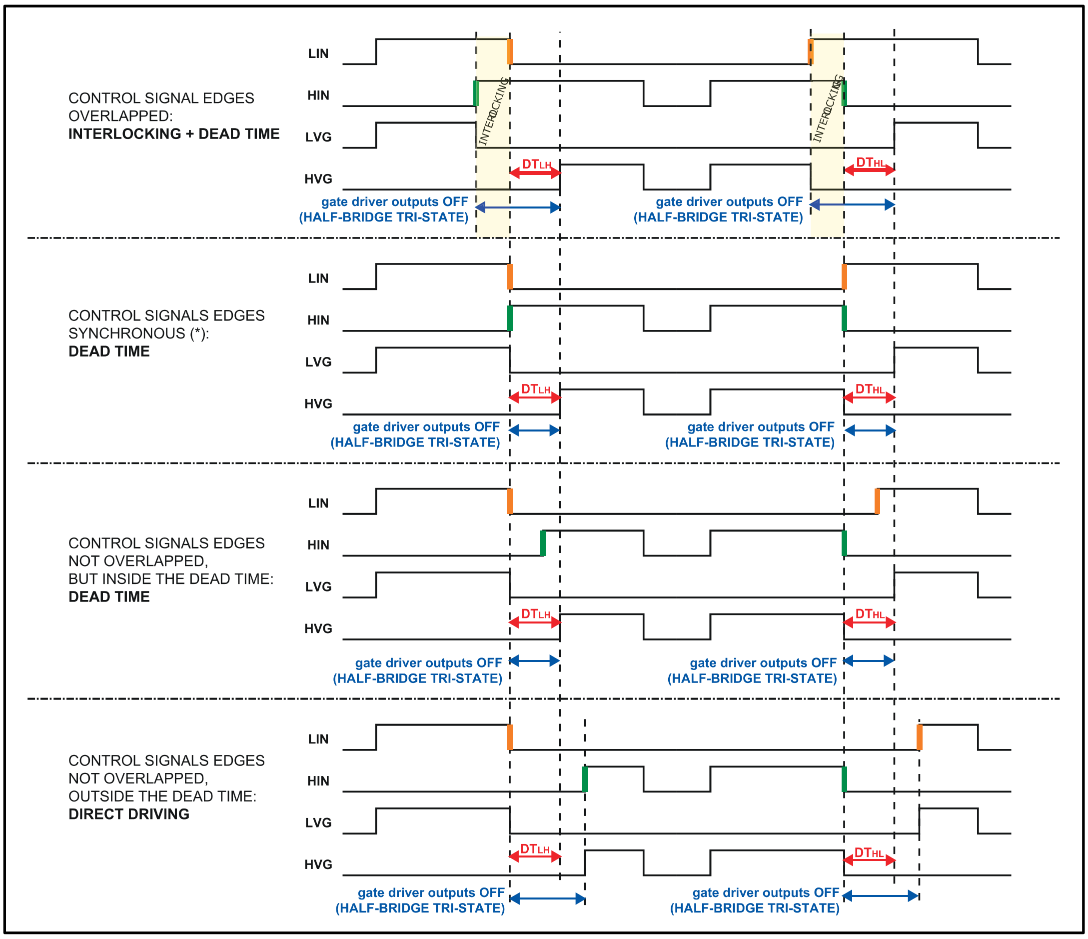


Figure 8: Voltage of T/$\overline{SD}$/OD pin according to NTC temperature



3.3 Waveform definitions

Figure 9: Dead time and interlocking waveform definitions



4 Smart shutdown function

The device integrates a comparator for fault sensing purposes. The comparator has an internal voltage reference V_{REF} connected to the inverting input, while the non-inverting input on pin (CIN) can be connected to an external shunt resistor for simple overcurrent protection.

When the comparator triggers, the device is set to the shutdown state and both of its outputs are set to the low level, causing the half-bridge to enter a tri-state.

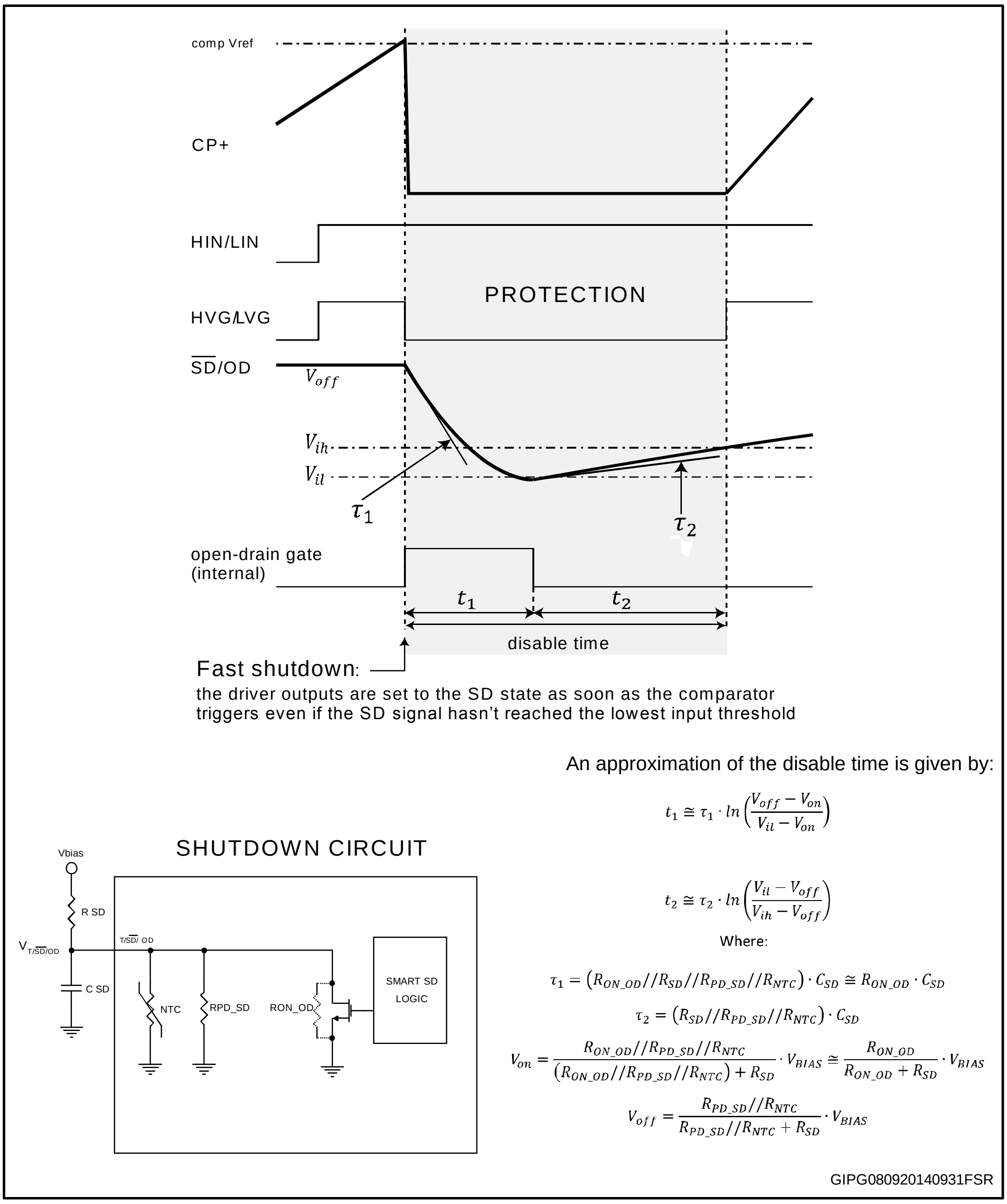
In common overcurrent protection architectures, the comparator output is usually connected to the shutdown input through an RC network so to provide a monostable circuit which implements a protection time following to a fault condition.

Our smart shutdown architecture immediately turns off the output gate driver in case of overcurrent through a preferential path for the fault signal which directly switches off the outputs. The time delay between the fault and output shutdown no longer depends on the RC values of the external network connected to the shutdown pin. At the same time, the DMOS connected to the open-drain output (pin T/$\overline{SD}$/OD) is turned on by the internal logic, which holds it on until the shutdown voltage is lower than the minimum value of logic input threshold.

Besides, the smart shutdown function allows the real disable time to be increased while the constant time of the external RC network remains as it is.

An NTC thermistor for temperature monitoring is internally connected in parallel to the $\overline{SD}$ pin. To avoid undesired shutdown, keep the voltage $V_{T/\overline{SD}/OD}$ higher than the high-level logic threshold by setting the pull-up resistor $R_{\overline{SD}}$ to 1 kΩ or 2.2 kΩ for 3.3 V or 5 V MCU power supplies, respectively.

Figure 10: Smart shutdown timing waveforms



Fast shutdown: the driver outputs are set to the SD state as soon as the comparator triggers even if the SD signal hasn't reached the lowest input threshold

An approximation of the disable time is given by:

$$t_1 \cong \tau_1 \cdot ln\left(\frac{V_{off} - V_{on}}{V_{il} - V_{on}}\right)$$

$$t_2 \cong \tau_2 \cdot ln\left(\frac{V_{il} - V_{off}}{V_{ih} - V_{off}}\right)$$

Where:

$$\tau_1 = \left(R_{ON\_OD}//R_{SD}//R_{PD\_SD}//R_{NTC}\right) \cdot C_{SD} \cong R_{ON\_OD} \cdot C_{SD}$$

$$\tau_2 = \left(R_{SD}//R_{PD\_SD}//R_{NTC}\right) \cdot C_{SD}$$

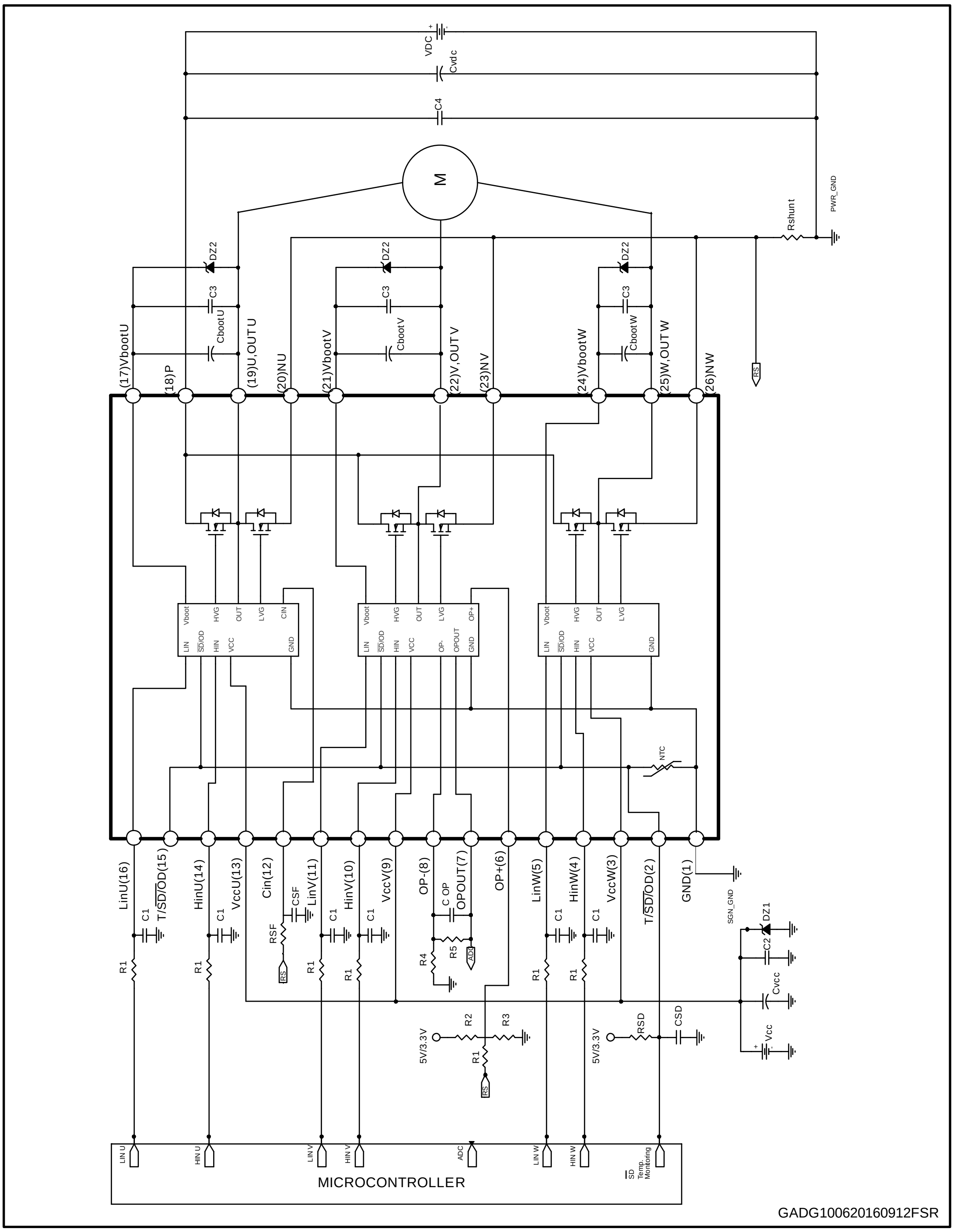
$$V_{on} = \frac{R_{ON\_OD}//R_{PD\_SD}//R_{NTC}}{\left(R_{ON\_OD}//R_{PD\_SD}//R_{NTC}\right) + R_{SD}} \cdot V_{BIAS} \cong \frac{R_{ON\_OD}}{R_{ON\_OD} + R_{SD}} \cdot V_{BIAS}$$

$$V_{off} = \frac{R_{PD\_SD}//R_{NTC}}{R_{PD\_SD}//R_{NTC} + R_{SD}} \cdot V_{BIAS}$$

Please refer to *Table 13: "Sense comparator characteristics"* for internal propagation delay time details.

5 Application circuit example

Figure 11: Application circuit example



GADG100620160912FSR

Application designers are free to use a different scheme according to the specifications of the device.

5.1 Guidelines

- Input signals HIN, LIN are active high logic. A 375 kΩ (typ.) pull-down resistor is built-in for each input. To prevent the input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters (R_1, C_1) on each input signal is suggested. The filters should be with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
- The use of a bypass capacitor CVCC (aluminum or tantalum) can help to reduce the transient circuit demand on the power supply. Besides, to reduce high frequency switching noise distributed on the power lines, a decoupling capacitor C_2 (100 to 220 nF, with low ESR and low ESL) should be placed as close as possible to V_{cc} pin and in parallel with the bypass capacitor.
- The use of RC filter (RSF, CSF) is recommended to avoid protection circuit malfunction. The time constant (RSF x CSF) should be set to 1 μs and the filter must be placed as close as possible to CIN pin.
- The $\overline{SD}$ is an input/output pin (open-drain type if used as output). A built-in thermistor NTC is internally connected between the $\overline{SD}$ pin and GND. The voltage VSD-GND decreases as the temperature increases, due to the pull-up resistor RSD. In order to keep the voltage always higher than the high level logic threshold, the pull-up resistor is suggested to be set to 1 kΩ or 2.2 kΩ for 3.3 V or 5 V MCU power supply, respectively. The CSD capacitor of the filter on $\overline{SD}$ should be fixed no higher than 3.3 nF in order to assure a $\overline{SD}$ activation time $T_1 \leq 500$ ns and the filter should be placed as close as possible to the $\overline{SD}$ pin.
- The decoupling capacitor C_3 (from 100 to 220 nF, ceramic with low ESR and low ESL), in parallel with each C_{boot}, filters the high frequency disturbance. Both C_{boot} and C_3 (if present) should be placed as close as possible to the U, V, W and V_{boot} pins. Bootstrap negative electrodes should be connected to U, V, W terminals directly and separated from the main output wires.
- To prevent the overvoltage on V_{cc} pin, a Zener diode (Dz1) can be used. Similarly on the V_{boot} pin, a Zener diode (Dz2) can be placed in parallel with each C_{boot}.
- The use of the decoupling capacitor C_4 (100 to 220 nF, with low ESR and low ESL), in parallel with the electrolytic capacitor C_{vdc},prevents surge destruction. Both capacitors C_4 and C_{vdc} should be placed as close as possible to the IPM (C_4 has priority over C_{vdc}).
- By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an optocoupler is possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- In order to avoid malfunctions, the wiring on N pins, the shunt resistor and PWR_GND should be as short as possible.
- The connection of SGN_GND to PWR_GND on one point only (close to the shunt resistor terminal) can help to reduce the impact of power ground fluctuation.

These guidelines are useful for application designs to ensure the specifications of the device. For further details, please refer to the relevant application note.

Table 15: Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply voltage	Applied among P-Nu, Nv, Nw		300	400	V
V_{CC}	Control supply voltage	Applied to V_{CC}-GND	13.5	15	18	V
V_{BS}	High-side bias voltage	Applied to V_{BOOTi}-OUT_i for i = U, V, W	13		18	V
t_{dead}	Blanking time to prevent arm-short	For each input signal	1			µs
f_{PWM}	PWM input signal	-40 °C < T_c < 100 °C -40 °C < T_j < 125 °C			25	kHz
T_C	Case operation temperature				100	°C

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

6.1 NSDIP-26L package information

Figure 12: NSDIP-26L package outline

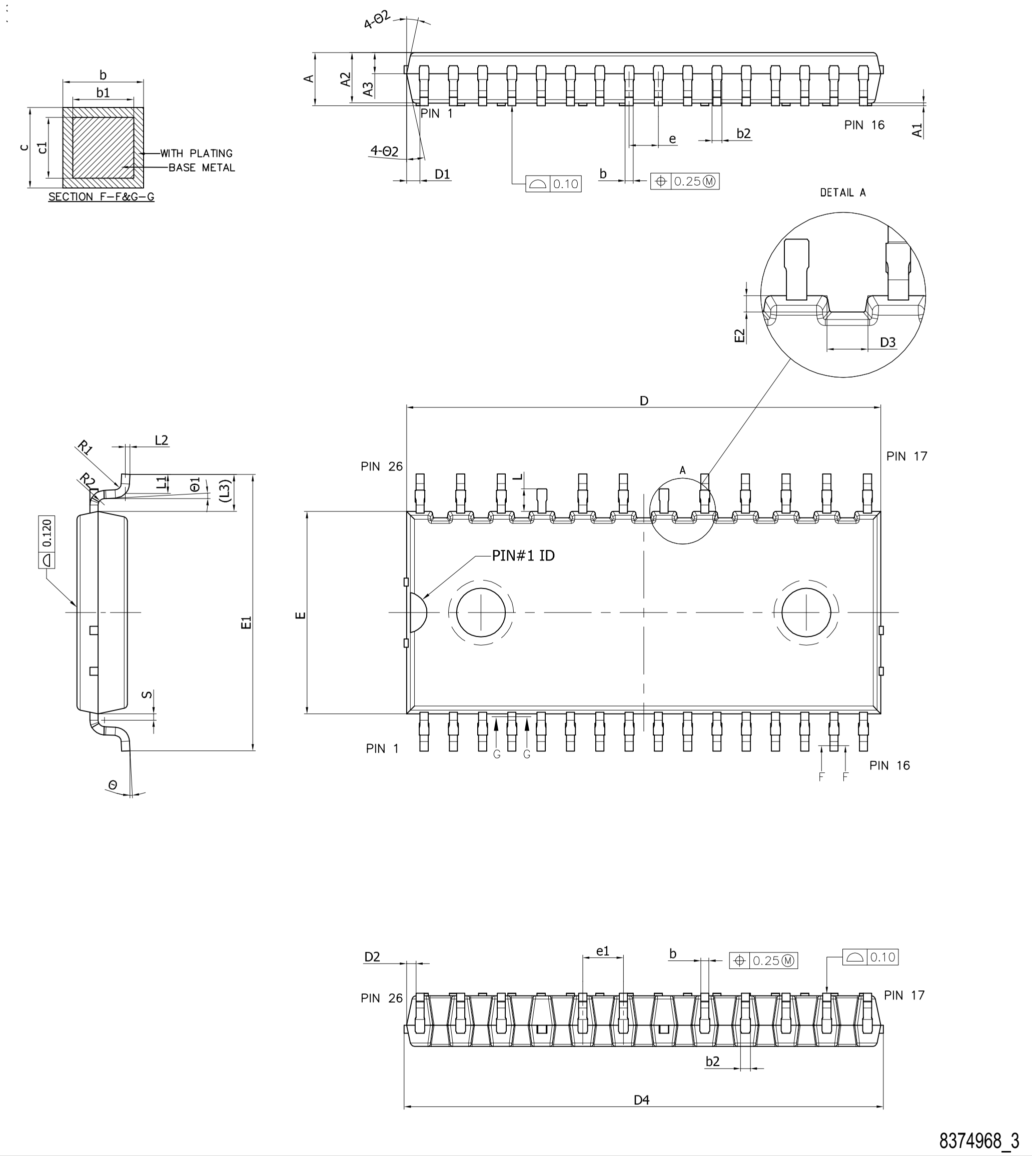


Table 16: NSDIP-26L package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			3.45
A1	0.10		0.25
A2	3.00	3.10	3.20
A3	1.70	1.80	1.90
b	0.47		0.57
b1	0.45	0.50	0.55
b2	0.63		0.67
c	0.47		0.57
c1	0.45	0.50	0.55
D	29.05	29.15	29.25
D1	0.70		
D2	0.45		
D3	0.90		
D4			29.65
E	12.35	12.45	12.55
E1	16.70	17.00	17.30
E2	0.35		
e	1.70	1.80	1.90
e1	2.40	2.50	2.60
L	1.24	1.39	1.54
L1	1.00	1.15	1.30
L2	0.25 BSC		
L3	2.275 REF		
R1	0.25	0.40	0.55
R2	0.25	0.40	0.55
S		0.39	0.55
ϴ	0°		8°
ϴ1	3° BSC		
ϴ2	10°	12°	14°

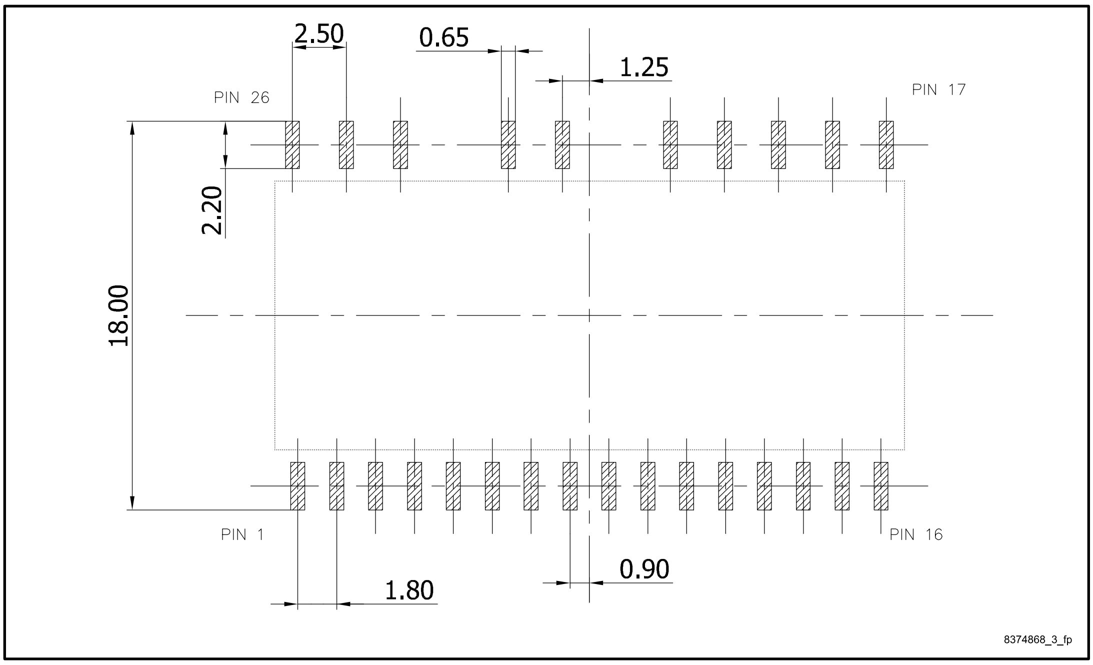


Figure 13: NSDIP-26L recommended footprint (dimensions are in mm)

7 Revision history

Table 17: Document revision history

Date	Revision	Changes
13-Apr-2017	1	Initial release.
08-Jan-2018	2	Datasheet status promoted from preliminary to production data. Updated features on cover page. Updated *Table 3: "Inverter part"*, *Table 5: "Total system"*, *Table 6: "Thermal data"* and *Table 13: "Sense comparator characteristics"* . Updated *Section 6.1: "NSDIP-26L package information"*.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения **«JONHON»**, а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов **«FORSTAR»**.

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А