

## HSP45102

### 12-Bit Numerically Controlled Oscillator

FN2810  
Rev 9.01  
Jan 28, 2020

The HSP45102 is Numerically Controlled Oscillator (NCO12) with 32-bit frequency resolution and 12-bit output. With over 69dB of spurious free dynamic range and worst case frequency resolution of 0.009Hz, the NCO12 provides significant accuracy for frequency synthesis solutions at a competitive price.

The frequency to be generated is selected from two frequency control words. A single control pin selects which word is used to determine the output frequency. Switching from one frequency to another occurs in one clock cycle, with a 6 clock pipeline delay from the time that the new control word is loaded until the new frequency appears on the output.

Two pins, PO-1, are provided for phase modulation. They are encoded and added to the top two bits of the phase accumulator to offset the phase in 90° increments.

The 13-bit output of the Phase Offset Adder is mapped to the sine wave amplitude via the Sine ROM. The output data format is offset binary to simplify interfacing to D/A converters. Spurious frequency components in the output sinusoid are less than -69dBc.

The NCO12 has applications as a Direct Digital Synthesizer and modulator in low cost digital radios, satellite terminals, and function generators.

### Features

- 33MHz, 40MHz Versions
- 32-Bit Frequency Control
- BFSK, QPSK Modulation
- Serial Frequency Load
- 12-Bit Sine Output
- Offset Binary Output Format
- 0.009Hz Tuning Resolution at 40MHz
- Spurious Frequency Components <-69dBc
- Fully Static CMOS
- Low Cost
- Pb-Free Plus Anneal Available (RoHS Compliant)

### Applications

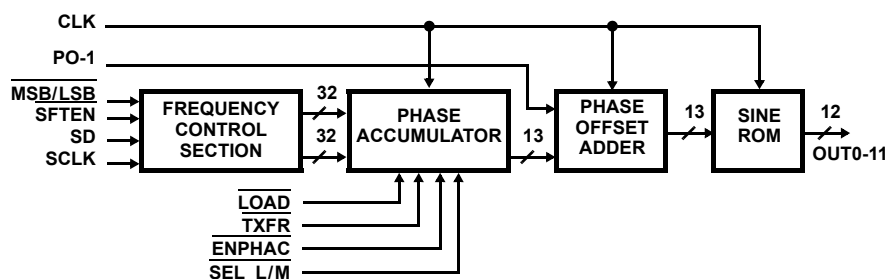
- Direct Digital Synthesis
- Modulation
- PSK Communications
- Related Products
  - HI5731 12-Bit, 100MHz D/A Converter

### Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HSP45102SC-33 (No longer available, recommended replacement: HSP45102SC-33Z)	HSP45102SC-33	0 to +70	28 Ld SOIC (300 mil)	M28.3
HSP45102SC-33Z (Note)	HSP45102SC-33Z	0 to +70	28 Ld SOIC (300 mil) (Pb-free)	M28.3
HSP45102SC-40	HSP45102SC -40	0 to +70	28 Ld SOIC (300 mil)	M28.3
HSP45102SC-40Z (Note)	HSP45102SC-40Z	0 to +70	28 Ld SOIC (300 mil)(Pb-free)	M28.3
HSP45102SI-33Z (Note)	HSP45102SI-33Z	0 to +70	28 Ld SOIC (300 mil) (Pb-free)	M28.3

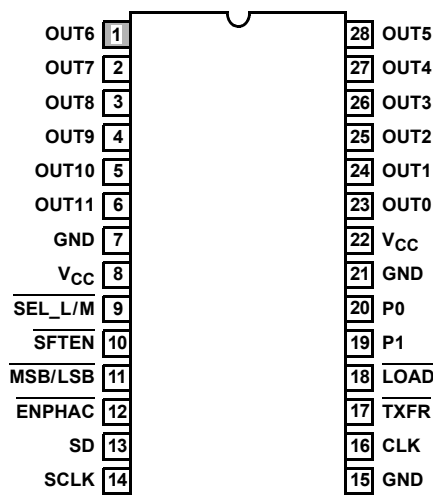
NOTE: Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

### Block Diagram



## Pinout

HSP45102  
(28 LEAD SOIC)  
TOP VIEW



## Pin Description

NAME	TYPE	DESCRIPTION
V <sub>CC</sub>		+5V power supply pin.
GND		Ground
P0-1	I	Phase modulation inputs (become active after a pipeline delay of four clocks). A phase shift of 0°, 90°, 180°, or 270° can be selected as shown in Table 1.
CLK	I	NCO clock. (CMOS level)
SCLK	I	This pin clocks the frequency control shift register.
SEL_L/M	I	A high on this input selects the least significant 32 bits of the 64-bit frequency register as the input to the phase accumulator; a low selects the most significant 32 bits.
SFTEN	I	The active low input enables the shifting of the frequency register.
MSB/LSB	I	This input selects the shift direction of the frequency register. A low on this input shifts in the data LSB first; a high shifts in the data MSB first.
ENPHAC	I	This pin, when low, enables the clocking of the Phase Accumulator. This input has a pipeline delay of four clocks.
SD	I	Data on this pin is shifted into the frequency register by the rising edge of SCLK when SFTEN is low.
TXFR	I	This active low input is clocked onto the chip by CLK and becomes active after a pipeline delay of four clocks. When low, the frequency control word selected by SEL_L/M is transferred from the frequency register to the phase accumulator's input register.
LOAD	I	This input becomes active after a pipeline delay of five clocks. When low, the feedback in the phase accumulator is zeroed.
OUT0-11	O	Output data. OUT0 is LSB. Unsigned.

All inputs are TTL level, with the exception of CLK.

Overline designates active low signals.

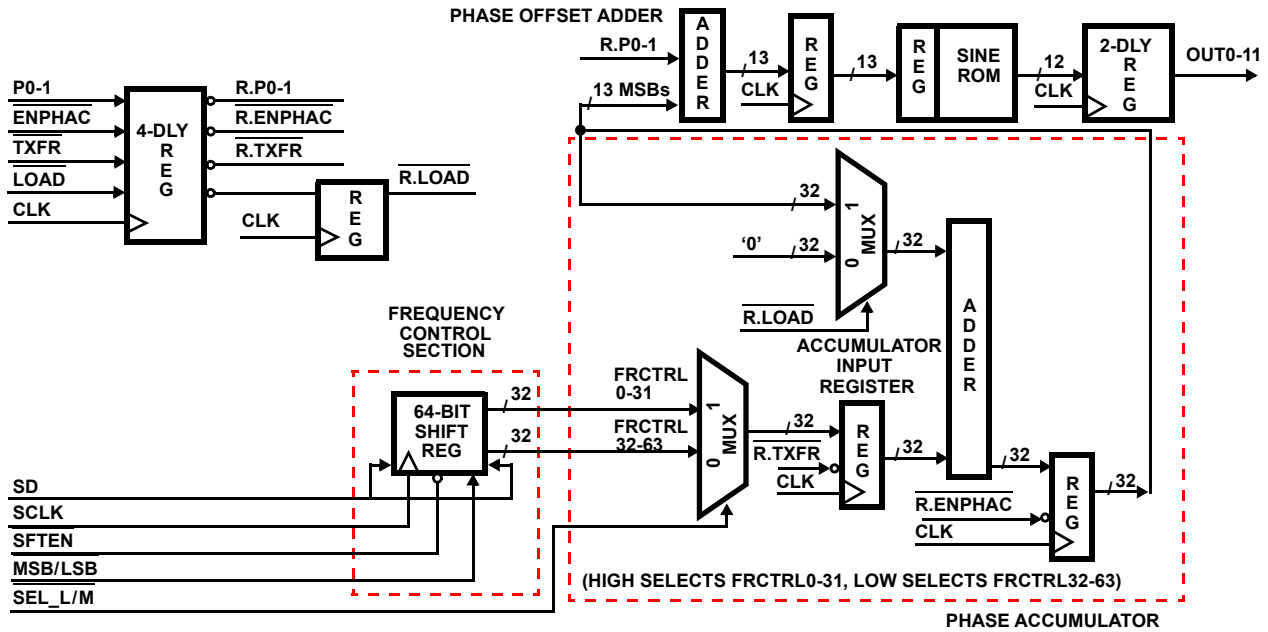


FIGURE 1. NCO-12 FUNCTIONAL BLOCK DIAGRAM

**Functional Description**

The NCO12 produces a 12-bit sinusoid whose frequency and phase are digitally controlled. The frequency of the sine wave is determined by one of two 32-bit words. Selection of the active word is made by SEL\_L/M. The phase of the output is controlled by the two-bit input P0-1, which is used to select a phase offset of 0°, 90°, 180°, or 270°.

As shown in the Block Diagram, the NCO12 consists of a Frequency Control Section, a Phase Accumulator, a Phase Offset Adder and a Sine ROM. The Frequency Control section serially loads the frequency control word into the frequency register. The Phase Accumulator and Phase Offset Adder compute the phase angle using the frequency control word and the two phase modulation inputs. The Sine ROM generates the sine of the computed phase angle. The format of the 12-bit output is offset binary.

**Frequency Control Section**

The Frequency Control Section shown in Figure 1 serially loads the frequency data into a 64-bit, bidirectional shift register. The shift direction is selected with the MSB/LSB input. When this input is high, the frequency control word on the SD input is shifted into the register MSB first. When MSB/LSB is low the data is shifted in LSB first. The register shifts on the rising edge of SCLK when SFTEN is low. The timing of these signals is shown in Figures 2A and 2B.

The 64 bits of the frequency register are sent to the Phase Accumulator Section where 32 bits are selected to control the frequency of the sinusoidal output.

**Phase Accumulator Section**

The phase accumulator and phase offset adder compute the phase of the sine wave from the frequency control word and the phase modulation bits P0-1. The architecture is shown in Figure 1. The most significant 13 bits of the 32-bit phase accumulator are summed with the two-bit phase offset to generate the 13-bit phase input to the Sine Rom. A value of 0 corresponds to 0°, a value of 1000 hexadecimal corresponds to a value of 180°.

The phase accumulator advances the phase by the amount programmed into the frequency control register. The output frequency is equal to:

$$f_{LO} = (N \times f_{CLK} / 2^{32}), \text{ or} \tag{EQ. 1}$$

$$N = \text{INT} \left[ \left( \frac{f_{OUT}}{f_{CLK}} \right) 2^{32} \right], \tag{EQ. 2}$$

where N is the 32 bits of frequency control word that is programmed. INT[\*] is the integer of the computation. For example, if the control word is 20000000 hexadecimal and the clock frequency is 30MHz, then the output frequency would be  $f_{CLK}/8$ , or 3.75MHz.

The frequency control multiplexer selects the least significant 32 bits from the 64-bit frequency control register when SEL\_L/M is high, and the most significant 32 bits when SEL\_L/M is low. When only one frequency word is desired, SEL\_L/M and MSB/LSB must be either both high or both low. This is due to the fact that when a frequency control word is loaded into the shift register LSB first, it enters through the most significant bit of the register. After 32 bits have been

shifted in, they will reside in the 32 most significant bits of the 64-bit register.

When  $\overline{\text{TXFR}}$  is asserted, the 32 bits selected by the frequency control multiplexer are clocked into the phase accumulator input register. At each clock, the contents of this register are summed with the current contents of the accumulator to step to the new phase. The phase accumulator stepping may be inhibited by holding ENPHAC high. The phase accumulator may be loaded with the value in the input register by asserting LOAD, which zeroes the feedback to the phase accumulator.

The phase adder sums the encoded phase modulation bits P0-1 and the output of the phase accumulator to offset the phase by 0°, 90°, 180° or 270°. The two bits are encoded to produce the phase mapping shown in Table 1. This phase mapping is provided for direct connection to the in-phase and quadrature data bits for QPSK modulation.

TABLE 1. PHASE MAPPING

P0-1 CODING		
P1	P0	PHASE SHIFT (DEGREES)
0	0	0
0	1	90
1	0	270
1	1	180

**ROM Section**

The ROM section generates the 12-bit sine value from the 13-bit output of the phase adder. The output format is offset binary and ranges from 001 to FFF hexadecimal, centered around 800 hexadecimal.

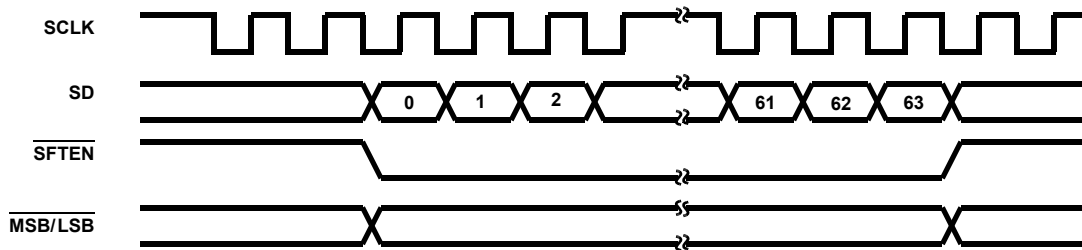


FIGURE 2A. FREQUENCY LOADING ENABLED BY  $\overline{\text{SFTEN}}$

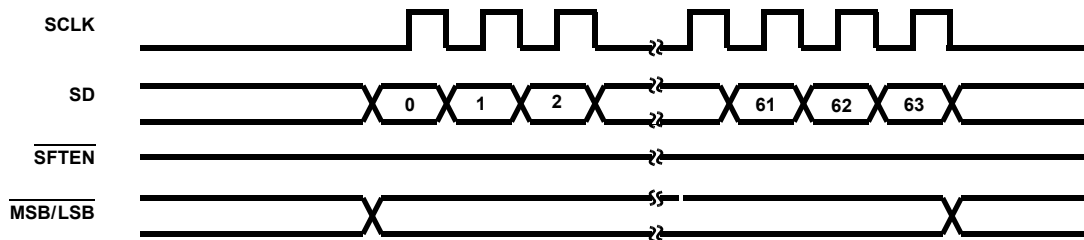


FIGURE 2B. FREQUENCY LOADING CONTROLLED BY SCLK

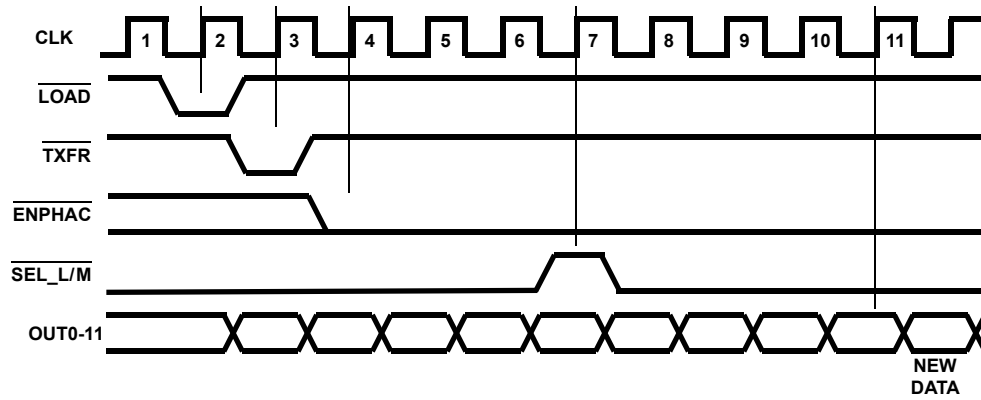


FIGURE 3. I/O TIMING

**Absolute Maximum Ratings**  $T_A = +25^\circ\text{C}$ 

Supply Voltage ..... +6.0V  
 Input, Output or I/O Voltage Applied ..... GND -0.5V to  $V_{CC} + 0.5\text{V}$   
 ESD Classification ..... Class 1

**Operating Conditions**

Operating Voltage Range (Commercial, Industrial) .. +4.75V to +5.25V  
 Operating Temperature Range (Commercial) .....  $0^\circ\text{C}$  to  $+70^\circ\text{C}$   
 Operating Temperature Range (Industrial) .....  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Thermal Information**

Thermal Resistance (Typical, Note 1) .....  $\theta_{JA}$  ( $^\circ\text{C}/\text{W}$ )  
 SOIC Package ..... 70  
 Maximum Junction Temperature .....  $+150^\circ\text{C}$   
 Maximum Storage Temperature Range .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Pb-free reflow profile ..... see TB493

**Die Characteristics**

Backside Potential .....  $V_{CC}$

**DC Electrical Specifications**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Logical One Input Voltage	$V_{IH}$	$V_{CC} = 5.25\text{V}$	2.0	-	V
Logical Zero Input Voltage	$V_{IL}$	$V_{CC} = 4.75\text{V}$	-	0.8	V
High Level Clock Input	$V_{IHC}$	$V_{CC} = 5.25\text{V}$	3.0	-	V
Low Level Clock Input	$V_{ILC}$	$V_{CC} = 4.75\text{V}$	-	0.8	V
Output HIGH Voltage	$V_{OH}$	$I_{OH} = -400\mu\text{A}$ , $V_{CC} = 4.75\text{V}$	2.6	-	V
Output LOW Voltage	$V_{OL}$	$I_{OL} = +2.0\text{mA}$ , $V_{CC} = 4.75\text{V}$	-	0.4	V
Input Leakage Current	$I_I$	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25\text{V}$	-10	10	$\mu\text{A}$
Standby Power Supply Current	$I_{CCSB}$	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25\text{V}$ , Note 4	-	500	$\mu\text{A}$
Operating Power Supply Current	$I_{CCOP}$	$f = 33\text{MHz}$ , $V_{IN} = V_{CC}$ or GND $V_{CC} = 5.25\text{V}$ , Notes 2 and 4	-	99	mA

**Capacitance**  $T_A = +25^\circ\text{C}$ , Note 3

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Input Capacitance	$C_{IN}$	FREQ = 1MHz, $V_{CC} = \text{Open}$ . All measurements are referenced to device ground	-	10	pF
Output Capacitance	$C_O$		-	10	pF

**NOTES:**

- Power supply current is proportional to operating frequency. Typical rating for  $I_{CCOP}$  is 3mA/MHz.
- Not tested, but characterized at initial design and at major process/design changes.
- Output load per test load circuit with switch open and  $C_L = 40\text{pF}$ .

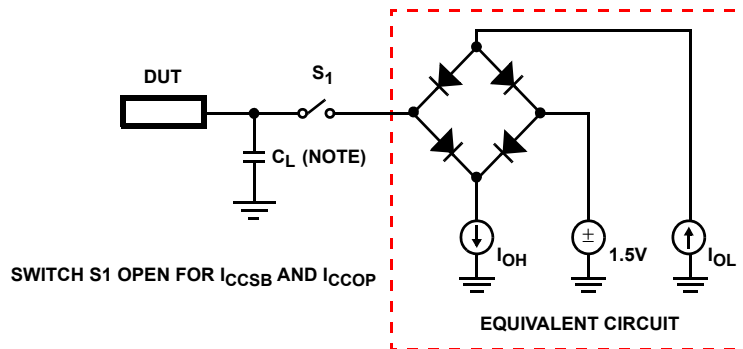
**AC Electrical Specifications**  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$  (Note 5)

PARAMETER	SYMBOL	NOTES	-33 (33MHz)		-40 (40MHz)		UNITS
			MIN	MAX	MIN	MAX	
Clock Period	$t_{CP}$		30	-	25	-	ns
Clock High	$t_{CH}$		12	-	10	-	ns
Clock Low	$t_{CL}$		12	-	10	-	ns
SCLK High/Low	$t_{SW}$		12	-	10	-	ns
Setup Time SD to SCLK Going High	$t_{DS}$		12	-	12	-	ns
Hold Time SD from SCLK Going High	$t_{DH}$		0	-	0	-	ns
Setup Time $\overline{SFTEN}$ , $\overline{MSB/LSB}$ to SCLK Going High	$t_{MS}$		15	-	12	-	ns
Hold Time $\overline{SFTEN}$ , $\overline{MSB/LSB}$ from SCLK Going High	$t_{MH}$		0	-	0	-	ns
Setup Time SCLK High to CLK Going High	$t_{SS}$	Note 6	16	-	15	-	ns
Setup Time P0-1 to CLK Going High	$t_{PS}$		15	-	12	-	ns
Hold Time P0-1 from CLK Going High	$t_{PH}$		1	-	1	-	ns
Setup Time $\overline{LOAD}$ , $\overline{TXFR}$ , $\overline{ENPHAC}$ , $\overline{SEL\_L/M}$ to CLK Going High	$t_{ES}$		15	-	13	-	ns
Hold Time $\overline{LOAD}$ , $\overline{TXFR}$ , $\overline{ENPHAC}$ , $\overline{SEL\_L/M}$ from CLK Going High	$t_{EH}$		1	-	1	-	ns
CLK to Output Delay	$t_{OH}$		2	15	2	13	ns
Output Rise, Fall Time	$t_{RF}$	Note 7	8	-	8	-	ns

NOTES:

- AC testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 0V and 3.0V; Timing reference levels (CLK) 2.0V; All others 1.5V. Output load per test load circuit with switch closed and  $C_L = 40pF$ . Output transition is measured at  $V_{OH} > 1.5V$  and  $V_{OL} < 1.5V$ .
- If TXFR is active, care must be taken to not violate setup and hold times as data from the shift registers may not have settled before CLK occurs.
- Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

**AC Test Load Circuit**



NOTE: Test head capacitance.

**Waveforms**

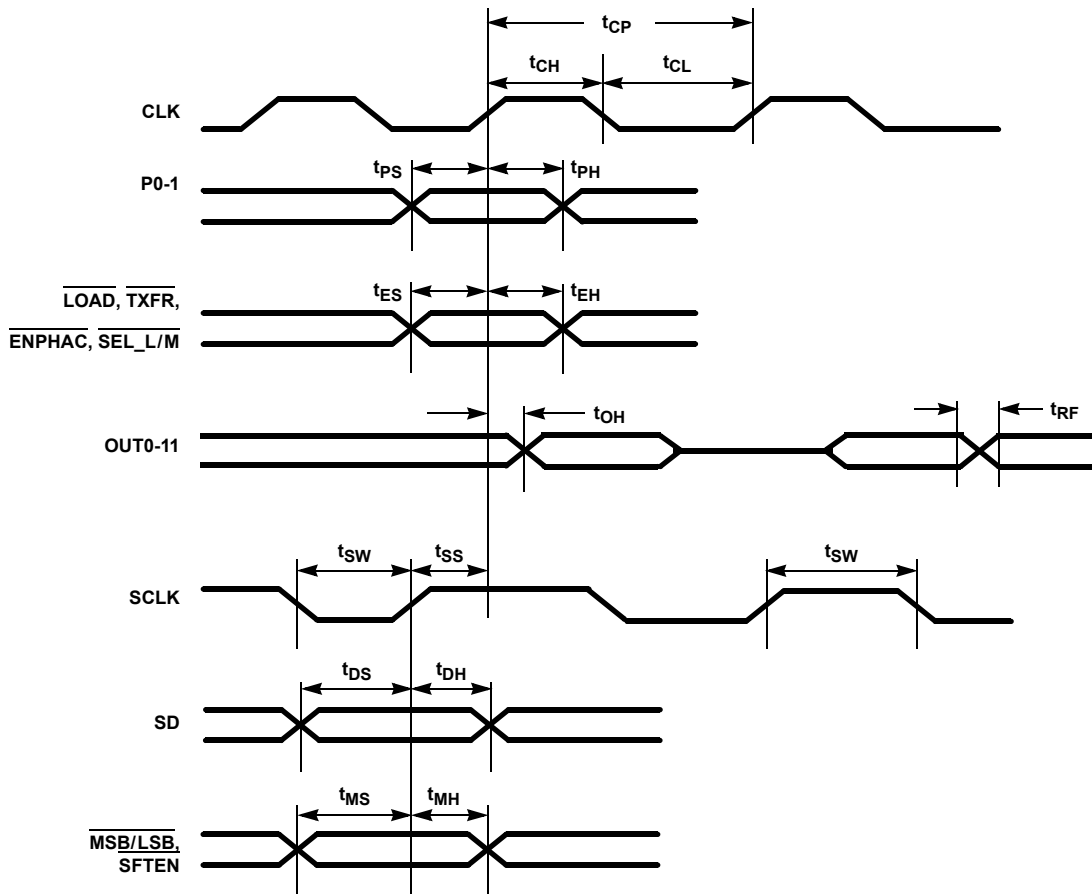


FIGURE 4.

**Revision History**

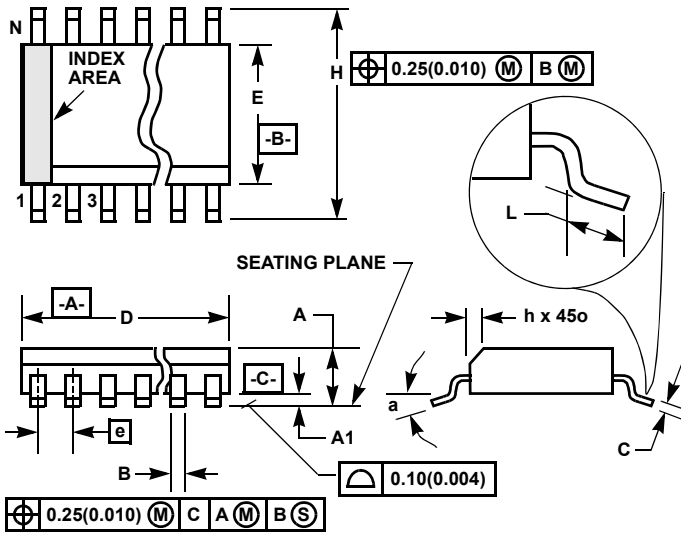
Rev.	Date	Description
9.01	Jan 28, 2020	Updated Ordering Information. Added Revision History table. Updated POD M28.3 from rev 0 to rev 1. Changes: - Added land pattern Updated Disclaimer.



**Small Outline Plastic Packages (SOIC)**

For the most recent package outline drawing, see [M28.3](#).

**M28.3 (JEDEC MS-013-AE ISSUE C)  
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE**



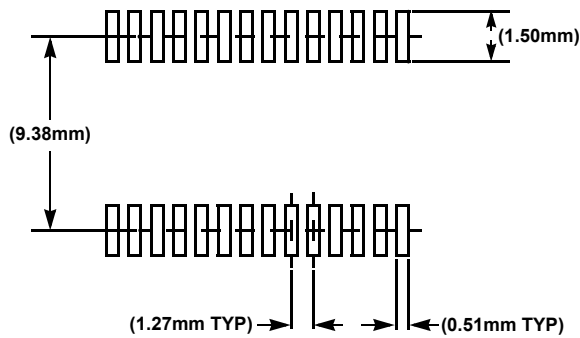
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
$\alpha$	0°	8°	0°	8°	-

Rev. 1, 1/13

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**TYPICAL RECOMMENDED LAND PATTERN**



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(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

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Электронная почта: [ocean@oceanchips.ru](mailto:ocean@oceanchips.ru)

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Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А