
N-Channel, Depletion-Mode, Vertical DMOS FET

Features

- High-input impedance
- Low-input capacitance
- Fast switching speeds
- Low on-resistance
- Free from secondary breakdown
- Low input and output leakages

Applications

- Normally-on switches
- Battery operated systems
- Converters
- Linear amplifiers
- Constant current sources
- Telecom

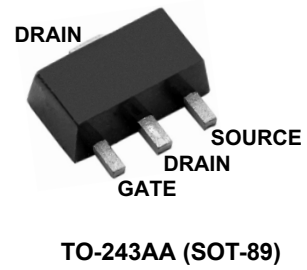
Description

This low threshold, depletion-mode, normally-on, transistor utilizes an advanced vertical Diffusion Metal Oxide Semiconductor (DMOS) structure and a well proven silicon-gate manufacturing process. This combination produces a device with the power-handling capabilities of bipolar transistors, plus the high-input impedance and positive-temperature coefficient inherent in Metal-Oxide Semiconductor (MOS) devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Vertical DMOS Field-Effect Transistors (FETs) are ideally suited to a wide range of switching and amplifying applications where a very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

DN1509

Package Type



See [Table 2-1](#) for pin information

1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Drain-to-source voltage.....	BV_{DSX}
Drain-to-gate voltage.....	BV_{DGX}
Gate-to-source voltage.....	$\pm 20V$
Operating and storage temperature.....	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Electrical Specifications

TABLE 1-1: DC AND AC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J = +25^{\circ}C$						
Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Parameters (Note 1, unless otherwise stated)						
BV_{DSX}	Drain-to-source breakdown voltage	90	–	–	V	$V_{GS} = -5V, I_D = 1.0\mu A$
$V_{GS(OFF)}$	Gate-to-source off voltage	-1.8	–	-3.5	V	$I_D = 10\mu A$
$\Delta V_{GS(OFF)}$	$V_{GS(OFF)}$ change with temperature	–	–	-4.5	mV/ $^{\circ}C$	$V_{DS} = 15V, I_D = 10\mu A$
I_{GSS}	Gate body leakage	–	–	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{D(OFF)}$	Drain-to-source leakage current	–	–	1.0	μA	$V_{DS} = BV_{DSX}, V_{GS} = -5.0V$
		–	–	1.0	mA	$V_{DS} = 0.8 BV_{DSX}, V_{GS} = -5.0V, T_A = 125^{\circ}C$
I_{DSS}	Saturated drain-to-source current	300	540	–	mA	$V_{GS} = 0V, V_{DS} = 25V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	–	3.2	6.0	Ω	$V_{GS} = 0V, I_D = 200mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	–	–	1.1	%/ $^{\circ}C$	$V_{GS} = 0V, I_D = 200mA$ (Note 2)
AC Parameters (Note 2)						
G_{FS}	Forward transconductance	200	–	–	mmho	$V_{DS} = 10V, I_D = 200mA$
C_{ISS}	Input capacitance	–	70	150	pF	$V_{GS} = -10V, V_{DS} = 25V, f = 1MHz$
C_{OSS}	Common source output capacitance	–	20	40		
C_{RSS}	Reverse transfer capacitance	–	6.0	15		
$t_{d(ON)}$	Turn-on delay time	–	12	30	ns	$V_{DD} = 25V, I_D = 100mA, R_{GEN} = 25\Omega$
t_r	Rise time	–	16	45		
$t_{d(OFF)}$	Turn-off delay time	–	15	45		
t_f	Fall time	–	25	60		
Diode Parameters						
V_{SD}	Diode forward voltage drop	–	–	1.8	V	$V_{GS} = -5.0V, I_{SD} = 500mA$ (Note 1)
t_{rr}	Reverse recovery time	–	400	–	ns	$V_{GS} = -5.0V, I_{SD} = 500mA$ (Note 2)

Note 1: All DC parameters are 100% tested at $25^{\circ}C$ unless otherwise stated. Pulse test: 300 μs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

DN1509

TABLE 1-2: TYPICAL THERMAL RESISTANCE

Package	θ_{ja}
5-lead SOT-23	253°C/W
TO-243AA (SOT-89)	78°C/W ¹

1. Mounted on FR4 board, 25mm x 25mm x 1.57 mm

TABLE 1-3: THERMAL CHARACTERISTICS

Package	I_D^1 continuous (mA)	I_D pulsed (mA)	Power Dissipation @ $T_A = 2.5^\circ\text{C}$ (W)	I_{DR}^1 (mA)	I_{DRM} (mA)
5-lead SOT-23	200	500	0.49	200	500
TO-243AA (SOT-89)	360	500	1.6 ²	360	500

1. I_D continuous is limited by max rated T_J
2. Mounted on FR4 board, 25mm x 25mm x 1.57 mm

2.0 PIN DESCRIPTION

The locations of the pins are listed in [Package Type](#).

TABLE 2-1: PIN DESCRIPTION

Pin # SOT-23	Pin # TO-243AA	Function
5	1	GATE
2	2	DRAIN
4	3	SOURCE
1,3		NC

3.0 APPLICATION INFORMATION

Figure 3-1 shows the switching waveform and test circuit for DN1509.

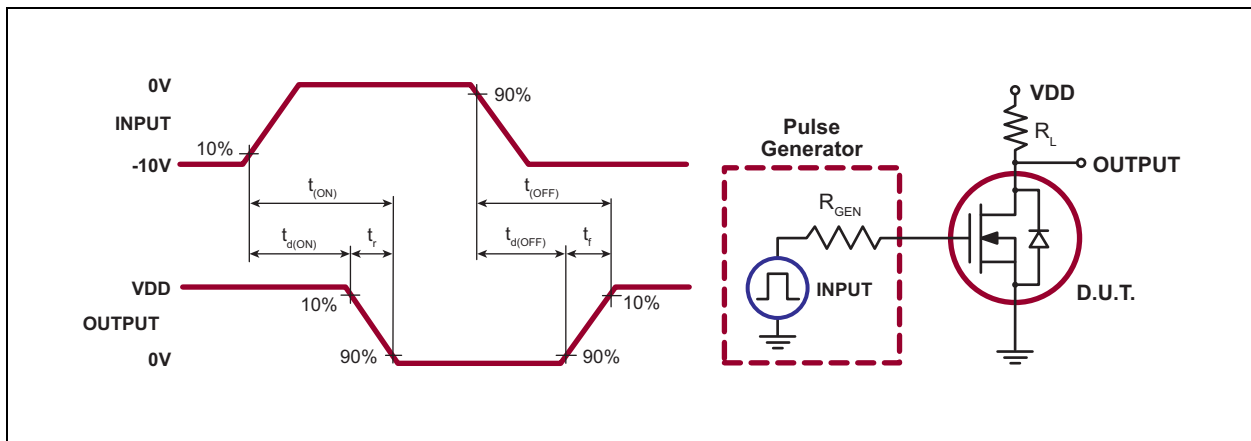


FIGURE 3-1: Switching Waveforms and Test Circuit

Product Summary

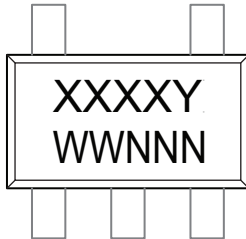
BV_{DSX}/BV_{DGX} (V)	$R_{DS(ON)}$ (max) (Ω)	I_{DSS} (min) (mA)
90	6.0	300

DN1509

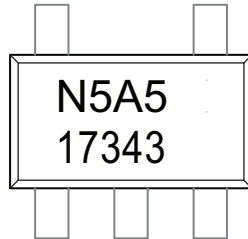
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

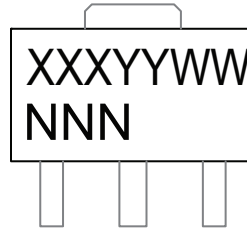
5-lead SOT-23 *



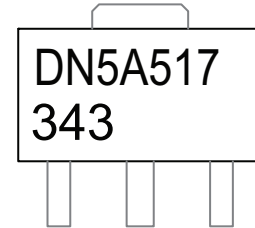
Example



3-lead TO-243AA *
(SOT-89)



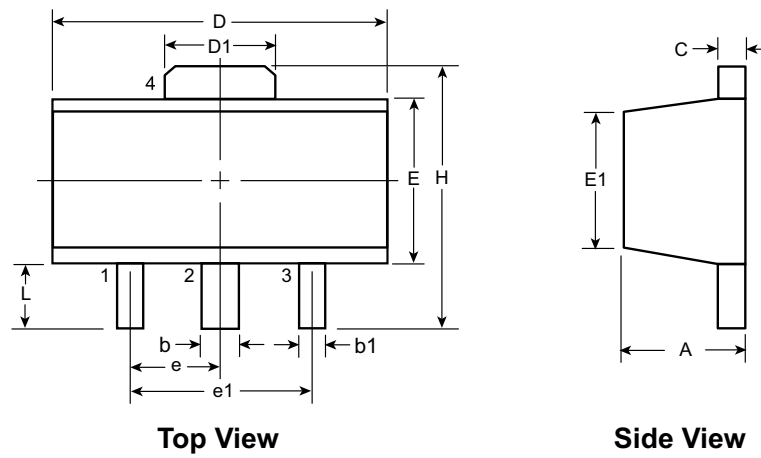
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

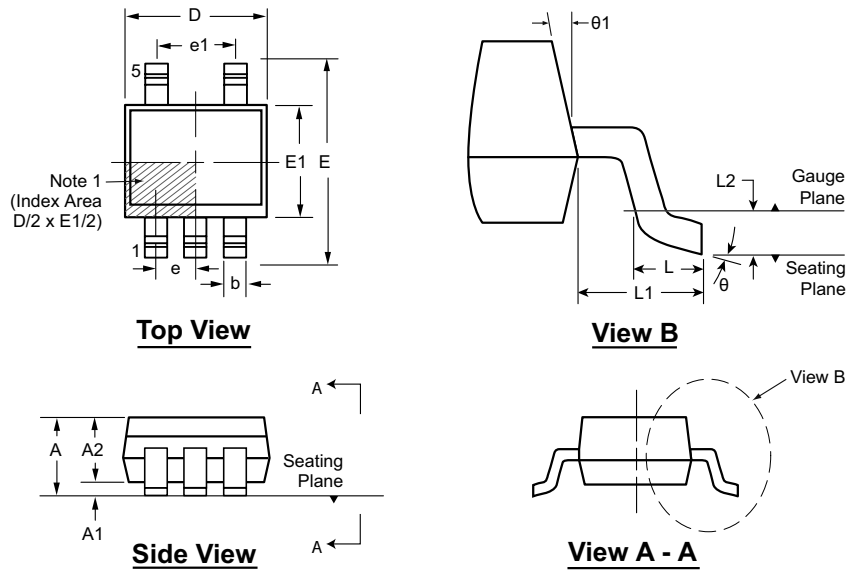
Symbol	A	b	b1	C	D	D1	E	E1	e	e1	H	L		
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00 [†]	1.50 BSC	3.00 BSC	3.94	0.73 [†]	
	NOM	-	-	-	-	-	-	-	-			-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20	

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

[†] This dimension differs from the JEDEC drawing

Drawings not to scale.

5-Lead SOT-23 Package Outline (K1) 2.90x1.60mm body, 1.45mm height (max), 0.95mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	E	E1	e	e1	L	L1	L2	θ	$\theta 1$	
Dimension (mm)	MIN	0.90*	0.00	0.90	0.30	2.75*	2.60*	1.45*	0.95 BSC	1.90 BSC	0.30	0.60 REF	0.25 BSC	0°	5°
	NOM	-	-	1.15	-	2.90	2.80	1.60			0.45			4°	10°
	MAX	1.45	0.15	1.30	0.50	3.05*	3.00*	1.75*			0.60			8°	15°

JEDEC Registration MO-178, Variation AA, Issue C, Feb. 2000.

* This dimension is not specified in the JEDEC drawing.

Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (June 2015)

- Update file to new format

DN1509

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	DN1509	=	N-Channel, Depletion-Mode, vertical DMOS FET		
Package:	K1	=	SOT-23, 5-lead		
	N8	=	TO-243AA (SOT-89), 3-lead		
Environmental	G	=	Lead (Pb)-free/ROHS-compliant package		
Media Type:	(blank)	=	3000/Reel for K1 packages		
		=	2000/Reel for N8 packages		

Examples:

a) DN1509K1-G SOT-23 package, 3000/reel

b) DN1509N8-G TO-243AA package, 2000/reel

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