



FRACTIONAL-N PLL WITH INTEGRATED VCO, 7.8 - 8.8 GHz

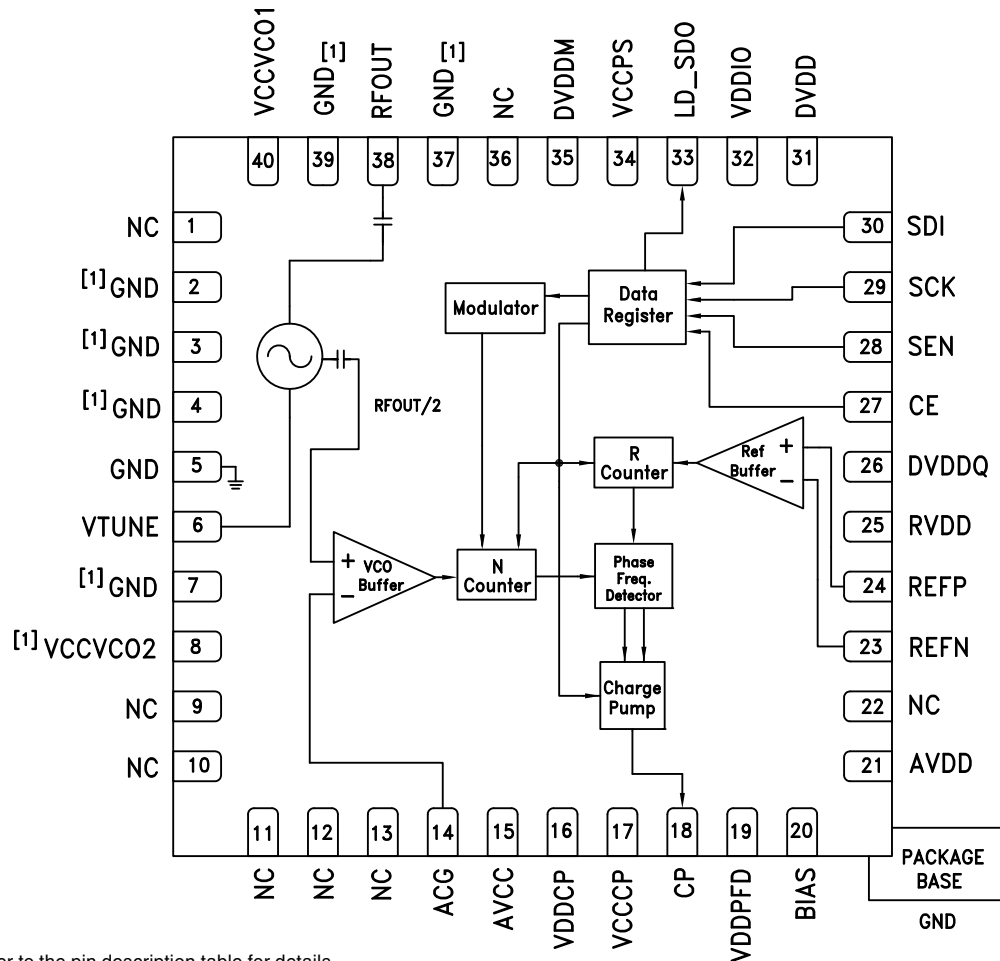
Features

- RF Bandwidth: 7.8 GHz to 8.8 GHz
- Fractional or Integer Modes
- Ultra Low Phase Noise
8.3 GHz; 50 MHz Ref.
-97 / -101 dBc/Hz @ 10 kHz (Frac / Int)
-140 dBc/Hz @ 1 MHz (Open Loop)
- Figure of Merit (FOM)
-221 / -226 dBc/Hz (Frac / Int)
- 24-bit Step Size, Resolution 3 Hz typ
- 225 MHz, 14-bit reference path input
- Direct FSK Modulation Mode
- Cycle Slip Prevention
- Read / Write Serial Port, Chip ID
- 40 Lead 6 x 6 mm SMT Package: 36 mm²

Typical Applications

- VSAT Radio
- Point-to-Point / Multi-Point Radio
- Test Equipment & Industrial Control
- Military End-Use
- Phased Array Applications

Functional Diagram



[1] Please refer to the pin description table for details

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FRACTIONAL-N PLL WITH INTEGRATED VCO, 7.8 - 8.8 GHz

General Description

The HMC765LP6CE is a fully functional Fractional-N Phase-Locked-Loop (PLL) with an Integrated Voltage Controlled Oscillator (VCO). The input reference frequency range is 100 kHz to 220 MHz while the advanced delta-sigma modulator design in the fractional PLL allows both ultra-fine step sizes and very low spurious products. The highly integrated structure provides excellent phase noise performance over temperature, shock and process. The HMC765LP6CE is packaged in a leadless QFN 6 x 6 mm surface mount package. The output power is 13 dBm typical, making the HMC765LP6CE ideal for driving the LO port of many of Hittite's Hi Linearity and I/Q mixer products.

For theory of operation and register map refer to the "PLLs w/ Integrated VCO - Microwave VCOs" Operating Guide. To view the [Operating Guide](#), please visit www.hittite.com and choose HMC765LP6CE from the "Search by Part Number" pull down menu.

Electrical Specifications, $T_A = +25^\circ\text{C}$; VCCVCO, VDDCP, VCCCP = +5V; AVCC, VCCPS VDDPFD, AVDD, RVDD, DVDD, DVDDM, DVDDQ, VDDIO = +3.3V; AGND = DGND = 0V

| Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|-------|-------------|-------|------------------|
| RF Output Characteristics | | | | | |
| VCO Output Frequency Range | | 7.8 | 8.3 | 8.8 | GHz |
| VCO Output Power | | 10 | | 15 | dBm |
| VCO Tuning Voltage | | 2 | | 13 | V |
| VCO Tuning Sensitivity | $V_{TUNE} = +5V$ | | 150 | | MHz/V |
| Frequency Pulling (into a 2:1 VSWR) | | | 5 | | MHz pp |
| Frequency Pushing | $V_{TUNE} = +5V$ | | 10 | | MHz/V |
| Frequency Drift Rate | | | 0.9 | | MHz/°C |
| Sub Harmonic (1/2) | | | 35 | | dBc |
| Harmonic (2 nd) | | | 10 | | dBc |
| Harmonic (3 rd) | | | 32 | | dBc |
| VCO SSB Phase Noise @ 100 kHz Offset (Open Loop) | $V_{TUNE} = +5V$ $F_{VCO} = 8.3\text{ GHz}$ | | -115 | | dBc/Hz |
| Synthesizer In-Band SSB Phase Noise @ 10 kHz Offset (Frac/Int) | $F_{ref} = 50\text{ MHz}$ $F_{vco} = 8.3\text{ GHz}$ Loop BW = 100 kHz | | -97 / -101 | | dBc/Hz |
| Synthesizer Normalized In-Band SSB Phase Noise Floor (Frac/Int) | | | -221 / -226 | | dBc/Hz |
| Synthesizer Fractional Spurs [1] | | | -65 | | dBc |
| Synthesizer Frequency Settling Time (100 MHz Step) | From 8.3 GHz to 8.4 GHz Loop BW = 100 kHz | | 110 | | μs |
| 16-Bit Divider Range (Int) | N Divider Ratio $2^{16}+31$ | 32 | | 65567 | |
| 16-Bit Divider Range (Frac) | N Divider Ratio $2^{16}-1$ | 36 | | 65535 | |
| REF Input Characteristics | | | | | |
| Max Ref Input Frequency (3.3V) | | 200 | 225 | | MHz |
| Min Ref Input Frequency | | | 100 | 200 | kHz |
| Ref Input Sensitivity | AC Coupled | | 500 | 700 | mV _{pp} |
| Max Ref Input | DC Coupled | 0 | | VDDIO | V |
| Ref Input Capacitance | | | | 5 | pF |
| 14-Bit Ref Divider Range | | 16383 | | 1 | |

[1] Actual spur level is dependent on loop parameters and will increase at division ratios closest to integer boundaries. Number listed is average value.



FRACTIONAL-N PLL WITH INTEGRATED VCO, 7.8 - 8.8 GHz

Electrical Specifications (Continued)

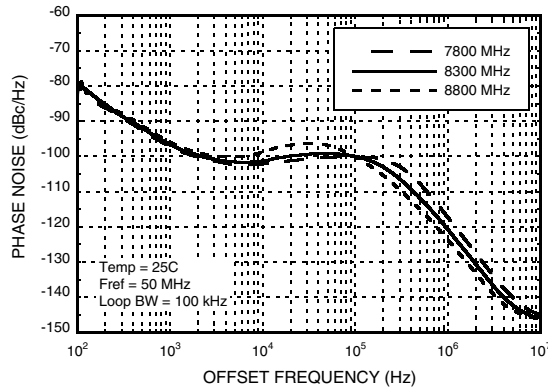
| Parameter | Condition | Min. | Typ. | Max. | Units |
|---|----------------------------|-----------|-------|-------|--------|
| Phase Detector | | | | | |
| Max Phase Detector Frequency (Frac) | | 70 | 105 | | MHz |
| Max Phase Detector Frequency (Int) | | 140 | 160 | | MHz |
| Min Phase Detector Frequency | | | | 100 | kHz |
| Charge Pump | | | | | |
| Max Output Current | | 2 | | | mA |
| Min Output Current | | 500 | | | μA |
| Charge Pump Noise | Input referred 50 MHz Ref. | | -145 | | dBc/Hz |
| Logic Inputs | | | | | |
| VIH Input High Voltage | | VDDIO-0.4 | | VDDIO | V |
| VIL Input Low Voltage | | 0 | | 0.4 | V |
| Logic Outputs | | | | | |
| VOH Output High Voltage | | VDDIO-0.4 | | VDDIO | V |
| VOL Output Low Voltage | | 0 | | 0.4 | V |
| Serial Port Max Clock | | | 50 | | MHz |
| Power Supply Voltages | | | | | |
| Analog 3.3V Supplies: AVCC, VDDPFD, AVDD, RVDD, VCCPS | AVDD must equal DVDD | 3 | 3.3 | 3.45 | V |
| Digital Internal Supplies: DVDD, DVDDQ, DVDDM | | 3 | 3.3 | 3.45 | V |
| Digital I/O Supplies: VDDIO | Logic I/O | 1.8 | 3.3 | 5.5 | V |
| Analog 5V Supplies: VCCVCO, VDDCP, VCCCP | VCCCP must equal VDDCP | 4.75 | 5 | 5.25 | V |
| Power Supply Currents | | | | | |
| Total Current Consumption (5V) | | | 245 | 290 | mA |
| Total Current Consumption (3.3V) | | | 90 | 110 | mA |
| Power Down Current ^[1] | CSP Disabled | | 1 | 10 | μA |
| | CSP Enabled | | 450 | | μA |
| Bias Reference Voltage | Measured with 10 GΩ meter | 1.880 | 1.920 | 1.960 | V |

[1] Refers only to the Synthesizer portion of the HMC765LP6CE

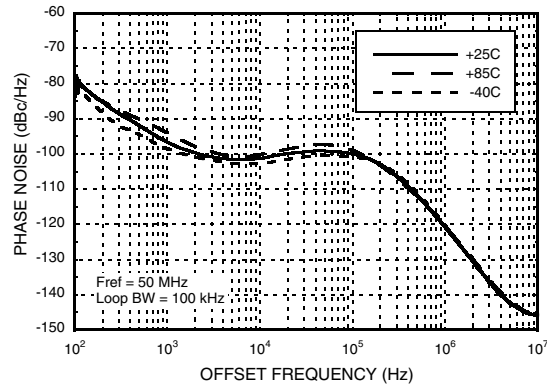


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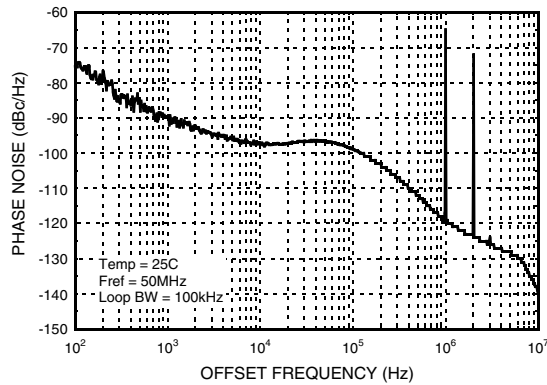
SSB Phase Noise vs. Frequency, Integer Mode



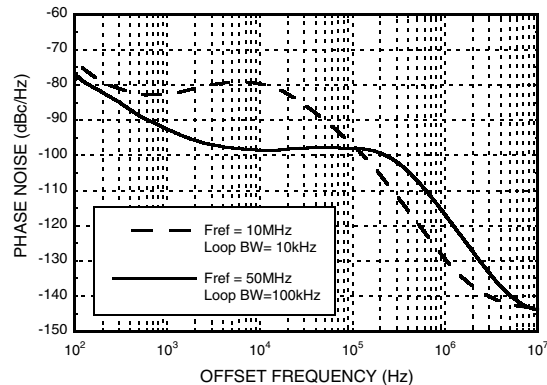
SSB Phase Noise vs. Temperature @ 8.3 GHz, Integer Mode



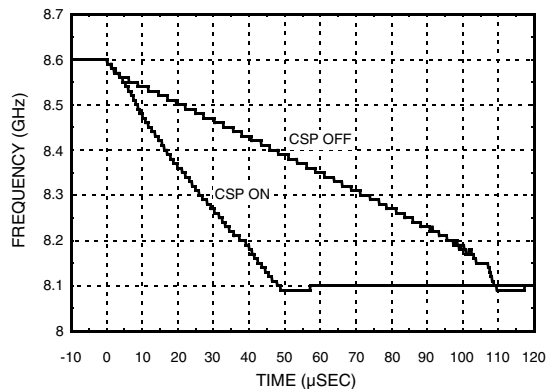
SSB Phase Noise Fractional Spurs @ 8.302 GHz



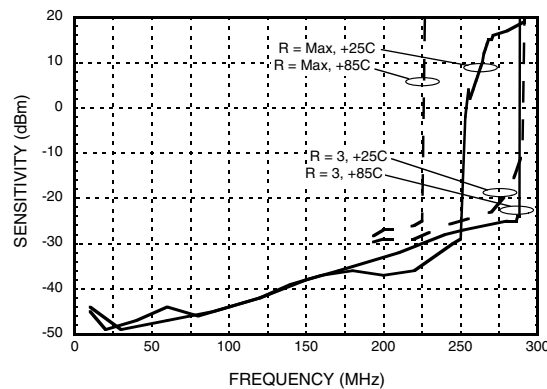
SSB Phase noise vs. Reference Freq. & Loop BW @ 8.3 GHz, Integer Mode



Example of Cycle Slip Prevention Hop from 8.6 to 8.1 GHz



Typical Reference Sensitivity vs. Frequency, 3.3V [1]

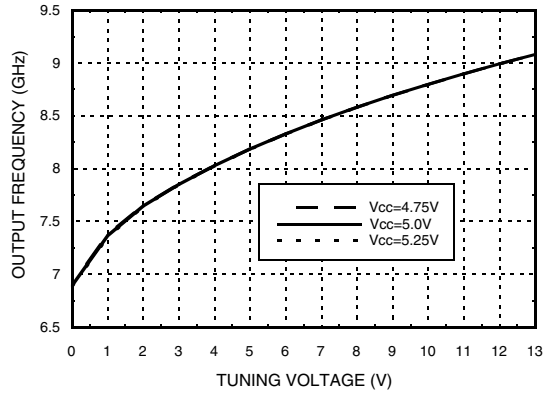


[1] R refers to the reference path division ratio

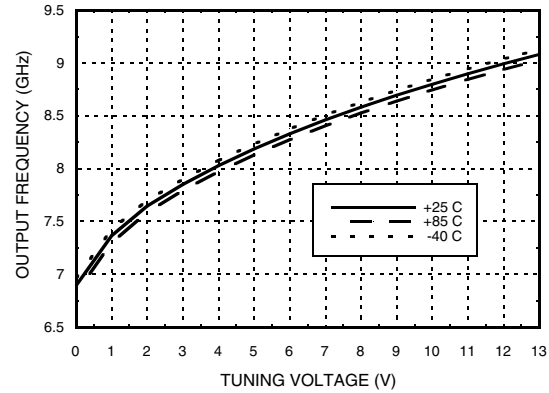


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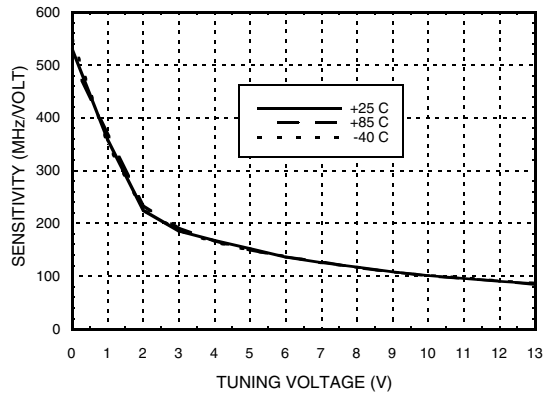
Frequency vs. Tuning Voltage, T = 25°C



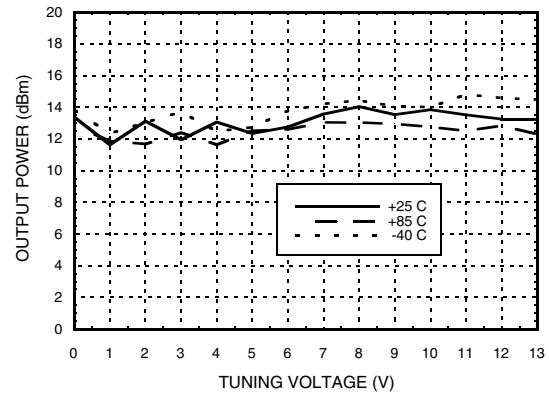
Frequency vs. Tuning Voltage, Vcc = +5V



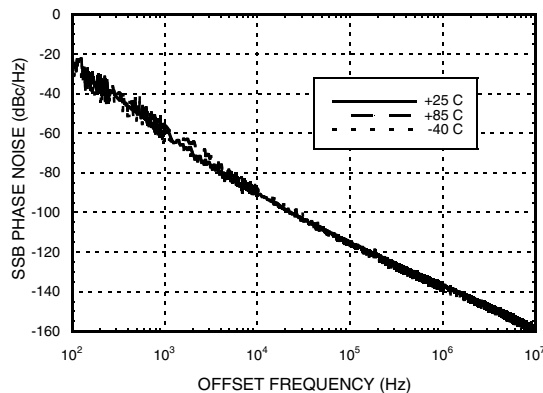
Sensitivity vs. Tuning Voltage, Vcc = +5V



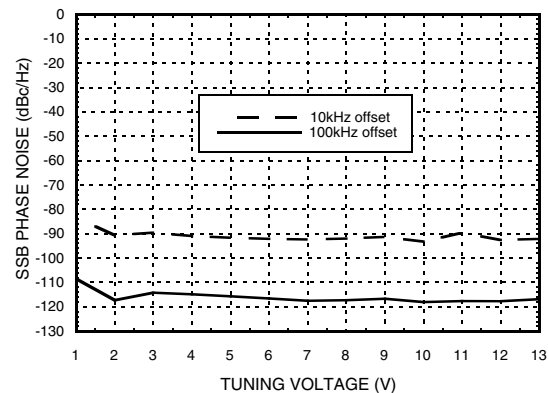
Output Power vs. Tuning Voltage, Vcc = +5V



Open Loop VCO SSB Phase Noise @ Vtune = +5V



Open Loop VCO SSB Phase Noise vs. Tuning Voltage



7

PLLS w/ INTEGRATED VCO - SMT

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Pin Descriptions

| Pin Number | Function | Description |
|-------------------|-------------|--|
| 1, 9 - 13, 22, 36 | N/C | No Connection. These pins may be connected to RF/DC ground. Performance will not be affected. |
| 2 - 4, 7, 37, 39 | GND [1] | These pins must be connected to RF/DC Ground |
| 5 | GND | These pins and package bottom must be connected to RF/DC Ground |
| 8 | VCCVCO2 [2] | +5V Power Supply for VCO |
| 40 | VCCVCO1 | |
| 6 | VTUNE | Control Voltage Input. Modulation port bandwidth dependent on drive source impedance. |
| 14 | ACG | AC Ground. This pin must be connected to an external capacitor to ground. |
| 15 | AVCC | Analog Power supply pin for the RF Section. A decoupling capacitor to the ground plane should be placed as close as possible to this pin. Nominally 3.3V |
| 16 | VDDCP | +5V Power Supply for charge pump digital section |
| 17 | VCCCP | +5V Power Supply for the charge pump analog section |
| 18 | CP | Charge pump output |
| 19 | VDDPFD | Analog Power supply for the phase frequency detector, Nominally 3.3V |
| 20 | BIAS [3] | External bypass decoupling for precision bias circuits, 1.920V ±20 mV is generated internally |
| 21 | AVDD | Analog Power supply for analog ref paths, Nominally 3.3V |
| 23 | REFN | Reference input (Negative or AC coupled to GND) |
| 24 | REFP | Reference input (Positive) |
| 25 | RVDD | Ref path supply |
| 26 | DVDDQ | Digital supply for Substrate, Nominally 3.3V |
| 27 | CE | Chip Enable |
| 28 | SEN | Serial port latch enable input |
| 29 | SCK | Serial port clock input |
| 30 | SDI | Serial port data input |
| 31 | DVDD | Power supply pin for internal digital circuitry. Nominally 3.3V |
| 32 | VDDIO | Power Supply for digital I/O driver |
| 33 | LD_SDO | Lock Detect, Main Serial Data Output or VCO Serial Port Data Out |
| 34 | VCCPS | Analog Power Supply for Prescaler, Nominally 3.3V |
| 35 | DVDDM | Digital Power Supply for M-Counter, Nominally 3.3V |
| 38 | RFOUT | RF output (AC coupled). |

[1] This pin is not connected internally, however, this pin must be connected to GND to maintain product family pin for pin compatibility.

[2] This pin is not connected internally, however, this pin must be connected to Vcc to maintain product family pin for pin compatibility.

[3] BIAS ref voltage (pin 20) cannot drive an external load, and must be measured with a 10 GOhm meter such as Agilent 34410A; a typical 10 Mohm DVM will read erroneously.

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Pin Schematic Equivalents

| Pins | Equivalent Schematic |
|-------------------|----------------------|
| RFOUT | |
| VCCVCO1 | |
| VTUNE | |
| GND | |
| SEN, CE, SCK, SDI | |
| LD_SDO | |
| CP | |

7

PLLS w/ INTEGRATED VCO - SMT



**FRACTIONAL-N PLL WITH
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Pin Schematic Equivalents (Continued)

| Pins | Equivalent Schematic |
|------------|----------------------|
| Bias | |
| REFN, REFP | |

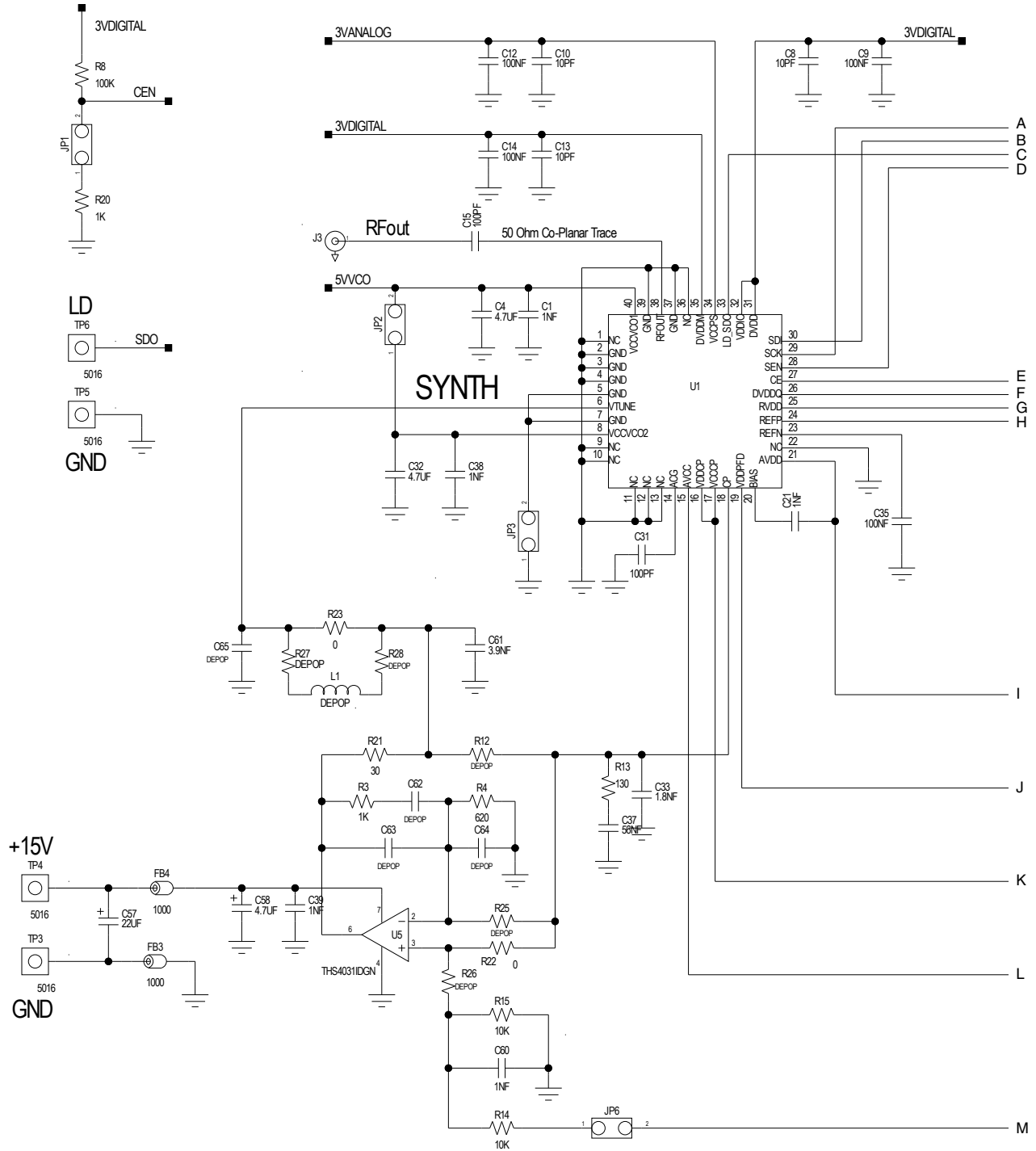
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**FRACTIONAL-N PLL WITH
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Evaluation Circuit



7

PLLS w/ INTEGRATED VCO - SMT

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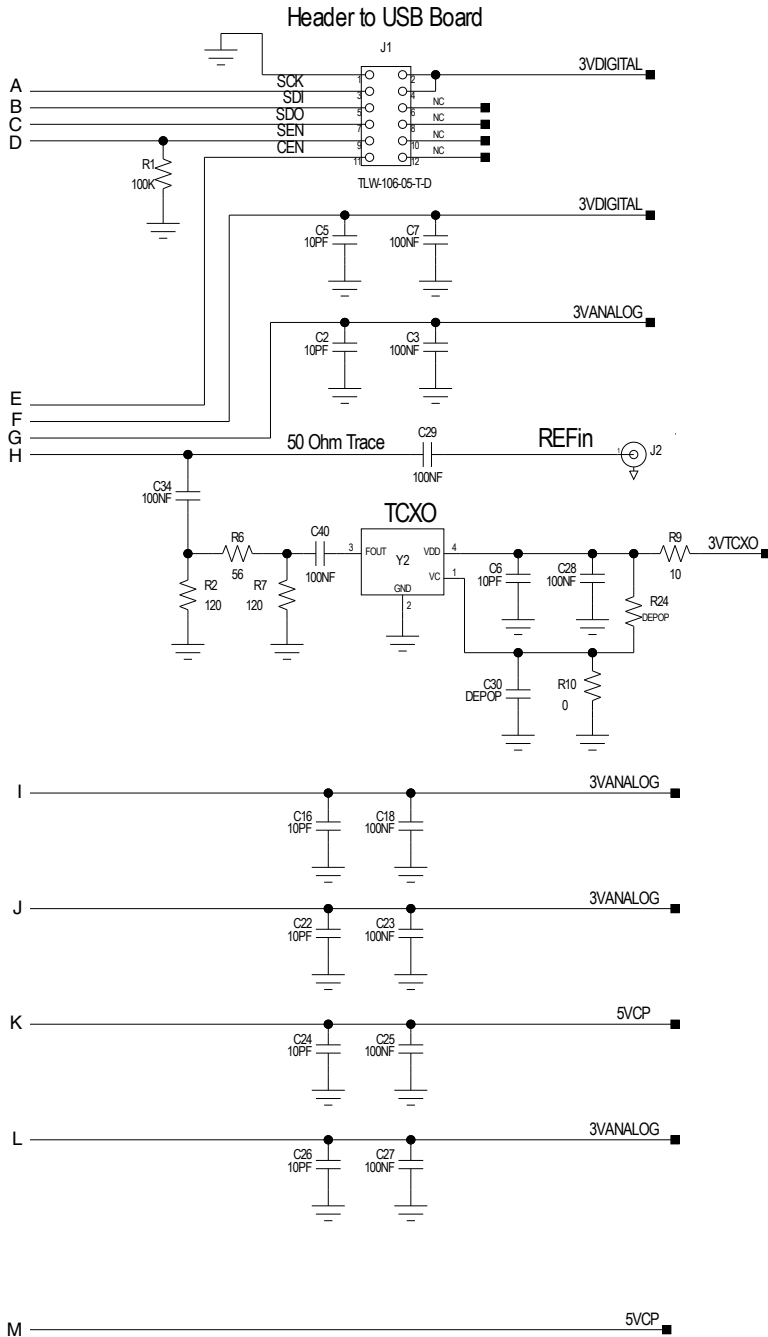


FRACTIONAL-N PLL WITH INTEGRATED VCO, 7.8 - 8.8 GHz

Evaluation Circuit (Continued from page 9)

7

PLLS w/ INTEGRATED VCO - SMT



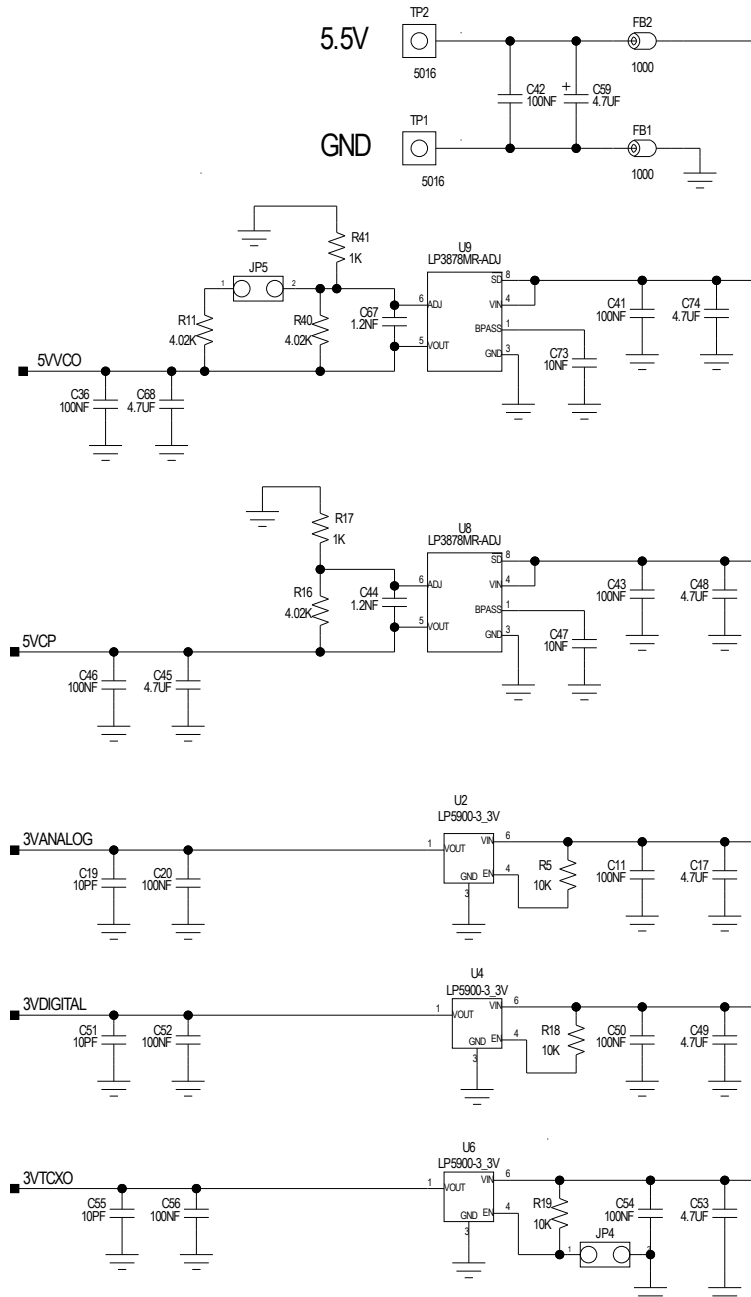
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FRACTIONAL-N PLL WITH INTEGRATED VCO, 7.8 - 8.8 GHz

Evaluation Circuit (Continued from page 10)



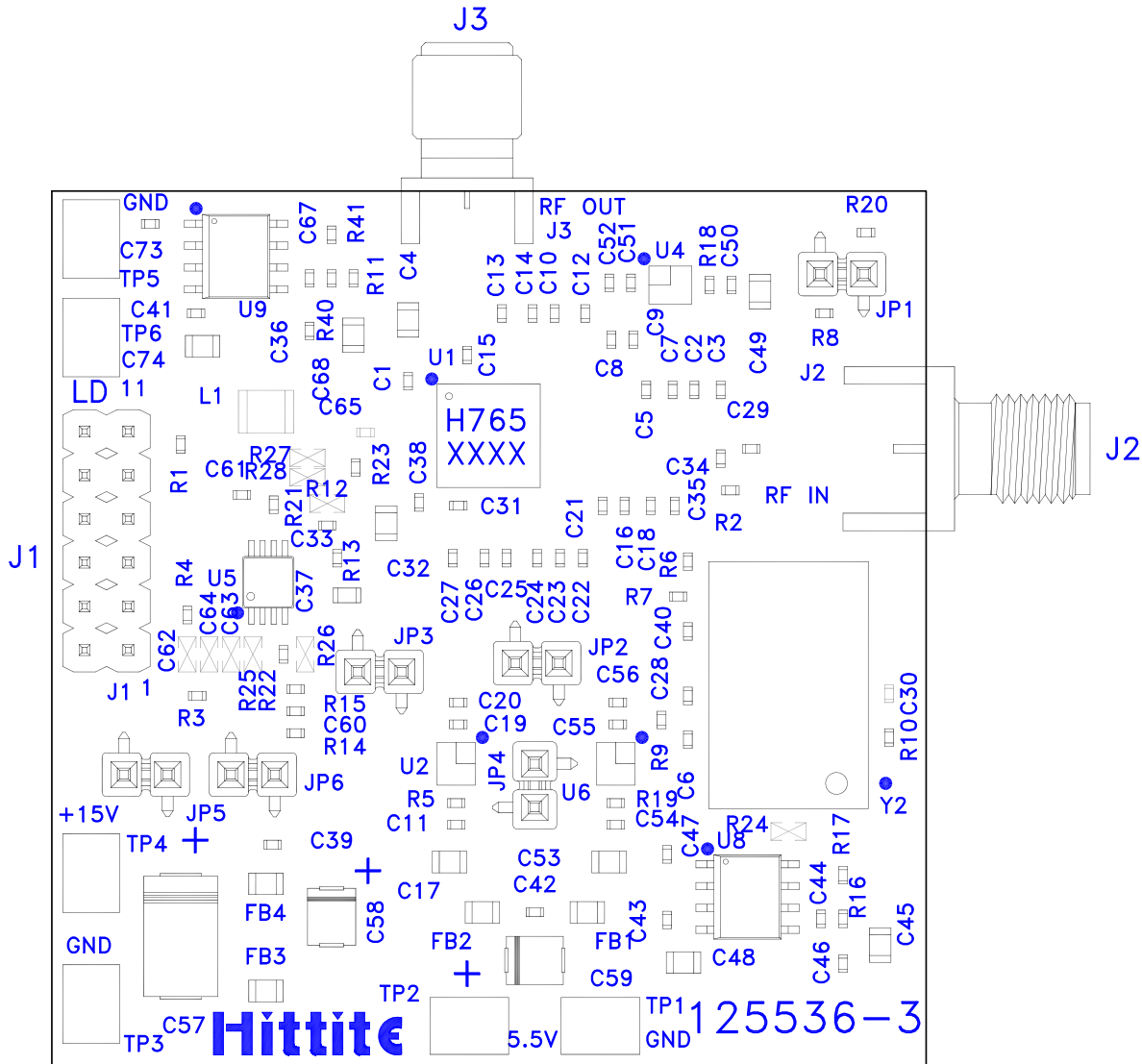
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PLLS w/ INTEGRATED VCO - SMT



FRACTIONAL-N PLL WITH INTEGRATED VCO, 7.8 - 8.8 GHz

Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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**FRACTIONAL-N PLL WITH
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List of Materials for Evaluation PCB 127270 [1]

| Item | Description |
|---|---|
| J1 | Dual Row Terminal Strip |
| J2, J3 | PCB Mount SMA RF Connector |
| JP1 - JP6 | Single Row Terminal Strip |
| C1, C21, C38 - C39, C60 | 1000 pF Capacitor, 0402 Pkg. |
| C2, C5, C6, C8, C10, C13, C16, C19, C22, C24, C26, C51, C55 | 10 pF Capacitor, 0402 Pkg. |
| C3, C7, C9, C11, C12, C14, C18, C20, C23, C25, C27 - C29, C34 - C36, C40 - C43, C46, C50, C52, C54, C56 | 0.1 μ F Capacitor, 0402 Pkg. |
| C4, C17, C32, C45, C48, C49, C53, C68, C74 | 4.7 μ F Capacitor, 0805 Pkg. |
| C15, C31 | 100 pF Capacitor, 0402 Pkg. |
| C33 | 1800 pF Capacitor, 0402 Pkg. |
| C37 | 0.056 μ F Capacitor, 0603 Pkg. |
| C44, C67 | 1200 pF Capacitor, 0402 Pkg. |
| C47, C73 | 10,000 pF Capacitor, 0402 Pkg. |
| C57 | 22 μ F Tantalum Capacitor, Case D |
| C58, C59 | 4.7 μ F Tantalum Capacitor, Case B |
| C61 | 3900 pF Capacitor, 0402 Pkg. |
| FB1 - FB4 | 1000 Ohm 200 mA Ferrite Chip, 0805 Pkg. |
| R1, R8 | 100k Ohm Resistor, 0402 Pkg. |
| R2, R7 | 120 Ohm Resistor, 0402 Pkg. |
| R3, R17, R20, R41 | 1k Ohm Resistor, 0402 Pkg. |
| R4 | 620 Ohm Resistor, 0402 Pkg. |
| R5, R14, R15, R18, R19 | 10k Ohm Resistor, 0402 Pkg. |
| R6 | 56 Ohm Resistor, 0402 Pkg. |
| R9 | 10 Ohm Resistor, 0402 Pkg. |
| R10, R22, R23 | Zero Ohm Resistor, 0402 Pkg. |
| R11, R16, R40 | 4.02k Ohm Resistor, 0402 Pkg. |
| R13 | 130 Ohm Resistor, 0402 Pkg. |
| R21 | 30 Ohm Resistor, 0402 Pkg. |
| TP1 - TP6 | Test Point PC Compact SMT |
| U1 | HMC765LP6CE Fractional-N PLL, with Integrated VCO |
| U2, U4, U6 | Low Noise 3.3V, 100 mA Linear Regulator |
| U5 | Low Noise Op-Amp, THS4031IDGN |
| U8, U9 | 5V, 800mA Voltage Regulator |
| Y2 | 3.3V, 50 MHz VCXO Crystal Oscillator |
| PCB [2] | 125536 Evaluation Board |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR and FR4

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JONHON

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