Dual-Channel Isolators with *iso*Power Integrated DC-to-DC Converter, 50 mW

Data Sheet

ADuM5240/ADuM5241/ADuM5242

FEATURES

- Integrated isolated dc-to-dc converter
- Regulated 5 V/10 mA output
- Dual dc to 1 Mbps (NRZ) signal isolation channels
- Narrow-body, 8-lead SOIC package
- RoHS compliant
- High temperature operation: 105°C
- Precise timing characteristics
  - 3 ns maximum pulse width distortion
  - 3 ns maximum channel-to-channel matching
  - 70 ns maximum propagation delay
- High common-mode transient immunity: >25 kV/µs
- Safety and regulatory approvals
  - UL recognition
    - 2500 V rms for 1 minute, per UL 1577
  - CSA Component Acceptance Notice #5A
  - VDE certificate of conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 560 V peak

GENERAL DESCRIPTION

The ADuM524x[1] are dual-channel digital isolators with *iso*Power® integrated, isolated power. Based on the Analog Devices, Inc., *i*Coupler® technology, a chip scale dc-to-dc converter provides up to 50 mW of regulated, isolated power at 5 V, which eliminates the need for a separate isolated dc-to-dc converter in low power isolated designs. The Analog Devices chip scale transformer *i*Coupler technology is used both for the isolation of the logic signals as well as for the dc-to-dc converter. The result is a small form factor, total isolation solution.

The ADuM524x isolators provide two independent isolation channels in a variety of channel configurations, operating from a 5 V input supply. ADuM524x units can be used in combination with other *i*Coupler products to achieve greater channel counts.

FUNCTIONAL BLOCK DIAGRAMS

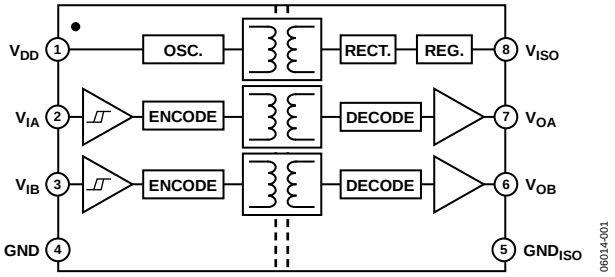

Figure 1. ADuM5240

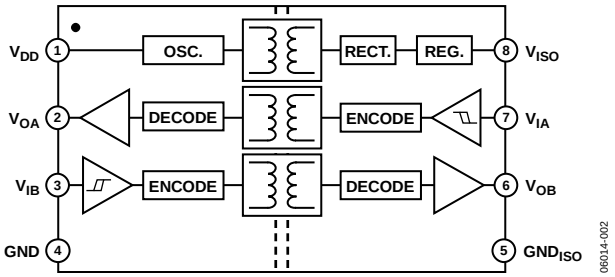

Figure 2. ADuM5241

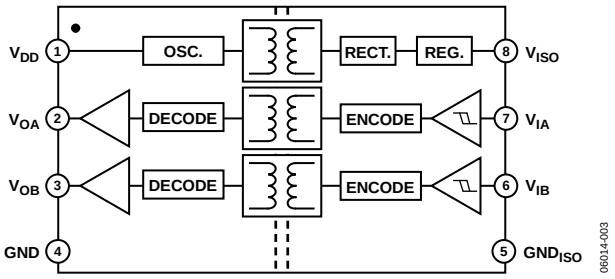

Figure 3. ADuM5242

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329.

Rev. B

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TABLE OF CONTENTS

Features ... 1
General Description ... 1
Functional Block Diagrams ... 1
Revision History ... 2
Specifications ... 3
Electrical Characteristics ... 3
Package Characteristics ... 5
Regulatory Information ... 5
Insulation and Safety-Related Specifications ... 5
DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics ... 6
Recommended Operating Conditions ... 6
Absolute Maximum Ratings ... 7
ESD Caution ... 7
Pin Configurations and Function Descriptions ... 8
Typical Performance Characteristics ... 10
Applications Information ... 11
DC-to-DC Converter ... 11
Propagation Delay-Related Parameters ... 11
DC Correctness and Magnetic Field Immunity ... 11
Thermal Analysis ... 12
PCB Layout ... 12
Increasing Available Power ... 13
Insulation Lifetime ... 13
Outline Dimensions ... 14
Ordering Guide ... 14

REVISION HISTORY

5/12—Rev. A to Rev. B

Created Hyperlink for Safety and Regulatory Approvals Entry in Features Section ... 1
Change to PCB Layout Section ... 12

7/07—Rev. 0 to Rev. A

Updated VDE Certification Throughout ... 1
Changes to Features ... 1
Changes to Regulatory Information Section and Table 4 ... 5
Changes to Table 5 and Figure 4 Caption ... 6
Changes to Table 7 ... 7
Added Table 8; Renumbered Sequentially ... 7
Added Insulation Lifetime Section ... 13

3/07—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

All voltages are relative to their respective ground. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD} = 5.0 V, V_{ISO} = 5.0 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC-TO-DC CONVERTER						
DC-to-DC Converter Enabled						
DC to 1 Mbps Data Rate						Logic signal frequency ≤ 1 MHz
Setpoint	$V_{ISO (SET)}$	4.5	5.2	5.5	V	I_{ISO} = 0 mA
Maximum V_{ISO} Output Current	$I_{ISO (max)}$	10			mA	V_{ISO} = 4.5 V
Noise[1]			250		mV p-p	
Input Supply Current						
At Maximum I_{ISO} Current	$I_{DD (max)}$			140	mA	I_{ISO} = 10 mA
No Load I_{ISO} Current	$I_{DD (Q)}$			104	mA	I_{ISO} = 0 mA
DC-to-DC Converter Disabled						
Primary Side Supply Input Current[2]						
ADuM5240	$I_{DD (DISABLE)}$			3.3	mA	V_{DD} = 4.0 V
ADuM5241	$I_{DD (DISABLE)}$			2.7	mA	V_{DD} = 4.0 V
ADuM5242	$I_{DD (DISABLE)}$			2.2	mA	V_{DD} = 4.0 V
Secondary Side Supply Input Current[3]						
ADuM5240	$I_{ISO (DISABLE)}$			2.6	mA	
ADuM5241	$I_{ISO (DISABLE)}$			2.8	mA	
ADuM5242	$I_{ISO (DISABLE)}$			3.0	mA	
DC-to-DC Converter Enable Threshold[4]	$V_{DD (ENABLE)}$	4.2		4.5	V	
DC-to-DC Converter Disable Threshold[4]	$V_{DD (DISABLE)}$	3.7			V	
LOGIC SPECIFICATIONS						
Logic Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	
Logic High Input Threshold	V_{IH}	0.7 (V_{DD} or V_{ISO})			V	
Logic Low Input Threshold	V_{IL}			0.3 (V_{DD} or V_{ISO})	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD} or V_{ISO}) − 0.1	(V_{DD} or V_{ISO})		V	I_{Ox} = −20 µA, V_{Ix} ≥ V_{IH}
		(V_{DD} or V_{ISO}) − 0.5	(V_{DD} or V_{ISO}) − 0.2		V	I_{Ox} = −4 mA, V_{Ix} ≥ V_{IH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} ≤ V_{IL}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} ≤ V_{IL}

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
AC SPECIFICATIONS						
Minimum Pulse Width[5]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[6]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[7]	t_{PHL}, t_{PLH}	25		70	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[8]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[8]	t_{PSK}			45	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[9]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[9]	t_{PSKCD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD}$, V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Frequency	f_r		1.0		MHz	
Switching Frequency	f_{OSC}		300		MHz	

[1] Peak noise occurs at frequency corresponding to the refresh frequency (see the PCB Layout section).
[2] $I_{DD (DISABLE)}$ supply current values are specified with no load present on the digital outputs.
[3] $I_{ISO (DISABLE)}$ supply current values are specified with no load present on the digital outputs and power sourced by an external supply.
[4] Enable/disable threshold is the V_{DD} voltage at which the internal dc-to-dc converter is enabled/disabled.
[5] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[6] The maximum data rate is the fastest data rate at which the specified pulse width distortion and V_{ISO} supply voltage is guaranteed.
[7] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[8] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[9] Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels when operated with identical loads.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)	C_{I-O}		1.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Air Thermal Resistance	θ_{JA}		80		°C/W	

REGULATORY INFORMATION

The ADuM524x are approved by the organizations listed in Table 3. Refer to Table 8 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 3.

UL	CSA	VDE
Recognized under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single/basic insulation, 2500 V rms isolation rating	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM524x is proof-tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 μA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM524x is proof-tested by applying an insulation test voltage ≥ 1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.90 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.01 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)
Maximum Working Voltage Compatible with 50-Year Service Life	V_{IORM}	425	V peak	Continuous peak voltage across the isolation barrier

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits.

Table 5.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	
Maximum Working Insulation Voltage		V_{IORM}	424	V peak
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	795	V peak
Input-to-Output Test Voltage, Method a		V_{PR}		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		680	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		510	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 seconds	V_{TR}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure; see Figure 4			
Case Temperature		T_S	150	°C
Supply Current		I_{S1}	312	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

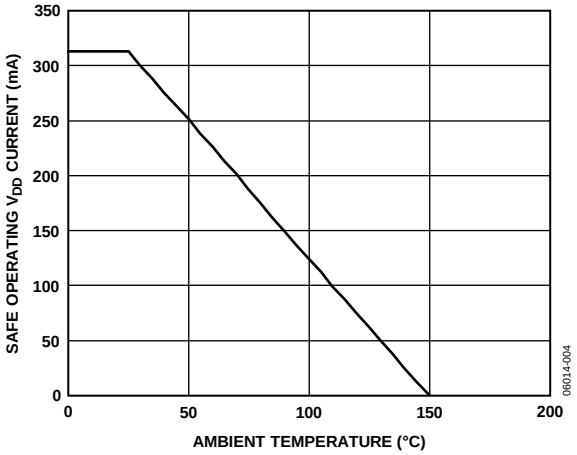

Figure 4. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 6.

Parameter	Value
Operating Temperature Range (T_A)	−40°C to +105°C
Supply Voltages[1]	
V_{DD}, DC-to-DC Converter Enabled	4.5 V to 5.5 V
V_{DD}, DC-to-DC Converter Disabled (V_{DD})	2.7 V to 4.0 V
V_{ISO}, DC-to-DC Converter Disabled (V_{ISO})	2.7 V to 5.5 V
Input Signal Rise/Fall Time	1.0 ms
Input Supply Slew Rate	10 V/ms

[1] All voltages are relative to their respective ground.

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Storage Temperature Range (T_{ST})	−55°C to +150°C
Ambient Operating Temperature Range (T_A)	−40°C to +105°C
Supply Voltages (V_{DD}, V_{ISO})[1]	−0.5 V to +7.0 V
Input Voltage (V_{IA}, V_{IB})[1]	−0.5 V to (V_{DD} or V_{ISO}) + 0.5 V
Output Voltage (V_{OA}, V_{OB})[1]	−0.5 V to (V_{DD} or V_{ISO}) + 0.5 V
Average Output Current per Pin (I_O)[2]	−18 mA to +18 mA
Common-Mode Transients (|CM|)[3]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] See Figure 4 for maximum rated current values for various temperatures.
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 8. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	425	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Basic Insulation	566	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per VDE V 0884-10
DC Voltage			
Basic Insulation	566	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per VDE V 0884-10

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

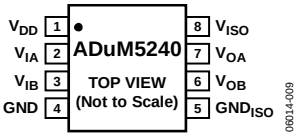

Figure 5. ADuM5240 Pin Configuration

Table 9. ADuM5240 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Supply Voltage for Isolator Primary Side, 4.5 V to 5.5 V (DC-to-DC Enabled) and 2.7 V to 4.0 V (DC-to-DC Disabled).
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND	Ground. Ground reference for isolator primary side.
5	GND_{ISO}	Isolated Ground. Ground reference for isolator secondary side.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{ISO}	Isolated Supply Voltage for Isolator Secondary Side, 4.5 V to 5.5 V Output (DC-to-DC Enabled), and 2.7 V to 5.5 V Input (DC-to-DC Disabled).

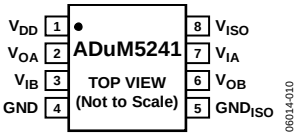

Figure 6. ADuM5241 Pin Configuration

Table 10. ADuM5241 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Supply Voltage for Isolator Primary Side, 4.5 V to 5.5 V (DC-to-DC Enabled) and 2.7 V to 4.0 V (DC-to-DC Disabled).
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND	Ground. Ground reference for isolator primary side.
5	GND_{ISO}	Isolated Ground. Ground reference for isolator secondary side.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{ISO}	Isolated Supply Voltage for Isolator Secondary Side, 4.5 V to 5.5 V Output (DC-to-DC Enabled), and 2.7 V to 5.5 V Input (DC-to-DC Disabled).

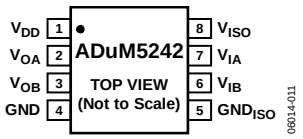

Figure 7. ADuM5242 Pin Configuration

Table 11. ADuM5242 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Supply Voltage for Isolator Primary Side, 4.5 V to 5.5 V (DC-to-DC Enabled) and 2.7 V to 4.0 V (DC-to-DC Disabled).
2	V_{OA}	Logic Output A.
3	V_{OB}	Logic Output B.
4	GND	Ground. Ground reference for isolator primary side.
5	GND_{ISO}	Isolated Ground. Ground reference for isolator secondary side.
6	V_{IB}	Logic Input B.
7	V_{IA}	Logic Input A.
8	V_{ISO}	Isolated Supply Voltage for Isolator Secondary Side, 4.5 V to 5.5 V Output (DC-to-DC Enabled), and 2.7 V to 5.5 V Input (DC-to-DC Disabled).

Table 12. ADuM5240 Truth Table

V_{DD} State	DC-to-DC Converter	V_{ISO} State	V_{IA} Input	V_{IB} Input	V_{OA} Output	V_{OB} Output
Powered	Enabled	Powered (Internally)	H	H	H	H
Powered	Enabled	Powered (Internally)	L	L	L	L
Powered	Enabled	Powered (Internally)	H	L	H	L
Powered	Enabled	Powered (Internally)	L	H	L	H
Powered	Disabled	Powered (Externally)	H	H	H	H
Powered	Disabled	Powered (Externally)	L	L	L	L
Powered	Disabled	Powered (Externally)	H	L	H	L
Powered	Disabled	Powered (Externally)	L	H	L	H
Powered	Disabled	Unpowered	X	X	Z	Z
Unpowered	Disabled	Powered (Externally)	X	X	L	L
Unpowered	Disabled	Unpowered	X	X	Z	Z

Table 13. ADuM5241 Truth Table

V_{DD} State	DC-to-DC Converter	V_{ISO} State	V_{IA} Input	V_{IB} Input	V_{OA} Output	V_{OB} Output
Powered	Enabled	Powered (Internally)	H	H	H	H
Powered	Enabled	Powered (Internally)	L	L	L	L
Powered	Enabled	Powered (Internally)	H	L	H	L
Powered	Enabled	Powered (Internally)	L	H	L	H
Powered	Disabled	Powered (Externally)	H	H	H	H
Powered	Disabled	Powered (Externally)	L	L	L	L
Powered	Disabled	Powered (Externally)	H	L	H	L
Powered	Disabled	Powered (Externally)	L	H	L	H
Powered	Disabled	Unpowered	X	X	L	Z
Unpowered	Disabled	Powered (Externally)	X	X	Z	L
Unpowered	Disabled	Unpowered	X	X	Z	Z

Table 14. ADuM5242 Truth Table

V_{DD} State	DC-to-DC Converter	V_{ISO} State	V_{IA} Input	V_{IB} Input	V_{OA} Output	V_{OB} Output
Powered	Enabled	Powered (Internally)	H	H	H	H
Powered	Enabled	Powered (Internally)	L	L	L	L
Powered	Enabled	Powered (Internally)	H	L	H	L
Powered	Enabled	Powered (Internally)	L	H	L	H
Powered	Disabled	Powered (Externally)	H	H	H	H
Powered	Disabled	Powered (Externally)	L	L	L	L
Powered	Disabled	Powered (Externally)	H	L	H	L
Powered	Disabled	Powered (Externally)	L	H	L	H
Powered	Disabled	Unpowered	X	X	L	L
Unpowered	Disabled	Powered (Externally)	X	X	Z	Z
Unpowered	Disabled	Unpowered	X	X	Z	Z

TYPICAL PERFORMANCE CHARACTERISTICS

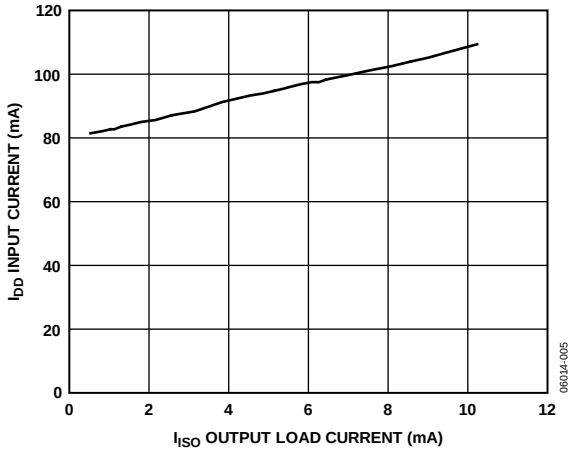

Figure 8. Typical I_{DD} Input Current vs. I_{ISO} Output Load Current

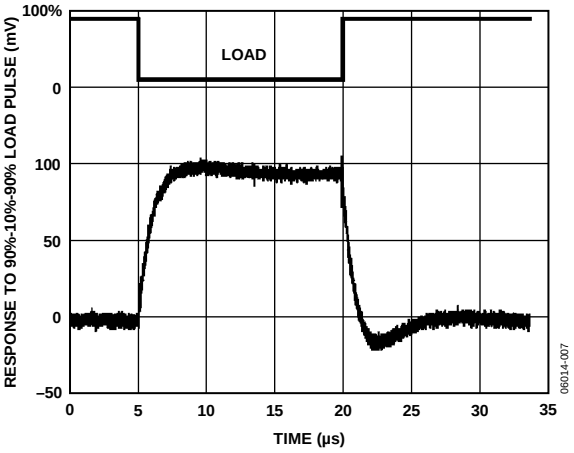

Figure 10. Typical V_{ISO} Transient Load Response, 5 V Output, 90% to 10% to 90% Pulsed Load, 100 nF Bypass Capacitance vs. Time

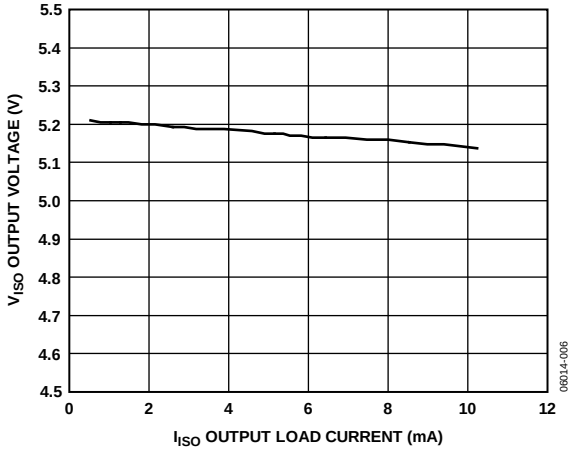

Figure 9. Typical Isolated V_{ISO} Output Voltage vs. I_{ISO} Output Load Current

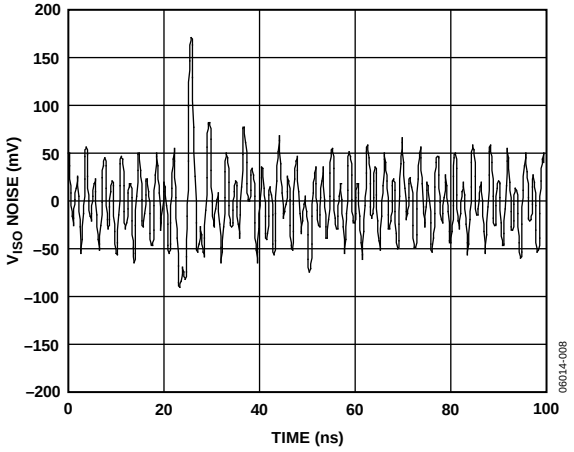

Figure 11. Typical Output Voltage Noise at 100% Load, 100 nF Bypass Capacitance vs. Time

APPLICATIONS INFORMATION

DC-TO-DC CONVERTER

The dc-to-dc converter section of the ADuM524x works on principles that are common to most modern power supply designs. V_{DD} power is supplied to an oscillating circuit that switches current into a chip scale air core transformer. Power is transferred to the secondary side where it is rectified to a high dc voltage. The power is then linearly regulated down to about 5.2 V and supplied to the secondary side data section and to the V_{ISO} pin for external use. This design allows for a physically small power section compatible with the 8-lead SOIC packaging of this device. Active feedback was not implemented in this version of *iso*Power for reasons of size and cost.

Because the oscillator runs at a constant high frequency independent of the load, excess power is internally dissipated in the output voltage regulation process. Limited space for transformer coils and components also adds to internal power dissipation. This results in low power conversion efficiency, especially at low load currents.

The load characteristic curve in Figure 8 shows that the V_{DD} current is typically 80 mA with no V_{ISO} load and 110 mA at full V_{ISO} load at the V_{DD} supply pin.

Alternate supply architectures are possible using this technology. Addition of a digital feedback path allows regulation of power on the primary side. Feedback would allow significantly higher power, efficiency, and synchronization of multiple supplies at the expense of size and cost. Future implementations of *iso*Power includes feedback to achieve these performance improvements.

The ADuM524x can be operated with the internal dc-to-dc enabled or disabled. With the internal dc-to-dc converter enabled, the isolated supply of Pin 8 provides the output power as well as power to the secondary-side circuitry of the part.

The internal dc-to-dc converter state of the ADuM524x is controlled by the input V_{DD} voltage, as defined in Table 6. In normal operating mode, V_{DD} is set between 4.5 V and 5.5 V and the internal dc-to-dc converter is enabled. When/if it is desired to disable the dc-to-dc converter, V_{DD} is lowered to a value between 2.7 V and 4.0 V. In this mode, V_{ISO} power is supplied externally by the user and the signal channels of the ADuM524x continue to operate normally.

There is hysteresis into the V_{DD} input voltage detect circuit. Once the dc-to-dc converter is active, the input voltage must be decreased below the turn-on threshold to disable the converter. This feature ensures that the converter does not go into oscillation due to noisy input power.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high.

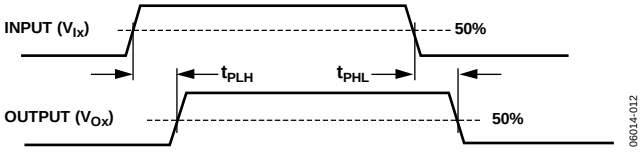

Figure 12. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM524x component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM524x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state by the watchdog timer circuit (see Table 12 through Table 14).

The limitation on the magnetic field immunity of the ADuM524x is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM524x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the n^{th} turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM524x and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 13.

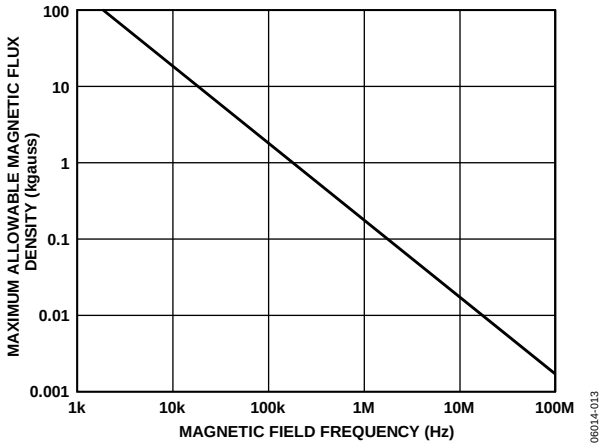

Figure 13. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM524x transformers. Figure 14 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 14, the ADuM524x is extremely immune and can only be affected by extremely large currents operated at high frequencies very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM524x to affect the operation of the component.

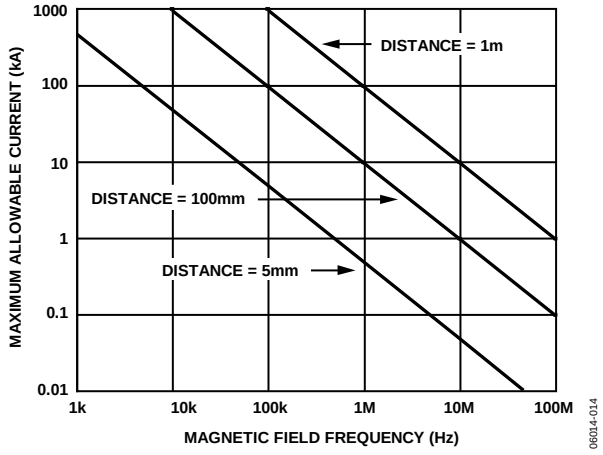

Figure 14. Maximum Allowable Current for Various Current-to-ADuM524x Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board (PCB) traces could induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

THERMAL ANALYSIS

Each ADuM524x component consists of two internal die, attached to a split-paddle lead frame. For the purposes of thermal analysis, it is treated as a thermal unit with the highest junction temperature reflected in the θ_{JA} value in Table 2. The value of θ_{JA} is based on measurements taken with the part mounted on a JEDEC standard 4-layer PCB with fine-width traces in still air. Under normal operating conditions, the ADuM524x operates at full load across the full temperature range without derating the output current. For example, a part with no external load drawing 80 mA and dissipating 400 mW causes a 32°C temperature rise above ambient. It is normal for these devices to run warm.

Following the recommendations in the PCB Layout section decreases the thermal resistance to the PCB allowing increased thermal margin at high ambient temperatures.

PCB LAYOUT

The ADuM524x requires no external circuitry for its logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 15).

The power supply section of the ADuM524x uses a 300 MHz oscillator frequency to pass power through its chip scale transformers. In addition, the normal operation of the data section of the *i*Coupler introduces switching transients, as described in the DC Correctness and Magnetic Field Immunity section, on the power supply pins (see Figure 11). Low inductance capacitors are required to bypass noise generated at the switching frequency as well as 1 ns pulses generated by the data transfer and dc refresh circuitry. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

In cases where EMI emission is a concern, series inductance may be added to critical power and ground traces. Discrete inductors should be added to the line such that the high frequency bypass capacitors are between the inductor and the ADuM524x device pin. Inductance can be added in the form of discrete inductors or ferrite beads added to both power and ground traces. The recommended value corresponds to impedance between 50 Ω and 100 Ω at approximately 300 MHz.

If the switching speed of the data outputs is causing unacceptable EMI, capacitance to ground can be added at output pins to slow the rise and fall time of the output. This slew rate limits the output. Capacitance values depend on application speed requirements.

See the AN-0971 Application Note for board layout guidelines.

Load regulation transients are the primary source of lower frequency power supply voltage excursions, as illustrated in Figure 10. These should be dealt with by adding an additional supply stiffening capacitor between V_{ISO} and GND_{ISO}. The stiffening capacitor can be of a more highly inductive type because the high frequency bypass is handled by the required low inductance capacitor.

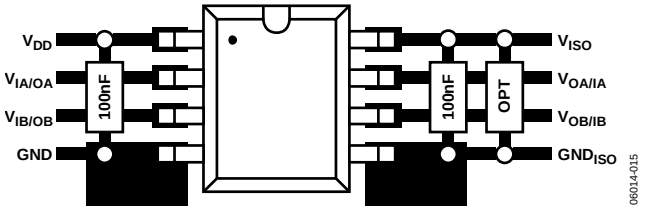

Figure 15. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings of the device (specified in Table 7), thereby leading to latch-up and/or permanent damage.

The ADuM524x is a power device that dissipates as much as 600 mW of power when fully loaded. Because it is not possible to apply a heat sink to an isolation device, the device primarily depends on heat dissipation into the PCB through the GND pins. If the device is used at high ambient temperatures, care should be taken to provide a thermal path from the GND pins to the PCB ground plane. The board layout in Figure 15 shows enlarged pads for Pin 4 and Pin 5. Multiple vias should be implemented from each of the pads to the ground plane, which significantly reduce the temperatures inside the chip. The dimensions of the expanded pads are left to the discretion of the designer and the available board space.

INCREASING AVAILABLE POWER

The ADuM524x devices are not designed with the capability of running several devices in parallel. However, if more power is required to run multiple loads, it is possible to group loads and run each group from an individual ADuM542x device. For example, if a transceiver and external logic must be powered, one ADuM524x could be dedicated to the transceiver and an additional ADuM524x could power the external logic, which prevents issues with load sharing because each load is dedicated to its own supply.

INSULATION LIFETIME

All insulation structures eventually breaks down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM524x. Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 8 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM524x depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 16, Figure 17, and Figure 18 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the recommended maximum working voltage of Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower, which allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 8 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 17 or Figure 18 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 8.

Note that the voltage presented in Figure 17 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

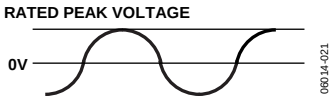

Figure 16. Bipolar AC Waveform

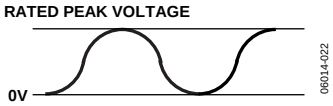

Figure 17. Unipolar AC Waveform

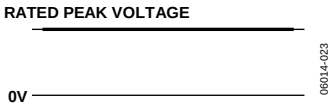

Figure 18. DC Waveform

OUTLINE DIMENSIONS

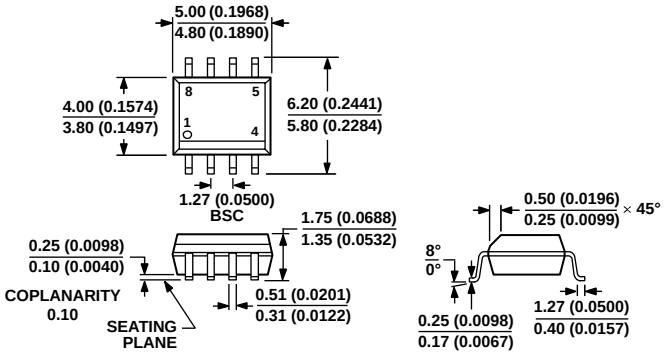

Figure 19. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Number of Inputs, V_{DD} Side	Number of Inputs, V_{ISO} Side	Maximum Data Rate (Mbps)	Temperature Range	Package Description	Package Option
ADuM5240ARZ	2	0	1	−40°C to +105°C	8-Lead SOIC_N	R-8
ADuM5240ARZ-RL7	2	0	1	−40°C to +105°C	8-Lead SOIC_N, 7″Tape and Reel	R-8
ADuM5241ARZ	1	1	1	−40°C to +105°C	8-Lead SOIC_N	R-8
ADuM5241ARZ-RL7	1	1	1	−40°C to +105°C	8-Lead SOIC_N, 7″Tape and Reel	R-8
ADuM5242ARZ	0	2	1	−40°C to +105°C	8-Lead SOIC_N	R-8
ADuM5242ARZ-RL7	0	2	1	−40°C to +105°C	8-Lead SOIC_N, 7″Tape and Reel	R-8

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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D06014-0-5/12(B)

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