

40V DUAL P-CHANNEL ENHANCEMENT MODE MOSFET

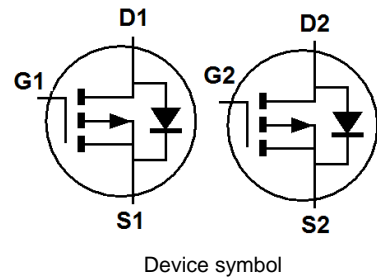
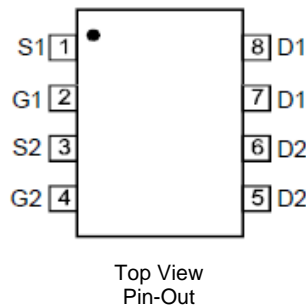
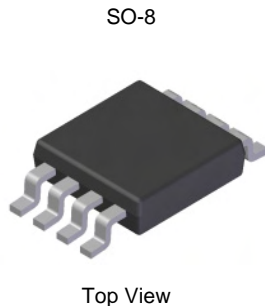
Product Summary

$V_{(BR)DSS}$	$R_{DS(on) \max}$	$I_D \max (A)$ $T_A = 25^\circ C$ (Notes 6 & 8)
-40V	25mΩ @ $V_{GS} = -10V$	-7.6
	45mΩ @ $V_{GS} = -4.5V$	-6.0

Description and Applications

This MOSFET has been designed to minimize the on-state resistance and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Motor control
- Backlighting
- DC-DC Converters
- Printer equipment



Features and Benefits

- Low $R_{DS(on)}$ – Minimizes conduction losses
- Fast switching speed – Minimizes switching losses
- **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

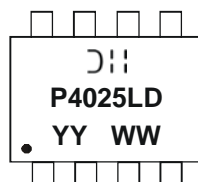
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0 (Note 1)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.074 grams (approximate)


Ordering Information (Note 4)

Product	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMP4025LSD-13	P4025LD	13	12	2,500

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen and Antimony free, "Green" and Lead-Free.
 3. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com>

Marking Information



 = Manufacturer's Marking
 P4025LD = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Year (ex: 10 = 2010)
 WW = Week (01 - 53)

Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

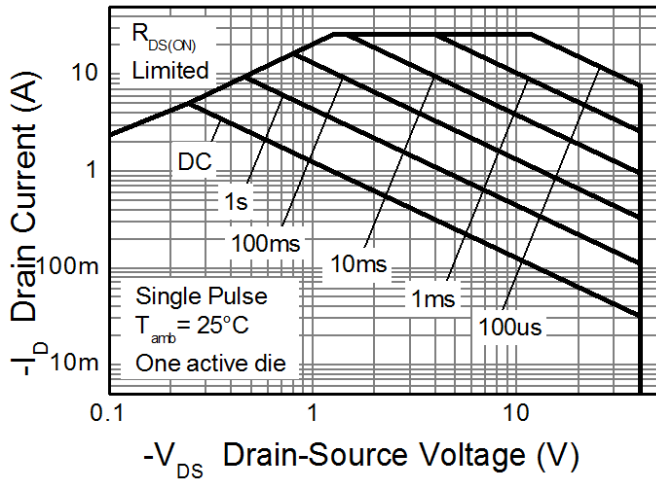
Characteristic		Symbol	Value	Units	
Drain-Source Voltage		V_{DSS}	-40	V	
Gate-Source Voltage		V_{GSS}	± 20		
Continuous Drain Current	$V_{GS} = -10\text{V}$	(Notes 6 & 8)	-7.6	A	
		$T_A = 70^\circ\text{C}$ (Notes 6 & 8)	-6.1		
		(Notes 5 & 8)	-5.8		
		(Notes 5 & 9)	-6.9		
Pulsed Drain Current	$V_{GS} = -10\text{V}$	(Notes 7 & 8)	I_{DM}		-28.0
Continuous Source Current (Body diode)		(Notes 6 & 8)	I_S		-3.0
Pulsed Source Current (Body diode)		(Notes 7 & 8)	I_{SM}	-28.0	

Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

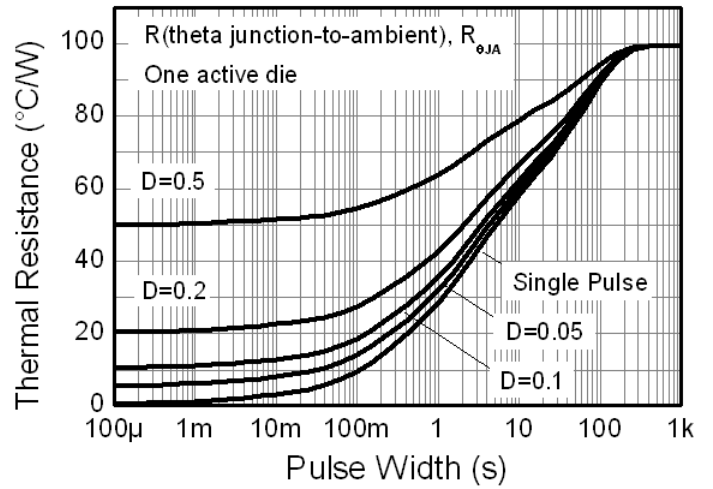
Characteristic		Symbol	Value	Unit
Power Dissipation Linear Derating Factor	(Notes 5 & 8)	P_D	1.25	W mW/ $^\circ\text{C}$
			10	
	(Notes 5 & 9)		1.8	
	(Notes 6 & 8)		14.3	
Thermal Resistance, Junction to Ambient	(Notes 5 & 8)	$R_{\theta JA}$	2.14	$^\circ\text{C/W}$
	(Notes 5 & 9)		17.2	
	(Notes 6 & 8)		100	
Thermal Resistance, Junction to Lead	(Notes 5 & 9)	$R_{\theta JL}$	70	
	(Notes 6 & 8)		58	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	

- Notes:
5. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 6. Same as note (2), except the device is measured at $t \leq 10$ sec.
 7. Same as note (2), except the device is pulsed with $D = 0.02$ and pulse width 300 μs .
 8. For a dual device with one active die.
 9. For a device with two active die running at equal power.
 10. Thermal resistance from junction to solder-point (at the end of the drain lead).

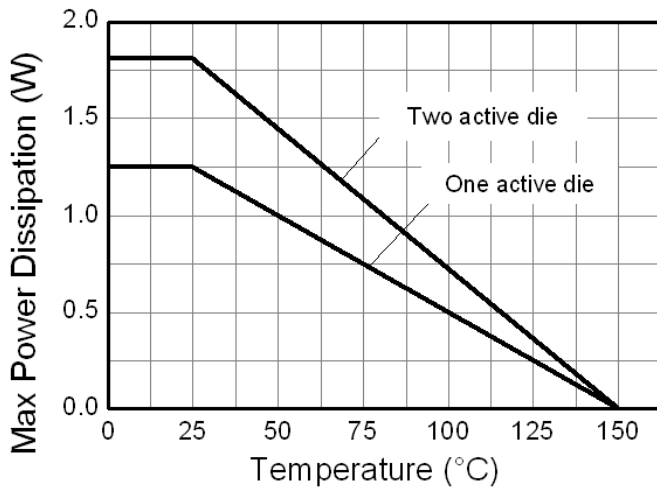
Thermal Characteristics



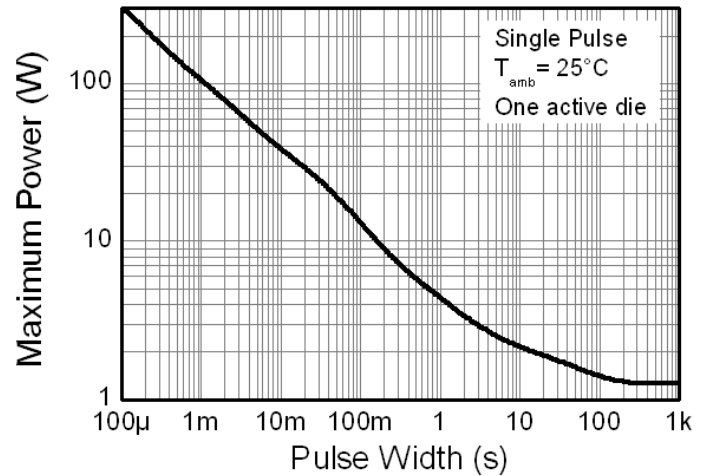
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	$I_D = -250\mu\text{A}$, $V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1.0	μA	$V_{DS} = -40\text{V}$, $V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	-0.8	-1.3	-1.8	V	$I_D = -250\mu\text{A}$, $V_{DS} = V_{GS}$
Static Drain-Source On-Resistance (Note 11)	$R_{DS(on)}$	—	18	25	m Ω	$V_{GS} = -10\text{V}$, $I_D = -3\text{A}$
			30	45		$V_{GS} = -4.5\text{V}$, $I_D = -3\text{A}$
Forward Transconductance (Notes 11 & 12)	g_{fs}	—	16.6	—	S	$V_{DS} = -5\text{V}$, $I_D = -3\text{A}$
Diode Forward Voltage (Note 11)	V_{SD}	—	-0.7	-1.0	V	$I_S = -1\text{A}$, $V_{GS} = 0\text{V}$
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C_{iss}	—	1640	—	pF	$V_{DS} = -20\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{oss}	—	179	—		
Reverse Transfer Capacitance	C_{rss}	—	128	—		
Gate Resistance	R_g	—	6.43	—	Ω	$V_{DS} = 0\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$
Total Gate Charge (Note 10)	Q_g	—	14.0	—	nC	$V_{GS} = -4.5\text{V}$ $V_{GS} = -10\text{V}$ $V_{DS} = -20\text{V}$ $I_D = -3\text{A}$
Total Gate Charge (Note 10)	Q_g	—	33.7	—		
Gate-Source Charge (Note 10)	Q_{gs}	—	5.5	—		
Gate-Drain Charge (Note 10)	Q_{gd}	—	7.3	—		
Turn-On Delay Time (Note 10)	$t_{D(on)}$	—	6.9	—	ns	$V_{DD} = -20\text{V}$, $V_{GS} = -10\text{V}$ $I_D = -3\text{A}$
Turn-On Rise Time (Note 10)	t_r	—	14.7	—		
Turn-Off Delay Time (Note 10)	$t_{D(off)}$	—	53.7	—		
Turn-Off Fall Time (Note 10)	t_f	—	30.9	—		

Notes: 11. Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$
 12. For design aid only, not subject to production testing.
 13. Switching characteristics are independent of operating junction temperatures.

Typical Characteristics

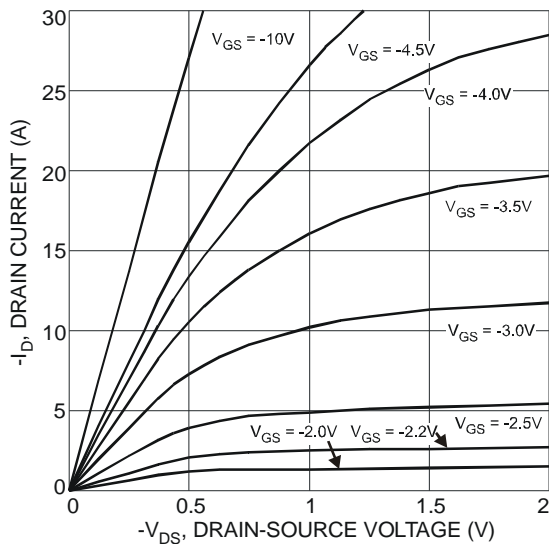


Fig. 1 Typical Output Characteristic

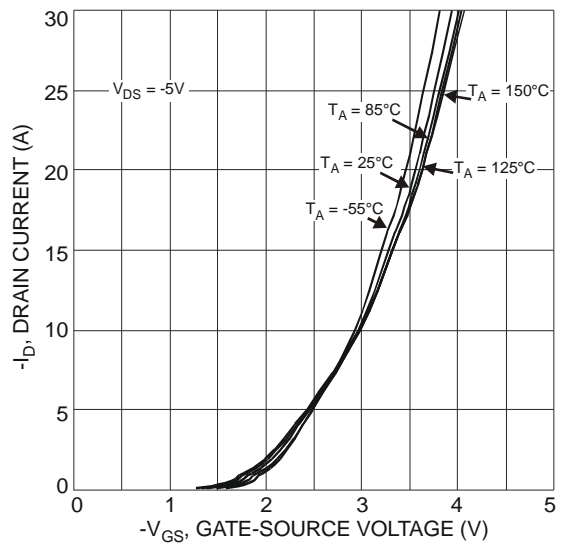


Fig. 2 Typical Transfer Characteristic

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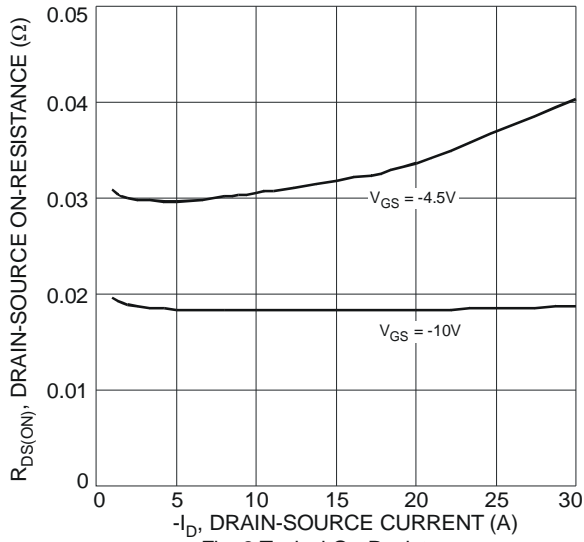


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

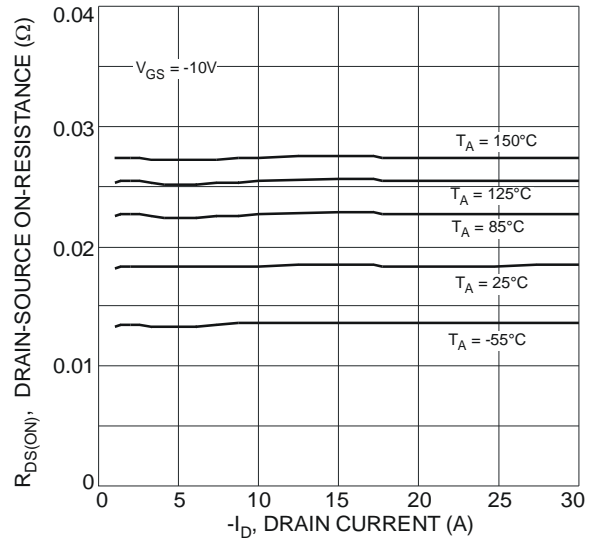


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

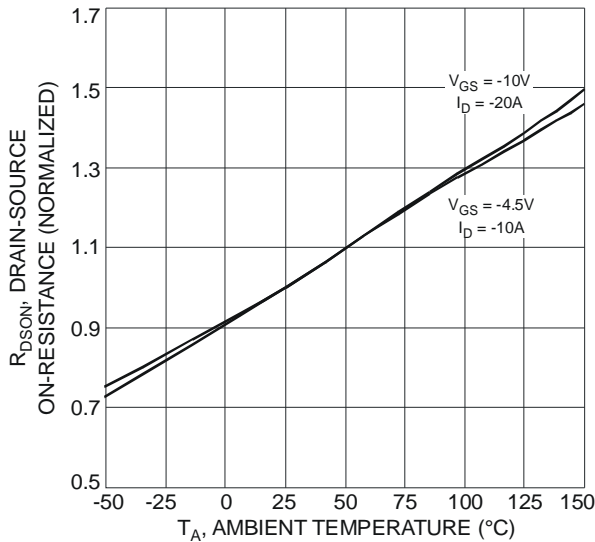


Fig. 5 On-Resistance Variation with Temperature

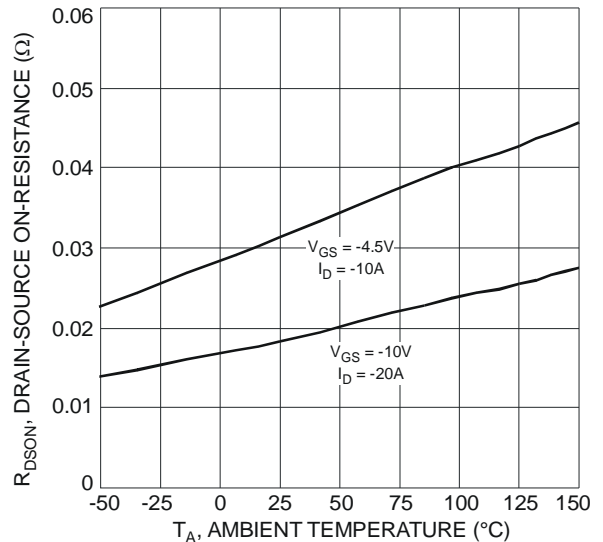


Fig. 6 On-Resistance Variation with Temperature

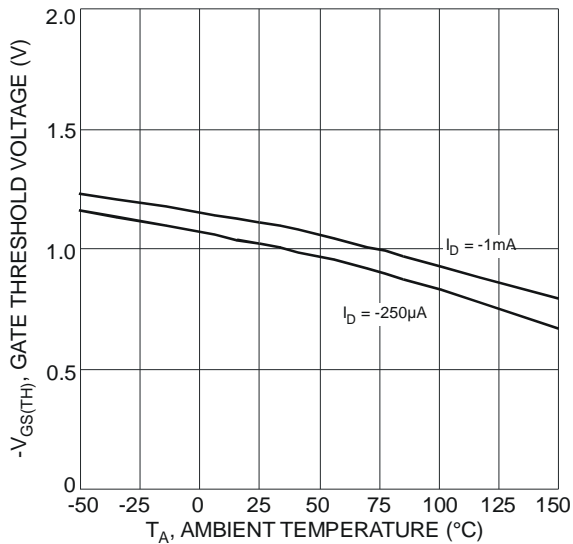


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

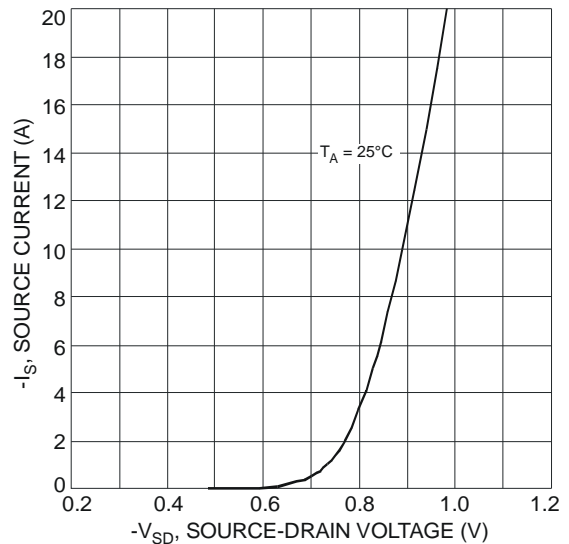
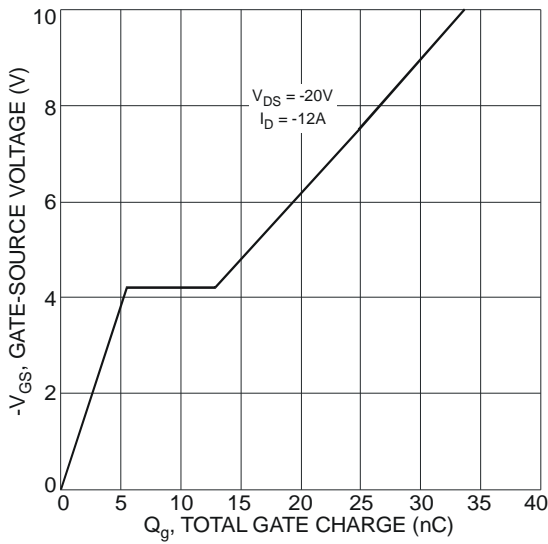
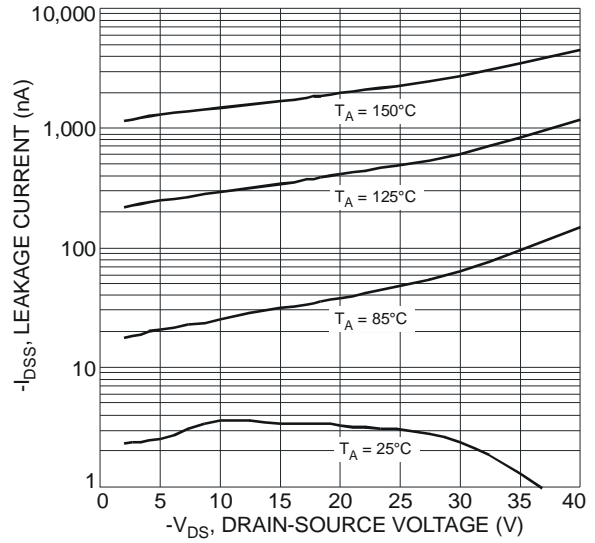
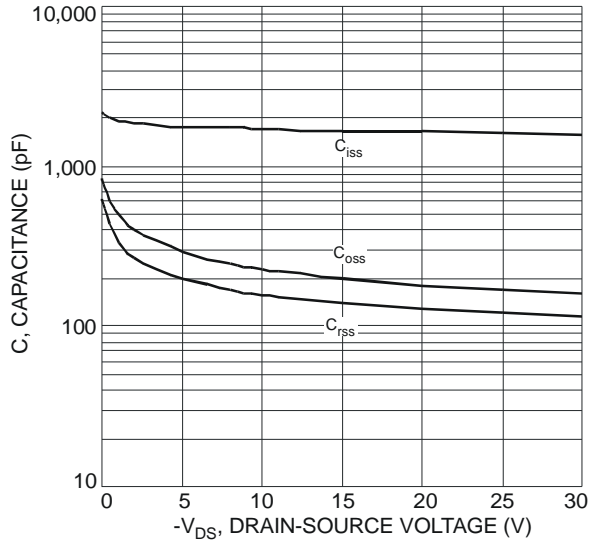


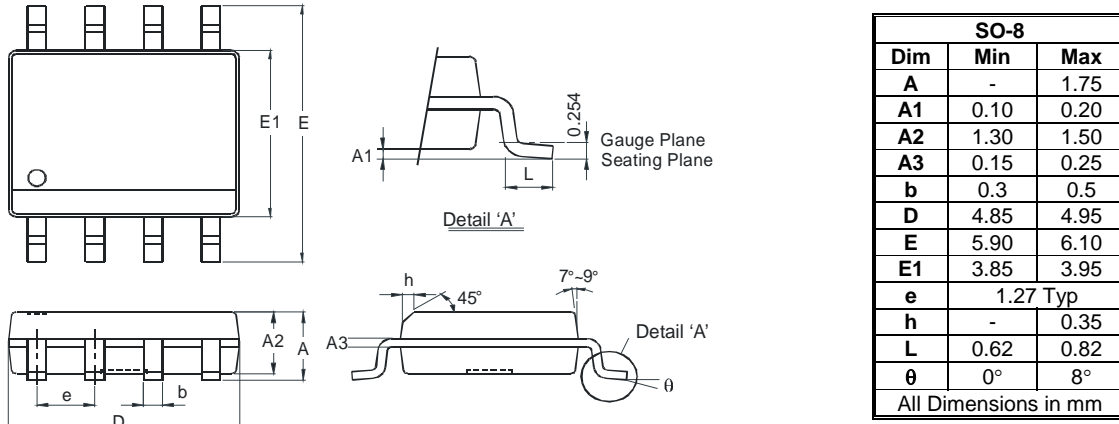
Fig. 8 Diode Forward Voltage vs. Current

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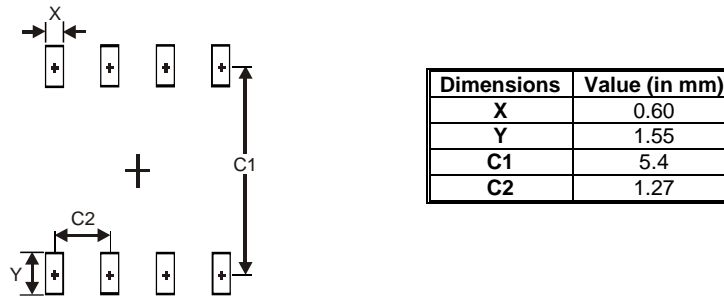


DMP4025LSD

Package Outline Dimensions



Suggested Pad Layout



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