

FEATURES

- Latch-up proof
- 2.8 pF off source capacitance
- 9 pF off drain capacitance
- 0.4 pC charge injection
- Low on resistance: 160 Ω typical
- ± 9 V to ± 22 V dual-supply operation
- 9 V to 40 V single-supply operation
- 48 V supply maximum ratings
- Fully specified at ± 15 V, ± 20 V, +12 V, and +36 V
- V_{DD} to V_{SS} analog signal range
- Human body model (HBM) ESD rating
 - 8 kV input/output port to supplies
 - 2 kV input/output port to input/output port
 - 8 kV all other pins

APPLICATIONS

- Automatic test equipment
- Data acquisition
- Instrumentation
- Avionics
- Audio and video switching
- Communication systems

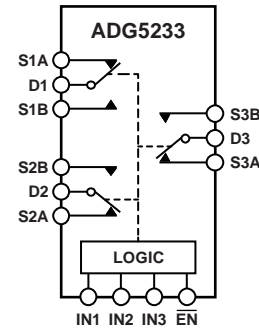
GENERAL DESCRIPTION

The [ADG5233](#) and [ADG5234](#) are monolithic industrial CMOS analog switches comprising three independently selectable single-pole, double throw (SPDT) switches and four independently selectable SPDT switches, respectively.

All channels exhibit break-before-make switching action that prevents momentary shorting when switching channels. An \overline{EN} input on the [ADG5233](#) (LFCSP and TSSOP packages) is used to enable or disable the device. When disabled, all channels are switched off.

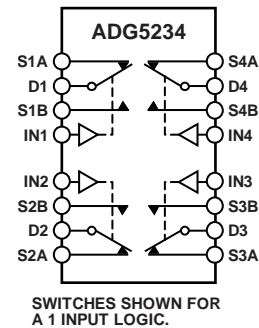
The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make these devices suitable for video signal switching.

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A 1 INPUT LOGIC.

Figure 1. [ADG5233](#) TSSOP and LFCSP_WQ



SWITCHES SHOWN FOR A 1 INPUT LOGIC.

Figure 2. [ADG5234](#) TSSOP and LFCSP_WQ

PRODUCT HIGHLIGHTS

1. Trench Isolation Guards Against Latch-Up.
A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
2. Ultralow Capacitance and 0.4 pC Charge Injection.
3. Dual-Supply Operation.
For applications where the analog signal is bipolar, the [ADG5233/ADG5234](#) can be operated from dual supplies up to ± 22 V.
4. Single-Supply Operation.
For applications where the analog signal is unipolar, the [ADG5233/ADG5234](#) can be operated from a single-rail power supply up to 40 V.
5. 3 V Logic-Compatible Digital Inputs.
 $V_{INH} = 2.0$ V, $V_{INL} = 0.8$ V.
6. No V_L Logic Power Supply Required.

Rev. D

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REVISION HISTORY

8/15—Rev. C to Rev. D

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12/14—Rev. B to Rev. C

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6/13—Rev. A to Rev. B

| | |
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| Added 20-Lead LFCSP | Universal |
| Updated Outline Dimensions | 21 |
| Changes to Ordering Guide | 22 |

3/12—Rev. 0 to Rev. A

| | |
|---------------------------------|-----------|
| Added 16-Lead LFCSP | Universal |
| Changes to Ordering Guide | 22 |

7/11—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 1.

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|------------|----------------|----------------------|-------------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{DD} to V_{SS} | V | |
| On Resistance, R_{ON} | 160 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$; see Figure 28 |
| On-Resistance Match Between Channels, ΔR_{ON} | 200 | 250 | 280 | Ω max | $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$ $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 3.5 | | | Ω typ | |
| | 8 | 9 | 10 | Ω max | |
| | 38 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 50 | 65 | 70 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.02 | | | nA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 30 |
| Drain Off Leakage, I_D (Off) | ± 0.1 | ± 0.2 | ± 0.4 | nA max | |
| | ± 0.02 | | | nA typ | $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 30 |
| Channel On Leakage, I_D (On), I_S (On) | ± 0.1 | ± 0.2 | ± 0.4 | nA max | |
| | ± 0.08 | | | nA typ | $V_S = V_D = \pm 10\text{ V}$; see Figure 26 |
| | ± 0.2 | ± 0.3 | ± 0.9 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.002 | | | μA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 3 | | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| Transition Time, $t_{TRANSITION}$ | 125 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 160 | 190 | 215 | ns max | $V_S = 10\text{ V}$; see Figure 33 |
| $t_{ON}(\overline{EN})$ | 145 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 175 | 210 | 240 | ns max | $V_S = 10\text{ V}$; see Figure 35 |
| $t_{OFF}(\overline{EN})$ | 125 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 155 | 170 | 180 | ns max | $V_S = 10\text{ V}$; see Figure 35 |
| Break-Before-Make Time Delay, t_D | 45 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | | 25 | ns min | $V_{S1} = V_{S2} = 10\text{ V}$; see Figure 34 |
| Charge Injection, Q_{INJ} | 0.4 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 36 |
| Off Isolation | -76 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 31 |
| Channel-to-Channel Crosstalk | -87 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Figure 29 |
| -3 dB Bandwidth | 355 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 32 |
| Insertion Loss | -6.4 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 32 |
| C_S (Off) | 2.8 | | | pF typ | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| C_D (Off) | 9 | | | pF typ | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| C_D (On), C_S (On) | 13 | | | pF typ | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--------------------|-------|----------------|-----------------|-------------------|---|
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 45 | | | μA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ Digital inputs = 0 V or V_{DD} |
| I_{SS} | 55 | | 70 | μA max | |
| | 0.001 | | | μA typ | Digital inputs = 0 V or V_{DD} |
| | | | 1 | μA max | |
| V_{DD}/V_{SS} | | | $\pm 9/\pm 22$ | V min/V max | GND = 0 V |

¹ Guaranteed by design; not subject to production test.

$\pm 20\text{ V}$ DUAL SUPPLY

$V_{DD} = +20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 2.

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|------------|----------------|----------------------|-------------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{DD} to V_{SS} | V | |
| On Resistance, R_{ON} | 140 | | | Ω typ | $V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$; see Figure 28 |
| | 160 | 200 | 230 | Ω max | $V_{DD} = +18\text{ V}$, $V_{SS} = -18\text{ V}$ |
| On-Resistance Match Between Channels, ΔR_{ON} | 3.5 | | | Ω typ | $V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$ |
| | 8 | 9 | 10 | Ω max | |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 33 | | | Ω typ | $V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$ |
| | 45 | 55 | 60 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.02 | | | nA typ | $V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$ $V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$; see Figure 30 |
| | ± 0.1 | ± 0.2 | ± 0.4 | nA max | |
| Drain Off Leakage, I_D (Off) | ± 0.02 | | | nA typ | $V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$; see Figure 30 |
| | ± 0.1 | ± 0.2 | ± 0.4 | nA max | |
| Channel On Leakage, I_D (On), I_S (On) | ± 0.08 | | | nA typ | $V_S = V_D = \pm 15\text{ V}$; see Figure 26 |
| | ± 0.2 | ± 0.3 | ± 0.9 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.002 | | | μA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 3 | | | pF typ | |
| DYNAMIC CHARACTERISTICS ¹ | | | | | |
| Transition Time, $t_{TRANSITION}$ | 125 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 155 | 180 | 200 | ns max | $V_S = 10\text{ V}$; see Figure 33 |
| $t_{ON}(\overline{EN})$ | 145 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 170 | 200 | 220 | ns max | $V_S = 10\text{ V}$; see Figure 35 |
| $t_{OFF}(\overline{EN})$ | 125 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 155 | 160 | 170 | ns max | $V_S = 10\text{ V}$; see Figure 35 |
| Break-Before-Make Time Delay, t_D | 40 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | | 20 | ns min | $V_{S1} = V_{S2} = 10\text{ V}$; see Figure 34 |
| Charge Injection, Q_{INJ} | 0.7 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 36 |
| Off Isolation | -76 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 31 |

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|------------------------------|-------|----------------|-----------------|-------------------|--|
| Channel-to-Channel Crosstalk | -87 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 29 |
| -3 dB Bandwidth | 370 | | | MHz typ | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 32 |
| Insertion Loss | -5.6 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 32 |
| C_S (Off) | 2.8 | | | pF typ | $V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$ |
| C_D (Off) | 9 | | | pF typ | $V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$ |
| C_D (On), C_S (On) | 13 | | | pF typ | $V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$ |
| POWER REQUIREMENTS | | | | | $V_{DD} = +22 \text{ V}$, $V_{SS} = -22 \text{ V}$ |
| I_{DD} | 50 | | | μA typ | Digital inputs = 0 V or V_{DD} |
| | 70 | | 110 | μA max | |
| I_{SS} | 0.001 | | | μA typ | Digital inputs = 0 V or V_{DD} |
| | | | 1 | μA max | |
| V_{DD}/V_{SS} | | | $\pm 9/\pm 22$ | V min/V max | GND = 0 V |

¹ Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, GND = 0 V, unless otherwise noted.

Table 3.

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|------------|----------------|-----------------|-------------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | |
| On Resistance, R_{ON} | 360 | | | Ω typ | $V_S = 0 \text{ V}$ to 10 V, $I_S = -1 \text{ mA}$; see Figure 28 |
| | 500 | 610 | 700 | Ω max | $V_{DD} = 10.8 \text{ V}$, $V_{SS} = 0 \text{ V}$ |
| On-Resistance Match Between Channels, ΔR_{ON} | 5.5 | | | Ω typ | $V_S = 0 \text{ V}$ to 10 V, $I_S = -1 \text{ mA}$ |
| | 20 | 21 | 22 | Ω max | |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 170 | | | Ω typ | $V_S = 0 \text{ V}$ to 10 V, $I_S = -1 \text{ mA}$ |
| | 280 | 335 | 370 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.02 | | | nA typ | $V_{DD} = 13.2 \text{ V}$, $V_{SS} = 0 \text{ V}$ $V_S = 1 \text{ V}/10 \text{ V}$, $V_D = 10 \text{ V}/1 \text{ V}$; see Figure 30 |
| | ± 0.1 | ± 0.2 | ± 0.4 | nA max | |
| Drain Off Leakage, I_D (Off) | ± 0.02 | | | nA typ | $V_S = 1 \text{ V}/10 \text{ V}$, $V_D = 10 \text{ V}/1 \text{ V}$; see Figure 30 |
| | ± 0.1 | ± 0.2 | ± 0.4 | nA max | |
| Channel On Leakage, I_D (On), I_S (On) | ± 0.08 | | | nA typ | $V_S = V_D = 1 \text{ V}/10 \text{ V}$; see Figure 26 |
| | ± 0.2 | ± 0.3 | ± 0.9 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.002 | | | μA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 3 | | | pF typ | |

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|------|----------------|-----------------|-------------------|---|
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| Transition Time, $t_{\text{TRANSITION}}$ | 165 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$ |
| $t_{\text{ON}}(\overline{\text{EN}})$ | 215 | 260 | 300 | ns max | $V_S = 8\ \text{V}$; see Figure 33 |
| | 200 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$ |
| $t_{\text{OFF}}(\overline{\text{EN}})$ | 245 | 305 | 350 | ns max | $V_S = 8\ \text{V}$; see Figure 35 |
| | 130 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$ |
| Break-Before-Make Time Delay, t_D | 165 | 180 | 200 | ns max | $V_S = 8\ \text{V}$; see Figure 35 |
| | 85 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$ |
| Charge Injection, Q_{INJ} | | | 45 | ns min | $V_{S1} = V_{S2} = 8\ \text{V}$; see Figure 34 |
| | 0 | | | pC typ | $V_S = 6\ \text{V}$, $R_S = 0\ \Omega$, $C_L = 1\ \text{nF}$; see Figure 36 |
| Off Isolation | -76 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 31 |
| Channel-to-Channel Crosstalk | -87 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 29 |
| -3 dB Bandwidth | 260 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$; see Figure 32 |
| Insertion Loss | -9 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 32 |
| C_S (Off) | 3 | | | pF typ | $V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$ |
| C_D (Off) | 10 | | | pF typ | $V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$ |
| C_D (On), C_S (On) | 14 | | | pF typ | $V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$ |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 40 | | | μA typ | $V_{\text{DD}} = 13.2\ \text{V}$ |
| | 50 | | 65 | μA max | Digital inputs = 0 V or V_{DD} |
| V_{DD} | | | 9/40 | V min/V max | GND = 0 V, $V_{\text{SS}} = 0\ \text{V}$ |

¹ Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

$V_{\text{DD}} = 36\ \text{V} \pm 10\%$, $V_{\text{SS}} = 0\ \text{V}$, GND = 0 V, unless otherwise noted.

Table 4.

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|------------|----------------|------------------------|--------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | |
| On Resistance, R_{ON} | 140 | | | Ω typ | $V_S = 0\ \text{V}$ to 30 V, $I_S = -1\ \text{mA}$; see Figure 28 |
| | 170 | 215 | 245 | Ω max | $V_{\text{DD}} = 32.4\ \text{V}$, $V_{\text{SS}} = 0\ \text{V}$ |
| On-Resistance Match Between Channels, ΔR_{ON} | 3.5 | | | Ω typ | $V_S = 0\ \text{V}$ to 30 V, $I_S = -1\ \text{mA}$ |
| | 8 | 9 | 10 | Ω max | |
| On-Resistance Flatness, $R_{\text{FLAT}}(\text{ON})$ | 35 | | | Ω typ | $V_S = 0\ \text{V}$ to 30 V, $I_S = -1\ \text{mA}$ |
| | 50 | 60 | 65 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.02 | | | nA typ | $V_{\text{DD}} = 39.6\ \text{V}$, $V_{\text{SS}} = 0\ \text{V}$ $V_S = 1\ \text{V}/30\ \text{V}$, $V_D = 30\ \text{V}/1\ \text{V}$; see Figure 30 |
| Drain Off Leakage, I_D (Off) | ± 0.1 | ± 0.2 | ± 0.4 | nA max | |
| | ± 0.02 | | | nA typ | $V_S = 1\ \text{V}/30\ \text{V}$, $V_D = 30\ \text{V}/1\ \text{V}$; see Figure 30 |
| Channel On Leakage, I_D (On), I_S (On) | ± 0.1 | ± 0.2 | ± 0.4 | nA max | |
| | ± 0.08 | | | nA typ | $V_S = V_D = 1\ \text{V}/30\ \text{V}$; see Figure 26 |
| | ± 0.2 | ± 0.3 | ± 0.9 | nA max | |

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|---|-------|----------------|-----------------|-----------------------|--|
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | $V_{IN} = V_{GND}$ or V_{DD} |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.002 | | | μA typ | |
| Digital Input Capacitance, C_{IN} | 3 | | ± 0.1 | μA max pF typ | |
| DYNAMIC CHARACTERISTICS ¹ | | | | | |
| Transition Time, $t_{TRANSITION}$ | 155 | | | ns typ | $R_L = 300 \Omega$, $C_L = 35$ pF |
| $t_{ON}(\overline{EN})$ | 200 | 215 | 230 | ns max | $V_S = 18$ V; see Figure 33 |
| $t_{OFF}(\overline{EN})$ | 180 | | | ns typ | $R_L = 300 \Omega$, $C_L = 35$ pF |
| | 215 | 235 | 250 | ns max | $V_S = 18$ V; see Figure 35 |
| | 150 | | | ns typ | $R_L = 300 \Omega$, $C_L = 35$ pF |
| Break-Before-Make Time Delay, t_D | 190 | 190 | 190 | ns max | $V_S = 18$ V; see Figure 35 |
| | 50 | | | ns typ | $R_L = 300 \Omega$, $C_L = 35$ pF |
| | | | 25 | ns min | $V_{S1} = V_{S2} = 18$ V; see Figure 34 |
| Charge Injection, Q_{INJ} | 0.5 | | | pC typ | $V_S = 18$ V, $R_S = 0 \Omega$, $C_L = 1$ nF; see Figure 36 |
| Off Isolation | -76 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz; see Figure 31 |
| Channel-to-Channel Crosstalk | -87 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz; see Figure 29 |
| -3 dB Bandwidth | 275 | | | MHz typ | $R_L = 50 \Omega$, $C_L = 5$ pF; see Figure 32 |
| Insertion Loss | -6.2 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz; see Figure 32 |
| C_S (Off) | 2.8 | | | pF typ | $V_S = 18$ V, $f = 1$ MHz |
| C_D (Off) | 9 | | | pF typ | $V_S = 18$ V, $f = 1$ MHz |
| C_D (On), C_S (On) | 13 | | | pF typ | $V_S = 18$ V, $f = 1$ MHz |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 80 | | | μA typ | $V_{DD} = 39.6$ V |
| | 100 | | 130 | μA max | Digital inputs = 0 V or V_{DD} |
| V_{DD} | | | 9/40 | V min/V max | $GND = 0$ V, $V_{SS} = 0$ V |

¹ Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S_x OR D_x

Table 5. ADG5233

| Parameter | 25°C | 85°C | 125°C | Unit |
|---|------|------|-------|------------|
| CONTINUOUS CURRENT, S_x OR D_x | | | | |
| $V_{DD} = +15$ V, $V_{SS} = -15$ V | | | | |
| TSSOP ($\theta_{JA} = 112.6^\circ C/W$) | 24 | 16 | 11 | mA maximum |
| LFCSP ($\theta_{JA} = 30.4^\circ C/W$) | 42 | 26.5 | 15 | mA maximum |
| $V_{DD} = +20$ V, $V_{SS} = -20$ V | | | | |
| TSSOP ($\theta_{JA} = 112.6^\circ C/W$) | 26 | 17 | 11 | mA maximum |
| LFCSP ($\theta_{JA} = 30.4^\circ C/W$) | 46 | 28 | 15 | mA maximum |
| $V_{DD} = 12$ V, $V_{SS} = 0$ V | | | | |
| TSSOP ($\theta_{JA} = 112.6^\circ C/W$) | 17 | 12 | 7.7 | mA maximum |
| LFCSP ($\theta_{JA} = 30.4^\circ C/W$) | 24 | 17 | 11 | mA maximum |
| $V_{DD} = 36$ V, $V_{SS} = 0$ V | | | | |
| TSSOP ($\theta_{JA} = 112.6^\circ C/W$) | 25 | 17 | 11 | mA maximum |
| LFCSP ($\theta_{JA} = 30.4^\circ C/W$) | 45 | 28 | 15 | mA maximum |

Table 6. ADG5234

| Parameter | 25°C | 85°C | 125°C | Unit |
|---|------|------|-------|------------|
| CONTINUOUS CURRENT, Sx OR Dx | | | | |
| $V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$ | | | | |
| TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$) | 21 | 15 | 10 | mA maximum |
| LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$) | 38 | 24 | 14 | mA maximum |
| $V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V}$ | | | | |
| TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$) | 22 | 15 | 10 | mA maximum |
| LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$) | 41 | 26 | 15 | mA maximum |
| $V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$ | | | | |
| TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$) | 15 | 11 | 7 | mA maximum |
| LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$) | 22 | 16 | 11 | mA maximum |
| $V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V}$ | | | | |
| TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$) | 22 | 15 | 10 | mA maximum |
| LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$) | 40 | 26 | 15 | mA maximum |

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 7.

| Parameter | Rating |
|---|--|
| V_{DD} to V_{SS} | 48 V |
| V_{DD} to GND | -0.3 V to +48 V |
| V_{SS} to GND | +0.3 V to -48 V |
| Analog Inputs ¹ | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first |
| Digital Inputs ¹ | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first |
| Peak Current, Sx or Dx Pins ADG5233 ADG5234 | 76 mA (pulsed at 1 ms, 10% duty cycle maximum) 67 mA (pulsed at 1 ms, 10% duty cycle maximum) |
| Continuous Current, Sx or Dx ² | Data + 15% |
| Temperature Range | |
| Operating | -40°C to +125°C |
| Storage | -65°C to +150°C |
| Junction Temperature | 150°C |
| Thermal Impedance, θ_{JA} | |
| 16-Lead TSSOP (4-Layer Board) | 112.6°C/W |
| 20-Lead TSSOP (4-Layer Board) | 143°C/W |
| 16-Lead LFCSP (4-Layer Board) | 30.4°C/W |
| 20-Lead LFCSP (4-Layer Board) | 30.4°C/W |
| Reflow Soldering Peak Temperature, Pb Free | 260(+0/-5)°C |
| Human Body Model (HBM) ESD | |
| Input/Output Port to Supplies | 8 kV |
| Input/Output Port to Input/Output Port | 2 kV |
| All Other Pins | 8 kV |

¹ Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

² See Table 5 and Table 6.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

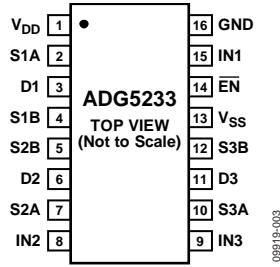
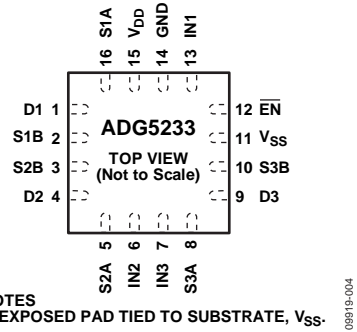


Figure 3. ADG5233 TSSOP Pin Configuration



NOTES
1. EXPOSED PAD TIED TO SUBSTRATE, V_{SS}.

Figure 4. ADG5233 LFCSP_WQ Pin Configuration

Table 8. ADG5233 Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|---------|----------|------------------------|--|
| TSSOP | LFCSP_WQ | | |
| 1 | 15 | V _{DD} | Most Positive Power Supply Potential. |
| 2 | 16 | S1A | Source Terminal 1A. This pin can be an input or an output. |
| 3 | 1 | D1 | Drain Terminal 1. This pin can be an input or an output. |
| 4 | 2 | S1B | Source Terminal 1B. This pin can be an input or an output. |
| 5 | 3 | S2B | Source Terminal 2B. This pin can be an input or an output. |
| 6 | 4 | D2 | Drain Terminal 2. This pin can be an input or an output. |
| 7 | 5 | S2A | Source Terminal 2A. This pin can be an input or an output. |
| 8 | 6 | IN2 | Logic Control Input 2. |
| 9 | 7 | IN3 | Logic Control Input 3. |
| 10 | 8 | S3A | Source Terminal 3A. This pin can be an input or an output. |
| 11 | 9 | D3 | Drain Terminal 3. This pin can be an input or an output. |
| 12 | 10 | S3B | Source Terminal 3B. This pin can be an input or an output. |
| 13 | 11 | V _{SS} | Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground. |
| 14 | 12 | $\overline{\text{EN}}$ | Active Low Digital Input. When high, the device is disabled and all switches are off. When low, IN _x logic inputs determine the on switches. |
| 15 | 13 | IN1 | Logic Control Input 1. |
| 16 | 14 | GND | Ground (0 V) Reference. |
| | 17 | EPAD | The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} . |

Table 9. ADG5233 Truth Table

| $\overline{\text{EN}}$ | IN _x | S _x A | S _x B |
|------------------------|-----------------|------------------|------------------|
| 1 | X ¹ | Off | Off |
| 0 | 0 | Off | On |
| 0 | 1 | On | Off |

¹ X is don't care.

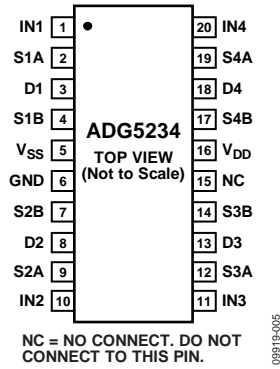
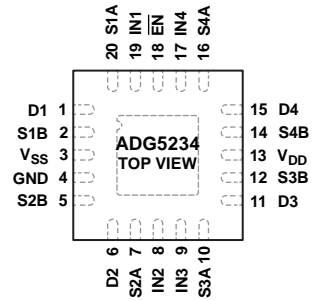


Figure 5. ADG5234 TSSOP Pin Configuration



NOTES
1. EXPOSED PAD TIED TO SUBSTRATE, V_{SS}.

Figure 6. ADG5234 LFCSP_WQ Pin Configuration

Table 10. ADG5234 Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|---------|----------|-----------------|---|
| TSSOP | LFCSP_WQ | | |
| 1 | 19 | IN1 | Logic Control Input 1. |
| 2 | 20 | S1A | Source Terminal 1A. This pin can be an input or an output. |
| 3 | 1 | D1 | Drain Terminal 1. This pin can be an input or an output. |
| 4 | 2 | S1B | Source Terminal 1B. This pin can be an input or an output. |
| 5 | 3 | V _{SS} | Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground. |
| 6 | 4 | GND | Ground (0 V) Reference. |
| 7 | 5 | S2B | Source Terminal 2B. This pin can be an input or an output. |
| 8 | 6 | D2 | Drain Terminal 2. This pin can be an input or an output. |
| 9 | 7 | S2A | Source Terminal 2A. This pin can be an input or an output. |
| 10 | 8 | IN2 | Logic Control Input 2. |
| 11 | 9 | IN3 | Logic Control Input 3. |
| 12 | 10 | S3A | Source Terminal 3A. This pin can be an input or an output. |
| 13 | 11 | D3 | Drain Terminal 3. This pin can be an input or an output. |
| 14 | 12 | S3B | Source Terminal 3B. This pin can be an input or an output. |
| 15 | N/A | NC | No Connect. This pin is open. |
| 16 | 13 | V _{DD} | Most Positive Power Supply Potential. |
| 17 | 14 | S4B | Source Terminal 4B. This pin can be an input or an output. |
| 18 | 15 | D4 | Drain Terminal 4. This pin can be an input or an output. |
| 19 | 16 | S4A | Source Terminal 4A. This pin can be an input or an output. |
| 20 | 17 | IN4 | Logic Control Input 4. |
| N/A | 18 | \overline{EN} | Active Low Digital Input. When high, the device is disabled and all switches are off. When low, IN _x logic inputs determine the on switches. |
| N/A | 21 | EP | Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} . |

Table 11. ADG5234 Truth Table

| IN _x | S _x A | S _x B |
|-----------------|------------------|------------------|
| 0 | Off | On |
| 1 | On | Off |

TYPICAL PERFORMANCE CHARACTERISTICS

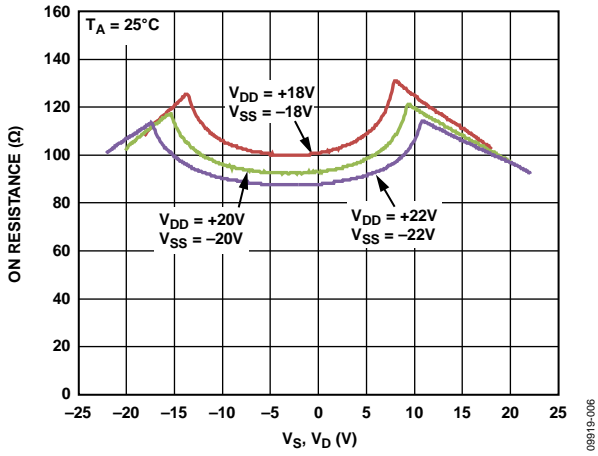


Figure 7. On Resistance as a Function of V_S, V_D (± 20 V Dual Supply)

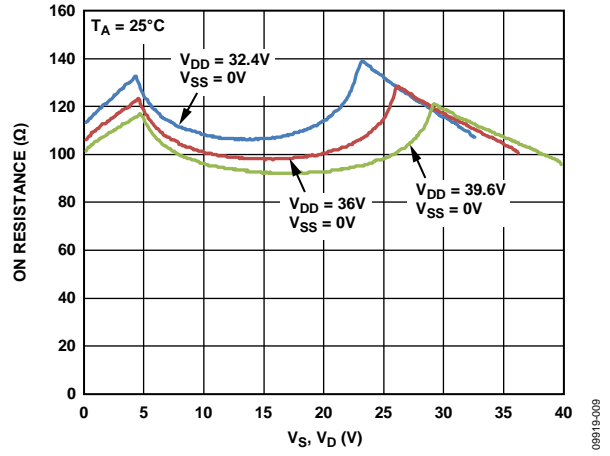


Figure 10. On Resistance as a Function of V_S, V_D (36 V Single Supply)

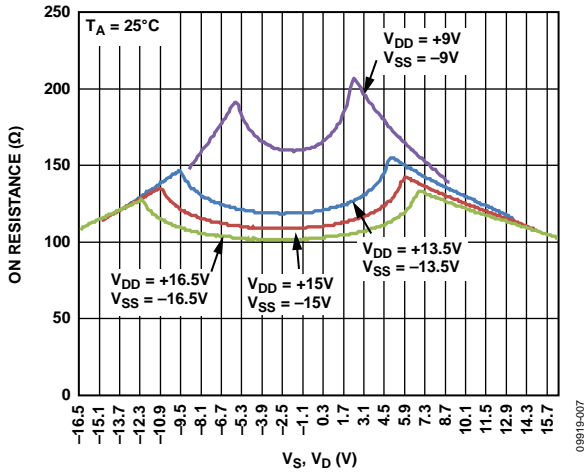


Figure 8. On Resistance as a Function of V_S, V_D (± 15 V Dual Supply)

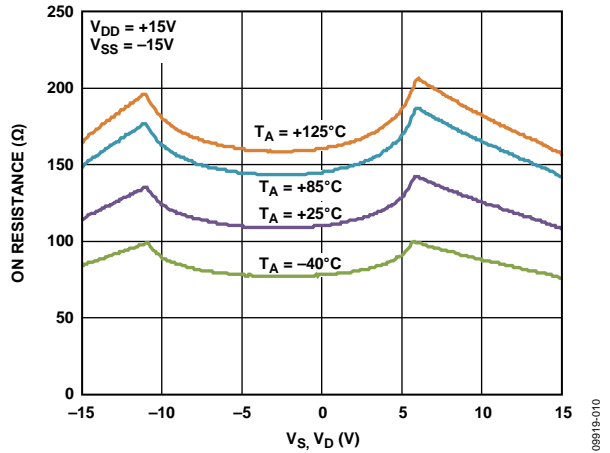


Figure 11. On Resistance as a Function of $V_S (V_D)$ for Different Temperatures, ± 15 V Dual Supply

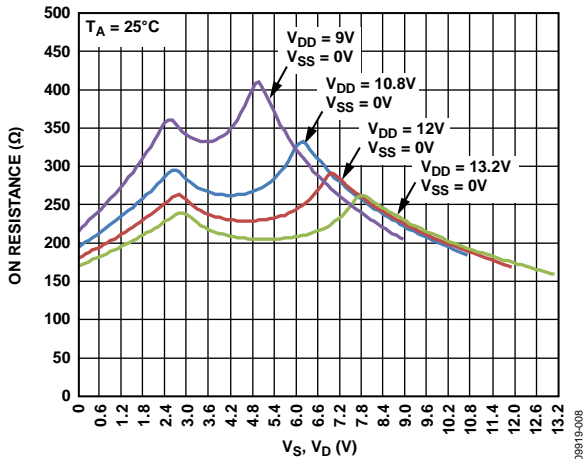


Figure 9. On Resistance as a Function of V_S, V_D (12 V Single Supply)

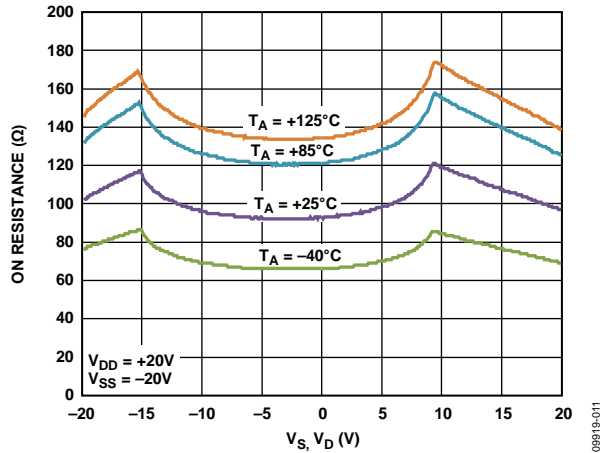


Figure 12. On Resistance as a Function of $V_S (V_D)$ for Different Temperatures, ± 20 V Dual Supply

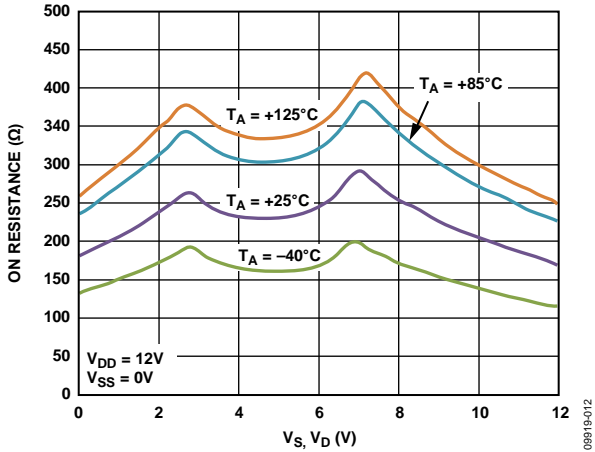


Figure 13. On Resistance as a Function of V_S (V_b) for Different Temperatures, 12 V Single Supply

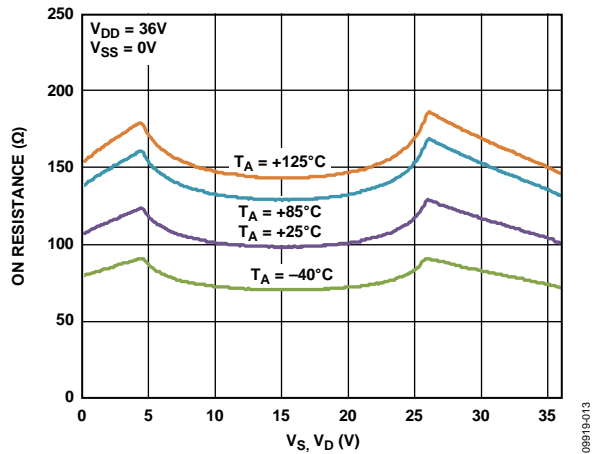


Figure 14. On Resistance as a Function of V_S (V_b) for Different Temperatures, 36 V Single Supply

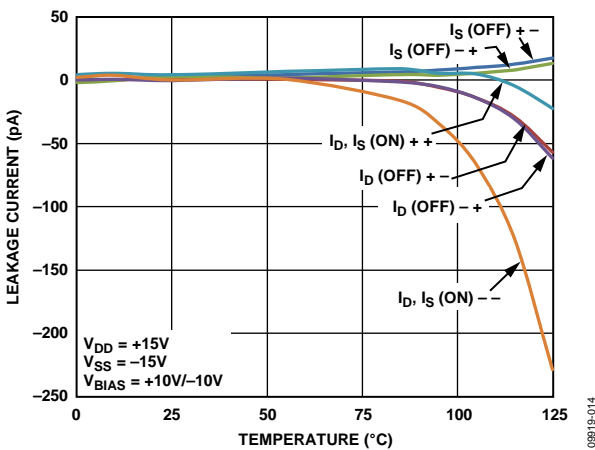


Figure 15. Leakage Currents as a Function of Temperature, ± 15 V Dual Supply

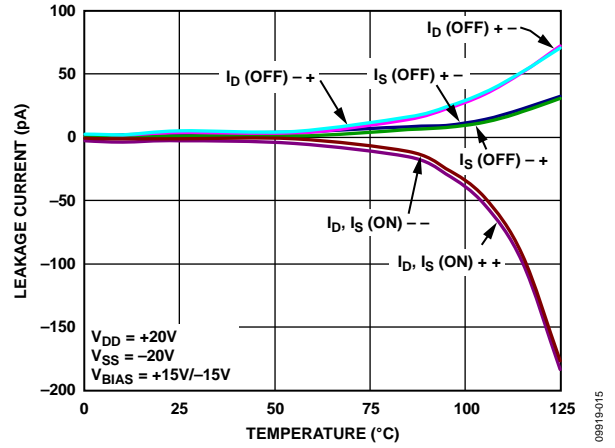


Figure 16. Leakage Currents as a Function of Temperature, ± 20 V Dual Supply

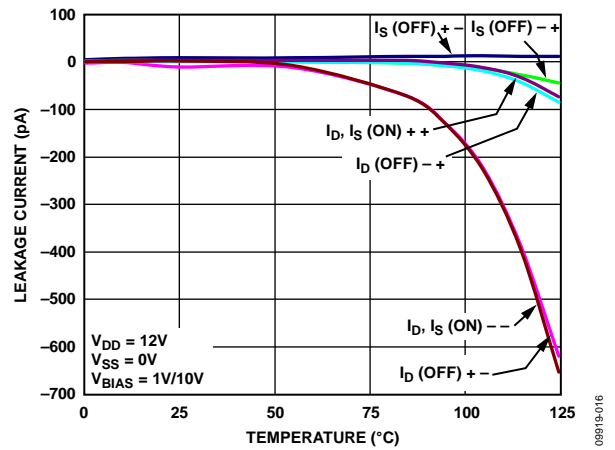


Figure 17. Leakage Currents as a Function of Temperature, 12 V Single Supply

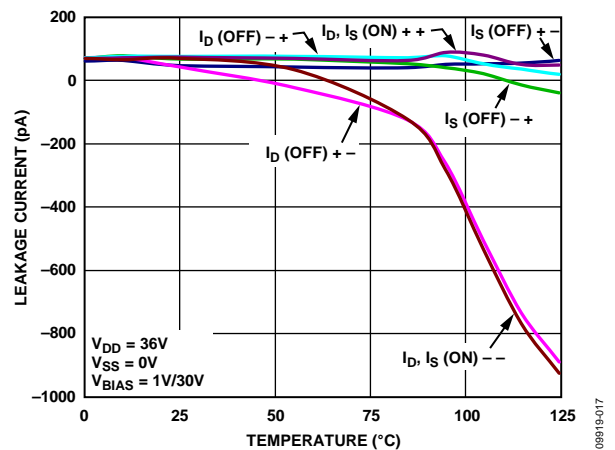


Figure 18. Leakage Currents as a Function of Temperature, 36 V Single Supply

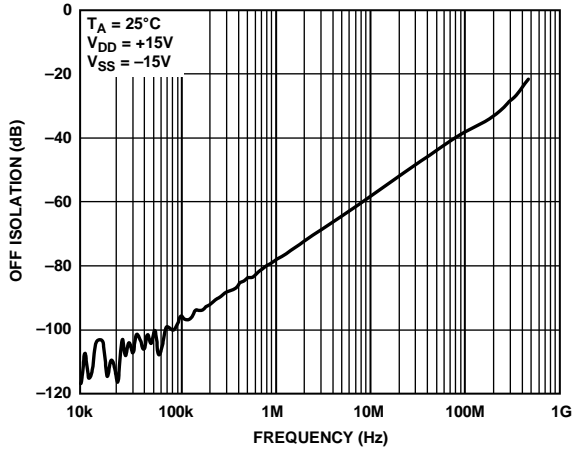


Figure 19. Off Isolation vs. Frequency, ±15 V Dual Supply

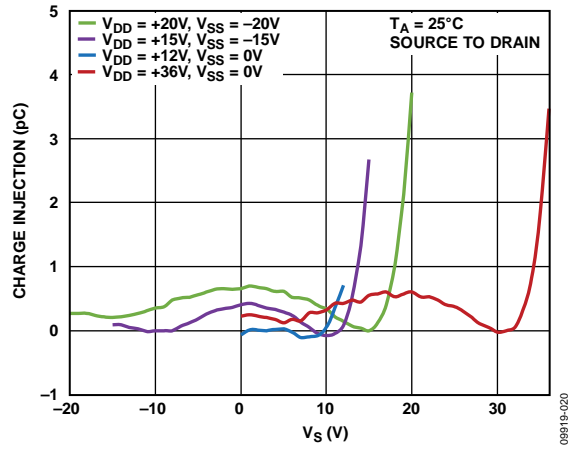


Figure 21. Charge Injection vs. Source Voltage, Source to Drain

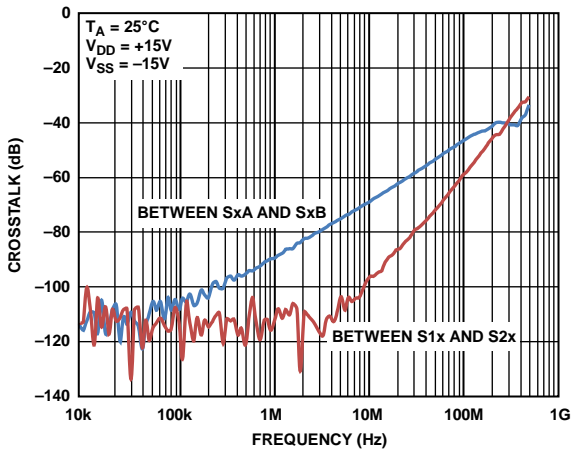


Figure 20. Crosstalk vs. Frequency, ±15 V Dual Supply

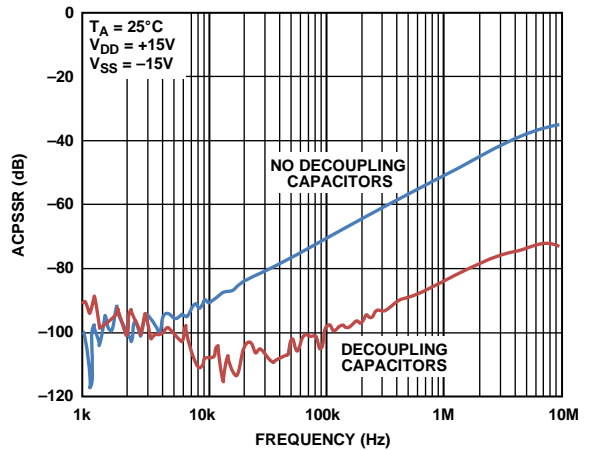


Figure 22. ACPSSR vs. Frequency, ±15 V Dual Supply

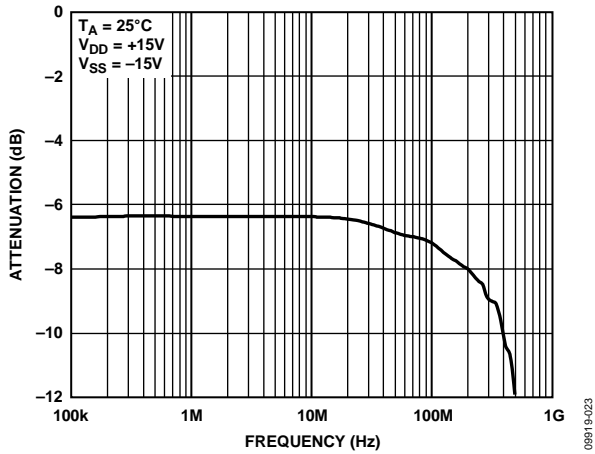


Figure 23. Bandwidth

09919-023

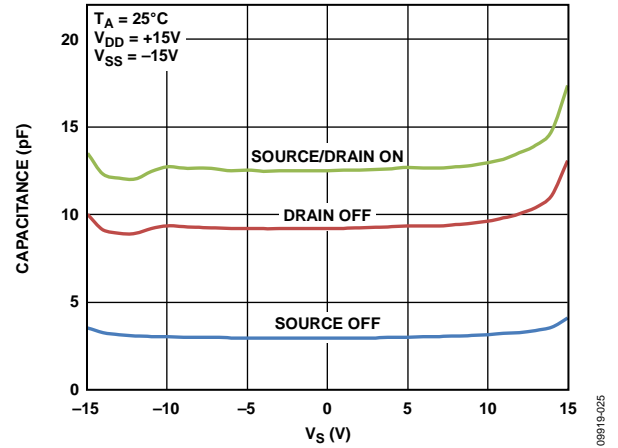


Figure 25. Capacitance vs. Source Voltage, $\pm 15\text{ V}$ Dual Supply

09919-025

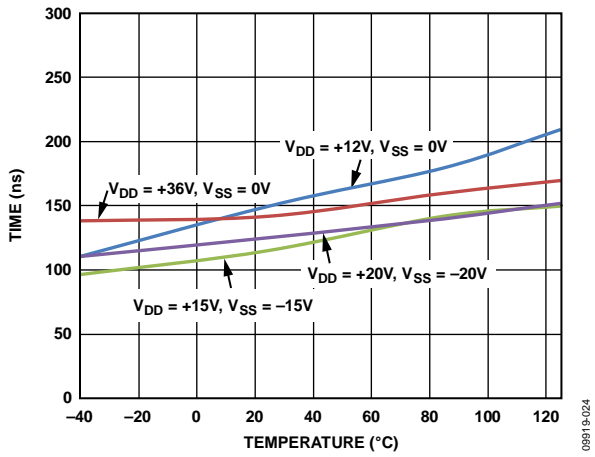


Figure 24. $t_{\text{TRANSITION}}$ Times vs. Temperature

09919-024

TEST CIRCUITS

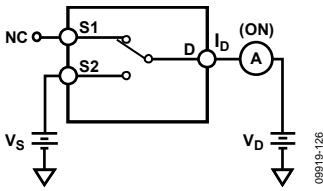


Figure 26. On Leakage

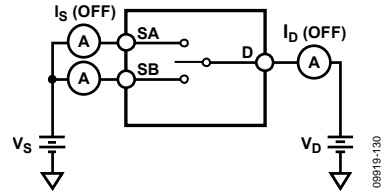


Figure 30. Off Leakage

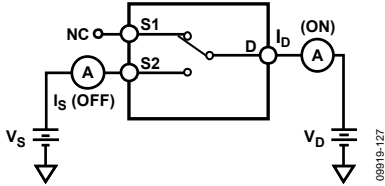
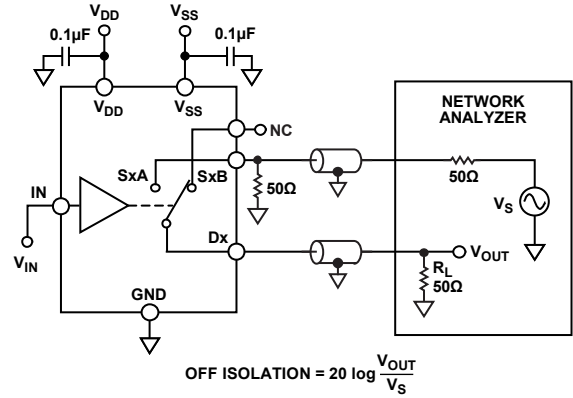


Figure 27. On and Off Leakage On and Off Leakage (ADG5234 TSSOP)



$$\text{OFF ISOLATION} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

Figure 31. Off Isolation

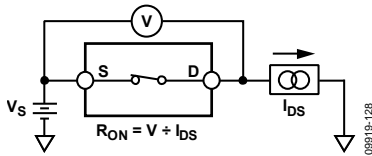
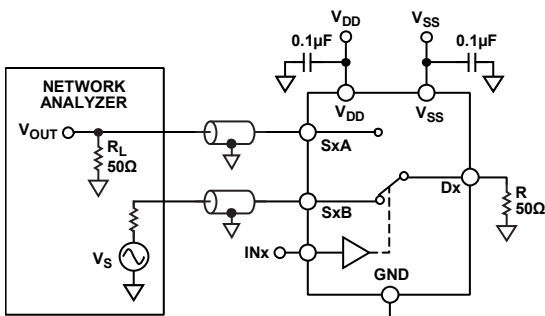
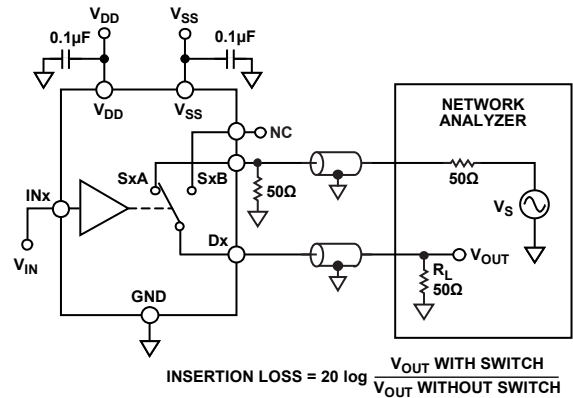


Figure 28. On Resistance



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

Figure 29. Channel-to-Channel Crosstalk



$$\text{INSERTION LOSS} = 20 \log \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Figure 32. Bandwidth

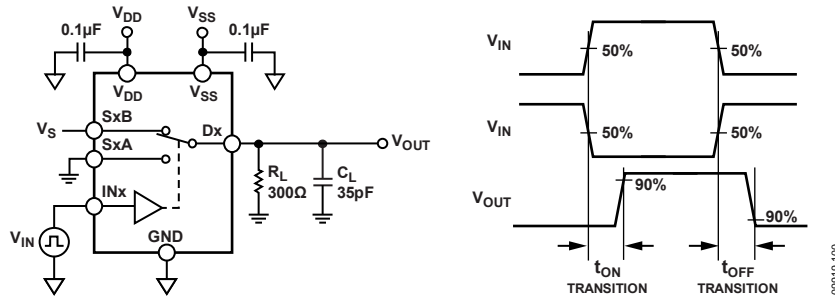


Figure 33. Switching Timing

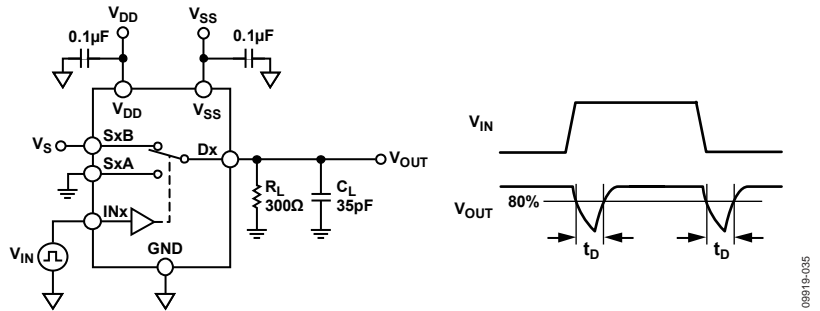


Figure 34. Break-Before-Make Delay, t_D

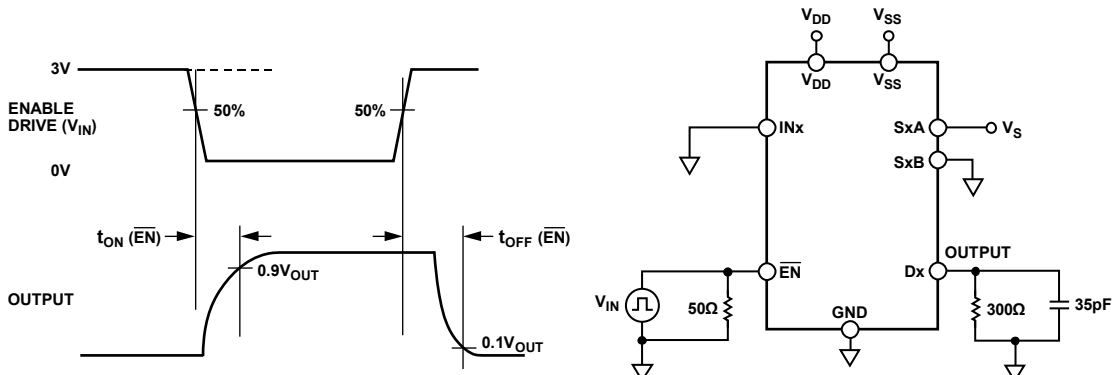


Figure 35. Enable Delay, $t_{ON}(\overline{EN})$, $t_{OFF}(\overline{EN})$

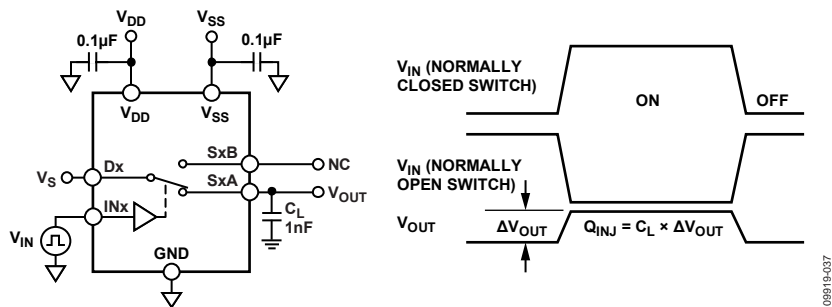


Figure 36. Charge Injection

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on Terminal Dx and Terminal Sx, respectively.

R_{ON}

R_{ON} is the ohmic resistance between Terminal Dx and Terminal Sx.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

The difference between the maximum and minimum value of on resistance as measured over the specified analog signal range is represented by $R_{FLAT(ON)}$.

I_S (Off)

I_S (Off) is the source leakage current with the switch off.

I_D (Off)

I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)

C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} represents digital input capacitance.

$t_{ON}(\overline{EN})$

$t_{ON}(\overline{EN})$ represents the delay time between the 50% and 90% points of the digital input and switch on condition.

$t_{OFF}(\overline{EN})$

$t_{OFF}(\overline{EN})$ represents the delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D

t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response

On response is the frequency response of the on switch.

AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is a measure of the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of the signal on the output to the amplitude of the modulation is the ACPSRR.

TRENCH ISOLATION

In the [ADG5233/ADG5234](#), an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

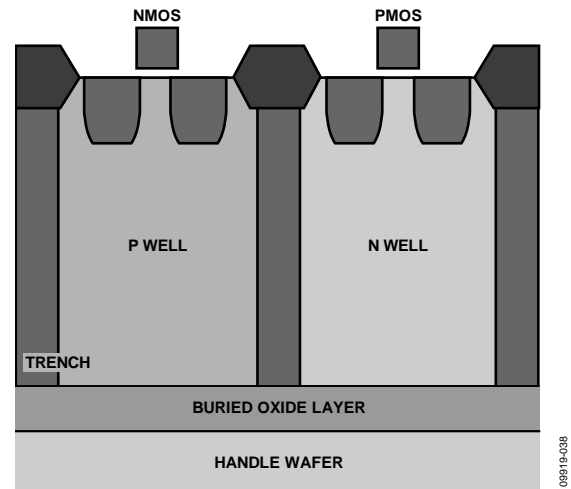


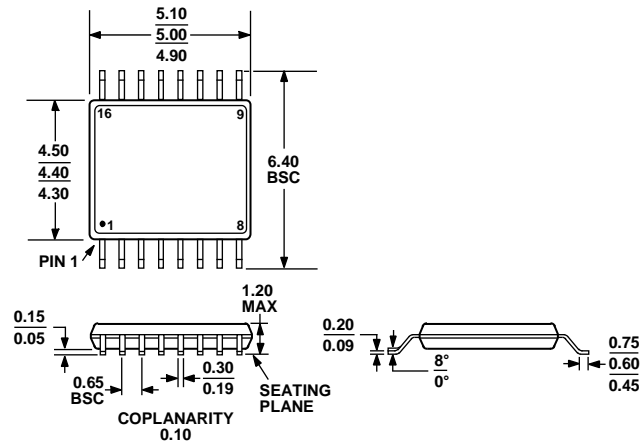
Figure 37. Trench Isolation

APPLICATIONS INFORMATION

The low capacitance latch-up immune family of switches and multiplexers provide a robust solution for instrumentation, industrial, automotive, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off.

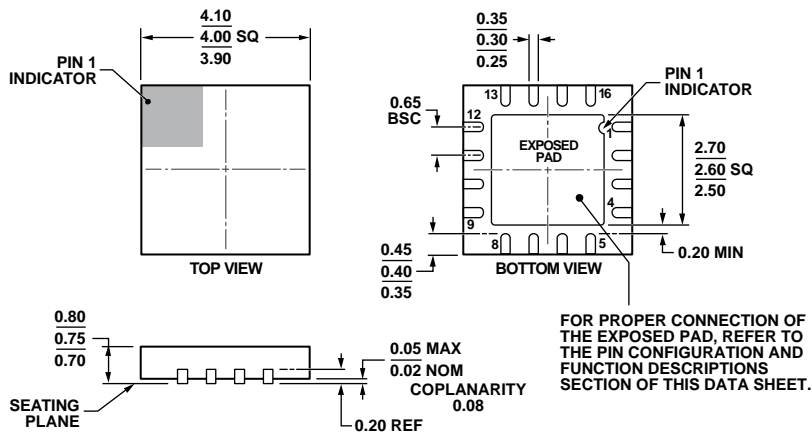
The [ADG5233/ADG5234](#) high voltage switches allow single-supply operation from 9 V to 40 V and dual supply operation from ± 9 V to ± 22 V.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

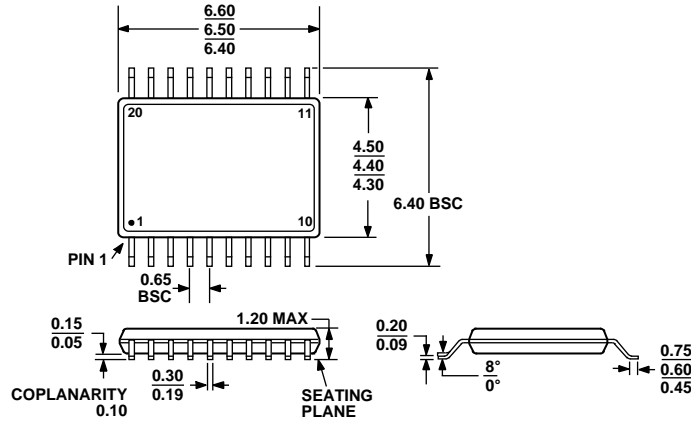
Figure 38. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 39. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] 4 mm x 4 mm Body, Very Very Thin Quad (CP-16-17)
Dimensions shown in millimeters

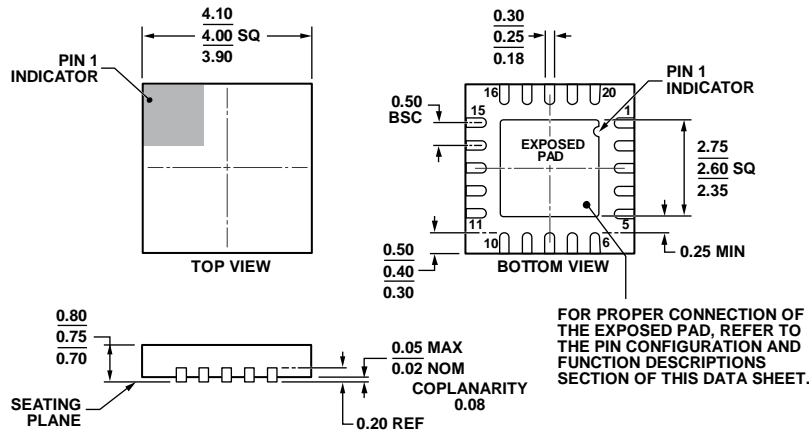
08-16-2010-C



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 40. 20-Lead Thin Shrink Small Outline Package [TSSOP] (RU-20)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD.

Figure 41. 20-LEAD LEAD FRAME CHIP SCALE PACKAGE [LFCSP_WQ] 4 mm x 4 mm BODY, VERY VERY THIN QUAD (CP-20-8)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Description | EN Pin | Package Option |
|--------------------|-------------------|---|--------|----------------|
| ADG5233BRUZ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | Yes | RU-16 |
| ADG5233BRUZ-RL7 | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | Yes | RU-16 |
| ADG5233BCPZ-RL7 | -40°C to +125°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | Yes | CP-16-17 |
| ADG5234BRUZ | -40°C to +125°C | 20-Lead Thin Shrink Small Outline Package [TSSOP] | No | RU-20 |
| ADG5234BRUZ-RL7 | -40°C to +125°C | 20-Lead Thin Shrink Small Outline Package [TSSOP] | No | RU-20 |
| ADG5234BCPZ-RL7 | -40°C to +125°C | 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | Yes | CP-20-8 |

¹ Z = RoHS Compliant Part.

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

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- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
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- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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JONHON

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Разъемы специального, военного и аэрокосмического назначения:

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ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



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