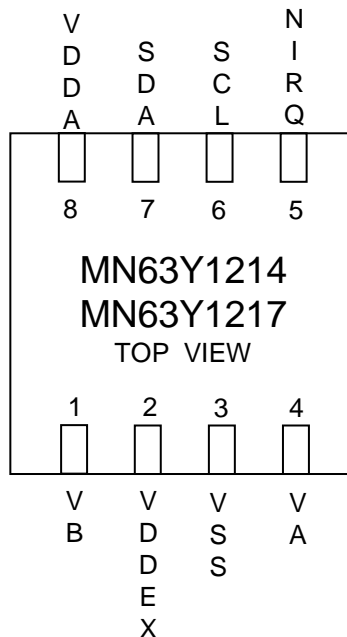


# **Evaluation board circuit diagram and implementation MN63Y1214/1217**

Ver. 1.1

Aug. 19, 2014

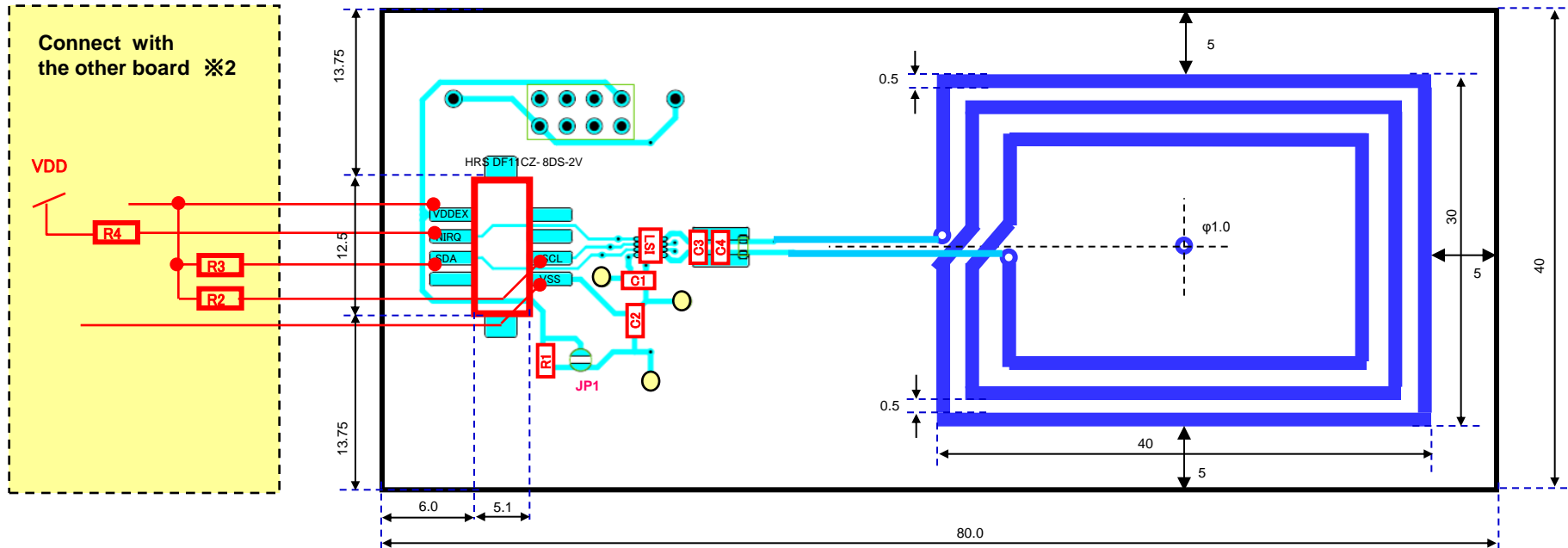
Sensing Systems Development Center  
Semiconductor Business Unit  
Panasonic Semiconductor Solutions Co.,Ltd.



Pin No.	Name	Input/Output	IO type	function
1	VB	I/O	---	Coil terminal
2	VDDEX	---	Power	External Power Supply
3	VSS	---	GND	Ground
4	VA	I/O	---	Coil terminal
5	NIRQ	Output	Open Drain	USE : Pull up to VDDEX NOT USE : Open or Connect to Ground
6	SCL	Input	---	I2C Clock input
7	SDA	I/O	Open Drain	I2C Data input/output. Pull up to VDDEX
8	VDDA	---	Power	Internal analog power supply (Connect a capacitor between this pin and VSS shortest as possible.)

■ ANT4030\_03\_0505\_B0\_L\_1214\_V0

Unit : mm

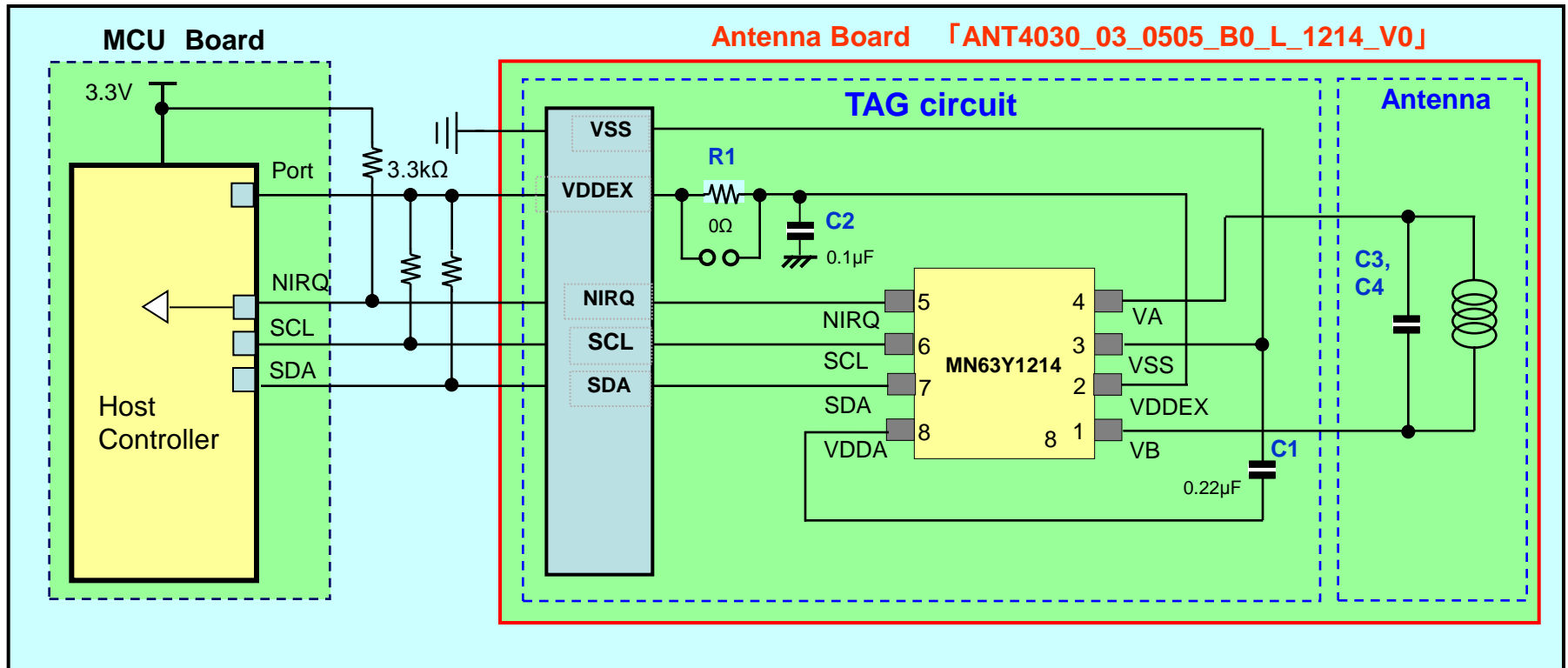
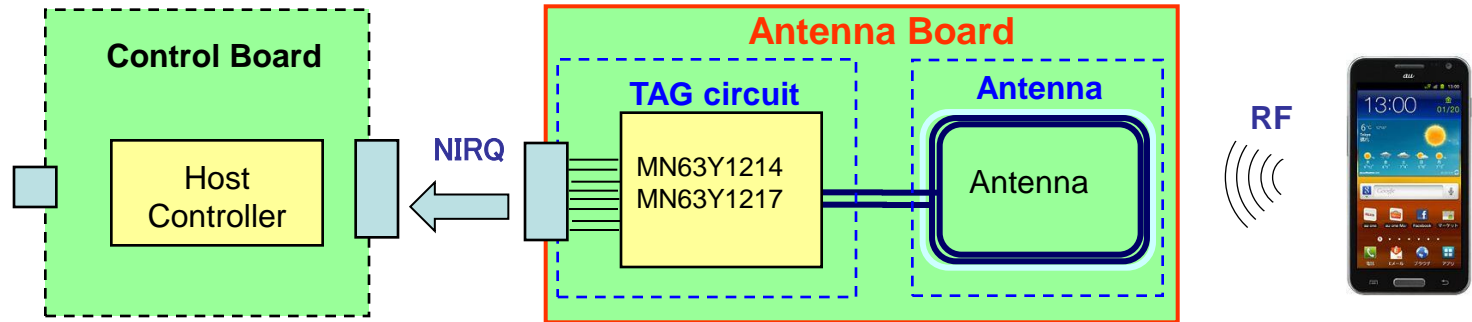


※ Substrate size may differ from the substrate which exists to a visitor.

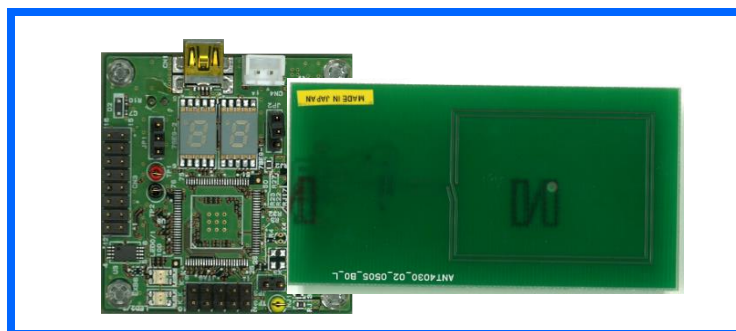
※ I connect pulling up resistance (R2,R3,R4) to the microcomputer board of our offer.

External parts	Recommended Value	Detail explanation
R2,R3	3.3kΩ	These are pull up resistor for I2C signal lines. Please choose the value considering data speed, parasitic capacitance of signal lines, and current drive performance. In our NFC tag board " ANT4030_03_0505_B0_L_1214_V0 " it is not implemented.
R4	3.3kΩ	This is pull up resistor for interrupt signal lines. Please choose the value considering data speed, parasitic capacitance of signal lines, and current drive performance. In our NFC tag board " ANT4030_03_0505_B0_L_1214_V0 " it is not implemented.
C1 C2	0.22μF 0.1μF	It is a fixed value at the capacity between the power supply for operation stabilization of the tag LSI. C1 is connected to VDDA, and C2 is connected to VDDEX.
C3, C4	-	It is Resonance capacity. The optimal values differ for every antenna design. It is connected VA to VB. In our NFC tag board " ANT4030_03_0505_B0_L_1214_V0 ", capacity C3=150pF, the C4=22pF has been implemented.
R1	-	In our NFC tag board " ANT4030_03_0505_B0_L_1214_V0 ", the resistance of R1=0Ω has been implemented.

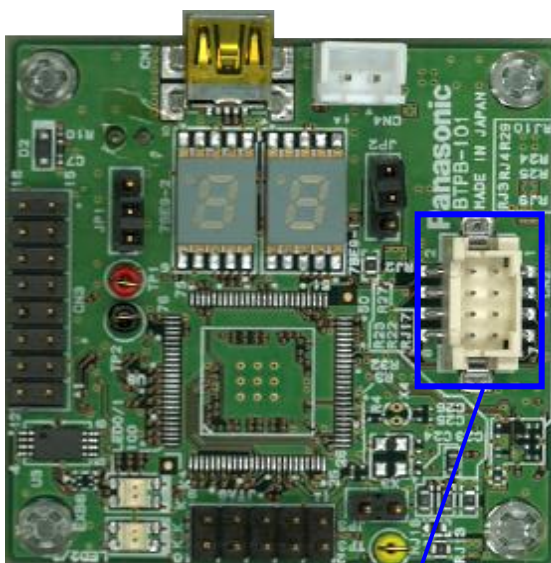
### NFC tag system constitution



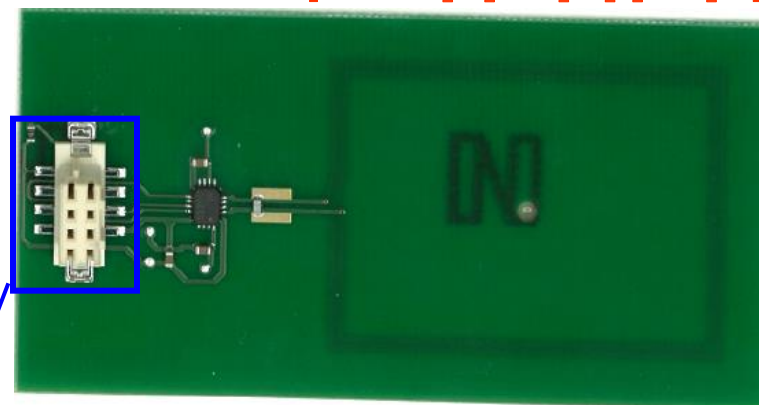
## Connection image (Top view)



Micon board [BTPB-101B]



Antenna board [ANT4030\_03\_0505\_B0\_L\_1214\_V0]

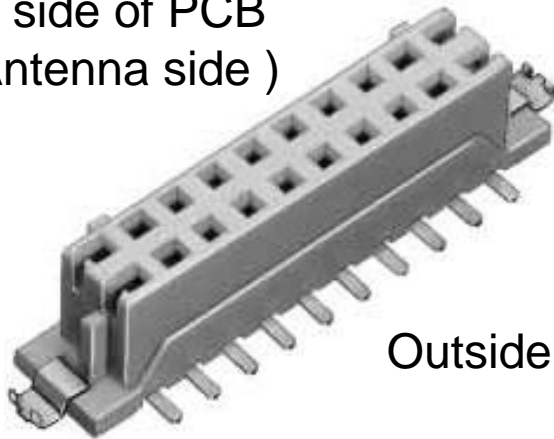
DF11CZ-8DP-2V(27)  
( Hirose Electric )

2		VSS	1
4	SDA	SCL	3
6	NIRQ		5
8	VDDEX		7

HRS DF11CZ- 8DS-2V  
( Hirose Electric )

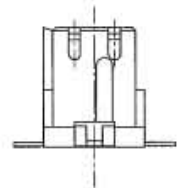
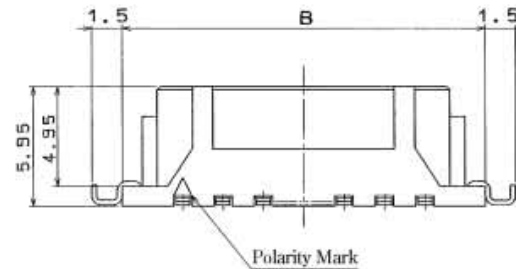
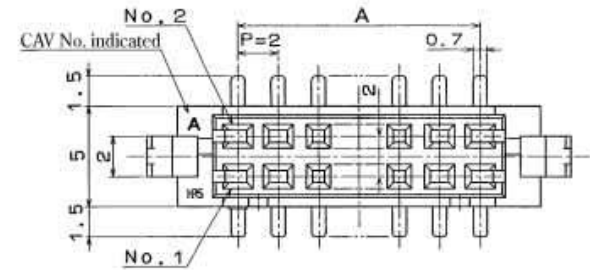
8	VDDEX		7
6	NIRQ		5
4	SDA	SCL	3
2		VSS	1

In side of PCB  
( Antenna side )



Outside of PCB

※Figure is an example



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