Features

- Supports AT&T TR62411 and Bellcore GR-1244-CORE Stratum 4 Enhanced and Stratum 4 timing for DS1 Interfaces
- Supports ETSI ETS 300 011, TBR 4, TBR 12 and TBR 13 timing for E1 Interfaces
- Selectable 1.544 MHz, 2.048 MHz or 8 kHz input reference signals
- Provides C1.5, C2, $\overline{C3}$, $\overline{C4}$, C8 and $\overline{C16}$ output clock signals
- Provides 3 different styles of 8 KHz framing pulses
- Attenuates wander from 1.9 Hz

Applications

- Synchronization and timing control for multitrunk T1 and E1 systems
- ST-BUS clock and frame pulse sources

March 2008

Ordering Information

MT9041BP1	28 Pin PLCC*	Tubes
MT9041BPR1	28 Pin PLCC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

Description

The MT9041B T1/E1 System Synchronizer contains a digital phase-locked loop (DPLL), which provides timing and synchronization signals for multitrunk T1 and E1 primary rate transmission links.

The MT9041B generates ST-BUS clock and framing signals that are phase locked to either a 2.048 MHz, 1.544 MHz, or 8 kHz input reference.

The MT9041B is compliant with AT&T TR62411 and Bellcore GR-1244-CORE Stratum 4 Enhanced, Stratum 4, and ETSI ETS 300 011. It will meet the jitter tolerance, jitter transfer, intrinsic jitter, frequency accuracy, capture range and phase change slope requirements for these specifications.

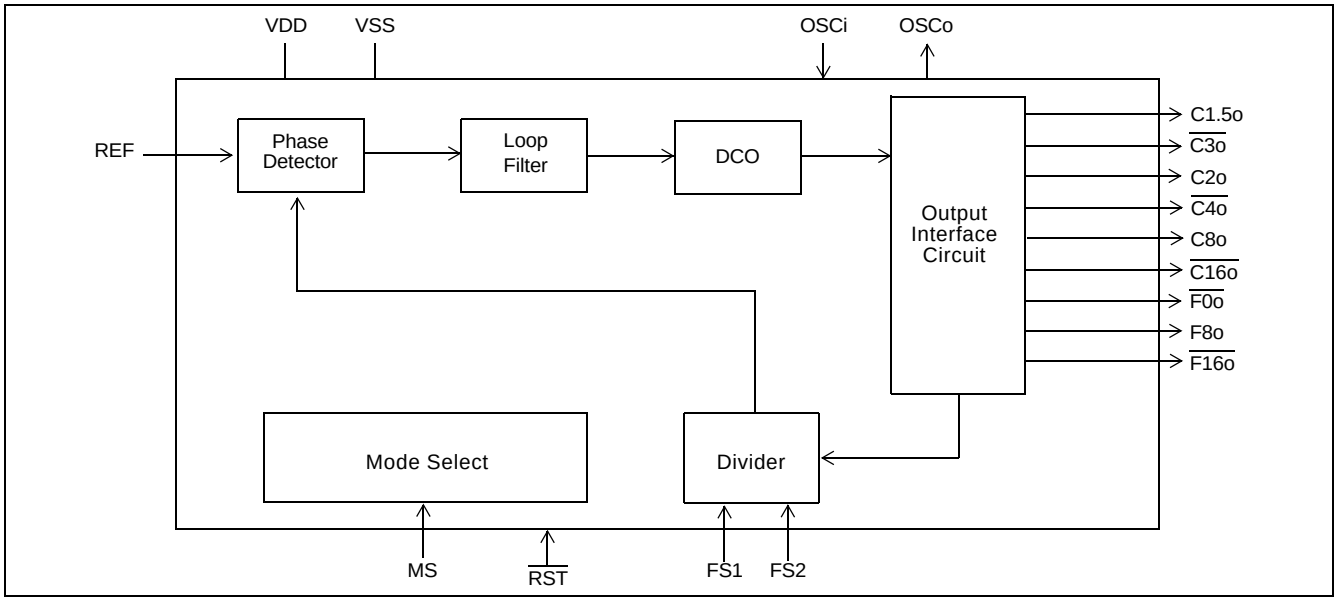


Figure 1 - Functional Block Diagram

Zarlink Semiconductor US Patent No. 5,602,884, UK Patent No. 0772912, France Brevete S.G.D.G. 0772912; Germany DBP No. 69502724.7-08

Change Summary

Changes from November 2005 Issue to March 2008 Issue. Page, section, figure and table numbers refer to this issue.

Page	Item	Change
1	Ordering Information	Updated ordering information.

Changes from November 2004 Issue to November 2005 Issue. Page, section, figure and table numbers refer to this issue.

Page	Item	Change
4	Pin Description - pin 28 $\overline{\text{RST}}$	The sentence "While the $\overline{\text{RST}}$ pin is low, all frame and clock outputs are at logic high." is changed to "While the $\overline{\text{RST}}$ pin is low, all frame and all clock outputs except $\overline{\text{C16o}}$ are at logic high; $\overline{\text{C16o}}$ is at logic low."

Changes from November 2003 Issue to November 2004 Issue. Page, section, figure and table numbers refer to this issue.

Page	Item	Change
14	Table "DC Electrical Characteristics" line item 7	Changed Minimum Schmitt high level input voltage V_{SIH} from 2.3 volts to 3.4 volts.

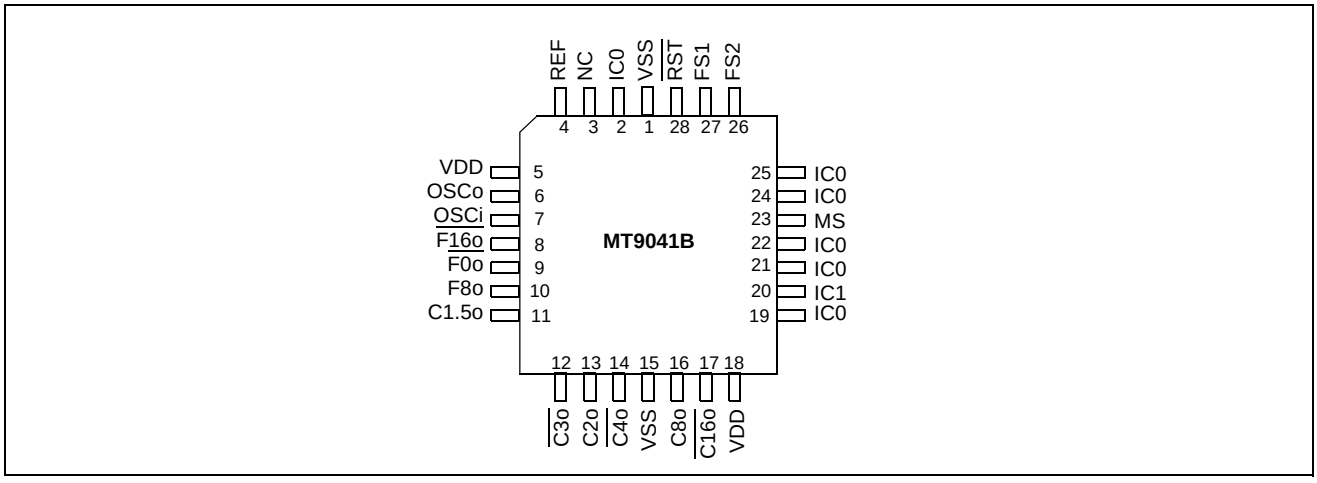


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	V_{SS}	**Ground.** 0 Volts.
2	IC0	**Internal Connect.** Connect to Vss
3	NC	**No Connect.** Connect to Vss
4	REF	**Reference (TTL Input).** PLL reference clock.
5	V_{DD}	**Positive Supply Voltage.** $+5V_{DC}$ nominal.
6	OSCo	**Oscillator Master Clock (CMOS Output).** For crystal operation, a 20 MHz crystal is connected from this pin to OSCi, see Figure 6. For clock oscillator operation, this pin is left unconnected, see Figure 5.
7	OSCi	**Oscillator Master Clock (CMOS Input).** For crystal operation, a 20 MHz crystal is connected from this pin to OSCo, see Figure 6. For clock oscillator operation, this pin is connected to a clock source, see Figure 5.
8	$\overline{F16o}$	**Frame Pulse ST-BUS 16.384 Mb/s (CMOS Output).** This is an 8 kHz 61 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 16.384 Mb/s. See Figure 11.
9	$\overline{F0o}$	**Frame Pulse ST-BUS 2.048 Mb/s (CMOS Output).** This is an 8 kHz 244 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048 Mb/s and 4.096 Mb/s. See Figure 11.
10	F8o	**Frame Pulse ST-BUS 8.192 Mb/s (CMOS Output).** This is an 8 kHz 122 ns active high framing pulse, which marks the beginning of an ST-BUS frame. This is used for ST-BUS operation at 8.192 Mb/s. See Figure 11.
11	C1.5o	**Clock 1.544 MHz (CMOS Output).** This output is used in T1 applications.
12	$\overline{C3o}$	**Clock 3.088 MHz (CMOS Output).** This optional output is used in T1 applications.
13	C2o	**Clock 2.048 MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048 Mb/s.
14	$\overline{C4o}$	**Clock 4.096 MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048 Mb/s and 4.096 Mb/s.
15	V_{SS}	**Ground.** 0 Volts.

Pin Description (continued)

Pin #	Name	Description
16	C8o	**Clock 8.192 MHz (CMOS Output).** This output is used for ST-BUS operation at 8.192 Mb/s.
17	$\overline{C16o}$	**Clock 16.384 MHz (CMOS Output).** This output is used for ST-BUS operation at 16.384 Mb/s.
18	V_{DD}	**Positive Supply Voltage.** +5V_{DC} nominal.
19	IC0	**Internal Connect.** Connect to Vss
20	IC1	**Internal Connect.** Leave open Circuit
21	IC0	**Internal Connect.** Connect to Vss
22	IC0	**Internal Connect.** Connect to Vss
23	MS	**Mode/Control Select (TTL Input).** This pin, determines the device's state (Normal, or Freerun) of operation. The logic level at this input is gated in by the rising edge of F8o. See Table 3.
24	IC0	**Internal Connect.** Connect to Vss
25	IC0	**Internal Connect.** Connect to Vss
26	FS2	**Frequency Select 2 (TTL Input).** This input, in conjunction with FS1, selects which of three possible frequencies (8 kHz, 1.544 MHz, or 2.048 MHz) may be input to the REF input. See Table 1.
27	FS1	**Frequency Select 1 (TTL Input).** See pin description for FS2.
28	$\overline{RST}$	**Reset (Schmitt Input).** A logic low at this input resets the MT9041B. To ensure proper operation, the device must be reset after reference signal frequency changes and power-up. The $\overline{RST}$ pin should be held low for a minimum of 300 ns. While the $\overline{RST}$ pin is low, all frame and all clock outputs except $\overline{C16o}$ are at logic high; $\overline{C16o}$ is at logic low. Following a reset, the input reference source and output clocks and frame pulses are phase aligned as shown in Figure 10.

Functional Description

The MT9041B is a System Synchronizer, providing timing (clock) and synchronization (frame) signals to interface circuits for T1 and E1 Primary Rate Digital Transmission links.

Figure 1 is a functional block diagram which is described in the following sections.

Frequency Select MUX Circuit

The MT9041B operates on the falling edges of one of three possible input reference frequencies (8 kHz, 1.544 MHz or 2.048 MHz). The frequency select inputs (FS1 and FS2) determine which of the three frequencies may be used at the reference input (REF). A reset ($\overline{RST}$) must be performed after every frequency select input change. Operation with FS1 and FS2 both at logic low is reserved and must not be used. See Table 1.

FS2	FS1	Input Frequency
0	0	Reserved
0	1	8kHz
1	0	1.544MHz
1	1	2.048MHz

Table 1 - Input Frequency Selection

Digital Phase Lock Loop (DPLL)

The DPLL of the MT9041B consists of a Phase Detector, Limiter, Loop Filter, Digitally Controlled Oscillator, and a Control Circuit (see Figure 3).

Phase Detector - the Phase Detector compares the primary reference signal (REF) with the feedback signal from the Frequency Select MUX circuit, and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the Limiter circuit. The Frequency Select MUX allows the proper feedback signal to be externally selected (e.g., 8 kHz, 1.544 MHz or 2.048 MHz).

Limiter - the Limiter receives the error signal from the Phase Detector and ensures that the DPLL responds to all input transient conditions with a maximum output phase slope of 5 ns per 125 us. This is well within the maximum phase slope of 7.6 ns per 125 us or 81 ns per 1.326 ms specified by Bellcore GR-1244-CORE Stratum 4E.

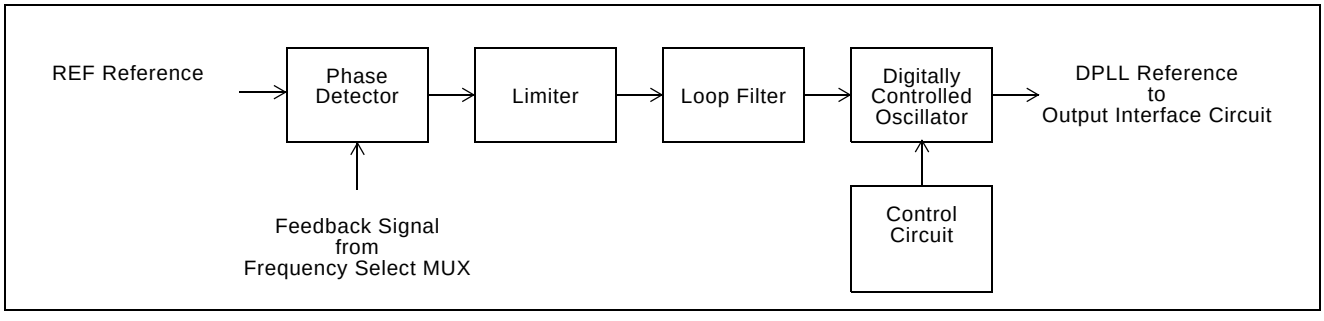


Figure 3 - DPLL Block Diagram

Loop Filter - the Loop Filter is similar to a first order low pass filter with a 1.9 Hz cutoff frequency for all three reference frequency selections (8 kHz, 1.544 MHz or 2.048 MHz). This filter ensures that the jitter transfer requirements in ETS 300 011 and AT&T TR62411 are met.

Control Circuit - the Control Circuit sets the mode of the DPLL. The two possible modes are Normal and Freerun.

Digitally Controlled Oscillator (DCO) - the DCO receives the limited and filtered signal from the Loop FIlter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the MT9041B.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the OSCi 20 MHz source.

Output Interface Circuit

The output of the DCO (DPLL) is used by the Output Interface Circuit to provide the output signals shown in Figure 4. The Output Interface Circuit uses two Tapped Delay Lines followed by a T1 Divider Circuit and an E1 Divider Circuit to generate the required output signals.

Two tapped delay lines are used to generate a 16.384 MHz and a 12.352 MHz signals.

The E1 Divider Circuit uses the 16.384 MHz signal to generate four clock outputs and three frame pulse outputs. The C8o, $\overline{\text{C4o}}$ and C2o clocks are generated by simply dividing the $\overline{\text{C16o}}$ clock by two, four and eight respectively. These outputs have a nominal 50% duty cycle.

The T1 Divider Circuit uses the 12.384 MHz signal to generate two clock outputs. C1.5o and $\overline{\text{C3o}}$ are generated by dividing the internal C12 clock by four and eight respectively. These outputs have a nominal 50% duty cycle.

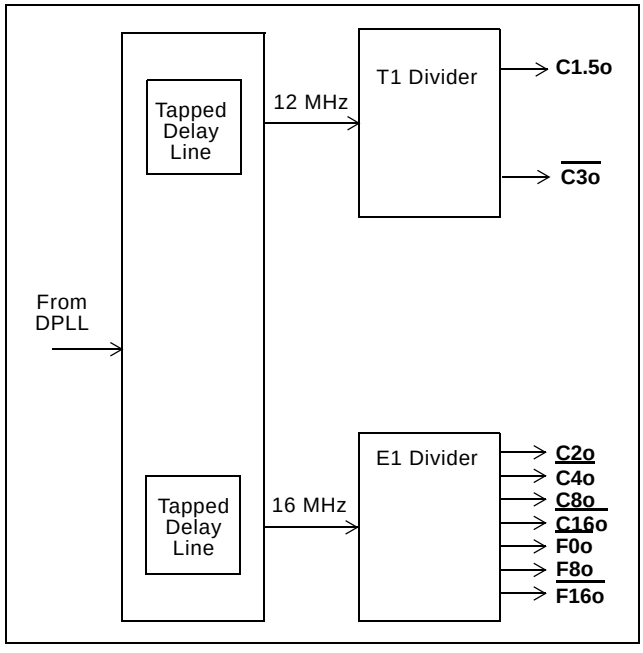


Figure 4 - Output Interface Circuit Block Diagram

The frame pulse outputs ($\overline{F0o}$, F8o, $\overline{F16o}$) are generated directly from the $\overline{C16}$ clock.

The T1 and E1 signals are generated from a common DPLL signal. Consequently, the clock outputs C1.5o, $\overline{C3o}$, C2o, $\overline{C4o}$, C8o, $\overline{C16o}$, $\overline{F0o}$ and $\overline{F16o}$ are locked to one another for all operating states, and are also locked to the selected input reference in Normal Mode. See Figures 11 and 12.

All frame pulse and clock outputs have limited driving capability, and should be buffered when driving high capacitance (e.g., 30 pF) loads.

Master Clock

The MT9041B can use either a clock or crystal as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

Control and Modes of Operation

The MT9041B can operate either in Normal or Freerun modes.

As shown in Table 2, pin MS selects between NORMAL and FREERUN modes.

MS	Description of Operation
0	NORMAL
1	FREERUN

Table 2 - Operating Modes

Normal Mode

Normal Mode is typically used when a slave clock source synchronized to the network is required.

In Normal Mode, the MT9041B provides timing (C1.5o, C2o, $\overline{\text{C3o}}$, $\overline{\text{C4o}}$, C8o and $\overline{\text{C16o}}$) and frame synchronization ($\overline{\text{F0o}}$, F8o, $\overline{\text{F16o}}$) signals, which are synchronized to reference input (REF). The input reference signal may have a nominal frequency of 8 kHz, 1.544 MHz or 2.048 MHz.

From a reset condition, the MT9041B will take up to 25 seconds for the output signal to be phase locked to the reference.

The reference frequencies are selected by the frequency control pins FS2 and FS1 as shown in Table 1.

Freerun Mode

Freerun Mode is typically used when a master clock source is required, or immediately following system power-up before network synchronization is achieved.

In Freerun Mode, the MT9041B provides timing and synchronization signals which are based on the master clock frequency (OSCi) only, and are not synchronized to the reference signal (REF).

The accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a ±32 ppm output clock is required, the master clock must also be ±32 ppm. See Applications - Crystal and Clock Oscillator sections.

MT9041B Measures of Performance

The following are some synchronizer performance indicators and their corresponding definitions.

Intrinsic Jitter

Intrinsic jitter is the jitter produced by the synchronizing circuit and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is in a non-synchronizing mode, i.e. free running mode, by measuring the output jitter of the device. Intrinsic jitter is usually measured with various bandlimiting filters depending on the applicable standards.

Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock and or regain lock), in the presence of large jitter magnitudes at various jitter frequencies applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards.

Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

For the MT9041B, two internal elements determine the jitter attenuation. This includes the internal 1.9 Hz low pass loop filter and the phase slope limiter. The phase slope limiter limits the output phase slope to 5 ns/125 us. Therefore, if the input signal exceeds this rate, such as for very large amplitude low frequency input jitter, the maximum output phase slope will be limited (i.e., attenuated) to 5 ns/125 us.

The MT9041B has nine outputs with three possible input frequencies for a total of 27 possible jitter transfer functions. However, the data sheet section on AC Electrical Characteristics - Jitter Transfer specifies transfer values for only three cases, 8 kHz to 8 kHz, 1.544 MHz to 1.544 MHz and 2.048 MHz to 2.048 MHz. Since all outputs are derived from the same signal, these transfer values apply to all outputs.

It should be noted that 1 UI at 1.544 MHz is 644 ns, which is not equal to 1 UI at 2.048 MHz, which is 488 ns. Consequently, a transfer value using different input and output frequencies must be calculated in common units (e.g., seconds) as shown in the following example.

What is the T1 and E1 output jitter when the T1 input jitter is 20UI (T1 UI Units) and the T1 to T1 jitter attenuation is 18dB?

$$OutputT1 = InputT1 \times 10^{\left(\frac{-A}{20}\right)}$$

$$OutputT1 = 20 \times 10^{\left(\frac{-18}{20}\right)} = 2.5UI(T1)$$

$$OutputE1 = OutputT1 \times \frac{(1UIT1)}{(1UIE1)}$$

$$OutputE1 = OutputT1 \times \frac{(644ns)}{(488ns)} = 3.3UI(T1)$$

Using the above method, the jitter attenuation can be calculated for all combinations of inputs and outputs based on the three jitter transfer functions provided.

Note that the resulting jitter transfer functions for all combinations of inputs (8 kHz, 1.544 MHz, 2.048 MHz) and outputs (8 kHz, 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz) for a given input signal (jitter frequency and jitter amplitude) are the same.

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

Frequency Accuracy

Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the MT9041B, the Freerun accuracy is equal to the Master Clock (OSCi) accuracy.

Capture Range

Also referred to as pull-in range. This is the input frequency range over which the synchronizer must be able to pull into synchronization. The MT9041B capture range is equal to ±230 ppm minus the accuracy of the master clock (OSCi). For example, a ±32 ppm master clock results in a capture range of ±198 ppm.

Lock Range

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the MT9041B.

Phase Slope

Phase slope is measured in seconds per second and is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. The ideal signal is of constant frequency and is nominally equal to the value of the final output signal or final input signal.

Phase Continuity

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the synchronizer after a signal disturbance due to a reference switch or a mode change. The observation period is usually the time from the disturbance, to just after the synchronizer has settled to a steady state.

In the case of the MT9041B, the output signal phase continuity is maintained to within ±5 ns at the instance (over one frame) of mode changes. The total phase shift may accumulate up to ±200 ns over many frames. The rate of change of the ±200 ns phase shift is limited to a maximum phase slope of approximately 5 ns/125 us. This meets the Bellcore GR-1244-CORE maximum phase slope requirement of 7.6 ns/125 us (81 ns/1.326 ms).

Phase Lock Time

This is the time it takes the synchronizer to phase lock to the input signal. Phase lock occurs when the input signal and output signal are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors which include:

i) initial input to output phase difference
ii) initial input to output frequency difference
iii) synchronizer loop filter
iv) synchronizer limiter

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. And better (smaller) phase slope performance (limiter) results in longer lock times. The MT9041B loop filter and limiter were optimized to meet the AT&T TR62411 jitter transfer and phase slope requirements. Consequently, phase lock time, which is not a standards requirement, may be longer than in other applications. See AC Electrical Characteristics - Performance for maximum phase lock time.

MT9041B and Network Specifications

The MT9041B fully meets all applicable PLL requirements (intrinsic jitter, jitter tolerance, jitter transfer, frequency accuracy, capture range and phase change slope) for the following specifications.

1. Bellcore GR-1244-CORE Issue 1, June 1995 for Stratum 4 Enhanced and Stratum 4
2. AT&T TR62411 (DS1) December 1990 for Stratum 4 Enhanced and Stratum 4
3. ANSI T1.101 (DS1) February 1994 for Stratum 4 Enhanced and Stratum 4
4. ETSI 300 011 (E1) April 1992 for Single Access and Multi Access
5. TBR 4 November 1995
6. TBR 12 December 1993
7. TBR 13 January 1996
8. ITU-T I.431 March 1993

Applications

This section contains MT9041B application specific details for clock and crystal operation, reset operation and power supply decoupling.

Master Clock

The MT9041B can use either a clock or crystal as the master timing source.

In Freerun Mode, the frequency tolerance at the clock outputs is identical to the frequency tolerance of the source at the OSCi pin. For applications not requiring an accurate Freerun Mode, tolerance of the master timing source may be ±100 ppm. For applications requiring an accurate Freerun Mode, such as Bellcore GR-1244-CORE, the tolerance of the master timing source must be no greater than ±32 ppm.

Another consideration in determining the accuracy of the master timing source is the desired capture range. The sum of the accuracy of the master timing source and the capture range of the MT9041B will always equal ±230 ppm. For example, if the master timing source is ±100 ppm, then the capture range will be ±130 ppm.

Clock Oscillator - when selecting a Clock Oscillator, numerous parameters must be considered. These include absolute frequency, frequency change over temperature, output rise and fall times, output levels and duty cycle. See AC Electrical Characteristics.

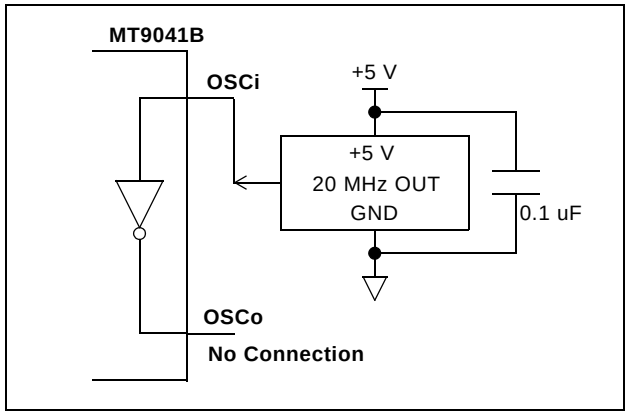


Figure 5 - Clock Oscillator Circuit

For applications requiring ±32 ppm clock accuracy, the following clock oscillator module may be used.

CTS CXO-65-HG-5-C-20.0 MHz

Frequency:	*20 MHz*
Tolerance:	*25 ppm 0C to 70C*
Rise & Fall Time:	*8 ns (0.5 V 4.5 V 50 pF)*
Duty Cycle:	*45% to 55%*

The output clock should be connected directly (not AC coupled) to the OSCi input of the MT9041B, and the OSCo output should be left open as shown in Figure 5.

Crystal Oscillator - Alternatively, a Crystal Oscillator may be used. A complete oscillator circuit made up of a crystal, resistor and capacitors is shown in Figure 6.

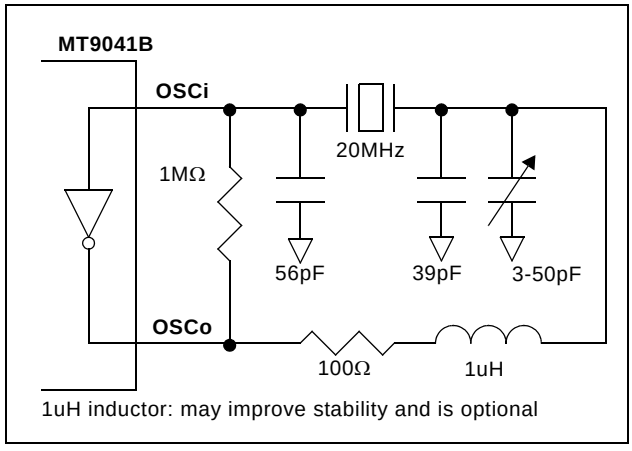


Figure 6 - Crystal Oscillator Circuit

The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 20 MHz crystal specified with a 32 pF load capacitance, each 1 pF change in load capacitance contributes approximately 9 ppm to the frequency deviation. Consequently, capacitor tolerances, and stray capacitances have a major effect on the accuracy of the oscillator frequency.

The trimmer capacitor shown in Figure 6 may be used to compensate for capacitive effects. If accuracy is not a concern, then the trimmer may be removed, the 39 pF capacitor may be increased to 56 pF, and a wider tolerance crystal may be substituted.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. The crystal specification is as follows.

Frequency:	*20 MHz*
Tolerance:	*As required*
Oscillation Mode:	*Fundamental*
Resonance Mode:	*Parallel*
Load Capacitance:	*32 pF*
Maximum Series Resistance:	*35 Ω*
Approximate Drive Level:	*1 mW*

e.g., CTS R1027-2BB-20.0MHZ

(±20 ppm absolute, ±6 ppm 0C to 50C, 32 pF, 25 Ω)

Reset Circuit

A simple power up reset circuit with about a 50 us reset low time is shown in Figure 7. Resistor R_P is for protection only and limits current into the $\overline{RST}$ pin during power down conditions. The reset low time is not critical but should be greater than 300 ns.

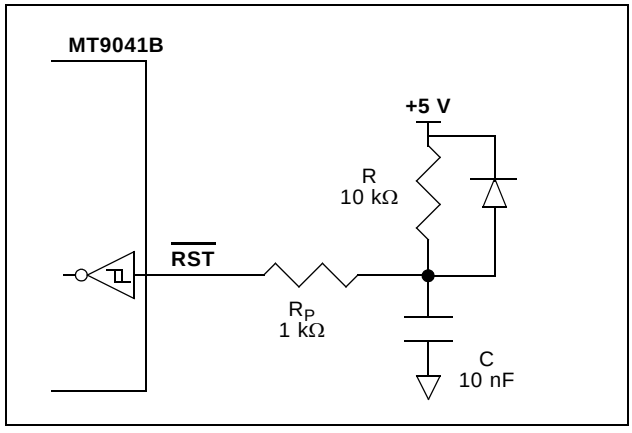


Figure 7 - Power-Up Reset Circuit

Power Supply Decoupling

The MT9041B has two VDD (+5 V) pins and two VSS (GND) pins. Power and decoupling capacitors should be included as shown in Figure 8.

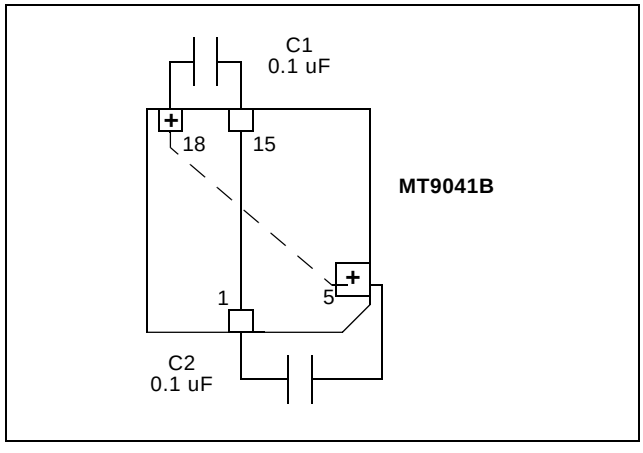


Figure 8 - Power Supply Decoupling

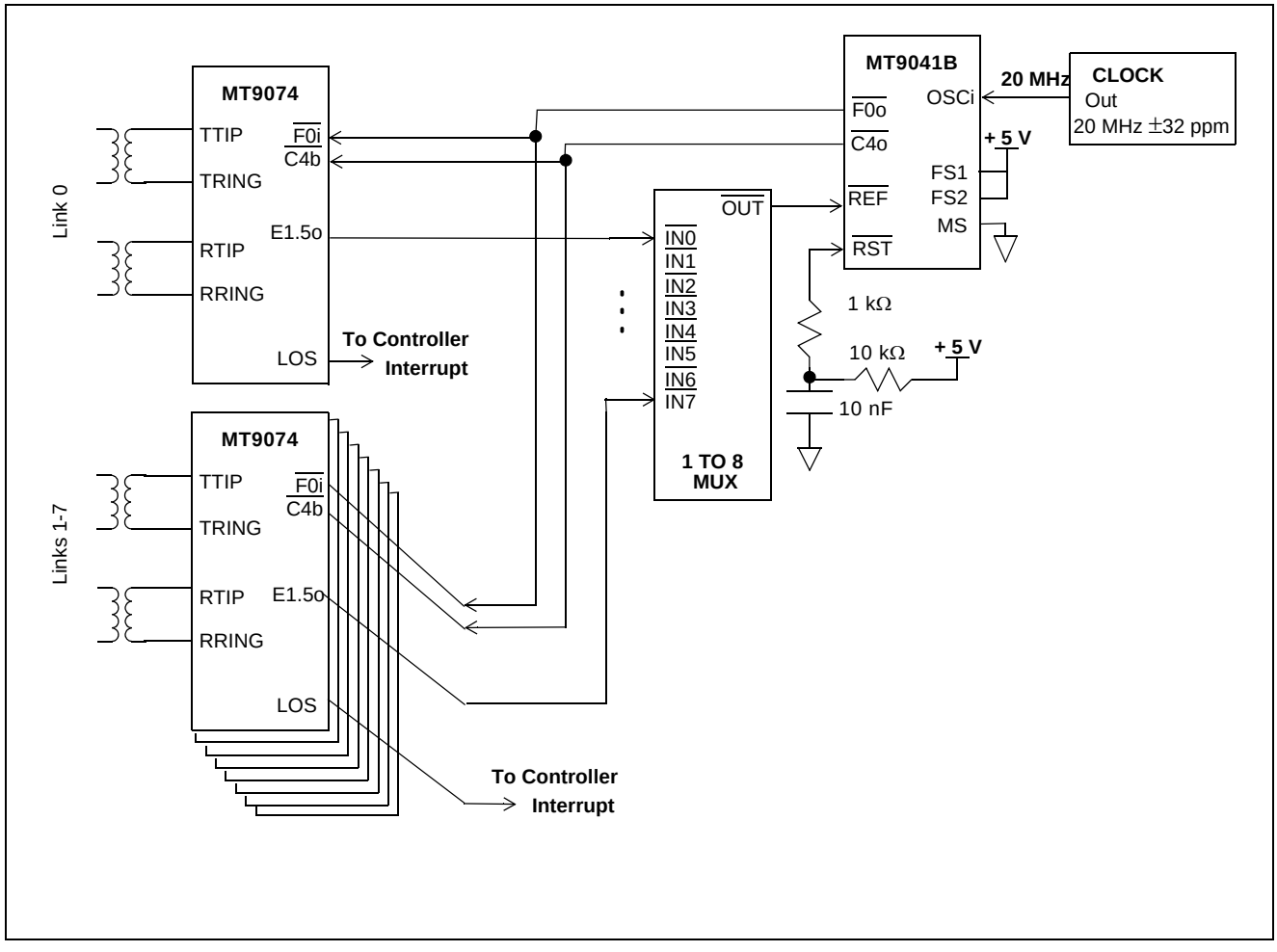


Figure 9 - Multiple E1 Reference Sources with MT9041B

Multiple E1 Reference Sources with MT9041B

In this example 8 E1 link framers (MT9074) are connected to a common system backplane clock using the MT9041B. Each of the extracted clocks E1.5o go to a mux which selects one of the eight input clocks as the reference to the MT9041B. The clock choice is made by a controller using the loss of signal pin LOS from the MT9074s to qualify potential references. In the event of loss of signal by one of the framers, an interrupt signals the controller to choose a different reference clock. Disturbances in the generated system backplane clocks C4b and F0b are minimized by the phase slope limitations of the MT9041B PLL. This ensures system integrity and minimizes the effect of clock switchover on downstream trunks.

Absolute Maximum Ratings* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD}	-0.3	7.0	V
2	Voltage on any pin	V_{PIN}	-0.3	V_{DD}+0.3	V
3	Current on any pin	I_{PIN}		20	mA
4	Storage temperature	T_{ST}	-55	125	°C
5	PLCC package power dissipation	P_{PD}		900	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (VSS) unless otherwise stated

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD}	4.5	5.0	5.5	V
2	Operating temperature	T_A	-40	25	85	°C

DC Electrical Characteristics* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Max.	Units	Conditions/Notes
1	Supply current with:OSCi = 0V	I_{DDS}		0.5	mA	Outputs unloaded
2	OSCi = Clock	I_{DD}		60	mA	Outputs unloaded
3	TTL high-level input voltage	V_{IH}	2.0		V	
4	TTL low-level input voltage	V_{IL}		0.8	V	
5	CMOS high-level input voltage	V_{CIH}	$0.7V_{DD}$		V	OSCi
6	CMOS low-level input voltage	V_{CIL}		$0.3V_{DD}$	V	OSCi
7	Schmitt high-level input voltage	V_{SIH}	3.4		V	$\overline{RST}$ Note the typical value is 3.1 volts at V_{DD} = 5.0 volts
8	Schmitt low-level input voltage	V_{SIL}		0.8	V	$\overline{RST}$
9	Schmitt hysteresis voltage	V_{HYS}	0.4		V	$\overline{RST}$
10	Input leakage current	I_{IL}	-50	+50	µA	V_I=V_{DD} or 0 V
11	High-level output voltage	V_{OH}	2.4V		V	I_{OH}=10 mA
12	Low-level output voltage	V_{OL}		0.4V	V	I_{OL}=10 mA

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

AC Electrical Characteristics - Performance

	Characteristics	Sym.	Min.	Max.	Units	Conditions/Notes†
1	Freerun Mode accuracy with OSCi at: 0ppm		-0	+0	ppm	2-5
2	±32 ppm		-32	+32	ppm	2-5
3	±100 ppm		-100	+100	ppm	2-5
4	Capture range with OSCi at: ±0 ppm		-230	+230	ppm	1,3-5,37
5	±32 ppm		-198	+198	ppm	1,3-5, 37
6	±100 ppm		-130	+130	ppm	1,3-5,37
7	Phase lock time			30	s	1, 3-11
8	Output phase continuity with:					
9	mode switch to Normal			200	ns	1-11
10	mode switch to Freerun			200	ns	1, 3-11
11	Output phase slope			45	us/s	1-11, 24

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels* - Voltages are with respect to ground (VSS) unless otherwise stated

	Characteristics	Sym.	Schmitt	TTL	CMOS	Units
1	Threshold Voltage	V_T	1.5	1.5	$0.5V_{DD}$	V
2	Rise and Fall Threshold Voltage High	V_{HM}	2.3	2.0	$0.7V_{DD}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	0.8	0.8	$0.3V_{DD}$	V

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Timing for input and output signals is based on the worst Chislehurst of the combination of TTL and CMOS thresholds.
* See Figure 10.

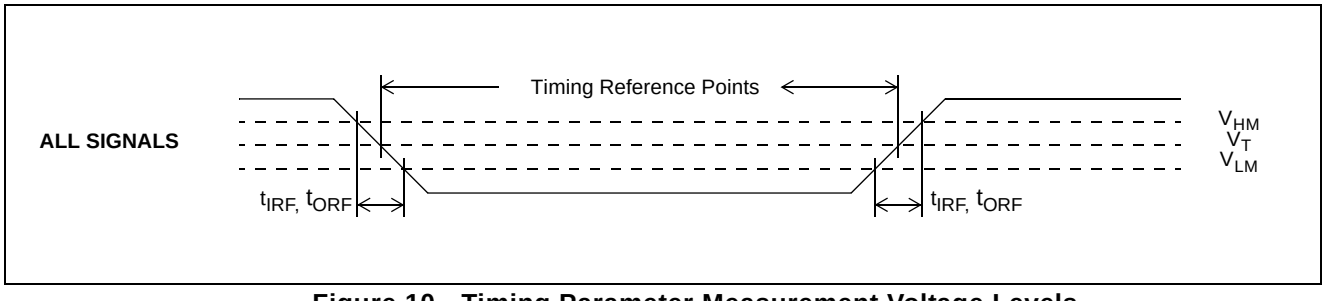
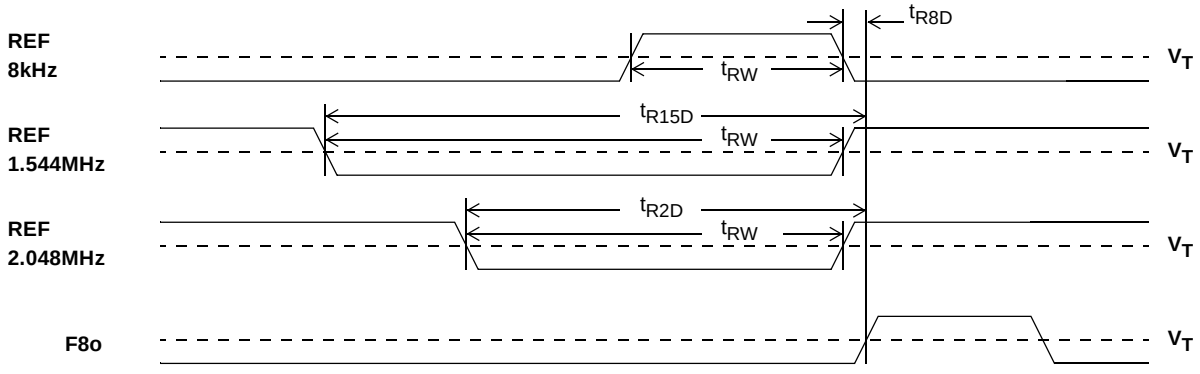


Figure 10 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics - Input/Output Timing

	Characteristics	Sym.	Min.	Max.	Units
1	Reference input pulse width high or low	t_{RW}	100		ns
2	Reference input rise or fall time	t_{IRF}		10	ns
3	8 kHz reference input to F8o delay	t_{R8D}	-21	6	ns
4	1.544 MHz reference input to F8o delay	t_{R15D}	337	363	ns
5	2.048 MHz reference input to F8o delay	t_{R2D}	222	238	ns
6	F8o to $\overline{\text{F0o}}$ delay	t_{F0D}	110	134	ns
7	$\overline{\text{F16o}}$ setup to $\overline{\text{C16o}}$ falling	t_{F16S}	11	35	ns
8	$\overline{\text{F16o}}$ hold from $\overline{\text{C16o}}$ rising	t_{F16H}	0	20	ns
9	F8o to C1.5o delay	t_{C15D}	-51	-37	ns
10	F8o to $\overline{\text{C3o}}$ delay	t_{C3D}	-51	-37	ns
11	F8o to C2o delay	t_{C2D}	-13	2	ns
12	F8o to $\overline{\text{C4o}}$ delay	t_{C4D}	-13	2	ns
13	F8o to C8o delay	t_{C8D}	-13	2	ns
14	F8o to $\overline{\text{C16o}}$ delay	t_{C16D}	-13	2	ns
15	C1.5o pulse width high or low	t_{C15W}	309	339	ns
16	$\overline{\text{C3o}}$ pulse width high or low	t_{C3W}	149	175	ns
17	C2o pulse width high or low	t_{C2W}	230	258	ns
18	$\overline{\text{C4o}}$ pulse width high or low	t_{C4W}	111	133	ns
19	C8o pulse width high or low	t_{C8W}	52	70	ns
20	$\overline{\text{C16o}}$ pulse width high or low	t_{C16WL}	24	35	ns
21	$\overline{\text{F0o}}$ pulse width low	t_{F0WL}	230	258	ns
22	F8o pulse width high	t_{F8WH}	111	133	ns
23	$\overline{\text{F16o}}$ pulse width low	t_{F16WL}	52	70	ns
24	Output clock and frame pulse rise or fall time	t_{ORF}		9	ns
25	Input Controls Setup Time	t_S	100		ns
26	Input Controls Hold Time	t_H	100		ns

† See "Notes" following AC Electrical Characteristics tables.



NOTES:

1. Input to output delay values are valid after a $\overline{TRST}$ or $\overline{RST}$ with no further state changes

Figure 11 - Input to Output Timing (Normal Mode)

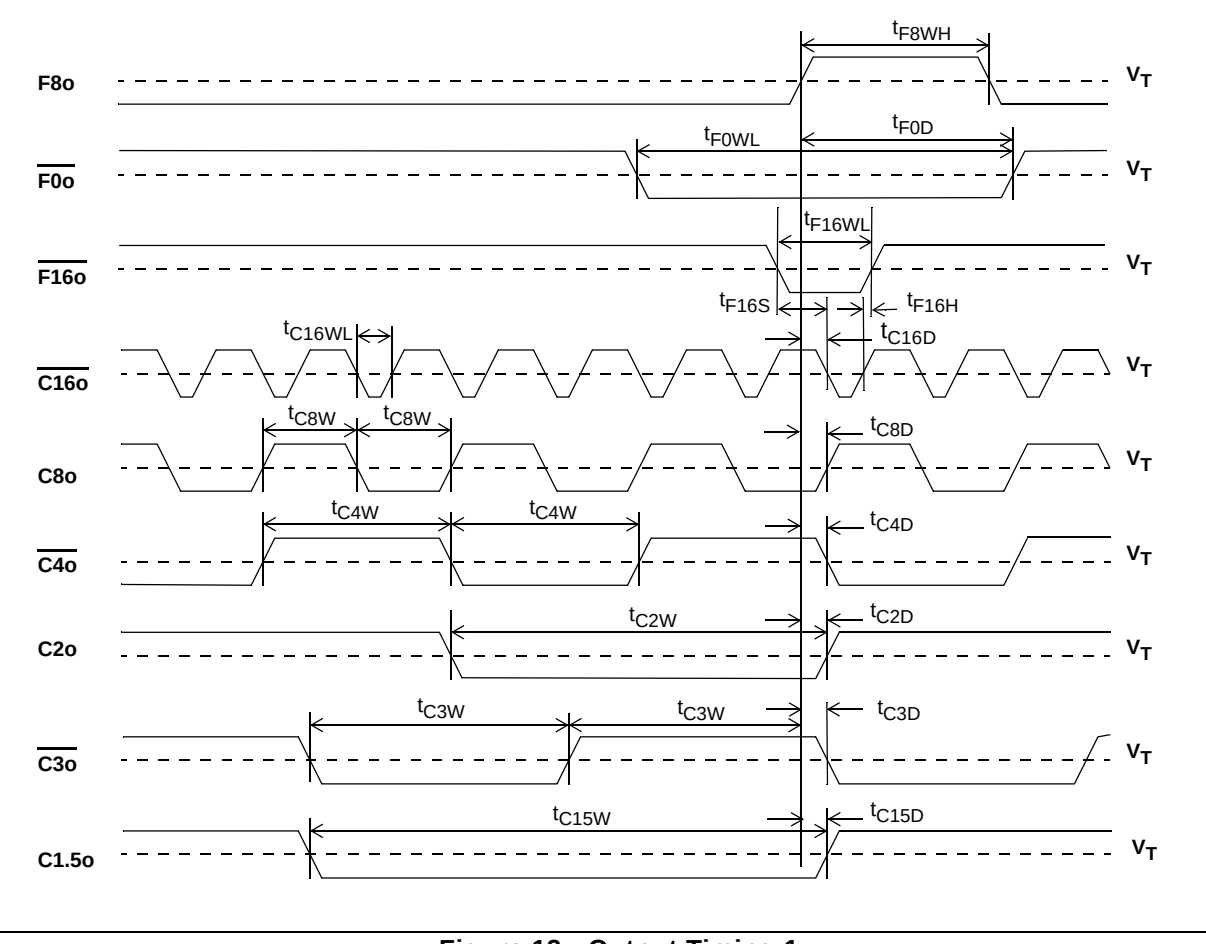


Figure 12 - Output Timing 1

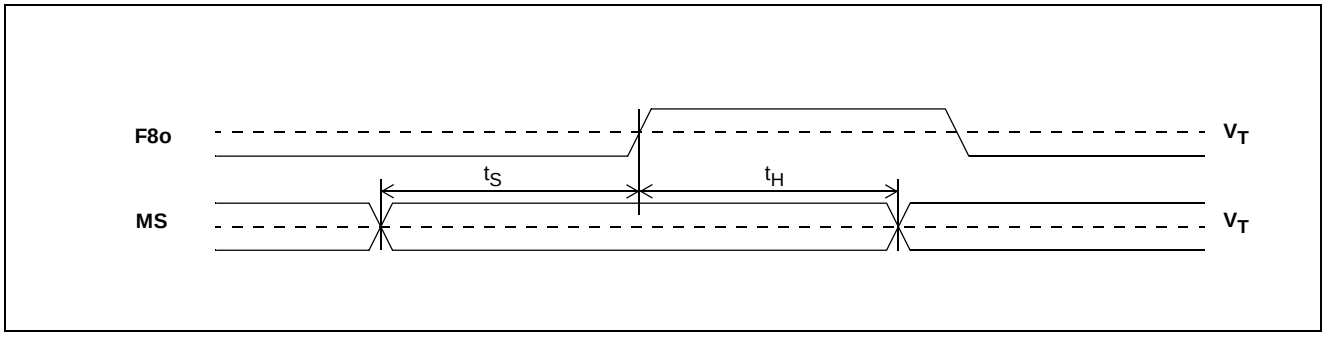


Figure 13 - Input Controls Setup and Hold Timing

AC Electrical Characteristics - Intrinsic Jitter Unfiltered

	Characteristics	Sym.	Min.	Max.	Units	Conditions/Notes†
1	Intrinsic jitter at F8o (8 kHz)			0.0002	UIpp	1-11,18-21,25
2	Intrinsic jitter at $\overline{\text{F0o}}$ (8 kHz)			0.0002	UIpp	1-11,18-21,25
3	Intrinsic jitter at $\overline{\text{F16o}}$ (8 kHz)			0.0002	UIpp	1-11,18-21,25
4	Intrinsic jitter at C1.5o (1.544 MHz)			0.030	UIpp	1-11,18-21,26
5	Intrinsic jitter at C2o (2.048 MHz)			0.040	UIpp	1-11,18-21,27
6	Intrinsic jitter at $\overline{\text{C3o}}$ (3.088 MHz)			0.060	UIpp	1-11,18-21,28
7	Intrinsic jitter at $\overline{\text{C4o}}$ (4.096 MHz)			0.080	UIpp	1-11,18-21,29
8	Intrinsic jitter at C8o (8.192 MHz)			0.160	UIpp	1-11,18-21,30
9	Intrinsic jitter at $\overline{\text{C16o}}$ (16.384 MHz)			0.320	UIpp	1-11,18-21,33

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - C1.5o (1.544 MHz) Intrinsic Jitter Filtered

	Characteristics	Sym.	Min.	Max.	Units	Conditions/Notes†
1	Intrinsic jitter (4 Hz to 100 kHz filter)			0.015	UIpp	1-11,18-21,26
2	Intrinsic jitter (10 Hz to 40 kHz filter)			0.010	UIpp	1-11,18-21,26
3	Intrinsic jitter (8 kHz to 40 kHz filter)			0.010	UIpp	1-11,18-21,26
4	Intrinsic jitter (10 Hz to 8 kHz filter)			0.005	UIpp	1-11,18-21,26

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - C2o (2.048 MHz) Intrinsic Jitter Filtered

	Characteristics	Sym.	Min.	Max.	Units	Conditions/Notes†
1	Intrinsic jitter (4 Hz to 100 kHz filter)			0.015	UIpp	1-11, 18-21, 27
2	Intrinsic jitter (10 Hz to 40 kHz filter)			0.010	UIpp	1-11, 18-21, 27
3	Intrinsic jitter (8 kHz to 40 kHz filter)			0.010	UIpp	1-11, 18-21, 27
4	Intrinsic jitter (10 Hz to 8 kHz filter)			0.005	UIpp	1-11, 18-21, 27

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 8 kHz Input to 8 kHz Output Jitter Transfer

	Characteristics	Sym.	Min.	Max.	Units	Conditions/Notes†
1	Jitter attenuation for 1 Hz@0.01 UIpp input		0	6	dB	1,3,6-11,18-19,21,25,32
2	Jitter attenuation for 1 Hz@0.54 UIpp input		6	16	dB	1,3,6-11,18-19,21,25,32
3	Jitter attenuation for 10 Hz@0.10 UIpp input		12	22	dB	1,3,6-11,18-19,21,25,32
4	Jitter attenuation for 60 Hz@0.10 UIpp input		28	38	dB	1,3,6-11,18-19,21,25,32
5	Jitter attenuation for 300 Hz@0.10 UIpp input		42		dB	1,3,6-11,18-19,21,25,32
6	Jitter attenuation for 3600 Hz@0.005 UIpp input		45		dB	1,3,6-11,18-19,21,25,32

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 1.544 MHz Input to 1.544 MHz Output Jitter Transfer

	Characteristics	Sym.	Min.	Max.	Units	Conditions/Notes†
1	Jitter attenuation for 1 Hz@20 UIpp input		0	6	dB	1,4,6-11,18-19,21,26,32
2	Jitter attenuation for 1 Hz@104 UIpp input		6	16	dB	1,4,6-11,18-19,21,26,32
3	Jitter attenuation for 10 Hz@20 UIpp input		12	22	dB	1,4,6-11,18-19,21,26,32
4	Jitter attenuation for 60 Hz@20 UIpp input		28	38	dB	1,4,6-11,18-19,21,26,32
5	Jitter attenuation for 300 Hz@20 UIpp input		42		dB	1,4,6-11,18-19,21,26,32
6	Jitter attenuation for 10 kHz@0.3 UIpp input		45		dB	1,4,6-11,18-19,21,26,32
7	Jitter attenuation for 100 kHz@0.3 UIpp input		45		dB	1,4,6-11,18-19,21,26,32

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 2.048 MHz Input to 2.048 MHz Output Jitter Transfer

	Characteristics	Sym.	Min.	Max.	Units	Conditions/Notes†
1	Jitter at output for 1 Hz@3.00 UIpp input			2.9	UIpp	1,5,6-11,18-19,21,27,32
2	with 40 Hz to 100 kHz filter			0.09	UIpp	1-5,6-11,18-19, 21,27,33
3	Jitter at output for 3 Hz@2.33 UIpp input			1.3	UIpp	1,5,6-11,18-19,21,27,32
4	with 40 Hz to 100 kHz filter			0.10	UIpp	1-5,6-11,18-19,21,2733
5	Jitter at output for 5 Hz@2.07 UIpp input			0.80	UIpp	1,5,6-11,18-19,21,27,32
6	with 40 Hz to 100 kHz filter			0.10	UIpp	1-5,6-11,18-19, 21,27,33
7	Jitter at output for 10 Hz@1.76 UIpp input			0.40	UIpp	1,5,6-11,18-19,21,27,32
8	with 40 Hz to 100 kHz filter			0.10	UIpp	1-5,6-11,18-19, 21,27,33
9	Jitter at output for 100 Hz@1.50 UIpp input			0.06	UIpp	1,5,6-11,18-19,21,27,32
10	with 40 Hz to 100 kHz filter			0.05	UIpp	1-5,6-11,18-19, 21,27,33
11	Jitter at output for 2400 Hz@1.50 UIpp input			0.04	UIpp	1,5,6-11,18-19,21,27,32
12	with 40 Hz to 100 kHz filter			0.03	UIpp	1-5,6-11,18-19,21,27,33
13	Jitter at output for 100 kHz@0.20 UIpp input			0.04	UIpp	1,5,6-11,18-19,21,27,32
14	with 40 Hz to 100 kHz filter			0.02	UIpp	1-5,6-11,18-19,21,27,33

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 8 kHz Input Jitter Tolerance

	Characteristics	Sym.	Min.	Max.	Units	Conditions/Notes†
1	Jitter tolerance for 1 Hz input		0.80		UIpp	1,3,6-11,18-19,21-23,25
2	Jitter tolerance for 5 Hz input		0.70		UIpp	1,3,6-11,18-19,21-23,25
3	Jitter tolerance for 20 Hz input		0.60		UIpp	1,3,6-11,18-19,21-23,25
4	Jitter tolerance for 300 Hz input		0.20		UIpp	1,3,6-11,18-19,21-23,25
5	Jitter tolerance for 400 Hz input		0.15		UIpp	1,3,6-11,18-19,21-23,25
6	Jitter tolerance for 700 Hz input		0.08		UIpp	1,3,6-11,18-19,21-23,25
7	Jitter tolerance for 2400 Hz input		0.02		UIpp	1,3,6-11,18-19,21-23,25
8	Jitter tolerance for 3600 Hz input		0.01		UIpp	1,3,6-11,18-19,21-23,25

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 1.544 MHz Input Jitter Tolerance

	Characteristics	Sym.	Min.	Max.	Units	Conditions/Notes†
1	Jitter tolerance for 1 Hz input		150		UIpp	1,4,6-11,18-19,21-23,26
2	Jitter tolerance for 5 Hz input		140		UIpp	1,4,6-11,18-19,21-23,26
3	Jitter tolerance for 20 Hz input		130		UIpp	1,4,6-11,18-19,21-23,26
4	Jitter tolerance for 300 Hz input		35		UIpp	1,4,6-11,18-19,21-23,26
5	Jitter tolerance for 400 Hz input		25		UIpp	1,4,6-11,18-19,21-23,26
6	Jitter tolerance for 700 Hz input		15		UIpp	1,4,6-11,18-19,21-23,26
7	Jitter tolerance for 2400 Hz input		4		UIpp	1,4,6-11,18-19,21-23,26
8	Jitter tolerance for 10 kHz input		1		UIpp	1,4,6-11,18-19,21-23,26
9	Jitter tolerance for 100 kHz input		0.5		UIpp	1,4,6-11,18-19,21-23,26

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 2.048 MHz Input Jitter Tolerance

	Characteristics	Sym.	Min.	Max.	Units	Conditions/Notes†
1	Jitter tolerance for 1 Hz input		150		UIpp	1,5,6-11,18-19,21-23,27
2	Jitter tolerance for 5 Hz input		140		UIpp	1,5,6-11,18-19,21-23,27
3	Jitter tolerance for 20 Hz input		130		UIpp	1,5,6-11,18-19,21-23,27
4	Jitter tolerance for 300 Hz input		50		UIpp	1,5,6-11,18-19,21-23,27
5	Jitter tolerance for 400 Hz input		40		UIpp	1,5,6-11,18-19,21-23,27
6	Jitter tolerance for 700 Hz input		20		UIpp	1,5,6-11,18-19,21-23,27
7	Jitter tolerance for 2400 Hz input		5		UIpp	1,5,6-11,18-19,21-23,27
8	Jitter tolerance for 10 kHz input		1		UIpp	1,5,6-11,18-19,21-23,27
9	Jitter tolerance for 100 kHz input		1		UIpp	1,5,6-11,18-19,21-23,27

† See "Notes" following AC Electrical Characteristics tables.

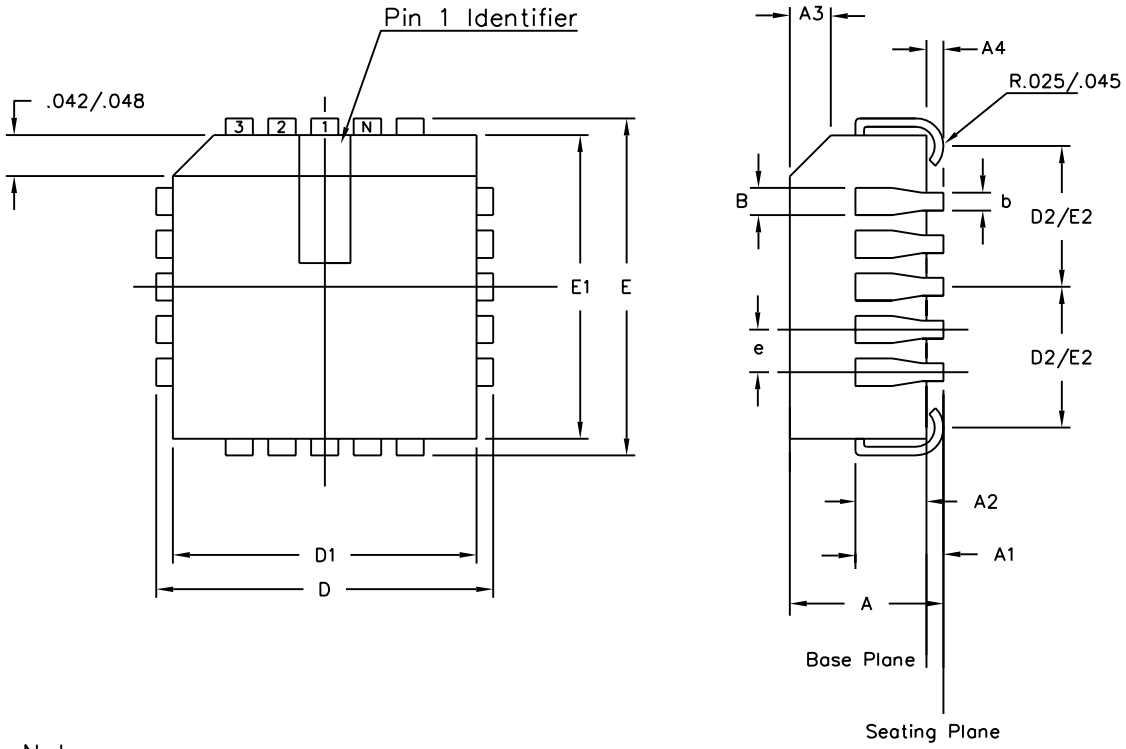
AC Electrical Characteristics - OSCi 20 MHz Master Clock Input

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Conditions/Notes†
1	Frequency accuracy (20 MHz nominal)		-0	0	+0	ppm	15,18
2			-32	0	+32	ppm	16,19
3			-100	0	+100	ppm	17,20
4	Duty cycle		40	50	60	%	
5	Rise time				10	ns	
6	Fall time				10	ns	

† Notes:

Voltages are with respect to ground (V_{SS}) unless otherwise stated.
Supply voltage and operating temperature are as per Recommended Operating Conditions.
Timing parameters are as per AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

1. Normal Mode selected.
2. Freerun Mode selected.
3. 8 kHz Frequency Mode selected.
4. 1.544 MHz Frequency Mode selected.
5. 2.048 MHz Frequency Mode selected.
6. Master clock input OSCi at 20 MHz ±0 ppm.
7. Master clock input OSCi at 20 MHz ±32 ppm.
8. Master clock input OSCi at 20 MHz ±100 ppm.
9. Selected reference input at ±0 ppm.
10. Selected reference input at ±32 ppm.
11. Selected reference input at ±100 ppm.
12. For Freerun Mode of ±0 ppm.
13. For Freerun Mode of ±32 ppm.
14. For Freerun Mode of ±100 ppm.
15. For capture range of ±230 ppm.
16. For capture range of ±198 ppm.
17. For capture range of ±130 ppm.
18. 25 pF capacitive load.
19. OSCi Master Clock jitter is less than 2 nspp, or 0.04 UIpp where1 UIpp=1/20 MHz.
20. Jitter on reference input is less than 7 nspp.
21. Applied jitter is sinusoidal.
22. Minimum applied input jitter magnitude to regain synchronization.
23. Loss of synchronization is obtained at slightly higher input jitter amplitudes.
24. Within 10 ms of the state, reference or input change.
25. 1 UIpp = 125 us for 8 kHz signals.
26. 1 UIpp = 648 ns for 1.544 MHz signals.
27. 1 UIpp = 488 ns for 2.048 MHz signals.
28. 1 UIpp = 323 ns for 3.088 MHz signals.
29. 1 UIpp = 244 ns for 4.096 MHz signals.
30. 1 UIpp = 122 ns for 8.192 MHz signals.
31. 1 UIpp = 61 ns for 16.384 MHz signals.
32. No filter.
33. 40 Hz to 100 kHz bandpass filter.
34. With respect to reference input signal frequency.
35. After a RST or TRST.
36. Master clock duty cycle 40% to 60%.



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.485	0.495	12.32	12.57
D1	0.450	0.456	11.43	11.58
D2	0.191	0.219	4.85	5.56
E	0.485	0.495	12.32	12.57
E1	0.450	0.456	11.43	11.58
E2	0.191	0.219	4.85	5.56
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	7			
NE	7			
N	28			
Note	Square			
Conforms to JEDEC MS-018AB Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

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