

2.5V Drive Nch MOSFET

1.5V Drive Pch MOSFET

TT8M2

●Structure

Silicon N-channel MOSFET/
Silicon P-channel MOSFET

●Features

- 1) Low on-state resistance.
- 2) Low voltage drive.
- 3) High power package.

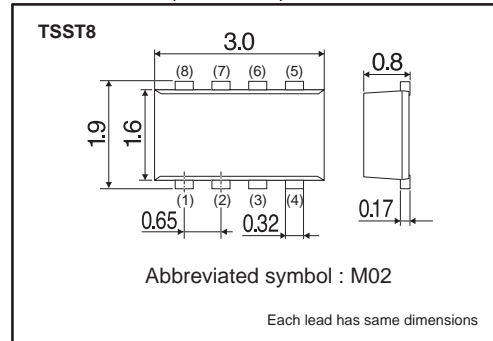
●Application

Switching

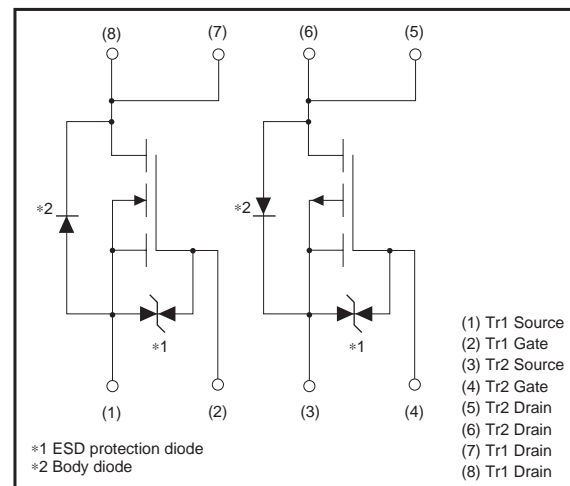
●Packaging specifications

| Type | Package | Taping |
|-------|------------------------------|--------|
| | Code | TR |
| | Basic ordering unit (pieces) | 3000 |
| TT8M2 | | ○ |

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

<Tr1 : Nch>

| Parameter | Symbol | Limits | Unit | |
|-----------------------------|------------|-------------|-----------|---|
| Drain-source voltage | V_{DS} | 30 | V | |
| Gate-source voltage | V_{GS} | ± 12 | V | |
| Drain current | Continuous | I_D | ± 2.5 | A |
| | Pulsed | I_{DP} *1 | ± 10 | A |
| Source current (Body diode) | Continuous | I_S | 0.8 | A |
| | Pulsed | I_{SP} *1 | 10 | A |

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

<Tr2 : Pch>

| Parameter | Symbol | Limits | Unit |
|--------------------------------|------------------|--------------------|------|
| Drain-source voltage | V _{DSS} | -20 | V |
| Gate-source voltage | V _{GSS} | ±10 | V |
| Drain current | Continuous | I _D | ±2.5 |
| | Pulsed | I _{DP} *1 | ±10 |
| Source current (Body diode) | Continuous | I _S | -0.8 |
| | Pulsed | I _{SP} *1 | -10 |

*1 Pw≤10μs, Duty cycle≤1%

<Tr1 AND Tr2>

| Parameter | Symbol | Limits | Unit |
|------------------------------|-------------------|-------------|-------------|
| Total power dissipation | P _D *2 | 1.25 | W / TOTAL |
| | | 1.0 | W / ELEMENT |
| Channel temperature | T _{ch} | 150 | °C |
| Range of Storage temperature | T _{stg} | -55 to +150 | °C |

*2 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

< Characteristics for the Tr1(Nch).>

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|-----------------------|------|------|------|------|---|
| Gate-source leakage | I _{GSS} | - | - | ±10 | μA | V _{GS} =±12V, V _{DS} =0V |
| Drain-source breakdown voltage | V _{(BR) DSS} | 30 | - | - | V | I _D =1mA, V _{GS} =0V |
| Zero gate voltage drain current | I _{DSS} | - | - | 1 | μA | V _{DS} =30V, V _{GS} =0V |
| Gate threshold voltage | V _{GS(th)} | 0.5 | - | 1.5 | V | V _{DS} =10V, I _D =1mA |
| Static drain-source on-state resistance | R _{DS(on)} * | - | 65 | 90 | mΩ | I _D =2.5A, V _{GS} =4.5V |
| | | - | 70 | 95 | mΩ | I _D =2.5A, V _{GS} =4V |
| | | - | 95 | 130 | mΩ | I _D =2.5A, V _{GS} =2.5V |
| Forward transfer admittance | Y _{fs} * | 2.2 | - | - | S | V _{DS} =10V, I _D =2.5A |
| Input capacitance | C _{iss} | - | 180 | - | pF | V _{DS} =10V |
| Output capacitance | C _{oss} | - | 60 | - | pF | V _{GS} =0V |
| Reverse transfer capacitance | C _{rss} | - | 35 | - | pF | f=1MHz |
| Turn-on delay time | t _{d(on)} * | - | 7 | - | ns | V _{DD} ≐15V |
| Rise time | t _r * | - | 30 | - | ns | I _D =1.2A |
| Turn-off delay time | t _{d(off)} * | - | 20 | - | ns | V _{GS} =4.5V |
| Fall time | t _f * | - | 20 | - | ns | R _L ≐12.5Ω |
| Total gate charge | Q _g * | - | 3.2 | - | nC | R _G =10Ω |
| Gate-source charge | Q _{gs} * | - | 0.9 | - | nC | V _{DD} ≐15V, I _D =2.5A |
| Gate-drain charge | Q _{gd} * | - | 0.4 | - | nC | V _{GS} =4.5V |
| | | | | | | R _L ≐6Ω, R _G =10Ω |

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|-----------------|-------------------|------|------|------|------|---|
| Forward voltage | V _{SD} * | - | - | 1.2 | V | I _S =2.5A, V _{GS} =0V |

*Pulsed

●Electrical characteristics (Ta=25°C)

< Characteristics for the Tr2(Pch).>

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|----------------|------|------|----------|------------|--------------------------------------|
| Gate-source leakage | I_{GSS} | – | – | ± 10 | μA | $V_{GS}=\pm 10V, V_{DS}=0V$ |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | –20 | – | – | V | $I_D = -1mA, V_{GS}=0V$ |
| Zero gate voltage drain current | I_{DSS} | – | – | –1 | μA | $V_{DS} = -20V, V_{GS}=0V$ |
| Gate threshold voltage | $V_{GS(th)}$ | –0.3 | – | –1.0 | V | $V_{DS} = -10V, I_D = -1mA$ |
| Static drain-source on-state resistance | $R_{DS(on)}$ * | – | 49 | 68 | m Ω | $I_D = -2.5A, V_{GS} = -4.5V$ |
| | | – | 68 | 95 | m Ω | $I_D = -1.2A, V_{GS} = -2.5V$ |
| | | – | 100 | 150 | m Ω | $I_D = -1.2A, V_{GS} = -1.8V$ |
| | | – | 140 | 280 | m Ω | $I_D = -0.5A, V_{GS} = -1.5V$ |
| Forward transfer admittance | $ Y_{fs} $ * | 2.5 | – | – | S | $V_{DS} = -10V, I_D = -2.5A$ |
| Input capacitance | C_{iss} | – | 1270 | – | pF | $V_{DS} = -10V$ |
| Output capacitance | C_{oss} | – | 100 | – | pF | $V_{GS} = 0V$ |
| Reverse transfer capacitance | C_{rss} | – | 90 | – | pF | $f = 1MHz$ |
| Turn-on delay time | $t_{d(on)}$ * | – | 9 | – | ns | $V_{DD} \doteq -10V$ |
| Rise time | t_r * | – | 30 | – | ns | $I_D = -1.2A$ |
| Turn-off delay time | $t_{d(off)}$ * | – | 120 | – | ns | $V_{GS} = -4.5V$ |
| Fall time | t_f * | – | 85 | – | ns | $R_L \doteq 8.3\Omega$ |
| Total gate charge | Q_g * | – | 12 | – | nC | $V_{DD} \doteq -10V, I_D = -2.5A$ |
| Gate-source charge | Q_{gs} * | – | 2.5 | – | nC | $V_{GS} = -4.5V$ |
| Gate-drain charge | Q_{gd} * | – | 2.0 | – | nC | $R_L \doteq 4\Omega, R_G = 10\Omega$ |

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|-----------------|------------|------|------|------|------|----------------------------|
| Forward voltage | V_{SD} * | – | – | –1.2 | V | $I_S = -2.5A, V_{GS} = 0V$ |

*Pulsed

●Electrical characteristics curves
<Nch>

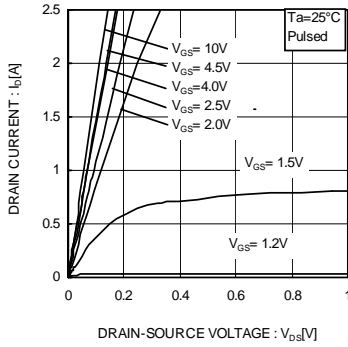


Fig.1 Typical Output Characteristics (I)

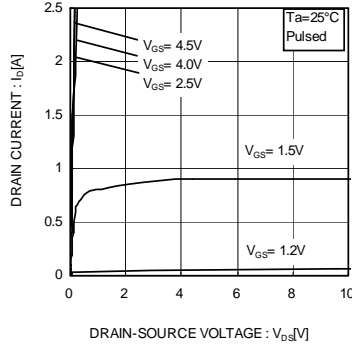


Fig.2 Typical Output Characteristics(II)

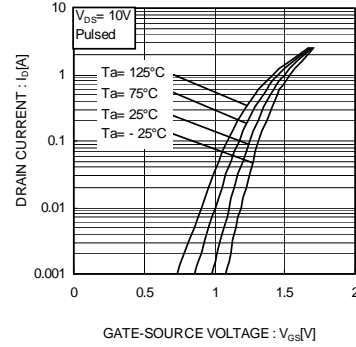


Fig.3 Typical Transfer Characteristics

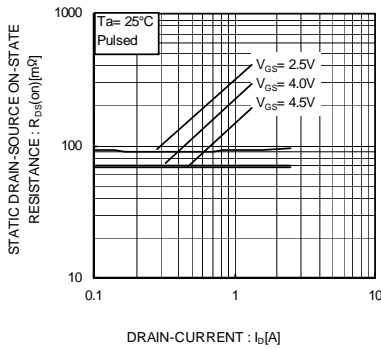


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)

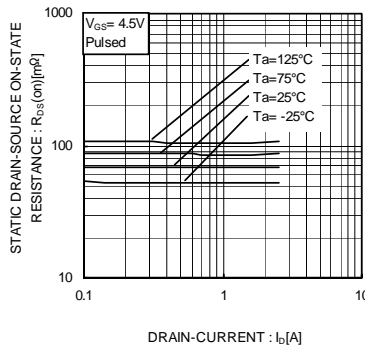


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

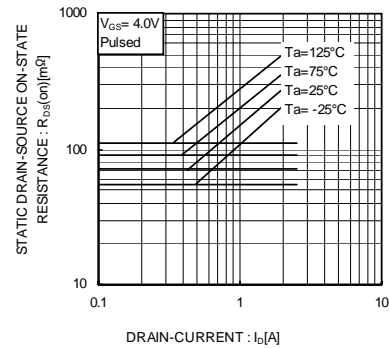


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

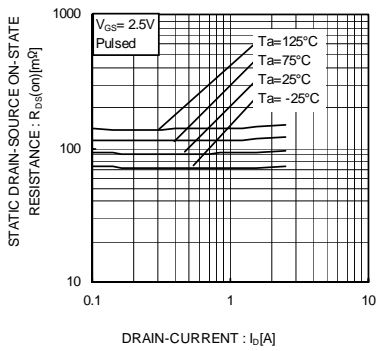


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

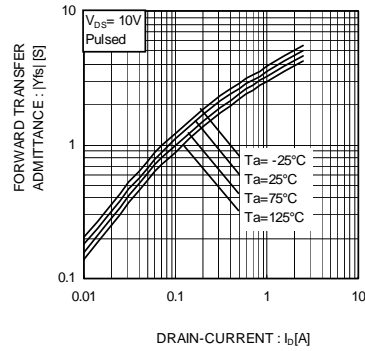


Fig.8 Forward Transfer Admittance vs. Drain Current

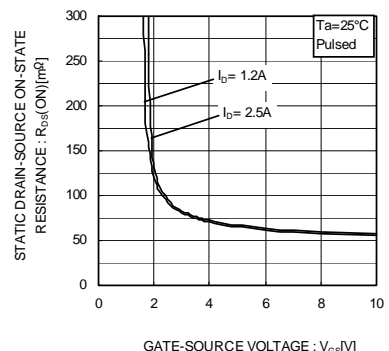


Fig.9 Static Drain-Source On-State Resistance vs. Gate Source Voltage

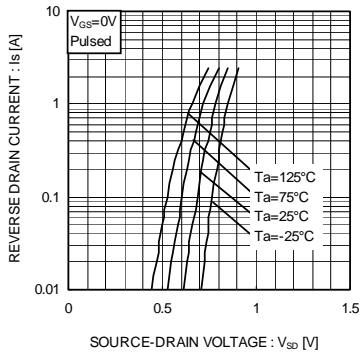


Fig.10 Reverse Drain Current vs. Source-Drain Voltage

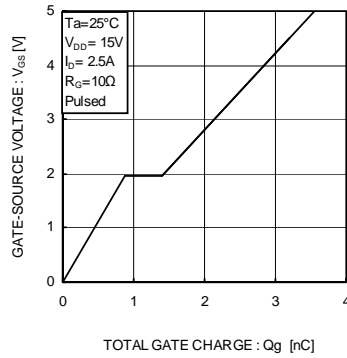


Fig.11 Dynamic Input Characteristics

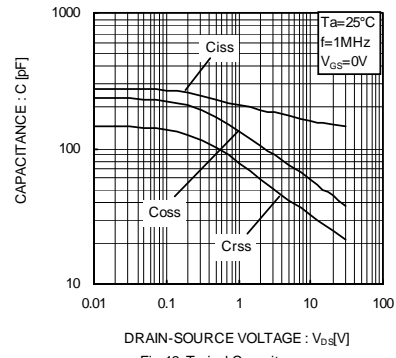


Fig.12 Typical Capacitance vs. Drain-Source Voltage

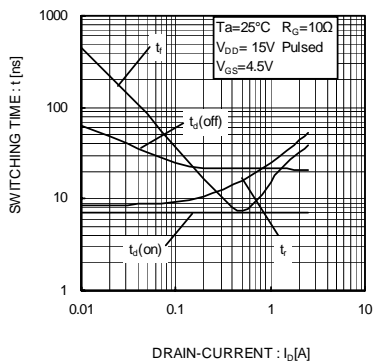


Fig.13 Switching Characteristics

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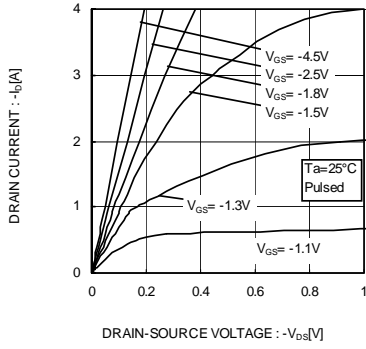


Fig.1 Typical Output Characteristics (I)

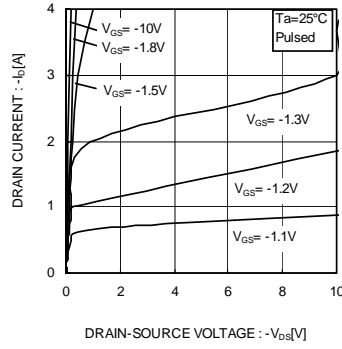


Fig.2 Typical Output Characteristics (II)

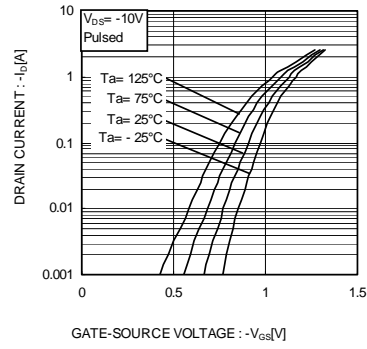


Fig.3 Typical Transfer Characteristics

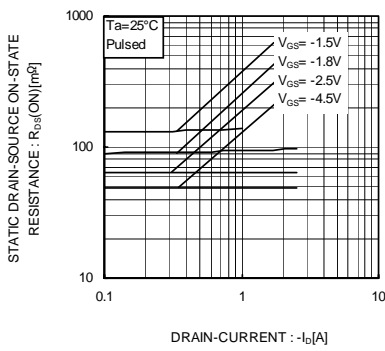


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)

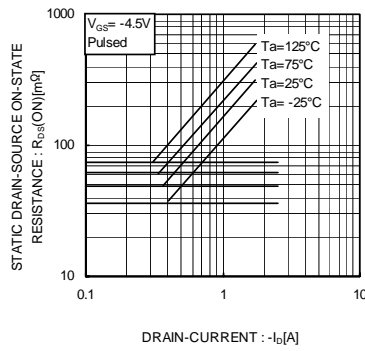


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (II)

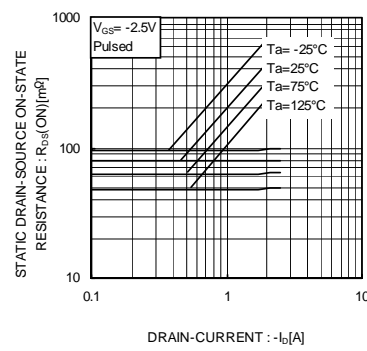


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (III)

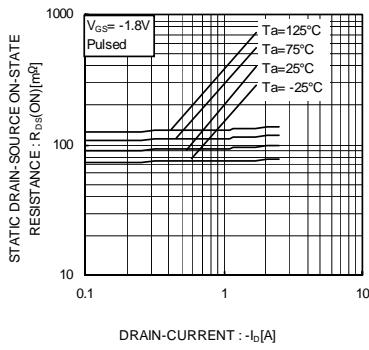


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

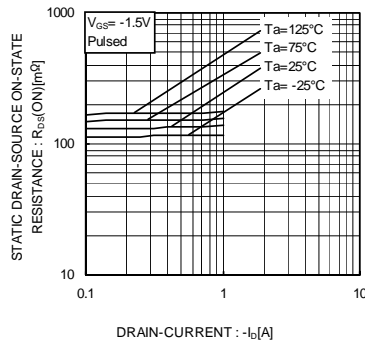


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(IV)

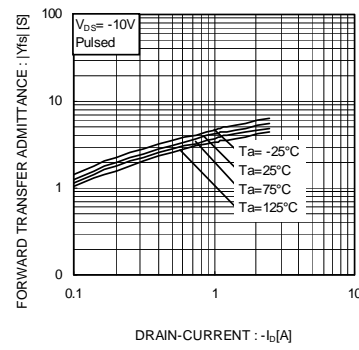


Fig.9 Forward Transfer Admittance vs. Drain Current

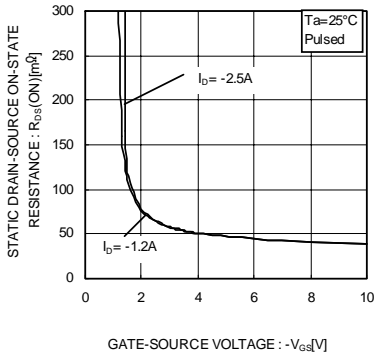


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

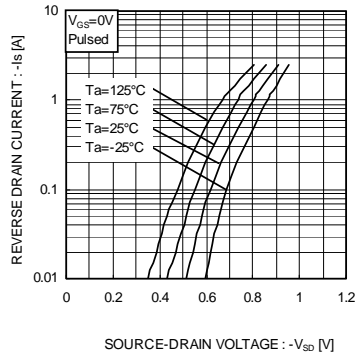


Fig.11 Reverse Drain Current vs. Source-Drain Voltage

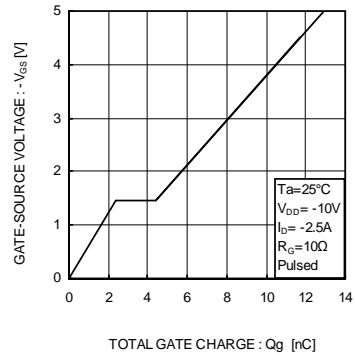


Fig.12 Dynamic Input Characteristics

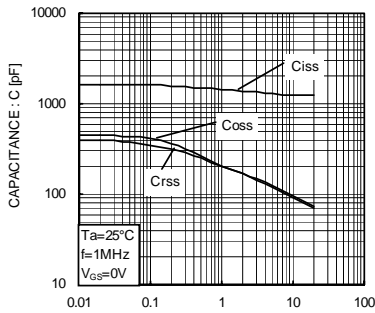


Fig.13 Typical Capacitance vs. Drain-Source Voltage

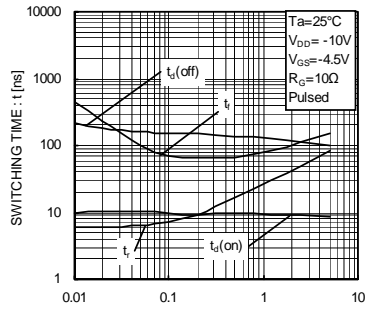


Fig.14 Switching Characteristics

●Measurement circuits

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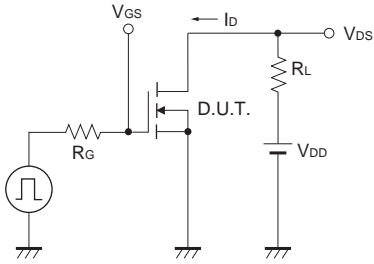


Fig.1-1 Switching Time Measurement Circuit

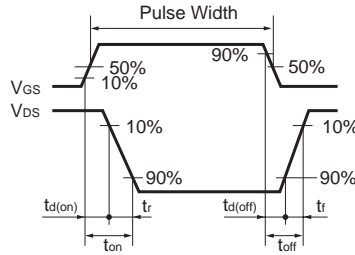


Fig.1-2 Switching Waveforms

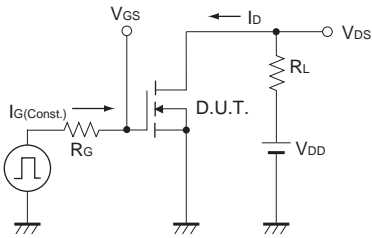


Fig.2-1 Gate charge measurement circuit

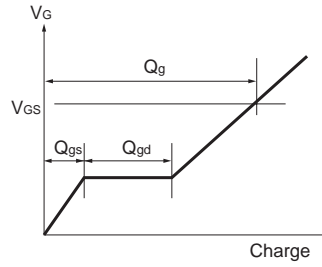


Fig.2-2 Gate Charge Waveform

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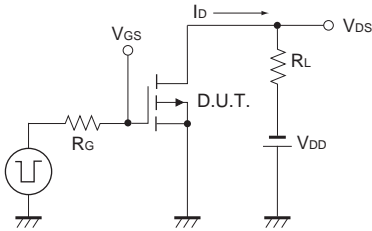


Fig.3-1 Switching time measurement circuit

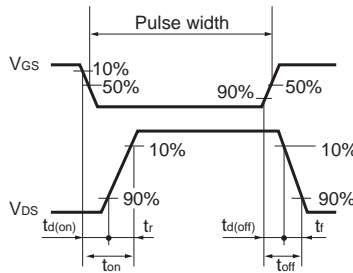


Fig.3-2 Switching waveforms

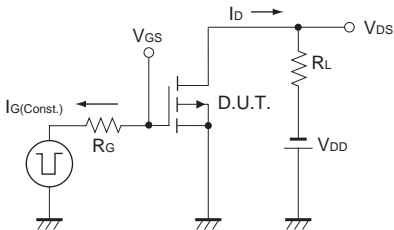


Fig.4-1 Gate charge measurement circuit

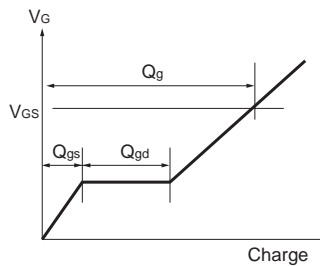


Fig.4-2 Gate charge waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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