

NB3L03

2.8 V, High Precision 1:3 Clock Fanout Buffer

Description

The NB3L03 is a low-skew, low jitter 1:3 clock fanout buffer, ideal for use in portable end-equipment, such as mobile phones or tablet applications. The MCLK_IN pin has an integrated AC coupling capacitor and will directly accept a square or sine wave clock input, such as a temperature compensated crystal oscillator (TCXO). The minimum acceptable input amplitude of the sine wave is 800 mV peak-to-peak. The NB3L03 is offered in a 0.4 mm pitch WLCSP6 (0.77 mm x 1.17 mm), wafer-level chip-scale package (WLCSP) (0.77 mm x 1.17 mm).

Features

- 800 mV Single Ended Outputs
- Low Additive Phase Jitter
- Ultra Small Package: 0.4 mm Pitch WLCSP6 (0.77 mm x 1.17 mm)
- Exceeds JEDEC ESD Standards: 4000 V HBM, 200 V MM
- Industrial Temperature Range: -40°C to +85°C
- These are Pb-Free Devices

PIN DESCRIPTIONS

| Ball No. | Name | I/O | Description |
|----------|-----------------|-----|----------------------|
| A1 | V _{DD} | I | Power Supply Voltage |
| A2 | CLK_OUT1 | O | Clock Output 1 |
| B1 | MCLK_IN | I | Master Clock Input |
| B2 | CLK_OUT3 | O | Clock Output 3 |
| C1 | GND | - | Ground |
| C2 | CLK_OUT2 | O | Clock Output 2 |



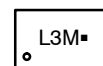
ON Semiconductor®

<http://onsemi.com>



WLCSP6
FC SUFFIX
CASE 567HJ

MARKING DIAGRAM



- L3 = Specific Device Code
- M = Date Code
- = Pb-Free Package

PINOUT DIAGRAM

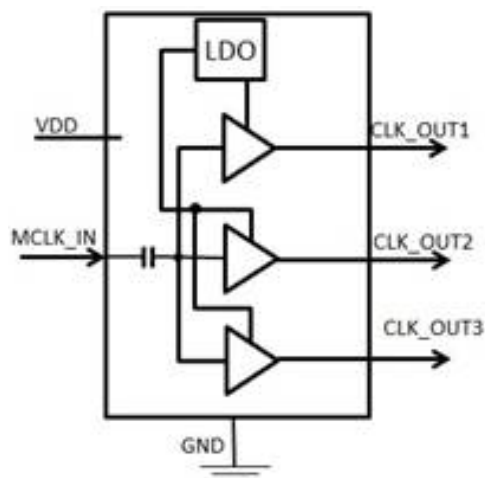
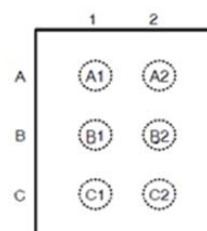


Figure 1. Simplified Block Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

NB3L03

Table 1. MAXIMUM RATINGS

| Symbol | Parameter | Condition | Min | Max | Unit |
|------------------|--------------------------------------|---------------------------------------|------|-----------------------|------|
| | Voltage Range (Note 1) | MCLK_IN, CLK_OUT1, CLK_OUT2, CLK_OUT3 | -0.3 | V _{DD} + 0.3 | V |
| I _O | Continuous Output Current | CLK_OUT1/2/3 | | ±20 | mA |
| T _J | Operating Junction Temperature Range | | -40 | 150 | °C |
| T _{stg} | Storage Temperature Range | | -55 | 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. All voltage values are with respect to network ground terminal.

Table 2. ATTRIBUTES

| Characteristic | | Value |
|--|------------------|----------------------|
| ESD Protection | Human Body Model | >4 kV |
| | Machine Model | >200 V |
| Moisture Sensitivity | WLCSP6 | Level 1 |
| Maximum Soldering Temperature for Lead-free Devices Using a Lead-free Solder Paste | | 260 |
| Flammability Rating Oxygen Index: 28 to 34 | | UL 94 V-0 @ 0.125 in |
| Transistor Count | | 149 |
| Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test II | | |

Table 3. ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|--------------------------------|--|-----|-----|-----------------|------|
| V _{DD} | Supply Voltage | 2.3 | 2.8 | 3.465 | V |
| V _{IN} | Input Voltage p-p | 800 | | V _{DD} | mV |
| V _{OUT} | Output Voltage p-p | 0.8 | 1.0 | 1.2 | V |
| I _{DDdynamic} | Dynamic Current at 26 MHz (Notes 2 and 3) | | 5.0 | 6.5 | mA |
| F _{IN} | MCLK_IN Frequency Range with 800 mV input p-p | 10 | 26 | 52 | MHz |
| t _{PD} | MCLK_IN to CLK_OUT_n Propagation Delay, input = 1 V _{p-p} @ 26 MHz | 2.0 | 4.0 | 6.5 | ns |
| DC | CLK_OUT_n Duty Cycle | 45 | 50 | 55 | % |
| t _{jit} | Additive Phase Jitter @ 12 kHz to 20 MHz, F _{IN} = 26 MHz @ 800 mV input p-p, input t _r /t _f < 1 ns | | 171 | | fs |
| t _r /t _f | Output Rise Time 20%-80% with 10 pF Load, V _{IN} = 800 mV _{p-p} , 26 MHz, input slew rate < 1 ns/V | 0.5 | 0.8 | 1.4 | ns |
| t _{sk} | Channel to Channel Skew | | 10 | 30 | ps |
| V _{oh} | High Level Output (V _{oh} -V _{ol} not to exceed V _{OUT}) | 0.8 | 1.0 | 1.2 | V |
| V _{ol} | Low Level Output (V _{oh} -V _{ol} not to exceed V _{OUT}) | | 0 | | V |

2. I_{DD} dynamic specified with no load on outputs.

3. Input amplitude 1.2 V p-p.

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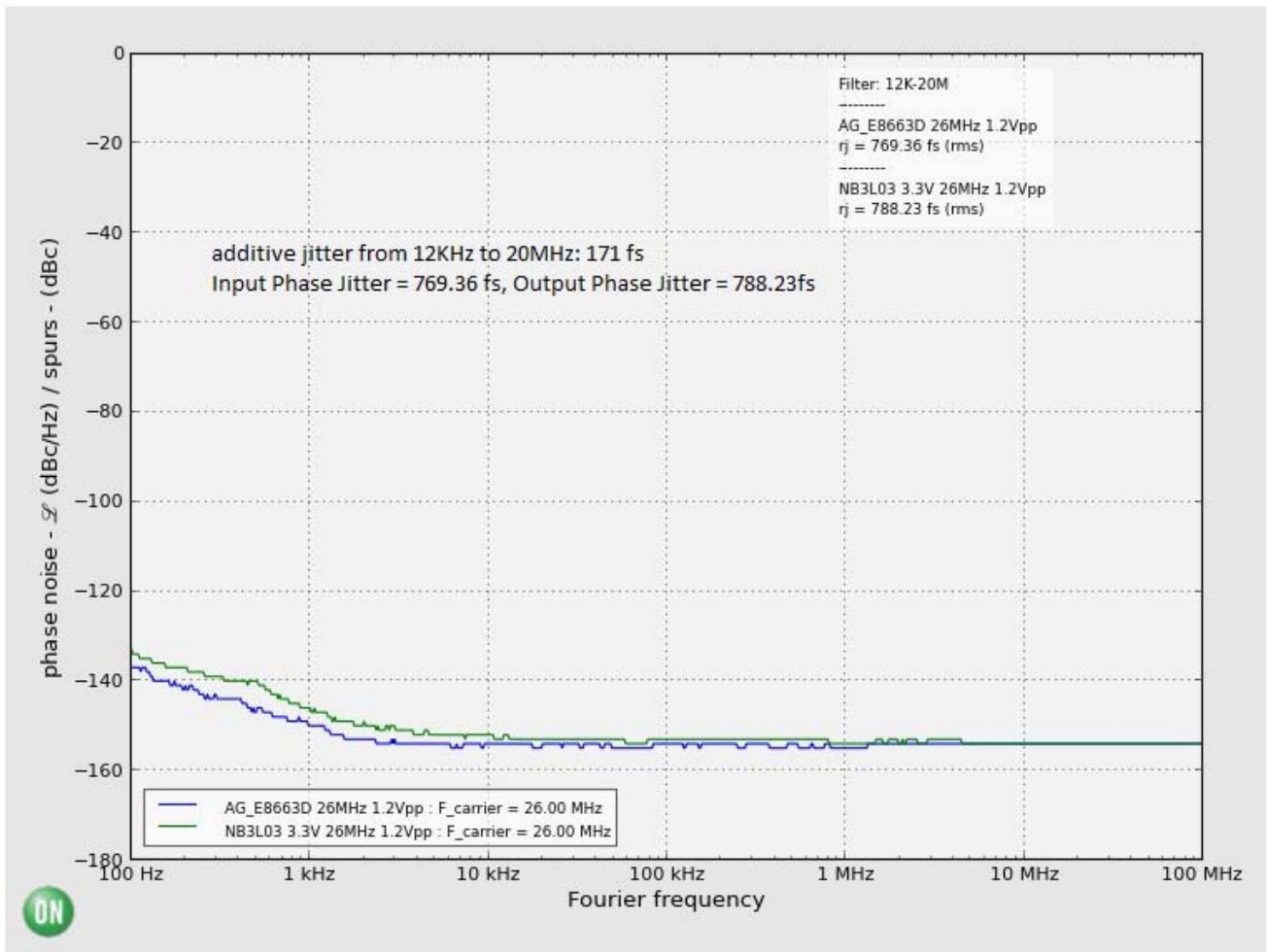


Figure 2. Typical Phase Jitter @ 26 MHz, INT Range (12 kHz to 20 MHz)

ORDERING INFORMATION

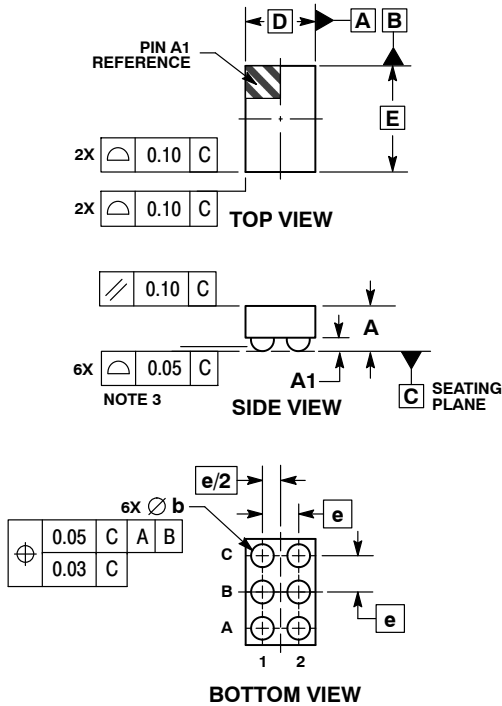
| Device | Package | Shipping [†] |
|-------------|---------------------|-----------------------|
| NB3L03FCT2G | WLCSP6 (Pb-Free) | 3000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

WLCSP6, 1.17x0.77
CASE 567HJ
ISSUE O

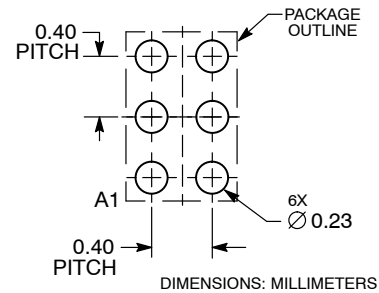


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | --- | 0.50 |
| A1 | 0.13 | 0.17 |
| b | 0.21 | 0.25 |
| D | 0.77 BSC | |
| E | 1.17 BSC | |
| e | 0.40 BSC | |

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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