ISL9440B, ISL9440C

Triple Step-Down PWM and Single Linear Controller with Programmable Soft-Start

FN6799
Rev 4.00
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The ISL9440B and ISL9440C are quad-output synchronous buck controllers that integrate three PWM controllers and one low drop-out linear regulator controller, which are full featured and designed to provide multi-rail power for use in products such as cable and satellite set-top boxes, VoIP gateways, cable modems, and other home connectivity products as well as a variety of industrial and general purpose applications. Each output is adjustable down to 0.8V. The PWMs are synchronized at 180° out-of-phase thus, reducing the RMS input current and ripple voltage.

The ISL9440B and ISL9440C offer programmable soft-start, independent enable inputs for ease of supply rail sequencing, and integrated UV/OV/OC/OT protections in a space conscious 5mmx5mm QFN package. An early warning function is offered to output a logic signal to warn the system to back up data when input voltage falls below a certain level.

The ISL9440B and ISL9440C utilize internal loop compensation to keep minimum peripheral components for compact design and a low total solution cost. These devices are implemented with current mode control with feed-forward to cover various applications even with fixed internal compensations.

Table 1 shows the difference in terms of ISL944xx family features.

TABLE 1.

PART NUMBER	EARLY WARNING	SWITCHING FREQUENCY (kHz)	SOFT-STARTING TIME (ms)
ISL9440	Yes	300	1.7
ISL9440A	Yes	600	1.7
ISL9441	No	300	1.7
ISL9440B	Yes	300	Programmable
ISL9440C **(No longer available or supported)**	Yes	600	Programmable

Features

- Three Integrated Synchronous Buck PWM Controllers
  - Internal Bootstrap Diodes
  - Internal Compensation
- Independent Control for each Regulator and Programmable Output Voltages; Independent Enable/Shutdown/Soft-start
- Fixed Switching Frequency: 300kHz(B), 600kHz(C)
- Adaptive Shoot-Through Protection on all Synchronous Buck Controllers
- Pre-biased Output Start-up Capability
- Out-of-Phase Switching to Reduce Input Capacitance (0°/180°/0°)
- No External Current Sense Resistor
  - Uses Lower MOSFET's $r_{DS(ON)}$
- Current Mode Controller with Voltage Feed-Forward
- Complete Protection
  - Overcurrent, Overvoltage, Undervoltage Lockout, Over-Temperature
- Cycle-by-Cycle Current Limiting
- Wide Input Voltage Range
  - Input Rail Powers VIN Pin: 5.6V to 24V
  - Input Rail Powers VCC_5V Pin (VIN tied to VCC_5V, for 5V input applications): 4.5V to 5.6V
- Early Warning on Input Voltage Failure
- Integrated Reset Function
- Pb-Free (RoHS Compliant)

Applications

- Satellite and Cable Set-Top Boxes
- Cable Modems
- VoX Gateway Devices
- NAS/SAN Devices
- ATX Power Supply

Related Literature

- Technical Brief TB389 "PCB Land Pattern Design and Surface Mount Guidelines for QFN (MLFP) Packages"

Ordering Information

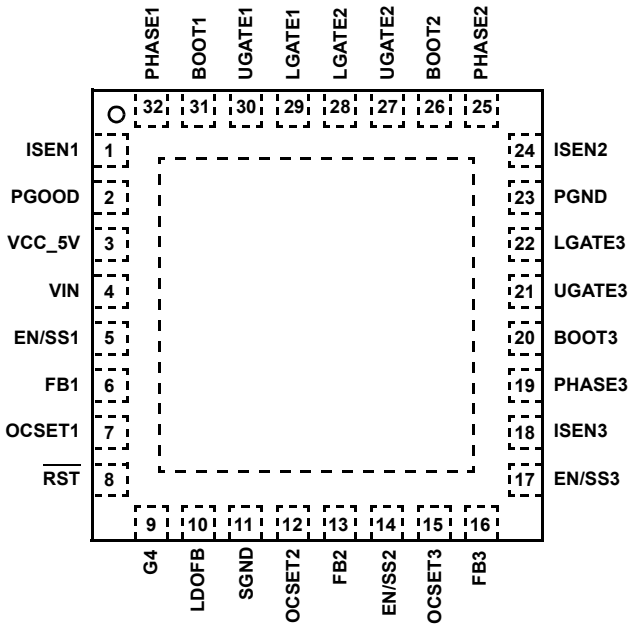
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL9440BIRZ	9440B IRZ	-40 to +85	32 Ld 5x5 QFN	L32.5x5B
ISL9440CIRZ **(No longer available, recommended replacement: ISL9440IRZ)**	9440C IRZ	-40 to +85	32 Ld 5x5 QFN	L32.5x5B

NOTES:

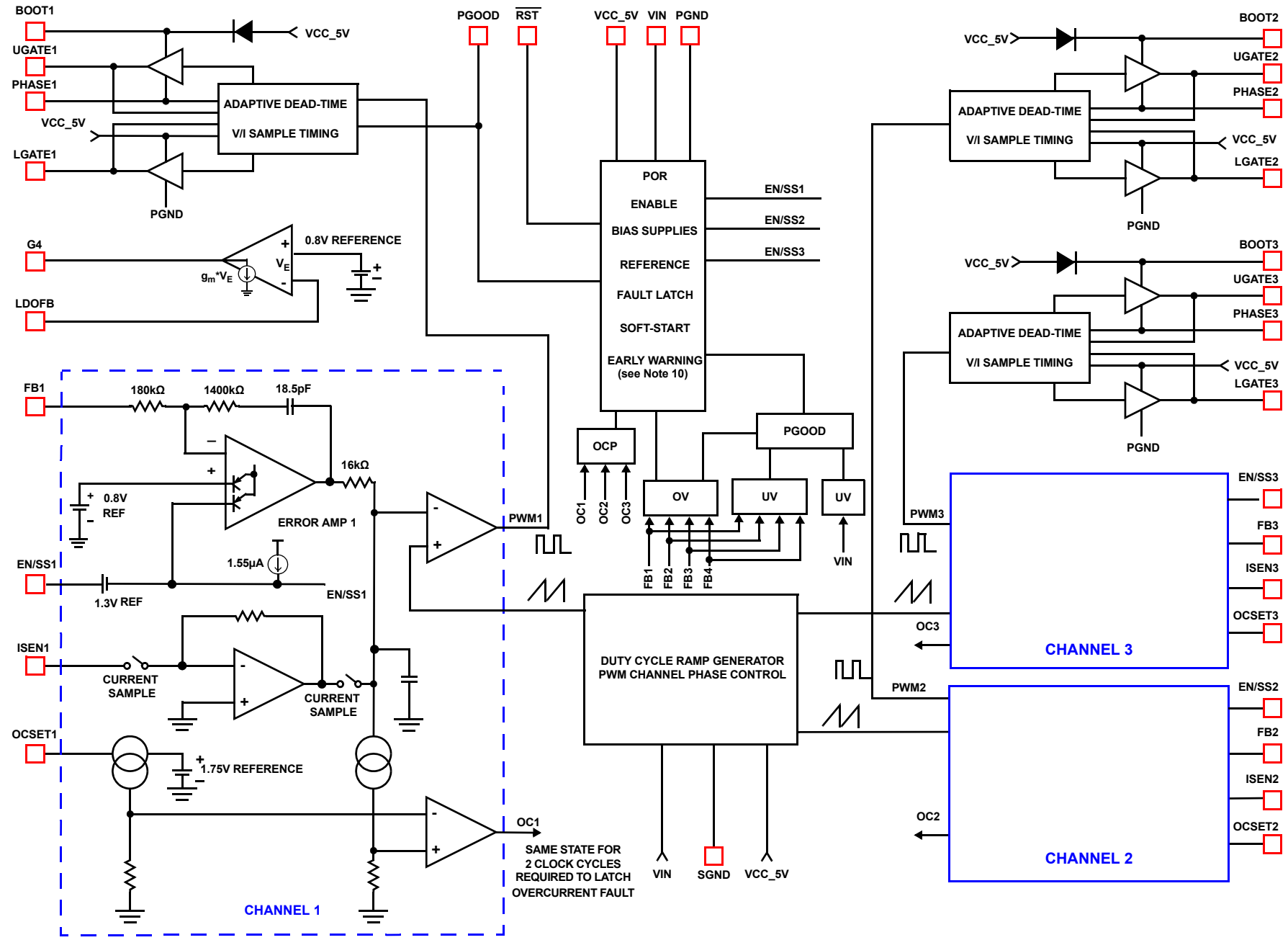
1. Add “-T” for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL9440B, ISL9440C. For more information on MSL please see techbrief TB363.

Pinout

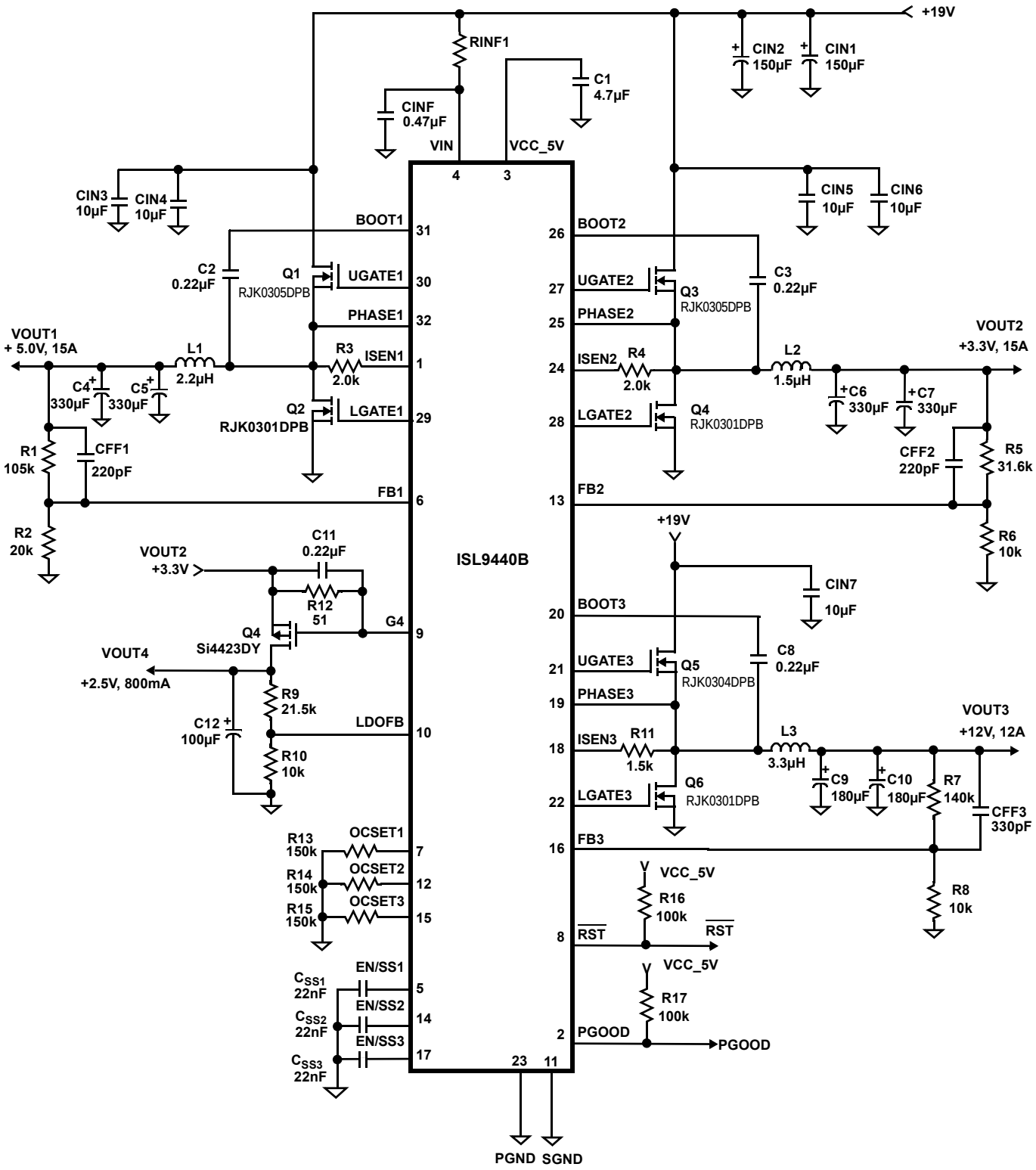
ISL9440B, ISL9440C
(32 LD 5x5 QFN)
TOP VIEW



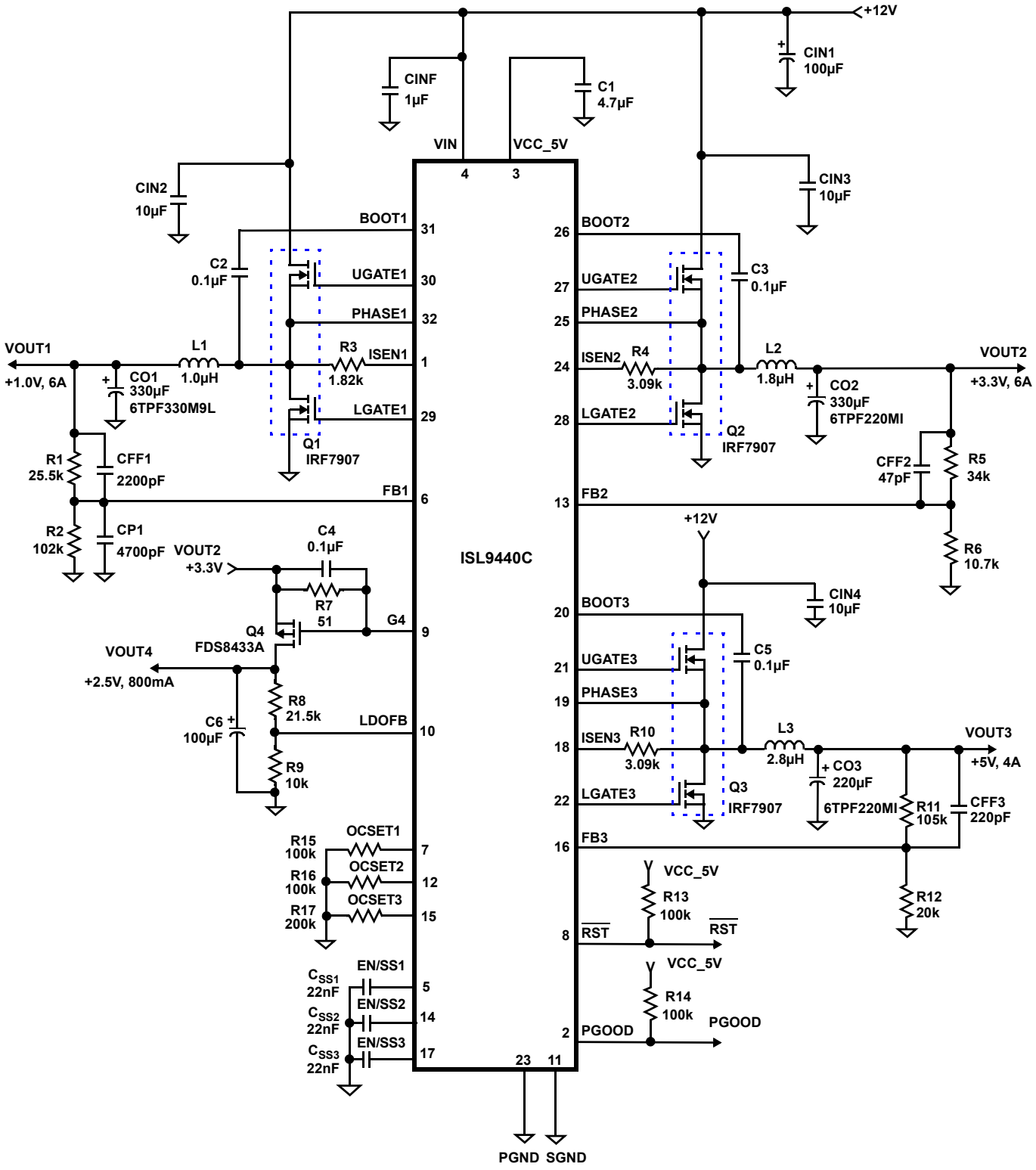
Block Diagram



Typical Application - ISL9440B



Typical Application - ISL9440C



Absolute Maximum Ratings

VCC_5V to GND . . . . . -0.3V to +6V
VCC_5V Output Current 100mA
VIN to GND . . . . . -0.3V to +28V
BOOT/UGATE to PHASE . . . . . -0.3V to VCC_5V + 0.3V
PHASE1,2,3 and ISEN1, 2, 3, to GND
. . . . . -5V (<100ns, 10µJ)/-0.3V (DC) to +28V
EN/SS1,EN/SS2, EN/SS3, FB1, FB2,
FB3, to GND. . . . . -0.3V to VCC_5V + 0.3V
LDOFB, OCSET1, OCSET2, OCSET3,
LGATE1, LGATE2, LGATE3, to GND. . . -0.3V to VCC_5V + 0.3V
PGOOD, RST, G4 to GND. . . . . -0.3V to +6V

Thermal Information

Thermal Resistance (Typical Notes 4, 5)	θ_{JA}(°C/W)	θ_{JC}(°C/W)
32 Ld QFN Package.	31	2.3

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Operating Temperature . . . . . -40°C to +85°C
Maximum Storage Temperature. . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to “Block Diagram” on page 3, “Typical Application - ISL9440B” on page 4 and “Typical Application - ISL9440C” on page 5. V_{IN} = 5.6V to 24V, or VCC_5V = 5V ±10%, C_VCC_5V = 4.7µF, T_A = -40°C to +85°C, Typical values are at T_A = +25°C.

PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNITS
V_{IN} SUPPLY					
Input Voltage Range		5.6	12.0	24.0	V
Input Voltage Range	V_{IN} = VCC_5V (Note 10)	4.5	5.0	5.6	V
VCC_5V SUPPLY (Note 6)					
Operation Voltage		4.5	5.0	5.6	V
Internal LDO Output Voltage	V_{IN} > 5.6V, I_L = 60mA	4.5	5.0	5.5	V
Maximum Supply Current of Internal LDO	V_{IN} = 12V	60			mA
V_{IN} SUPPLY CURRENT					
Shutdown Current (Note 7)	EN/SS1 = EN/SS2 = EN/SS3 = 0, V_{IN} =12V. PGOOD and $\overline{RST}$ are floating.		75	110	µA
Operating Current (Note 8)			3	5	mA
REFERENCE SECTION					
Internal Reference Voltage	Across specified temperature range		0.8		V
Reference Voltage Accuracy	Across specified temperature range	-1		+1	%
PWM CONTROLLER ERROR AMPLIFIERS					
DC Gain (Note 9)			88		dB
Gain-BW Product (Note 9)			15		MHz
Slew Rate (Note 9)			2.0		V/µs
PWM REGULATOR					
Switching Frequency (ISL9440B)		260	300	340	kHz
Maximum Duty Cycle (ISL9440B)			93		%
Minimum Duty Cycle (ISL9440B)			3		%
Switching Frequency (ISL9440C)		522	600	678	kHz

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to “Block Diagram” on page 3, “Typical Application - ISL9440B” on page 4 and “Typical Application - ISL9440C” on page 5. V_{IN} = 5.6V to 24V, or VCC_5V = 5V ±10%, C_VCC_5V = 4.7µF, T_A = -40°C to +85°C, Typical values are at T_A = +25°C. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNITS
Maximum Duty Cycle (ISL9440C)			86		%
Minimum Duty Cycle (ISL9440C)			6		%
FB Bias Current (Note 9)				50	nA
Peak-to-Peak Sawtooth Amplitude (Note 9)	V_{IN} = 12V		1.6		V
	V_{IN} = 5.5V		0.667		V
Ramp Offset			1		V
PWM GATE DRIVER CHANNEL 1, 2 (UGATE1, 2; LGATE 1, 2) (Note 9)					
Source Current			800		mA
Sink Current			2000		mA
Upper Drive Pull-Up	VCC_5V = 5.0V		4	8	Ω
Upper Drive Pull-Down	VCC_5V = 5.0V		1.6	3	Ω
Lower Drive Pull-Up	VCC_5V = 5.0V		4	8	Ω
Lower Drive Pull-Down	VCC_5V = 5.0V		0.9	2	Ω
Rise Time	C_{OUT} = 1000pF		18		ns
Fall Time	C_{OUT} = 1000pF		18		ns
PWM GATE DRIVER CHANNEL 3 (UGATE3; LGATE 3) (Note 9)					
Sink/Source Current			400		mA
Upper Drive Pull-Up	VCC_5V = 5.0V		8.0	12	Ω
Upper Drive Pull-Down	VCC_5V = 5.0V		3.2	6.0	Ω
Lower Drive Pull-Up	VCC_5V = 5.0V		8	12	Ω
Lower Drive Pull-Down	VCC_5V = 5.0V		1.8	3.5	Ω
Rise Time	C_{OUT} = 1000pF		18		ns
Fall Time	C_{OUT} = 1000pF		18		ns
LOW DROP OUT CONTROLLER					
Drive Sink Current	LDOFB = 0.76V	50			mA
FB Threshold Voltage	IG4 = 21mA		0.800		V
Amplifier Trans-conductance			2		A/V
LDOFB Input Leakage Current (Note 9)	LDOFB = 0.8V			50	nA
ENABLE1, ENABLE2, ENABLE3 THRESHOLD and SOFT-START CURRENT					
EN/SSx Enable Threshold		1.1	1.3	1.55	V
EN/SSx Soft-Start Charge Current	VEN/SSx = 1.3V	1.1	1.55	2.0	µA
POWER-GOOD MONITORS					
PGOOD Upper Threshold, PWM 1, 2 and 3		105.5	111	115.5	%
PGOOD Lower Threshold, PWM 1, 2 and 3		87	91	96	%
PGOOD for Linear Controller		70	75	80	%
PGOOD Low Level Voltage	I_SINK = 4mA			0.4	V
PGOOD Leakage Current	PGOOD = 5V		0.025	1	µA

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to “Block Diagram” on page 3, “Typical Application - ISL9440B” on page 4 and “Typical Application - ISL9440C” on page 5. V_{IN} = 5.6V to 24V, or VCC_5V = 5V ±10%, C_VCC_5V = 4.7µF, T_A = -40°C to +85°C, Typical values are at T_A = +25°C. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNITS
PGOOD Rise Time	R_{PULLUP} = 10k to 3.3V		0.05		µs
PGOOD Fall Time	R_{PULLUP} = 10k to 3.3V		0.05		µs
EARLY WARNING FUNCTIONS					
Undervoltage Lockout Rising (VCC_5V Pin)		3.40	3.85	4.30	V
Undervoltage Lockout Falling (VCC_5V Pin)		3.25	3.70	4.15	V
Early Warning Voltage Rising			5.75	5.95	V
Early Warning Voltage Falling		5.30	5.55		V
RST					
$\overline{RST}$ Voltage Low	I_SINK = 4mA			0.4	V
$\overline{RST}$ Leakage Current	$\overline{RST}$ = 5V		0.025	1	µA
$\overline{RST}$ Rise Time	R_{PULLUP} = 10k to 3.3V		0.05		µs
$\overline{RST}$ Fall Time	R_{PULLUP} = 10k to 3.3V		0.05		µs
PGOOD/$\overline{RST}$ TIMING RISING					
VIN/VOUT Rising Threshold to PGOOD High Rising		100	200	300	ms
PGOOD Rising to $\overline{RST}$ Rising			1.0		µs
PGOOD/$\overline{RST}$ TIMING FALLING					
V_{IN}/V_{OUT} Falling Threshold to PGOOD Falling		35	70	110	µs
PGOOD Falling to $\overline{RST}$ Falling		4.5	5.5	6.5	µs
OVERVOLTAGE PROTECTION					
OV Trip Point			118		%
OVERCURRENT PROTECTION					
Overcurrent Threshold (OCSET_) (Note 8)	R_{OCSET} = 55kΩ		32		µA
Full-Scale Input Current (ISEN_) (Note 8)			15		µA
Overcurrent Set Voltage (OCSET_)		1.70	1.75	1.80	V
OVER-TEMPERATURE					
Over-Temperature Shutdown			150		°C
Over-Temperature Hysteresis			20		°C

NOTES:

6. In normal operation, where the device is supplied with voltage on the V_{IN} pin, the VCC_5V pin provides a 5V output capable of 60mA (min). When the VCC_5V pin is used as a 5V supply input, the internal LDO regulator is disabled and the V_{IN} input pin must be connected to the VCC_5V pin. (Refer to the“Pin Descriptions” on page 9 for more details.)
7. This is the total shutdown current with V_{IN} = 5.6 and 24V.
8. Operating current is the supply current consumed when the device is active but not switching. It does not include gate drive current.
9. Limits established by characterization and are not production tested.
10. Check Note 6 for VCC_5V and VIN configurations at 5V ±10% input applications. ISL9440B, ISL9440C’s PGOOD signal will fall LOW when VIN pin voltage drops below 5.55V (TYP), which results from the early warning detection on VIN pin voltage.
11. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Pin Descriptions

BOOT3, BOOT2, BOOT1 (Pin 20, 26, 31)

These pins are bootstrap pins to provide bias for high side driver. The bootstrap diodes are integrated to help reduce total cost and reduce layout complexity.

UGATE3, UGATE2, UGATE1 (Pins 21, 27, 30)

These pins provide the gate drive for the upper MOSFETs.

PHASE3, PHASE2, PHASE1 (Pins 19, 25, 32)

These pins are connected to the junction of the upper MOSFETs source, output filter inductor, and lower MOSFETs drain.

LGATE3, LGATE2, LGATE1 (Pins 22, 28, 29)

These pins provide the gate drive for the lower MOSFETs.

PGND (Pin 23)

This pin provides the power ground connection for the lower gate drivers for all PWM1, PWM2 and PWM3. This pin should be connected to the sources of the lower MOSFETs and the (-) terminals of the external input capacitors.

FB3, FB2, FB1, LDOFB (Pin 16, 13, 6, 10)

These pins are connected to the feedback resistor divider and provide the voltage feedback signals for the respective controller. They set the output voltage of the converter. In addition, the PGOOD circuit uses these inputs to monitor the output voltage status.

ISEN3, ISEN2, ISEN1 (Pin 18, 24, 1)

These pins are used to monitor the voltage drop across the lower MOSFET for current loop feedback and overcurrent protection.

PGOOD (Pin 2)

This is an open drain logic output used to indicate the status of the output voltages AND input voltage. This pin is pulled low when any of the three PWM outputs is not within 10% of the respective nominal voltage, or if the linear controller output is less than 75% of its nominal value, or VIN pin voltage drops below 5.55V.

The PGOOD pin also indicates the VIN pin status for early warning function. If the voltage on VIN pin drops below 5.55V, this pin will be pulled low.

SGND (Pin 11)

This is the small-signal ground, common to all 4 controllers, and is suggested to be routed separately from the high current ground (PGND). In case of one whole solid ground and no noisy current going through around chip, SGND and PGND can be tied to the same ground copper plane. All voltage levels are measured with respect to this pin. A small ceramic capacitor should be connected right next to this pin for noise decoupling.

VIN (Pin 4)

Use this pin to power the device with an external supply voltage with a range of 5.6V to 24V. For 5V ±10% operation, connect this pin to VCC_5V.

For ISL9440B and ISL9440C, the voltage on this pin is monitored for early warning function. If the voltage on this pin drop below 5.55V, the PGOOD will be pulled low. $\overline{RST}$ will be low after PGOOD toggles to low for 5.5µs (TYP). Refer to Figure 1 for detailed time sequence.

VCC_5V (Pin 3)

This pin is the output of the internal 5V linear regulator. This output supplies the bias for the IC, the low-side gate drivers, and the external boot circuitry for the high-side gate drivers. The IC may be powered directly from a single 5V (±10%) supply at this pin. When used as a 5V supply input, this pin must be externally connected to V_{IN}. The VCC_5V pin must be always decoupled to power ground with a minimum of 4.7µF ceramic capacitor, placed very close to the pin.

EN/SS3, EN/SS2, EN/SS1 (Pin 17, 14, 5)

These pins provide an enable/disable function and soft starting for their respective PWM outputs. The output is disabled when the pin is pulled to GND. When a capacitor is connected from one of these pins to the ground, a regulated 1.55µA soft-start current charges this capacitor during soft starting. When the voltage on the EN/SSx pin reaches 1.3V, the corresponding PWM output is active. From 1.3V to 2.1V, the reference voltage of the corresponding PWM channel is clamped to the voltage at EN/SSx minus 1.3V. The capacitance of the soft-start capacitors sets the soft-starting time and enable delay time. Setting the soft-starting time too short might create undesirable overshoot at the output during start-up. It is recommended that the soft-starting time be greater than 1.0ms. Please do not float this pin.

The typical soft-start time is set according to Equation 1:

$$t_{SSx} = 0.8V\left(\frac{C_{SSx}}{1.55\mu A}\right) \quad \text{(EQ. 1)}$$

G4 (Pin 9)

This pin is the open drain output of the linear regulator controller.

OCSET3, OCSET2, OCSET1 (Pin 15, 12, 7)

A resistor from this pin to ground sets the overcurrent threshold for the respective PWM.

$\overline{RST}$ (Pin 8)

Reset pulse output. This pin outputs a logic LOW signal after PGOOD toggles to low for 5.5µs (TYP). It can be used to reset system.

Refer to Figure 1 for detailed time sequence with early warning function.

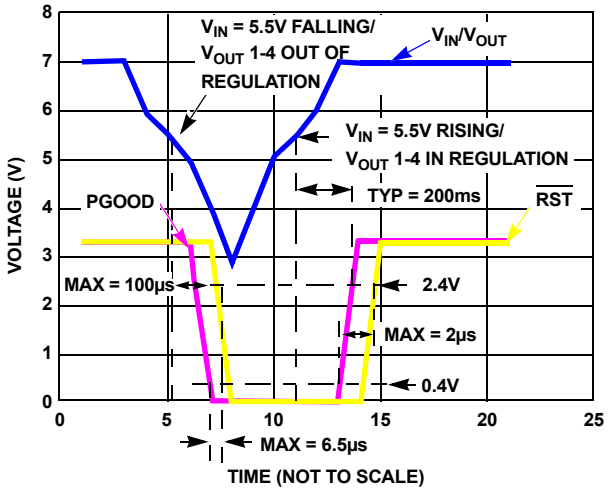


FIGURE 1. PGOOD AND $\overline{RST}$ TIMING

Typical Performance Curves

(Oscilloscope Plots are Taken Using the ISL9440BEVAL1Z Evaluation Board, V_{IN} = 19V Unless Otherwise Noted).

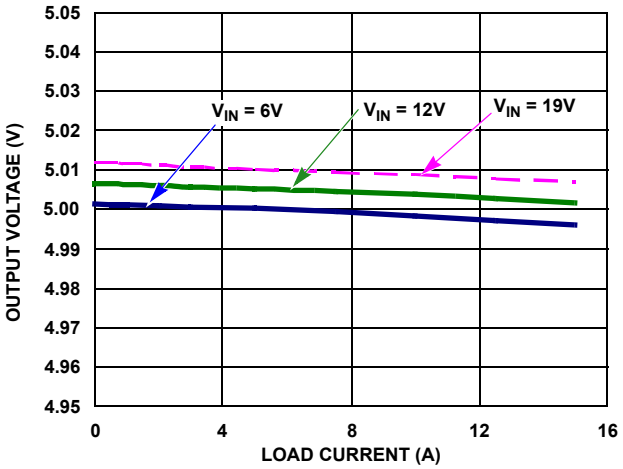


FIGURE 2. PWM1 LOAD REGULATION

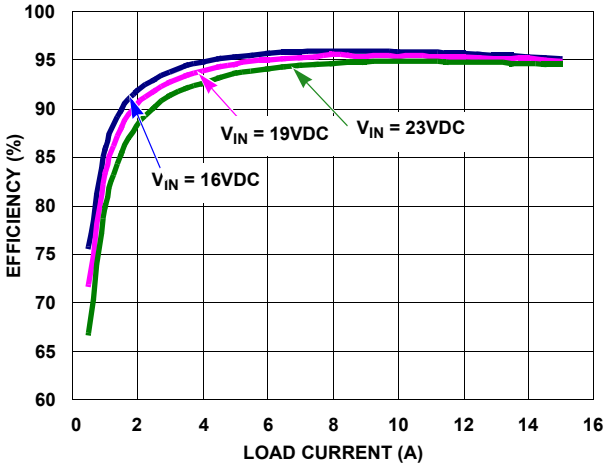


FIGURE 3. PWM1 EFFICIENCY vs LOAD (V_O = 5.0V), RJK0305DPB FOR UPPER MOSFET AND RJK0301DPB FOR LOWER MOSFET

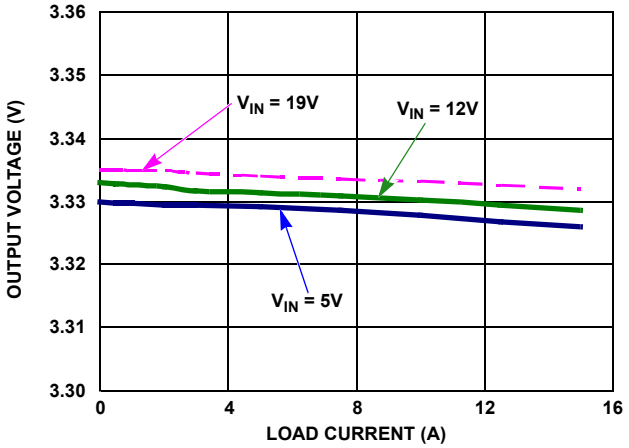


FIGURE 4. PWM2 LOAD REGULATION

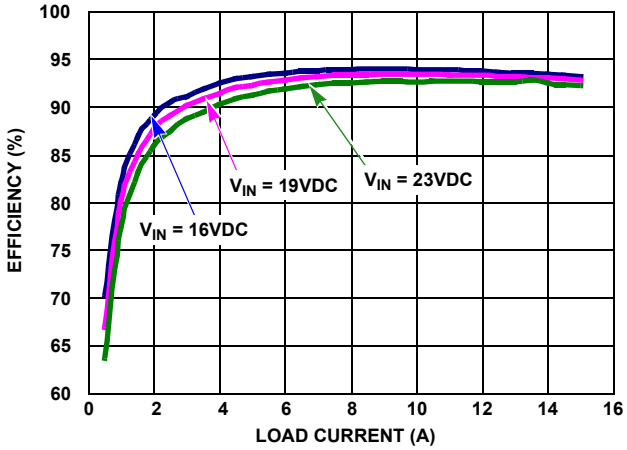


FIGURE 5. PWM2 EFFICIENCY vs LOAD (V_O = 3.3V), RJK0305DPB FOR UPPER MOSFET AND RJK0301DPB FOR LOWER MOSFET

Typical Performance Curves (Continued)

(Oscilloscope Plots are Taken Using the ISL9440BEVAL1Z Evaluation Board, V_{IN} = 19V Unless Otherwise Noted).

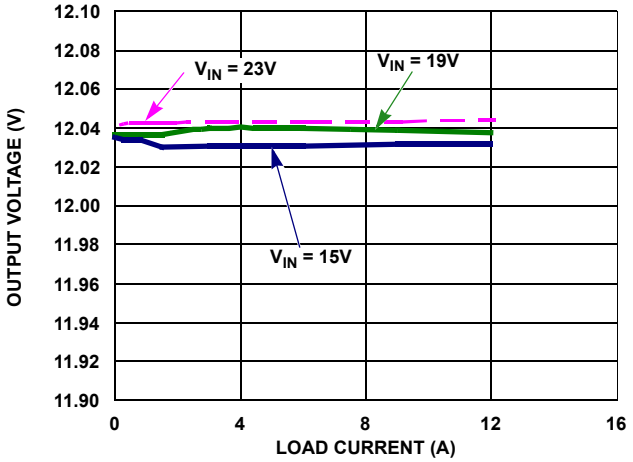


FIGURE 6. PWM3 LOAD REGULATION

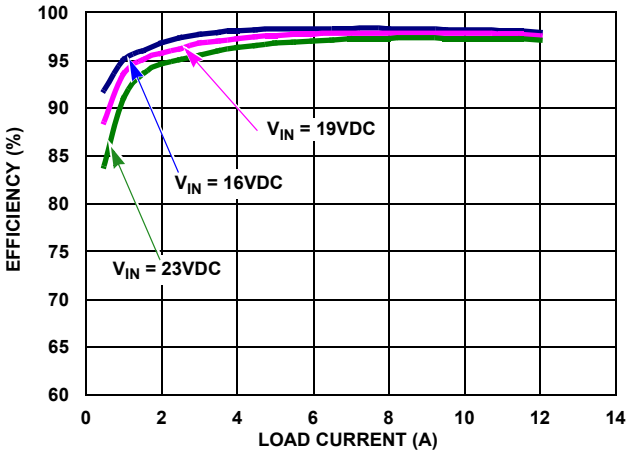


FIGURE 7. PWM3 EFFICIENCY vs LOAD (V_O = 12V), RJK0304DPB FOR UPPER MOSFET AND RJK0301DPB FOR LOWER MOSFET

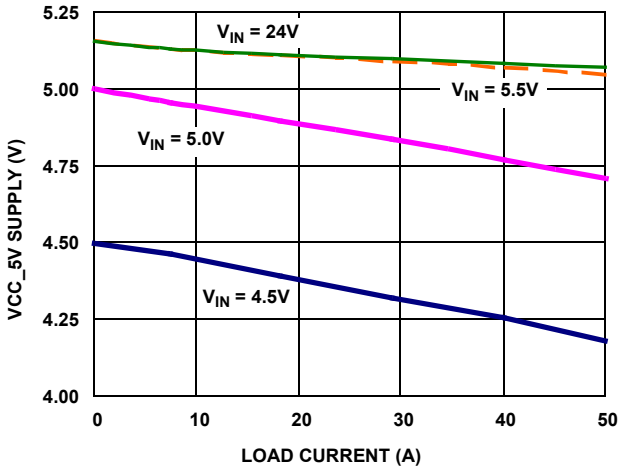


FIGURE 8. VCC_5V vs SUPPLY

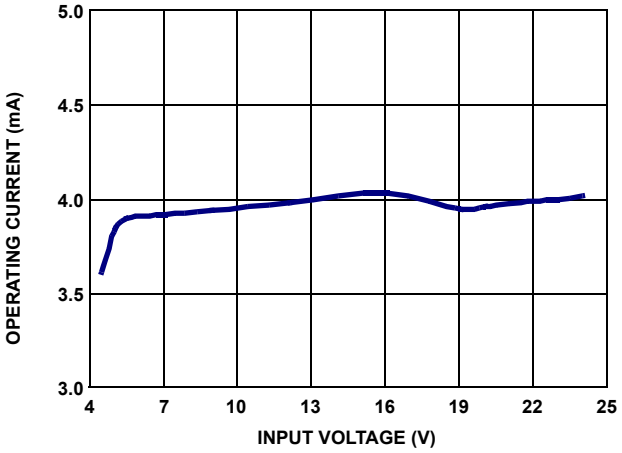


FIGURE 9. OPERATING CURRENT vs V_{IN} (RPG = RRST = 100kΩ, R_{OCSET} = 121kΩ)

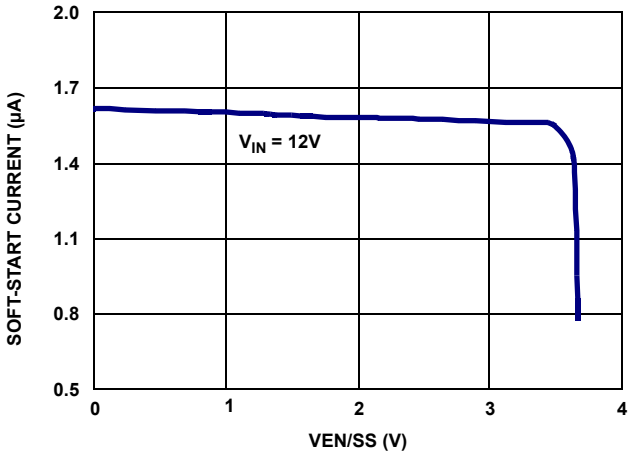


FIGURE 10. SOFT-START CURRENT vs VEN/SS

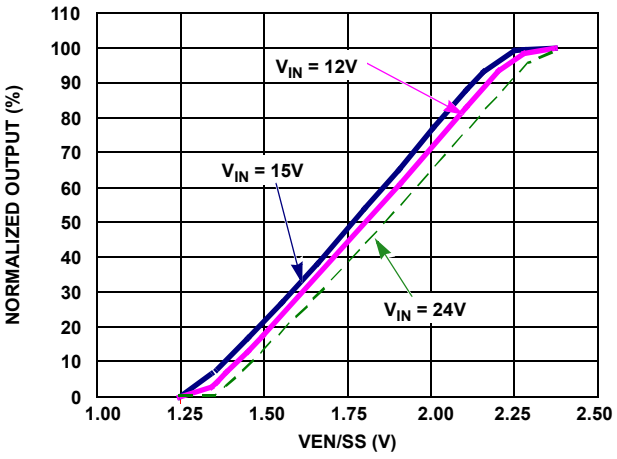


FIGURE 11. NORMALIZED OUTPUT VOLTAGE vs VEN/SS

Typical Performance Curves (Continued)

(Oscilloscope Plots are Taken Using the ISL9440BEVAL1Z Evaluation Board, V_{IN} = 19V Unless Otherwise Noted).

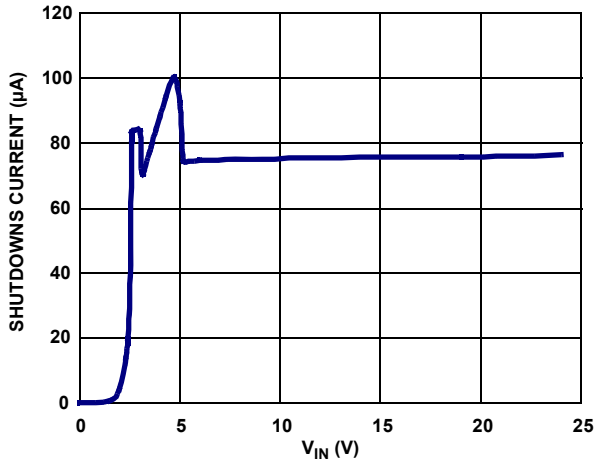


FIGURE 12. SHUTDOWN CURRENT vs V_{IN} (PGOOD and RST FLOATING)

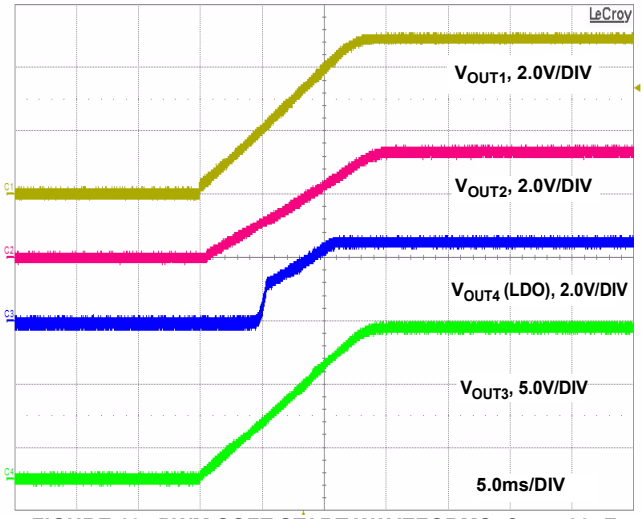


FIGURE 13. PWM SOFT-START WAVEFORMS, C_{SS} = 22nF

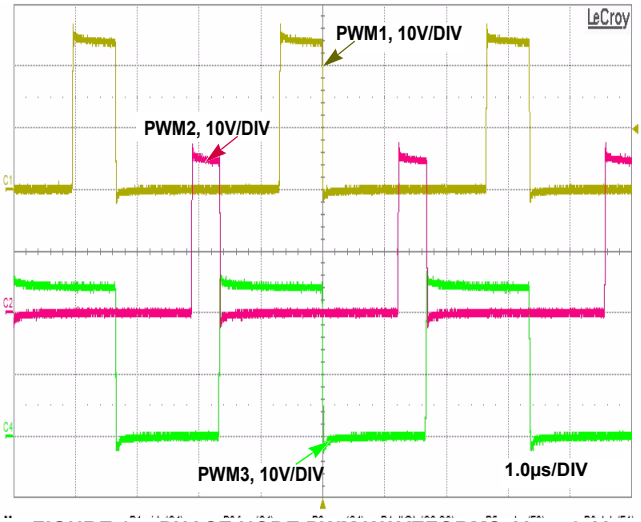


FIGURE 14. PHASE NODE PWM WAVEFORMS, V_{IN} = 24V

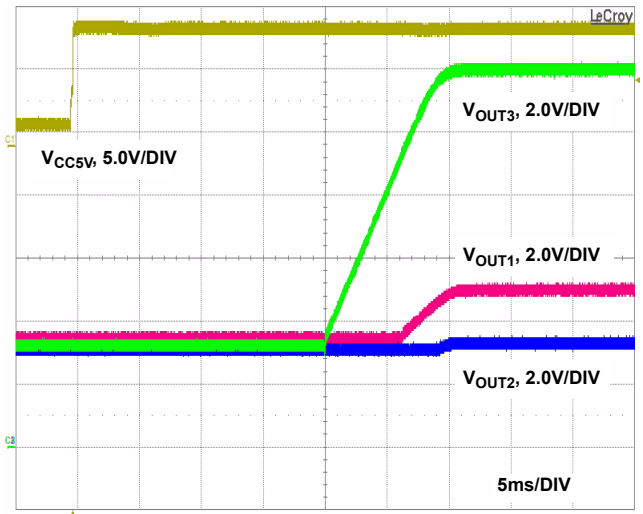


FIGURE 15. PWM SOFT-START WAVEFORMS, PRE-BIASED, C_{SS} = 22nF

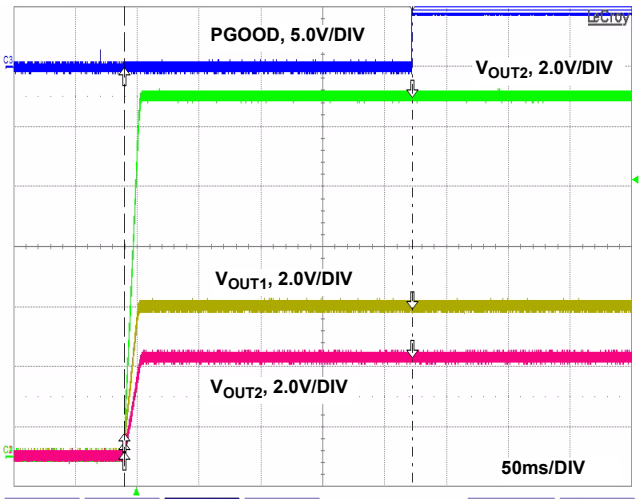


FIGURE 16. PGOOD RISING AFTER START UP

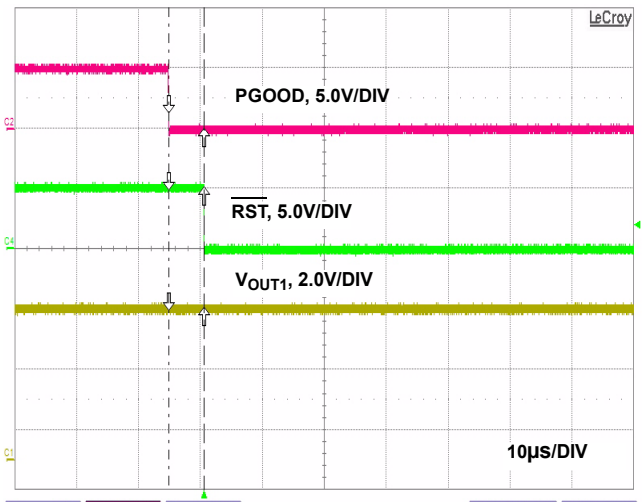


FIGURE 17. PGOOD FALLING TO RST FALLING

Typical Performance Curves (Continued)

(Oscilloscope Plots are Taken Using the ISL9440BEVAL1Z Evaluation Board, V_{IN} = 19V Unless Otherwise Noted).

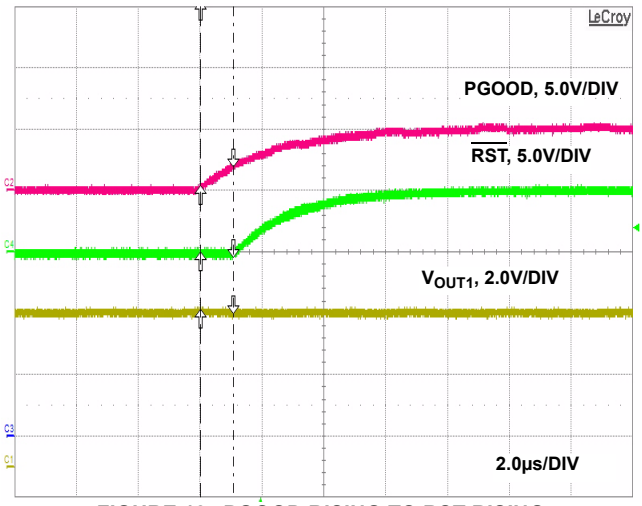


FIGURE 18. PGOOD RISING TO RST RISING

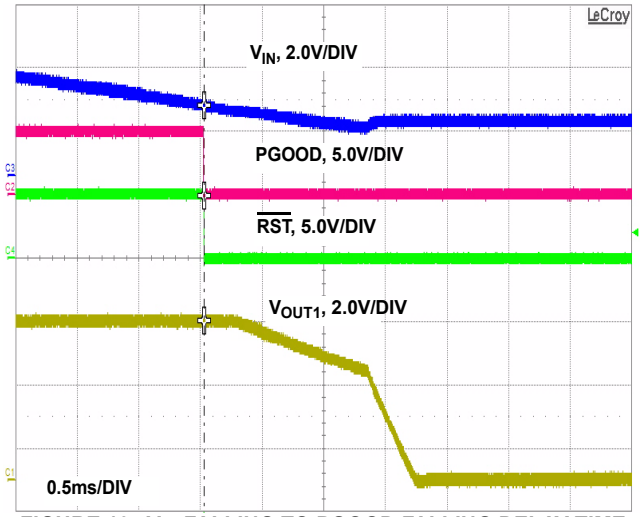


FIGURE 19. V_{IN} FALLING TO PGOOD FALLING DELAY TIME

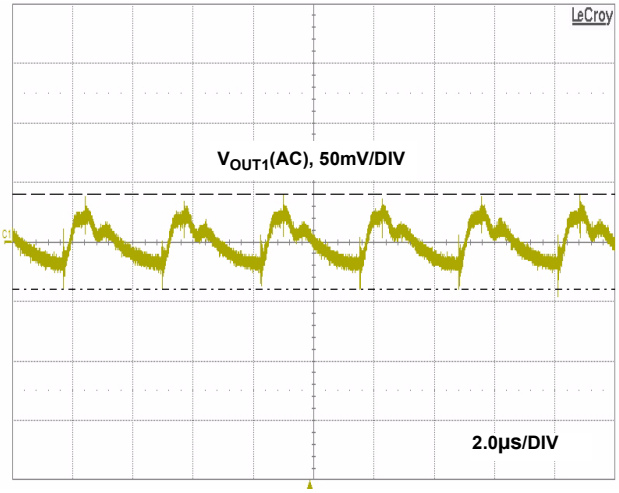


FIGURE 20. PWM1 OUTPUT RIPPLE UNDER MAX LOAD (V_{IN} = 23V, I_{O1} = I_{O2} = 15A, I_{O3} = 12A, FULL BANDWIDTH)

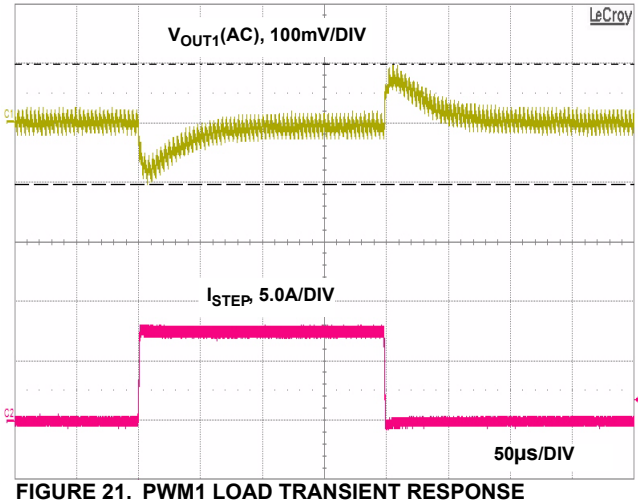


FIGURE 21. PWM1 LOAD TRANSIENT RESPONSE (LOAD STEP FROM 3.75A TO 11.25A)

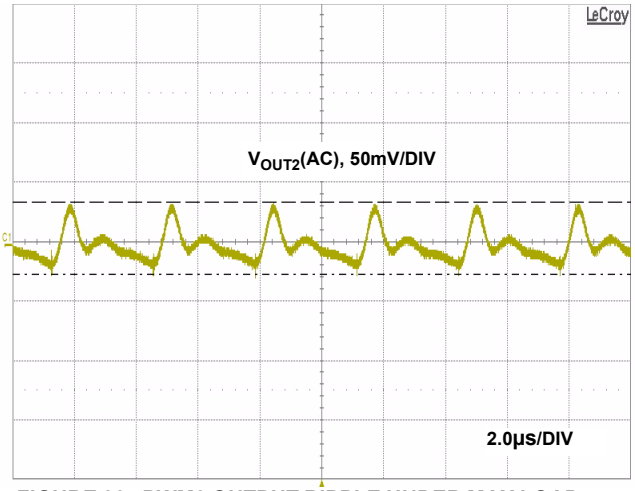


FIGURE 22. PWM2 OUTPUT RIPPLE UNDER MAX LOAD (V_{IN} = 23V, I_{O1} = I_{O2} = 15A, I_{O3} = 12A, FULL BANDWIDTH)

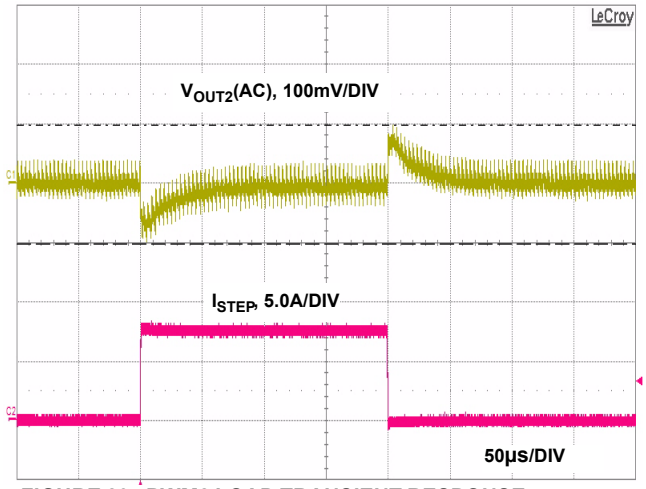


FIGURE 23. PWM2 LOAD TRANSIENT RESPONSE (LOAD STEP FROM 3.75A TO 11.25A)

Typical Performance Curves (Continued)

(Oscilloscope Plots are Taken Using the ISL9440BEVAL1Z Evaluation Board, V_{IN} = 19V Unless Otherwise Noted).

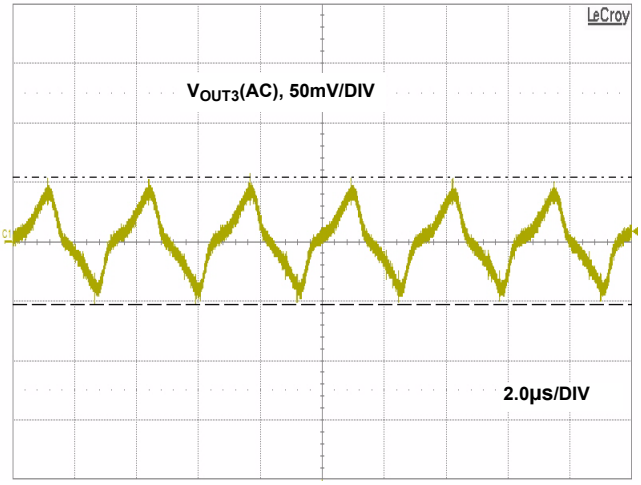


FIGURE 24. PWM3 OUTPUT RIPPLE UNDER MAX LOAD (V_{IN} = 23V, I_{O1} = I_{O2} = 15A, I_{O3} = 12A, FULL BANDWIDTH)

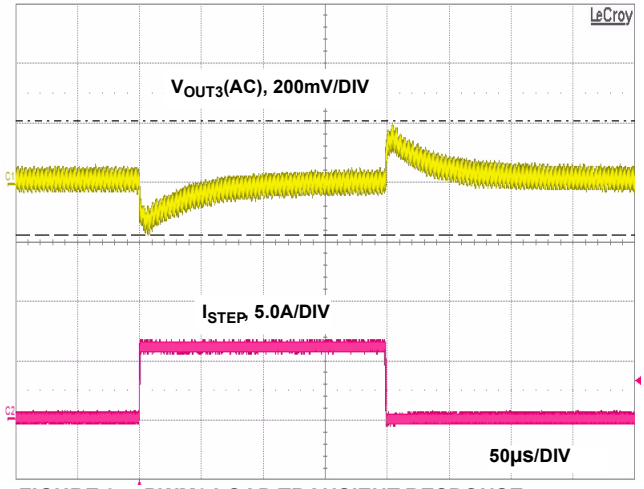


FIGURE 25. PWM3 LOAD TRANSIENT RESPONSE (LOAD STEP FROM 3A TO 9A)

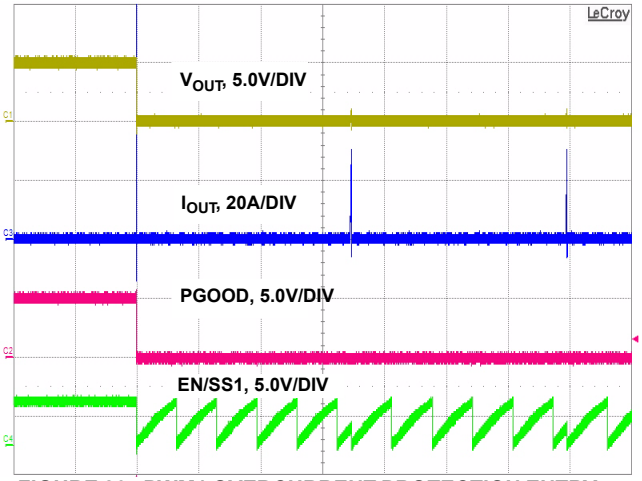


FIGURE 26. PWM1 OVERCURRENT PROTECTION ENTRY WAVEFORM

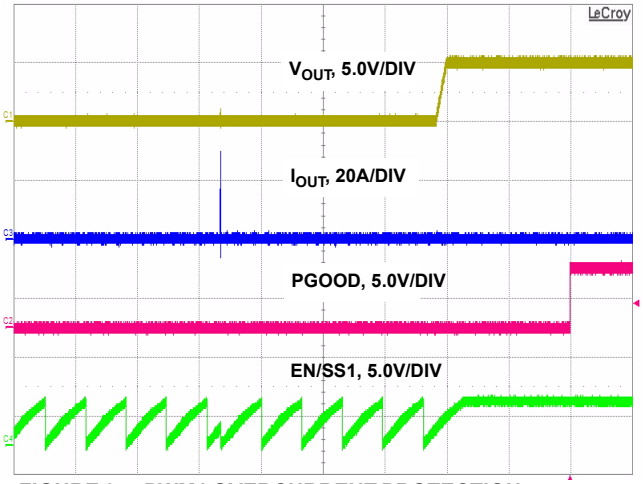


FIGURE 27. PWM1 OVERCURRENT PROTECTION RECOVERY WAVEFORM

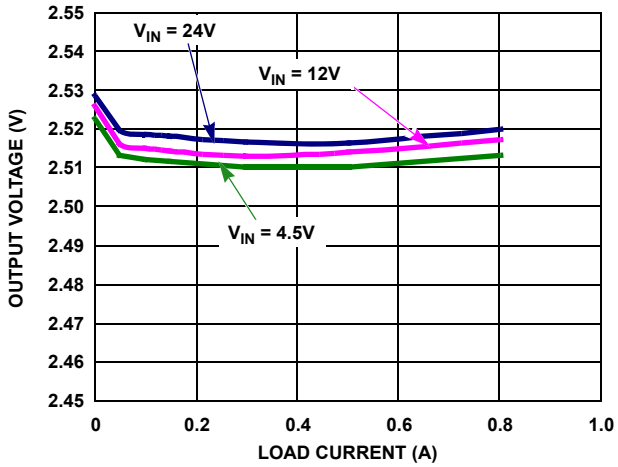


FIGURE 28. LDO LOAD REGULATION

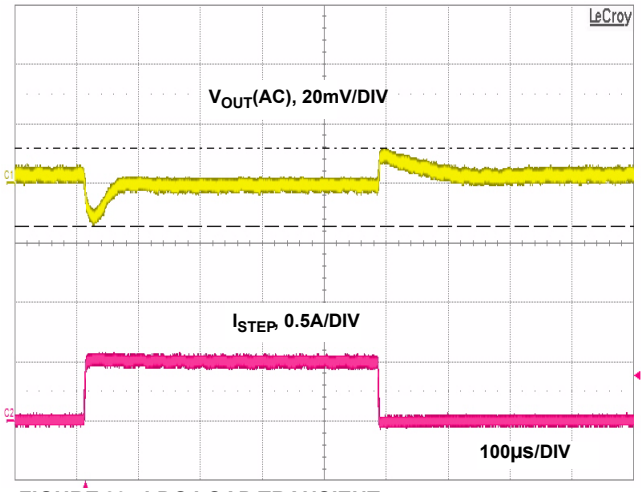


FIGURE 29. LDO LOAD TRANSIENT (LOAD STEP FROM 0.1A TO 0.6A)

Typical Performance Curves (Continued)

(Oscilloscope Plots are Taken Using the ISL9440BEVAL1Z Evaluation Board, V_{IN} = 19V Unless Otherwise Noted).

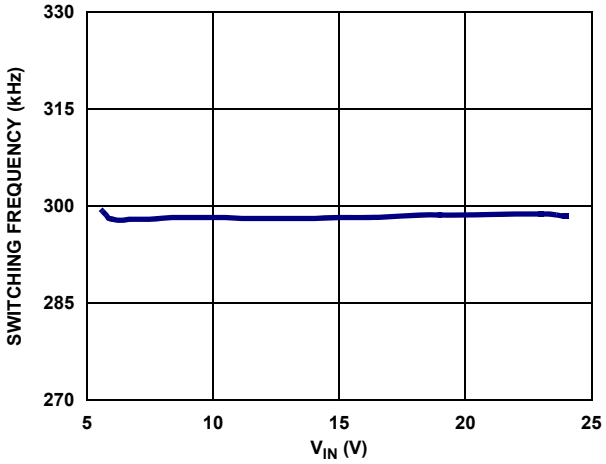


FIGURE 30. SWITCHING FREQUENCY vs V_{IN}

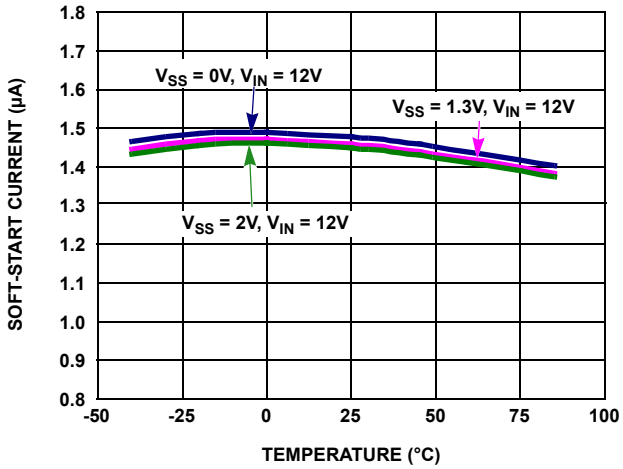


FIGURE 31. SOFT-START CURRENT vs TEMPERATURE

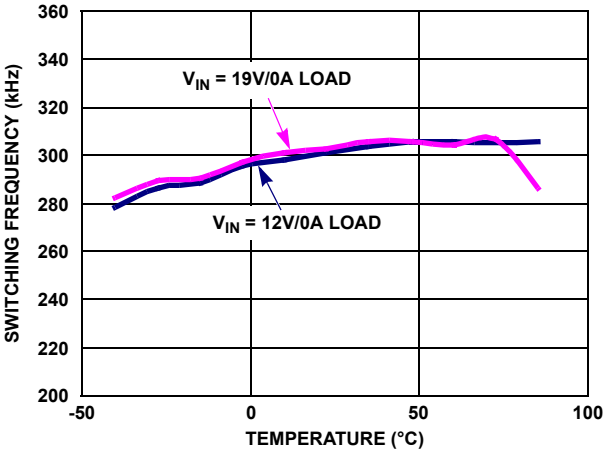


FIGURE 32. SWITCHING FREQUENCY vs TEMPERATURE

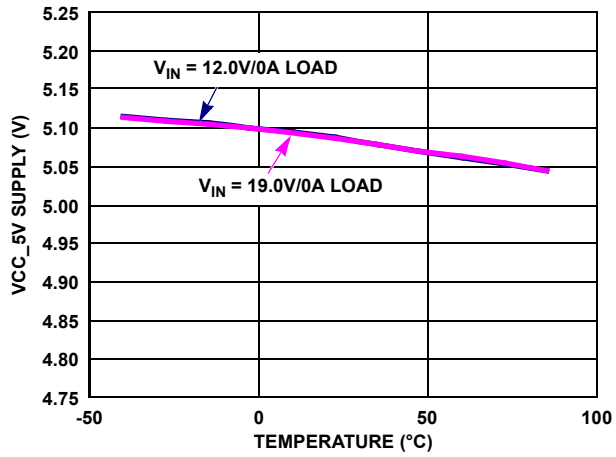


FIGURE 33. VCC_5V vs TEMPERATURE

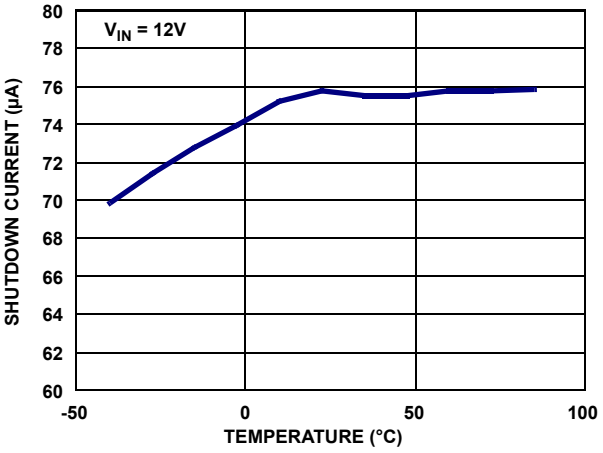


FIGURE 34. SHUTDOWN CURRENT vs TEMPERATURE

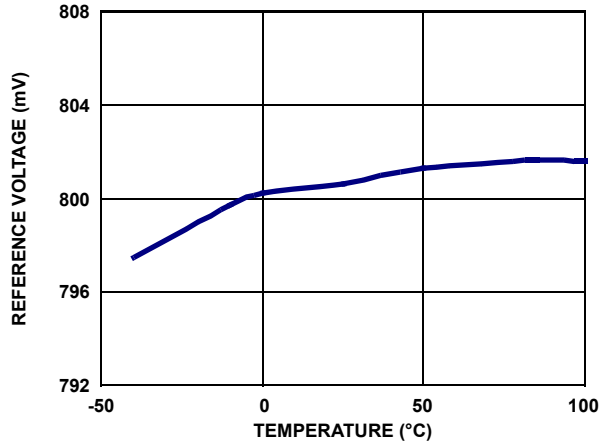


FIGURE 35. REFERENCE VOLTAGE vs TEMPERATURE

Typical Performance Curves of ISL9440C

(Oscilloscope Plots are Taken Using the ISL9440CEVAL1Z Evaluation Board, V_{IN} = 12V Unless Otherwise Noted).

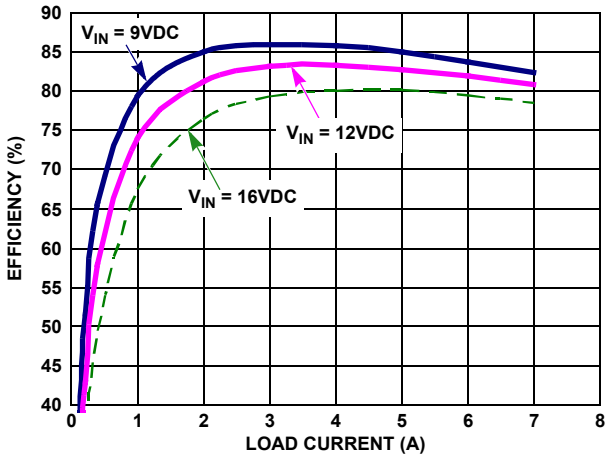


FIGURE 36. PWM1 EFFICIENCY vs LOAD (V_O = 1.0V, IRF7907 FOR UPPER MOSFET AND LOWER MOSFET)

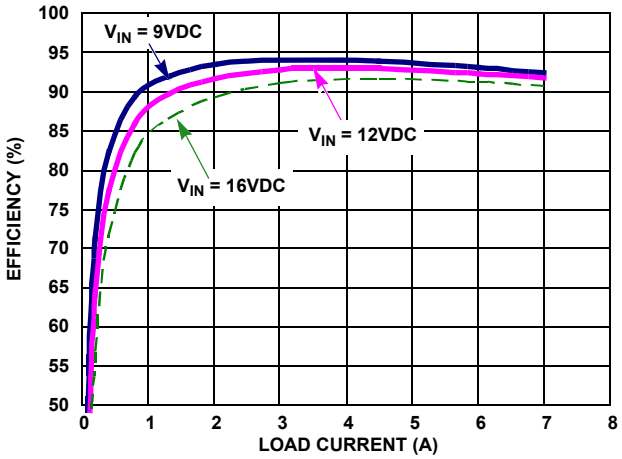


FIGURE 37. PWM2 EFFICIENCY vs LOAD (V_O = 3.3V, IRF7907 FOR UPPER MOSFET AND LOWER MOSFET)

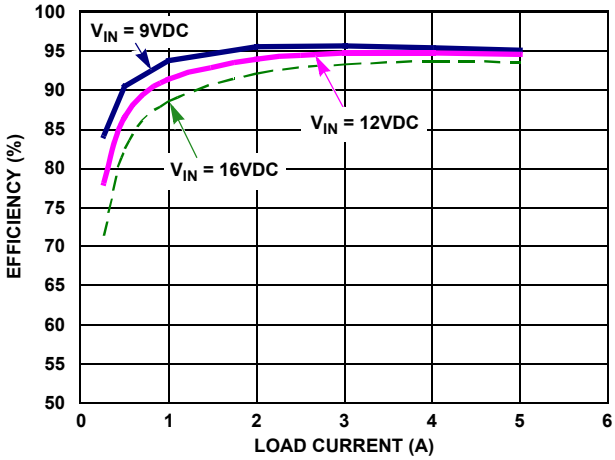


FIGURE 38. PWM3 EFFICIENCY vs LOAD (V_O = 5.0V, IRF7907 FOR UPPER MOSFET AND LOWER MOSFET)

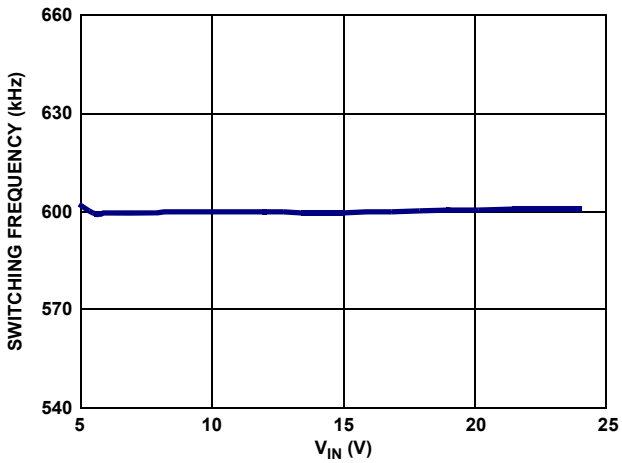


FIGURE 39. SWITCHING FREQUENCY vs V_{IN}

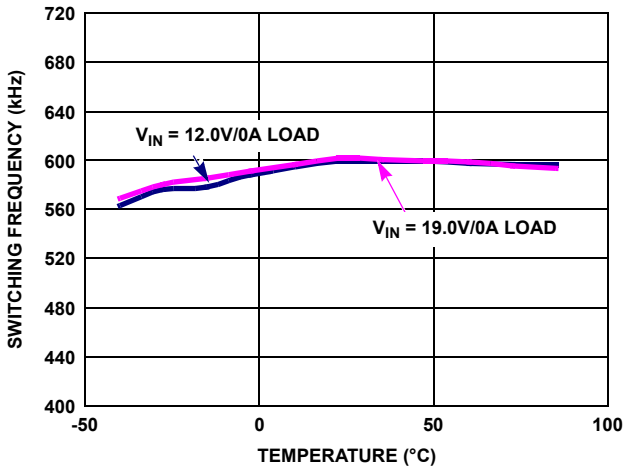


FIGURE 40. SWITCHING FREQUENCY vs TEMPERATURE

Functional Description

General Description

The ISL9440B and ISL9440C integrate control circuits for three synchronous buck converters and one linear controller. The three synchronous bucks operate out-of-phase to substantially reduce the input ripple and thus reduce the input filter requirements. Each part has 3 control lines (EN/SS1, EN/SS2 and EN/SS3), which provide independent control and programmable soft-start for each of the synchronous buck outputs.

The buck PWM controllers employ free-running frequency of 300kHz (ISL9440B) and 600kHz (ISL9440C). The current mode control scheme with an input voltage feed-forward ramp input to the PWM modulator provides an excellent rejection of input voltage variations and simplifies loop compensation design.

The linear controller can drive either a PNP bipolar junction transistor or P-Channel MOSFET to provide ultra low-dropout regulation with programmable voltages.

Internal 5V Linear Regulator (VCC_5V)

All ISL9440B and ISL9440C functions are internally powered from an on-chip, low dropout 5V regulator. The maximum regulator input voltage is 24V. Bypass the regulator's output (VCC_5V) with a 4.7µF capacitor to ground. The dropout voltage for this LDO is typically 600mV, so when V_{IN} is greater than 5.6V, VCC_5V is typically 5V. The ISL9440B and ISL9440C also employ an undervoltage lockout circuit that disables both regulators when VCC_5V falls below 3.7V.

The internal LDO can source over 60mA to supply the IC, power the low-side gate drivers and charge the external boot capacitor. When driving large FETs especially at 300kHz frequency, little or no regulator current may be available for external loads.

For example, a single large FET with 15nC total gate charge requires 15nC x 300kHz = 4.5mA (15nC x 600kHz = 9mA). Also, at higher input voltages with larger FETs, the power dissipation across the internal 5V will increase. Excessive dissipation across this regulator must be avoided to prevent junction temperature rise. Larger FETs can be used with 5V ±10% input applications. The thermal overload protection circuit will be triggered, if the VCC_5V output is short-circuit. Connect VCC_5V to V_{IN} for 5V ±10% input applications.

Enable Signals and Soft-Start Operation

The typical applications for the ISL9440B and ISL9440C are using programmable analog soft-start. The soft-start time can be set by the value of the soft-start capacitors connected from the EN/SSx pins to the ground. The start-up in-rush current can be alleviated by adjusting the soft starting time.

After the VCC_5V pin reaches the UVLO threshold, the ISL9440B and ISL9440C soft-start circuitry becomes active. The internal 1.55µA charge current begins charging up the soft-start capacitors connected from the EN/SSx pin to the GND. The PWM output remains inactive until the voltage on the corresponding EN/SSx pin reaches 1.3V. After that, the reference voltage is clamped to the voltage on the EN/SSx pin minus 1.3V. Then the output voltage ramps up with the voltage on EN/SSx until the voltage reaches 2.1V. The charging continues until the voltage on the EN/SSx reaches 3.5V.

Each PWM output can be disabled by pulling the corresponding EN/SSx to the ground.

PGOOD will not toggle to high until soft-start is complete and all the four outputs are up and in regulations.

Output Voltage Programming

The ISL9440B and ISL9440C use a precision internal reference voltage to set the output voltage. Based on this internal reference, the output voltage can thus be set from 0.8V up to a level determined by the input voltage, the maximum duty cycle, and the conversion efficiency of the circuit.

A resistive divider from the output to ground sets the output voltage of either PWM channel. The center point of the divider shall be connected to the FBx pin. The output voltage value is determined by Equation 2.

$$V_{OUTx} = 0.8V\left(\frac{R1 + R2}{R2}\right) \quad \text{(EQ. 2)}$$

Where R1 is the top resistor of the feedback divider network and R2 is the resistor connected from FBx to ground.

Out-of-Phase Operation

To reduce input ripple current, Channel 1 and Channel 2 operate 180° out-of-phase, Channel 3 keeps 0° phase with Channel 1. Channel 1 and Channel 2 typically output higher load compared to Channel 3 because of their stronger drivers. This reduces the input capacitor ripple current requirements, reduces power supply-induced noise, and improves EMI. This effectively helps to lower component cost, save board space and reduce EMI.

Triple PWMs typically operate in-phase and turn on both upper FETs at the same time. The input capacitor must then support the instantaneous current requirements of the three switching regulators simultaneously, resulting in increased ripple voltage and current. The higher RMS ripple current lowers the efficiency due to the power loss associated with the ESR of the input capacitor. This typically requires more low-ESR capacitors in parallel to minimize the input voltage ripple and ESR-related losses, or to meet the required ripple current rating.

With synchronized out-of-phase operation, the high-side MOSFETs turn on 180° out-of-phase. The instantaneous input current peaks of both regulators no longer overlap, resulting in reduced RMS ripple current and input voltage ripple. This reduces the required input capacitor ripple current rating, allowing fewer or less expensive capacitors, and reducing the shielding requirements for EMI. The typical operating curves show the synchronized 180° out-of-phase operation.

Input Voltage Range

The ISL9440B and ISL9440C are designed to operate from input supplies ranging from 4.5V to 24V.

For 5V ±10% input applications, the ISL9441 is suggested. The reason is that V_{IN} and VCC_5V Pin should be tied together for this input application. The early warning function will pull PGOOD and $\overline{RST}$ low for ISL9440B and ISL9440C.

The input voltage range can be effectively limited by the available maximum duty cycle (D_{MAX} = 93% for ISL9440B, and D_{MAX} = 86% for ISL9440C), as shown in Equation 3.

$$V_{IN(min)} = \left(\frac{V_{OUT} + V_{d1}}{0.93}\right) + V_{d2} - V_{d1} \quad \text{(EQ. 3)}$$

Where:
V_{d1} = Sum of the parasitic voltage drops in the inductor discharge path, including the lower FET, inductor and PC board.
V_{d2} = Sum of the voltage drops in the charging path, including the upper FET, inductor and PC board resistances.

The maximum input voltage and minimum output voltage is limited by the minimum ON-time ($t_{ON(min)}$).(see Equation 4).

$$V_{IN(max)} \leq \frac{V_{OUT}}{t_{ON(min)} \times 300kHz} \quad \text{(EQ. 4)}$$

where, $t_{ON(min)}$ = 30ns

Gate Control Logic

The gate control logic translates generated PWM signals into gate drive signals providing amplification, level shifting and shoot-through protection. The gate drivers have some circuitry that helps optimize the IC performance over a wide range of operational conditions. As MOSFET switching times can vary dramatically from type to type and with input voltage, the gate control logic provides adaptive dead-time by monitoring real gate waveforms of both the upper and the lower MOSFETs. Shoot-through control logic provides a 20ns dead-time to ensure that both the upper and lower MOSFETs will not turn on simultaneously and cause a shoot-through condition.

Gate Drivers

The low-side gate driver is supplied from VCC_5V and provides a peak sink current of 2A/2A/200mA and source current of 800mA/800mA/400mA for Channels 1, 2, 3 respectively. The high-side gate driver is also capable of delivering the same current as those in low-side gate driver. Gate-drive voltages for the upper N-Channel MOSFET are generated by the flying capacitor boot circuit. A boot capacitor connected from the BOOT pin to the PHASE node provides power to the high-side MOSFET driver. To limit the peak current in the IC, an external resistor may be placed between the UGATE pin and the gate of the external MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

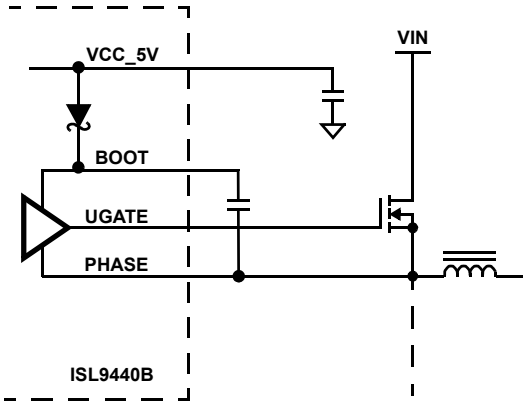


FIGURE 41.

At start-up, the low-side MOSFET turns on and forces PHASE to ground in order to charge the BOOT capacitor to 5V. After the low-side MOSFET turns off, the high-side MOSFET is turned on by closing an internal switch between BOOT and UGATE. This provides the necessary gate-to-source voltage to turn on the upper MOSFET, an action that boosts the 5V gate drive signal above VIN. The current required to drive the upper MOSFET is drawn from the internal 5V regulator.

Adaptive Dead Time

The ISL9440B and ISL9440C incorporate an adaptive dead-time algorithm on the synchronous buck PWM controllers that optimizes operation with varying MOSFET conditions. This algorithm provides an approximately 20ns of dead-time between switching the upper and lower MOSFETs. This dead time is adaptive and allows operation with different MOSFETs without having to externally adjust the dead-time using a resistor or capacitor. During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a 1V threshold, at which time the UGATE is released to rise. Adaptive dead time circuitry monitors the upper MOSFET gate voltage during UGATE turn-off. Once the upper MOSFET gate-to-source voltage has dropped below a threshold of 1V, the LGATE is allowed to rise.

Internal Bootstrap Diode

The ISL9440B and ISL9440C have integrated bootstrap diodes to help reduce total cost and reduce layout complexity. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap capacitor must have a maximum voltage rating above the maximum battery voltage plus 5V. The bootstrap capacitor can be chosen from Equation 5.

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}} \quad \text{(EQ. 5)}$$

Where Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET. The ΔV_{BOOT} term is defined as the allowable droop in the rail of the upper drive.

As an example, suppose an upper MOSFET has a gate charge (QGATE) of 25nC at 5V and also assume the droop in the drive voltage over a PWM cycle is 200mV. One will find that a bootstrap capacitance of at least 0.125µF is required. The next larger standard value capacitance is 0.22µF. A good quality ceramic capacitor is recommended.

Protection Circuits

The converter output is monitored and protected against overload, short circuit and undervoltage conditions. A sustained overload on the output sets the PGOOD low and initiates hiccup mode.

Undervoltage Lockout

The ISL9440B and ISL9440C include VCC UVLO protection that will keep the devices in a reset condition until a proper operating voltage is applied and that will also shut down the ISL9440B and ISL9440C if the operating voltage drops below a pre-defined value. All controllers are disabled when UVLO is asserted. When UVLO is asserted, PGOOD will be valid and de-asserted.

Overcurrent Protection

All the PWM controllers use the lower MOSFETs ON-resistance, $r_{DS(ON)}$, to monitor the current in the converter. The sensed voltage drop is compared with a threshold set by a resistor connected from the OCSETx pin to ground.

$$R_{OCSET} = \frac{(7)(R_{CS})}{(I_{OC})(r_{DS(ON)})} \quad \text{(EQ. 6)}$$

Where, I_{OC} is the desired overcurrent protection threshold, and R_{CS} is a value of the current sense resistor connected to the ISENx pin.

When an overcurrent is detected, the upper MOSFET remains off and the lower MOSFET remains on until the current drops below I_{OC}. As a result, the converter skips PWM pulses. When the overload condition is removed, the converter will resume normal operation. This action will protect the converter against overcurrent conditions at temporary overload or during high di/dt load transient. The converter remains active and can return to normal operation immediately after the overcurrent is removed.

When the overload condition persists or at output short circuit conditions, the overcurrent condition lasts for more than 2 consecutive cycles. When the overcurrent is detected for 2 consecutive clock cycles, the IC enters a hiccup mode by turning off the gate drivers and entering into soft-start. The IC will cycle 5 times through soft-start before trying to restart. The IC will continue to cycle through soft-start until the overcurrent condition is removed. Hiccup mode is active during soft-start so care must be taken to ensure that the peak inductor current does not exceed the overcurrent threshold during soft-start.

Because of the nature of this current sensing technique, and to accommodate a wide range of $r_{DS(ON)}$ variations, the value of the overcurrent threshold should represent an overload current about 150% to 180% of the maximum operating current. If more accurate current protection is desired, place a current sense resistor in series with the lower MOSFET source and connect R_{CS} to the source of the MOSFET.

Overvoltage Protection

All switching controllers within the ISL9440B and ISL9440C have fixed overvoltage set points. The overvoltage set point is set at 118% of the nominal output voltage, the output voltage set by the feedback resistors. In the case of an overvoltage event, the IC will attempt to bring the output voltage back into regulation by keeping the upper MOSFET turned off and modulating the lower MOSFET for 2 consecutive PWM cycles. If the overvoltage condition has not been corrected in 2 cycles and the output voltage is above 118% of the nominal output voltage, the ISL9440B and ISL9440C will turn off both the upper MOSFET and the lower MOSFET. The ISL9440B and ISL9440C will enter hiccup mode until the output voltage return to 110% of the nominal output voltage.

Over-Temperature Protection

The IC incorporates an over-temperature protection circuit that shuts the IC down when a die temperature of +150°C is reached. Normal operation resumes when the die temperatures drops below +130°C through the initiation of a full soft-start cycle.

Feedback Loop Compensation

To reduce the number of external components and to simplify the process of determining compensation components, all PWM controllers have internally compensated error amplifiers. To make internal compensation possible several design measures were taken.

First, the ramp signal applied to the PWM comparator is proportional to the input voltage provided via the VIN pin. This keeps the modulator gain constant with variation in the input voltage. Second, the load current proportional signal is derived from the voltage drop across the lower MOSFET during the $\overline{PWM}$ time interval and is subtracted from the amplified error signal on the comparator input. This creates an internal current control loop. The resistor connected to the ISEN pin sets the gain in the current feedback loop. Equation 7 estimates the required value of the current sense resistor depending on the maximum operating load current and the value of the MOSFETs $r_{DS(ON)}$.

$$R_{CS} \geq \frac{(I_{MAX})(r_{DS(ON)})}{30\mu A} \quad \text{(EQ. 7)}$$

Choosing R_{CS} to provide 30µA of current to the current sample and hold circuitry is recommended, but values down to 2µA

and up to 100µA can be used. The higher sampling current will help to stabilize the loop.

Due to the current loop feedback, the modulator has a single pole response with -20dB slope at a frequency determined by the load, as shown in Equation 8.

$$F_{PO} = \frac{1}{2\pi \cdot R_O \cdot C_O} \quad \text{(EQ. 8)}$$

Where, R_O is load resistance and C_O is load capacitance. For this type of modulator, a Type 2 compensation circuit is usually sufficient.

Figure 42 shows a Type 2 amplifier and its response along with the responses of the current mode modulator and the converter. The Type 2 amplifier, in addition to the pole at origin, has a zero-pole pair that causes a flat gain region at frequencies in between the zero and the pole.

$$F_Z = \frac{1}{2\pi \cdot R_2 \cdot C_1} = 6\text{kHz} \quad \text{(EQ. 9)}$$

$$F_P = \frac{1}{2\pi \cdot R_1 \cdot C_2} = 600\text{kHz} \quad \text{(EQ. 10)}$$

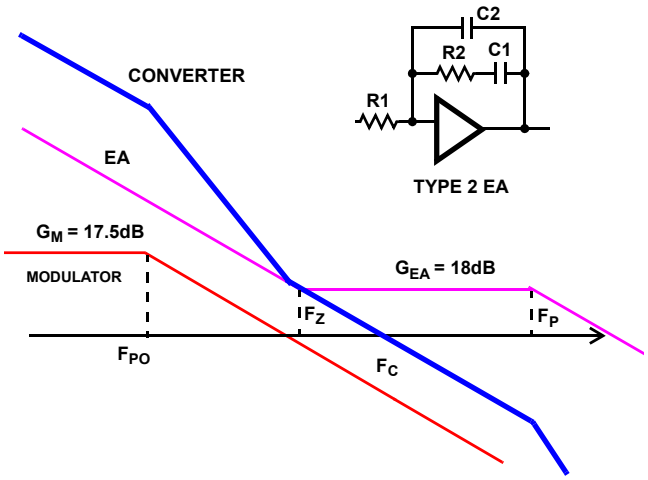


FIGURE 42. FEEDBACK LOOP COMPENSATION

The zero frequency, the amplifier high-frequency gain, and the modulator gain are chosen to satisfy most typical applications. The crossover frequency will appear at the point where the modulator attenuation equals the amplifier high frequency gain. The only task that the system designer has to complete is to specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. With this type of compensation plenty of phase margin is easily achieved due to zero-pole pair phase ‘boost’.

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within the 1.2kHz to 30kHz range gives some additional phase ‘boost’. Some phase boost can also be achieved by connecting capacitor C_Z in parallel with the upper resistor R_1 of the divider that sets the output voltage value. Please refer to “Output Capacitor Selection” on page 22 and “Input Capacitor Selection” on page 23 for further details.

Linear Regulator

The linear regulator controller is a trans-conductance amplifier with a nominal gain of 2A/V. The N-Channel MOSFET output buffer can sink a minimum of 50mA.

The reference voltage is 0.8V. With 0V differential at its input, the controller sinks 21mA of current. For better load regulation, it is recommended that the resistor from the LDO input to the base of the PNP (or gate of the PFET) is set so that the sink current at G4 pin is within 9mA to 31mA over the entire load and temperature range.

An external PNP transistor or P-Channel MOSFET pass device can be used. The dominant pole for the loop can be placed at the base of the PNP (or gate of the PFET), as a capacitor from emitter-to-base (source to gate of a PFET). Better load transient response is achieved however, if the dominant pole is placed at the output with a capacitor to ground at the output of the regulator.

Under no-load conditions, leakage currents from the pass transistors supply the output capacitors, even when the transistor is off. Generally, this is not a problem since the feedback resistor drains the excess charge. However, charge may build up on the output capacitor making V_{LDO} rise above its set point. Care must be taken to insure that the feedback resistor’s current exceeds the pass transistors leakage current over the entire temperature range.

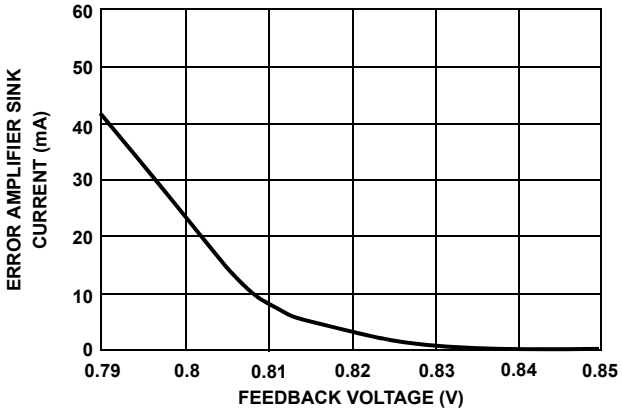


FIGURE 43. LINEAR CONTROLLER GAIN

The linear regulator output can be supplied by the output of one of the PWMs. When using a PFET, the output of the linear regulator will track the PWM supply after the PWM output rises to a voltage greater than the threshold of the PFET pass device. The voltage differential between the PWM and the linear output will be the load current times the $r_{DS(ON)}$.

Base-Drive Noise Reduction

The high-impedance base driver is susceptible to system noise, especially when the linear regulator is lightly loaded. Capacitively coupled switching noise or inductively coupled EMI onto the base drive causes fluctuations in the base current, which appear as noise on the linear regulator's output. Keep the base drive traces away from the step-down converter, and as short as possible, to minimize noise coupling. A resistor in series with the gate drivers reduces the switching noise generated by PWM. Additionally, a bypass capacitor may be placed across the base-to-emitter resistor. This bypass capacitor, in addition to the transistor's input capacitor, could bring in a second pole that will destabilize the linear regulator. Therefore, the stability requirements determine the maximum base-to-emitter capacitance.

Layout Guidelines

Careful attention to layout requirements is necessary for successful implementation of an ISL9440B and ISL9440C based DC/DC converter. The ISL9440B and ISL9440C switch at a very high frequency and therefore, the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. Also, the peak gate drive current rises significantly in an extremely short time. Transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, increase device overvoltage stress and ringing. Careful component selection and proper PC board layout minimizes the magnitude of these voltage spikes.

There are three sets of critical components in a DC/DC converter using the ISL9440B and ISL9440C: the controller, the switching power components and the small signal components. The switching power components are the most critical from a layout point of view because they switch a large amount of energy so they tend to generate a large amount of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bias currents. A multi-layer printed circuit board is recommended.

Layout Considerations

1. The Input capacitors, Upper FET, Lower FET, Inductor and Output capacitor should be placed first. Isolate these power components on the topside of the board with their ground terminals adjacent to one another. Place the input high frequency decoupling ceramic capacitor very close to the MOSFETs.
2. Use separate ground planes for power ground and small signal ground. Connect the SGND and PGND together close to the IC. Do not connect them together anywhere else.
3. The loop formed by Input capacitor, the top FET and the bottom FET must be kept as small as possible.
4. Ensure the current paths from the input capacitor to the MOSFET, to the output inductor and output capacitor are as short as possible with maximum allowable trace widths.
5. Place The PWM controller IC close to lower FET. The LGATE connection should be short and wide. The IC can be best placed over a quiet ground area. Avoid switching ground loop current in this area.
6. Place VCC_5V bypass capacitor very close to VCC_5V pin of the IC and connect its ground to the PGND plane.
7. Place the gate drive components BOOT diode and BOOT capacitors together near controller IC.
8. The output capacitors should be placed as close to the load as possible. Use short wide copper regions to connect output capacitors-to-load to avoid inductance and resistances.
9. Use copper filled polygons or wide but short trace to connect the junction of upper FET, Lower FET and output inductor. Also keep the PHASE node connection to the IC short. Do not unnecessarily oversize the copper islands for PHASE node. Since the phase nodes are subjected to very high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry will tend to couple switching noise.
10. Route all high speed switching nodes away from the control circuitry.
11. Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. All small signal grounding paths including feedback resistors, current limit setting resistors and ENx pull-down resistors should be connected to this SGND plane.
12. Separate current sensing traces from PHASE node connections
13. Ensure the feedback connection to the output capacitor is short and direct.

Component Selection Guidelines

MOSFET Considerations

The logic level MOSFETs are chosen for optimum efficiency given the potentially wide input voltage range and output power requirements. Two N-Channel MOSFETs are used in each of the synchronous-rectified buck converters for the 3 PWM outputs. These MOSFETs should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

The power dissipation includes two loss components; conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty cycle (see Equations 11 and 12). The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFET has significant

switching losses, since the lower device turns on and off into near zero voltage. The equations assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFETs body diode (see

$$P_{UPPER} = \frac{(I_O^2)(r_{DS(ON)})(V_{OUT})}{V_{IN}} + \frac{(I_O)(V_{IN})(t_{SW})(F_{SW})}{2} \quad \text{(EQ. 11)}$$

Equations 11 and 12).

$$P_{LOWER} = \frac{(I_O^2)(r_{DS(ON)})(V_{IN} - V_{OUT})}{V_{IN}} \quad \text{(EQ. 12)}$$

A large gate-charge increases the switching time, t_{SW}, which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications.

Output Inductor Selection

The PWM converters require output inductors. The output inductor is selected to meet the output voltage ripple requirements. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current and output capacitor(s) ESR. The ripple voltage expression is given beginning in the "Output Capacitor Selection" on page 22 and the ripple current is approximated by Equation 13:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_S)(L)(V_{IN})} \quad \text{(EQ. 13)}$$

Output Capacitor Selection

The output capacitors for each output have unique requirements. In general, the output capacitors should be selected to meet the dynamic regulation requirements including ripple voltage and load transients. Selection of output capacitors is also dependent on the output inductor, so some inductor analysis is required to select the output capacitors.

One of the parameters limiting the converter's response to a load transient is the time required for the inductor current to slew to its new level. The ISL9440B and ISL9440C will provide either 0% or maximum duty cycle in response to a load transient.

The response time is the time interval required to slew the inductor current from an initial current value to the load current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required. Also, if the load transient rise time is slower than the inductor response time, as in a hard drive or CD drive, it reduces the requirement on the output capacitor.

The maximum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is shown in Equation 14:

$$C_{OUT} = \frac{(L_O)(I_{TRAN})^2}{2(V_{IN} - V_O)(DV_{OUT})} \quad \text{(EQ. 14)}$$

where, C_{OUT} is the output capacitor(s) required, L_O is the output inductor, I_{TRAN} is the transient load current step, V_{IN} is the input voltage, V_O is output voltage, and DV_{OUT} is the drop in output voltage allowed during the load transient.

High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Equivalent Series Resistance) and voltage rating requirements as well as actual capacitance requirements.

The output voltage ripple is due to the inductor ripple current and the ESR of the output capacitors as defined by Equation 15:

$$V_{RIPPLE} = \Delta I_L(ESR) \quad \text{(EQ. 15)}$$

Where, ΔI_L is calculated in the "Output Inductor Selection" on page 22.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications at 300kHz (ISL9440B)/600kHz (ISL9440C) for the bulk capacitors. In most cases, multiple small-case electrolytic capacitors perform better than a single large-case capacitor.

The stability requirement on the selection of the output capacitor is that the 'ESR zero' (f_Z) be between 1.2kHz and 30kHz. This range is set by an internal, single compensation zero at 6kHz. The ESR zero can be a factor of five on either side of the internal zero and still contribute to increased phase margin of the control loop. Therefore:

$$C_{OUT} = \frac{1}{2\pi(ESR)(f_Z)} \quad \text{(EQ. 16)}$$

In conclusion, the output capacitors must meet three criteria:

1. They must have sufficient bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient.
2. The ESR must be sufficiently low to meet the desired output voltage ripple due to the output inductor current.
3. The ESR zero should be placed, in a rather large range, to provide additional phase margin.

The recommended output capacitor value for the ISL9440B and ISL9440C is between 150µF to 680µF, to meet stability criteria

with external compensation. Use of aluminum electrolytic (POSCAP) or tantalum type capacitors is recommended. Use of low ESR ceramic capacitors is possible but would take more rigorous loop analysis to ensure stability.

Input Capacitor Selection

The important parameters for the bulk input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25x greater than the maximum input voltage and 1.5x is a conservative guideline. The AC RMS Input current varies with the load. The total RMS current supplied by the input capacitance is shown in Equations 17 and 18:

$$I_{RMS} = \sqrt{I_{RMS1}^2 + I_{RMS2}^2} \quad \text{(EQ. 17)}$$

where,

$$I_{RMSx} = \sqrt{DC - DC^2} \cdot I_O \quad \text{(EQ. 18)}$$

DC is duty cycle of the respective PWM.

Depending on the specifics of the input power and its impedance, most (or all) of this current is supplied by the input capacitor(s). Figure 44 shows the advantage of having the PWM converters operating out-of-phase. If the converters were operating in-phase, the combined RMS current would be the algebraic sum, which is a much larger value as shown. The combined out-of-phase current is the square root of the sum of the square of the individual reflected currents and is significantly less than the combined in-phase current.

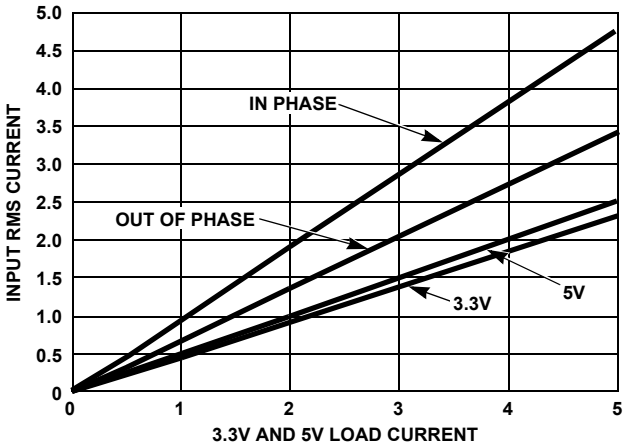


FIGURE 44. INPUT RMS CURRENT vs LOAD

Use a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For board designs that allow through-hole components, the Sanyo OS-CON™ series offer low ESR and good temperature performance. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX is surge current tested.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
February 18, 2016	FN6799.4	Updated the ordering information table on page 2. Added Revision History and About Intersil sections. Updated POD L32.5x5B to the latest revision. Changes are as follows: -Correct Note 4 from “Dimension b applies...” to “Dimension applies...” -Added triangles around Notes 4, 5 and 6

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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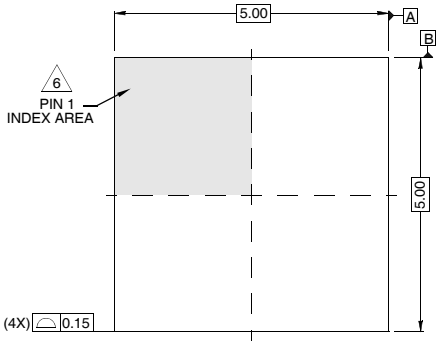
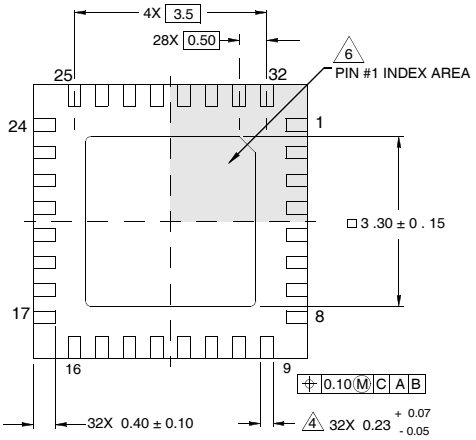
Package Outline Drawing

L32.5x5B

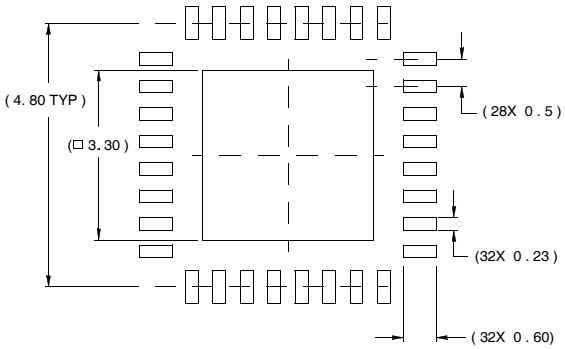
32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 5/10



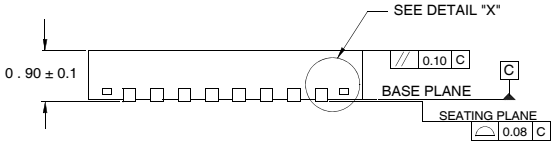
TOP VIEW



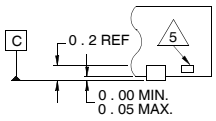
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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