Title	***Reference Design Report for a Dual Output 17.5 W Power Supply Using InnoSwitch™-EP INN2904K***
Specification	85 VAC – 484 VAC Input; 12 V, 1.25 A and 5 V, 0.5 A Outputs
Application	Embedded Power Supply
Author	Applications Engineering Department
Document Number	RDR-531
Date	September 7, 2016
Revision	1.3

Summary and Features

- InnoSwitch-EP - industry first AC/DC ICs with isolated, safety rated integrated feedback
    - 900 V rated MOSFET
- Built in synchronous rectification for higher efficiency
- All the benefits of secondary side control with the simplicity of primary side regulation
    - Insensitive to transformer variation
    - Extremely fast transient response independent of load timing
- Meets output cross regulation requirements without linear regulators
- Primary sensed output overvoltage protection (OVP) eliminates optocoupler for fault protection
- Accurate thermal protection with hysteretic shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a 1.25 A, 12 V and 0.5 A, 5 V dual output embedded power supply utilizing the INN2904K, with a 900 V rated MOSFET, from the InnoSwitch-EP family of ICs.

This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

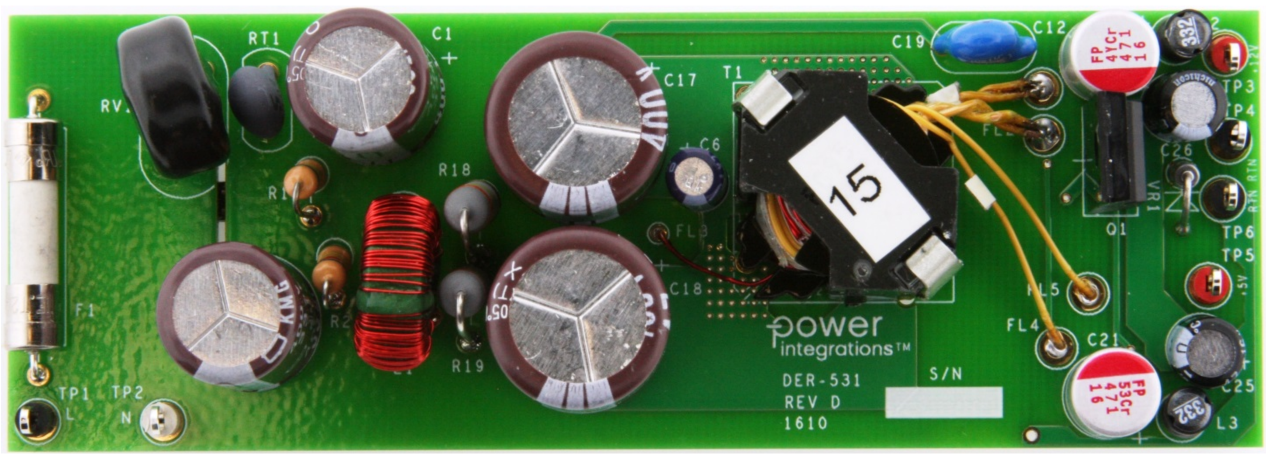

Figure 1 – Populated Circuit Board Photograph, Top.

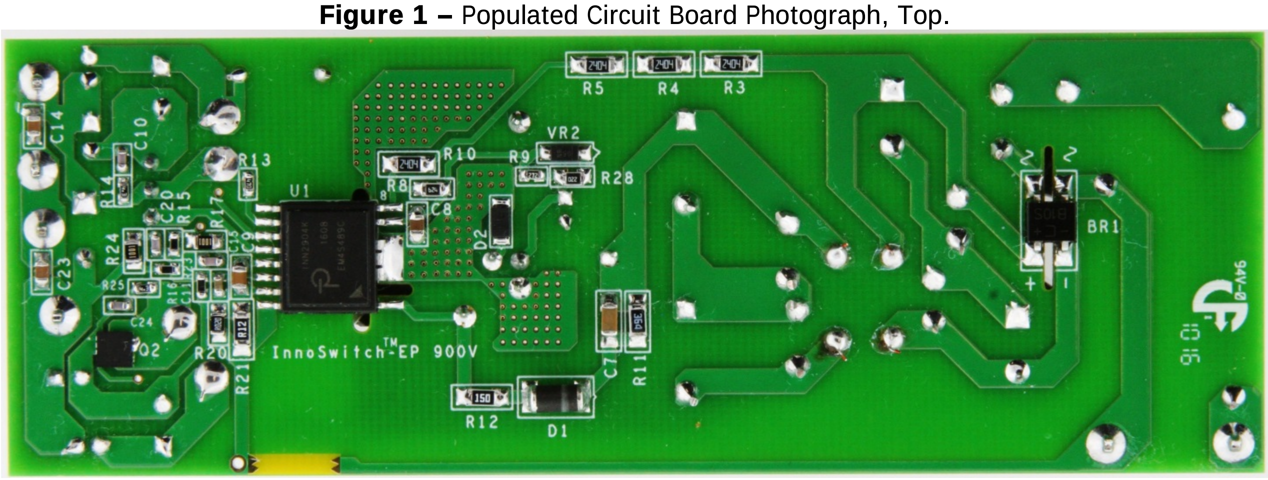

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		484	VAC	2 Wire Input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	±5 %.
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0		0.5	A	
Output Voltage 2	V_{OUT2}	10.2	12	13.8	V	±15 %, (±10 % with 0.1 A Min Load on 12 V.)
Output Ripple Voltage 2	$V_{RIPPLE2}$			150	mV	20 MHz Bandwidth.
Output Current 2	I_{OUT2}	0		1.25	A	
Total Output Power						
Continuous Output Power	P_{OUT}		17.5		W	
Efficiency						
Full Load	η	86			%	Measured at 110 / 230 VAC, P_{OUT} 25 °C.
No-Load Input Power				280	mW	V_{IN} at 230 VAC.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge Differential		2			kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω.
Surge Common mode Ring Wave		6			kV	100 kHz Ring Wave, 12 Ω. Common Mode.
ESD		±16.5 ±8			kV kV	Air discharge Contact discharge No degradation in performance
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

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3 Schematic

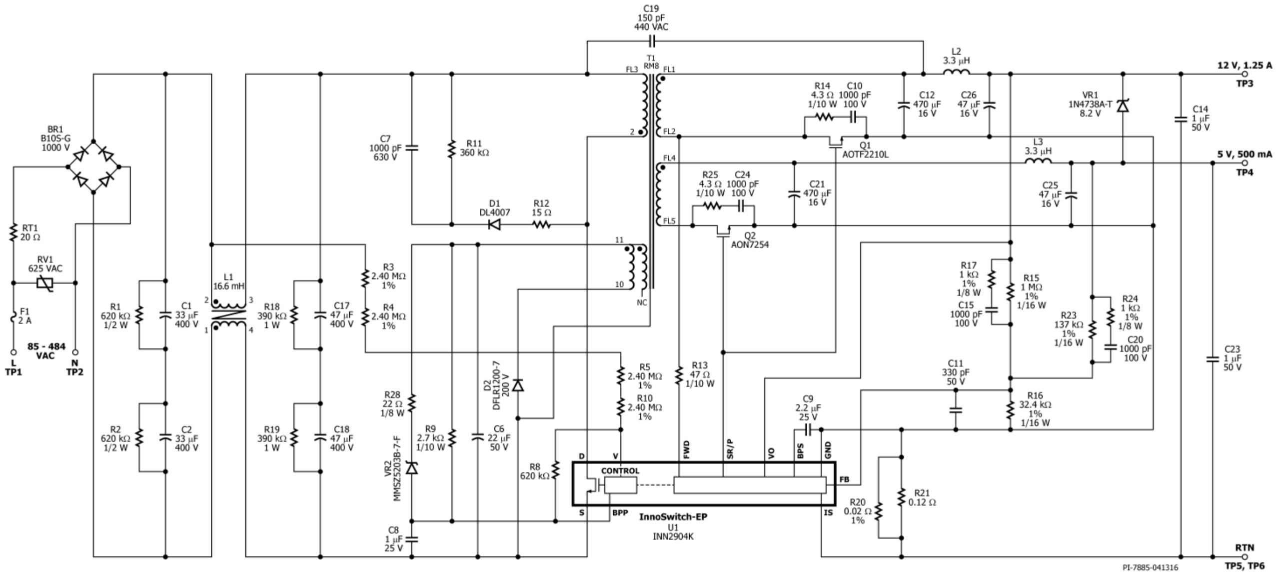

Figure 3 – Schematic.

4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 isolates the circuit and provides protection from component failure and the common mode chokes L1 with capacitors, C1, C2, C17 and C18, provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter consisting of C1 and C2. Thermistor RT1 is an inrush current limiter in the circuit with the high peak forward surge current rated bridge rectifier.

4.2 *InnoSwitch-EP Primary*

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 900 V power MOSFET inside the InnoSwitch-EP IC (U1).

A low cost RCD clamp formed by D1, R11, R12, and C7 limits the peak drain voltage due to the effects of transformer leakage reactance and output trace inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C8, when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C6, and fed in the BPP pin via a current limiting resistor R9. The primary side overvoltage protection is obtained using Zener diode VR2 and R28. In the event of overvoltage at output, the increased voltage at the output of the bias winding cause the Zener diode VR2 to conduct and triggers the OVP latch in the primary side controller of the InnoSwitch-EP IC.

Resistor R3, R4, R5, R10 and R8 provide line voltage sensing and provide a current to U1, which is proportional to the DC voltage across capacitors C1 and C2. At approximately 78 V DC, the current through these resistors exceeds the line under-voltage threshold, which results in enabling of U1. At approximately 700 V DC, the current through these resistors exceeds the line over-voltage threshold, which results in disabling of U1.

4.3 *InnoSwitch-EP Secondary*

The secondary side of the InnoSwitch-EP provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Output rectification for the 5 V output is provided by SR FET Q2. Very low ESR capacitor C21 provides filtering, and inductor L3 and capacitor C25 form a second stage filter that significantly attenuates the high frequency ripple and noise at the 5 V output.

Output rectification for the 12 V output is provided by SR FET Q1. Very low ESR capacitors C12 provides filtering, and inductor L2 and capacitor C26 form a second stage

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filter that significantly attenuates the high frequency ripple and noise at the 12 V output. C14 and C23 capacitors are used to high frequency switching ripple and radiated EMI.

RC snubber networks comprising R25 and C24 for Q2, R14 and C10 for Q1 damp high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances.

In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). Secondary side control of the primary side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR/P pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the V_O pin and charges the decoupling capacitor C9 via an internal regulator during CV region and forward secondary winding forward voltage powers the device during startup and CC region through R13. The unit enters auto-restart when the sensed output voltage is lower than 3 V.

Resistor R16, R15 and R23 form a voltage divider network that senses the output voltage from both outputs for better cross-regulation. Zener diode VR1 improves the cross regulation when only the 5 V output is loaded, which results in the 12 V output operating at the higher end of the specification. The InnoSwitch-EP IC has an internal reference of 1.265 V. Feedback compensation networks comprising capacitors C20, C15 and resistors R24, R17 reduce the output ripple voltage. Capacitor C11 provides decoupling from high frequency noise affecting power supply operation. Total output current is sensed by R20 and R21 with a threshold of approximately 33 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current

5 PCB Layout

PCB copper thickness is 2 oz (2.8 mils / 70 μm) unless otherwise stated.

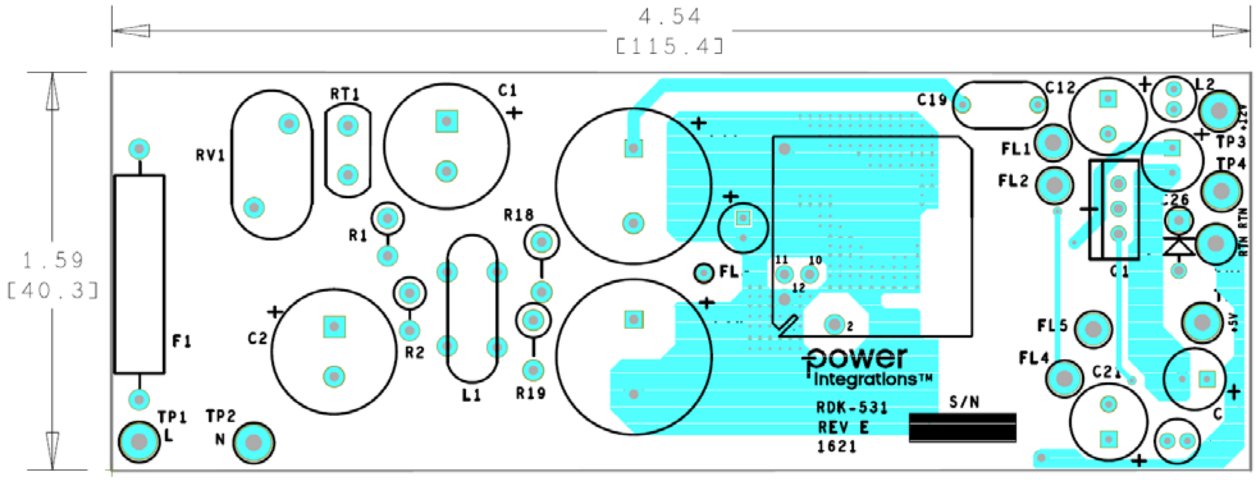

Figure 4 – Printed Circuit Layout, Top.

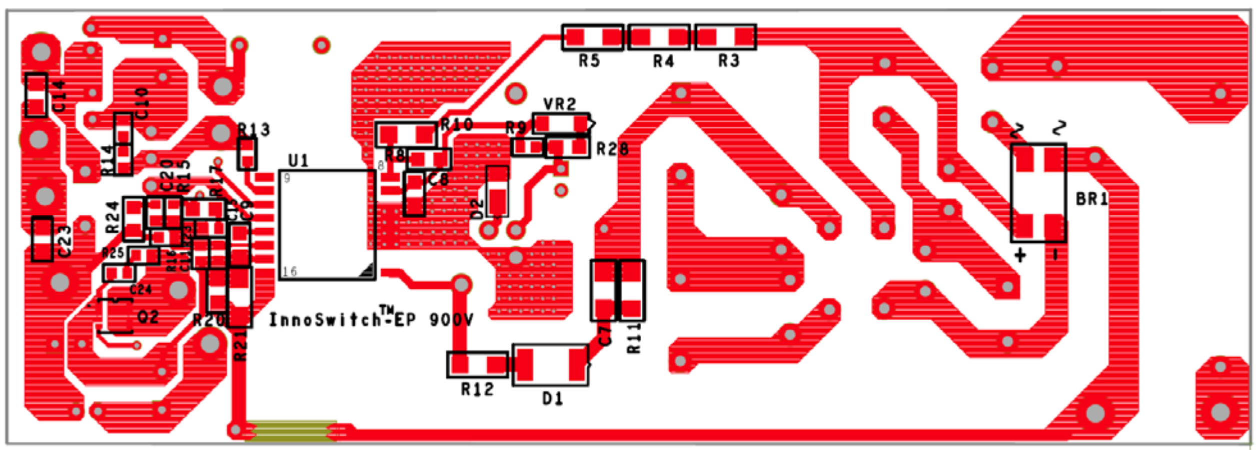

Figure 5 – Printed Circuit Layout, Bottom.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	2	C1 C2	33 μF, 400 V, Electrolytic, (12.5 x 20)	KMG401ELL330MK20S	Nippon Chemi-Con
3	1	C6	22 μF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
4	1	C7	1000 pF, 630 V, Ceramic, X7R, 1206	C1206C102KBRACTU	Kemet
5	1	C8	1 μF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
6	1	C9	2.2 uF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
7	4	C10 C15 C20 C24	1000 pF, 100 V, Ceramic, NPO, 0603	C1608C0G2A102J	TDK
8	1	C11	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
9	2	C12 C21	470 μF, 16 V,Al Organic Polymer, 12 mΩ, (8 x 11.5)	RNE1C471MDN1	Nichicon
10	2	C14 C23	1 μF,50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK Corp
11	2	C17 C18	47 μF, 400 V, Electrolytic (16 x 20)	EKXJ401ELL470ML20S	United Chemi-Con
12	1	C19	150 pF, 440 Vac, Thru Hole, Ceramic Y-Capacitor	WKO151MCPCF0KR	Vishay
13	2	C25 C26	47 μF, 16 V, Electrolytic, Gen. Purpose, (6.3 x 7)	USA1C470MDD	Nichicon
14	1	D1	1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4007-13-F	Diodes, Inc.
15	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
16	1	F1	FUSE, CERM, 2A, 500VAC, 400VDC, 5X20	0477002.MXEP	Littlefuse
17	4	FL1 FL2 FL4 FL5	Flying Lead , Hole size 70mils	N/A	N/A
18	1	FL3	Flying Lead , Hole size 30mils	N/A	N/A
19	1	L1	16.6 mH,xA, Ferite Toroid, 4 Pin, Output CMC Assembly CMC Assembly	SNX-R1840 TSD-3760	Santronics Premier Magnetics
20	2	L2 L3	3.3 μH, 1.5 A	11R332C	Murata
21	1	Q1	200 V, 13 A, N-Channel, TO-220	AOTF2210L	Alpha & Omega
22	1	Q2	150 V, 17A N-Channel, 8DFN	AON7254	Alpha & Omega
23	2	R1 R2	RES, 620 k, 5%, 1/2 W, Carbon Film	CFR-50JB-620K	Yageo
24	4	R3 R4 R5 R10	RES, 2.4 M, 1%, 1/4 W, Thick Film, 1206	RC1206FR-072M4L	Yageo
25	1	R8	RES, 620 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ624V	Panasonic
26	1	R9	RES, 2.7 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ272V	Panasonic
27	1	R11	RES, 360 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ364V	Panasonic
28	1	R12	RES, 15 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ150V	Panasonic
29	1	R13	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
30	2	R14 R25	RES, 4.3 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ4R3V	Panasonic
31	1	R15	RES, 1.00 MΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1004V	Panasonic
32	1	R16	RES, 32.4 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3242V	Panasonic
33	2	R17 R24	RES, 1.00 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1001V	Panasonic
34	2	R18 R19	RES, 390 kΩ, 5%, 1 W, Metal Oxide	RSF100JB-390K	Yageo
35	1	R20	RES, 0.02 Ω, 1%, 1/4 W, Thick Film, 0805	RL0805FR-7W0R02L	Yageo
36	1	R21	RES, 0.12 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8RSJR12V	Panasonic
37	1	R23	RES, 137 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1373V	Panasonic
38	1	R28	RES, 22 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ220V	Panasonic
39	1	RT1	NTC Thermistor, 20 Ω, 0.3 A	20D2-05LD	Semitec
40	1	RV1	625 V,100 J, 14 mm, RADIAL	ERZ-V14D102	Panasonic
41	1	T1	Bobbin, RM8, Vertical, 12 pins Transformer Assembly Transformer Assembly	RM8/12/1 SNX-R1839 POL-INN014	Schwartzpunkt Santronics Premier Magnetics
42	1	TP1	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
43	3	TP2 TP4 TP6	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
44	2	TP3 TP5	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone

45	1	U1	InnoSwitch-EP, Off-Line CV/CC Flyback Switcher	INN2904K	Power Integrations
46	1	VR1	8.2 V, 5%, 1 W, DO-41	1N4738A,113	NXP Semi
47	1	VR2	DIODE ZENER 4.7V 500MW SOD123	MMSZ5230B-7-F	Diodes, Inc.

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7 Transformer (T1) Specification

7.1 *Transformer Electrical Diagram*

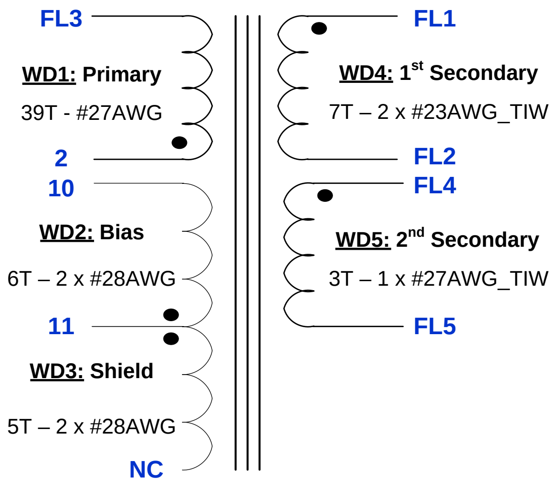

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 2 and FL3, with all other windings open.	381 µH ±10%
Resonant Frequency	Between pin 2 and FL3, other windings open.	1100 kHz (Min.)
Primary Leakage Inductance	Between pin 2 and FL3, with FL1, FL2, FL4, FL5 shorted.	10 µH (Max).

7.3 *Material List*

Item	Description
[1]	Core: RM8, PC95 TDK or DMR95 from DMEGC magnetics.
[2]	Bobbin: RM8, Vertical, 12 pins (6/6-circular) (PI P/N: 25-01084-00).
[3]	Core Clip: Allstar Magnetic, P/N: CLI/P-RM8/I.
[4]	Magnet Wire: #27 AWG, double coated.
[5]	Magnet Wire: #28 AWG, double coated.
[6]	Magnet Wire: #23 AWG, Triple Insulated Wire.
[7]	Magnet Wire: #27 AWG, Triple Insulated Wire.
[8]	Barrier Tape: 3M 1298 Polyester Film, 1 mil thickness, 9.5 mm wide.
[9]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

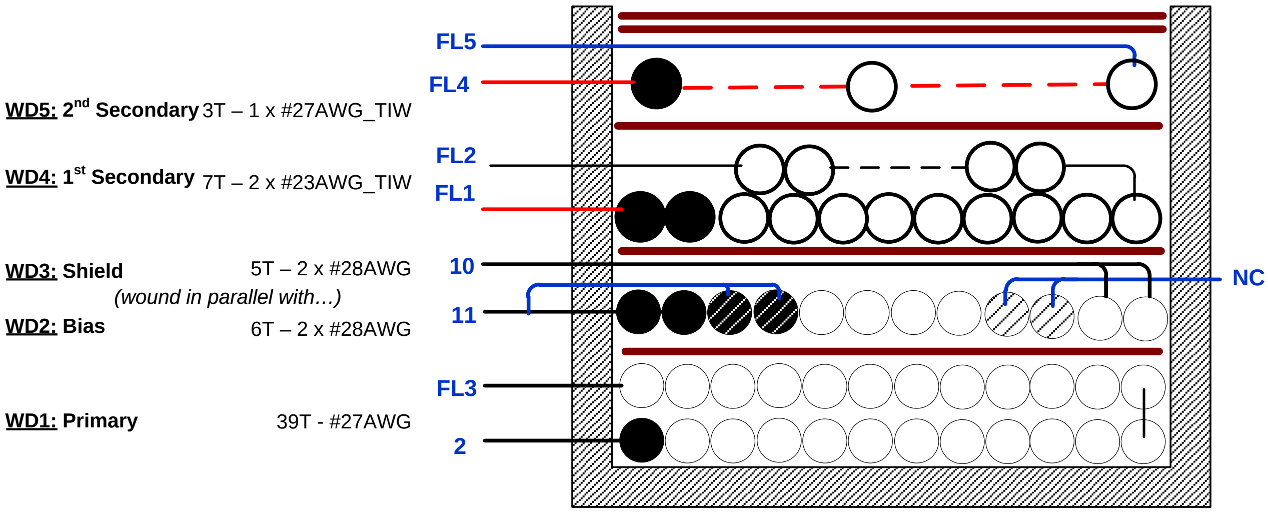

Figure 7 – Transformer Build Diagram.

7.5 *Transformer construction*

Winding Preparation	Position the bobbin item [2] on the mandrel such that the pin side of the bobbin is on the left side. Winding direction is clock-wise direction.
WD1 Primary	Start at pin 2, wind 39 turns of wire item [4] in 2 layers, with tight tension, spread wire evenly for 2nd layer. At the last turn leave ~1" floating and mark as FL3.
Insulation	1 layer of tape item [8].
WD2 & WD3 Bias & Shield	Start at pin 11, use 4 wires item [5], wind 5 turns, cut 2 wires as No-Connect for WD3. Continue winding other 2 wires 1 more turn and finish at pin 10 for WD2.
Insulation	1 layer of tape item [8].
WD4 1st Secondary	Use 2 wires item [6], leave ~1" floating for start leads FL1, wind 7 turns in 1 ½ layers and finish with ~1" floating for end leads FL2.
Insulation	1 layer of tape item [8].
WD5 2nd Secondary	Use single wire item [7], leave ~1" floating for start lead FL4, wind 3 turns in 1 layer, spread wire evenly across the bobbin, and finish with ~1" floating for end lead FL5.
Insulation	2 layers of tape item [8] for insulation and secure the windings.
Finish	Gap cores to get 381 μH, assemble cores with tape. Varnish with item [9].

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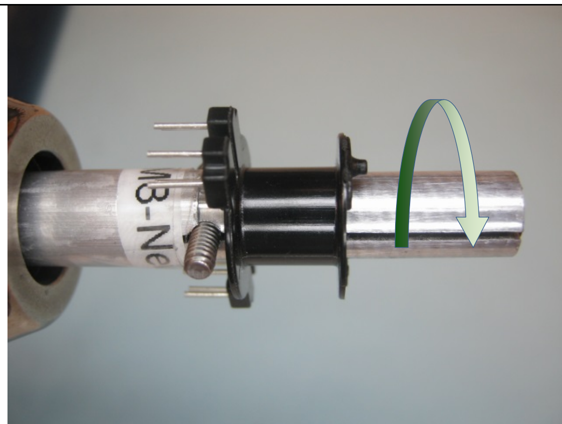
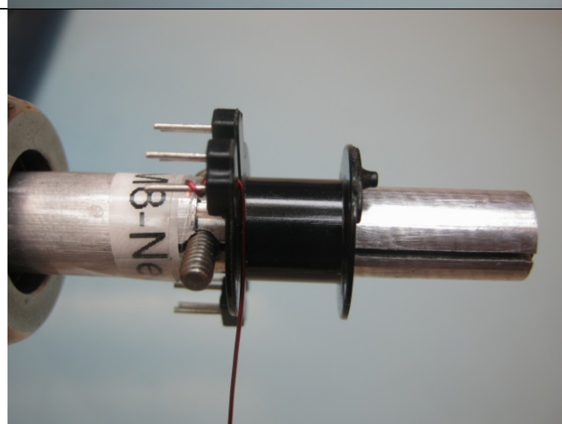
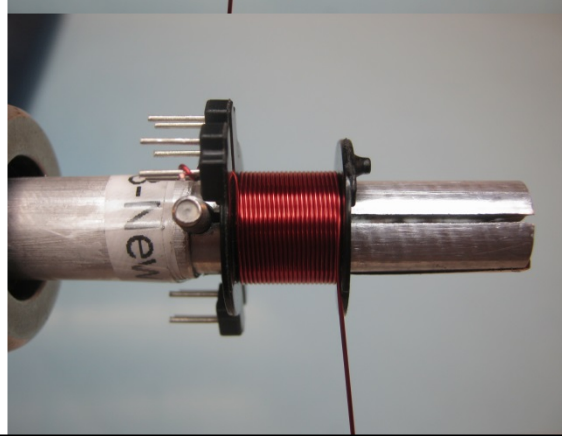
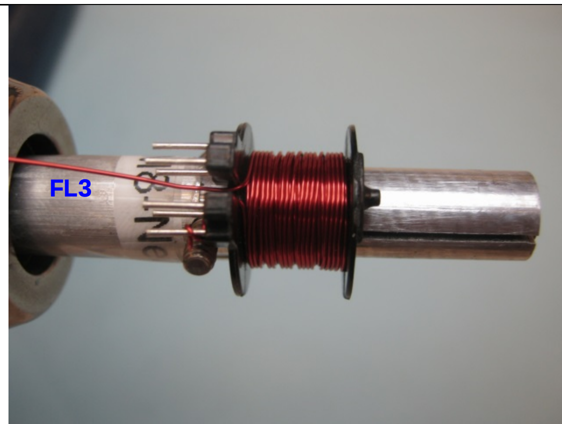
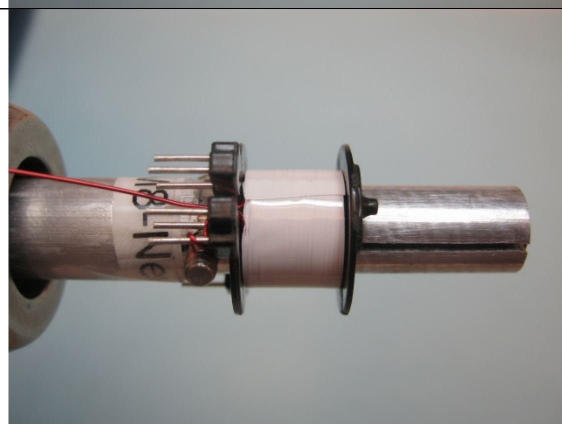
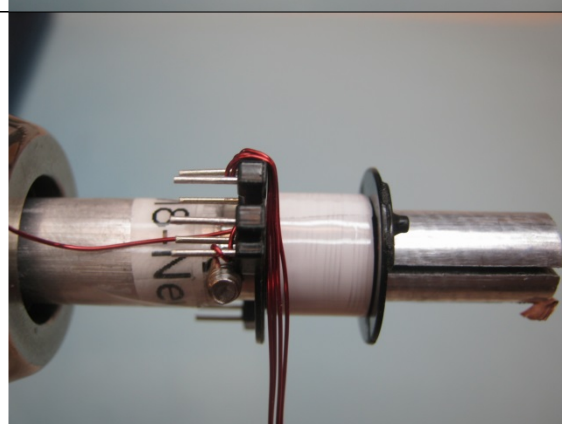
7.6 *Winding Illustrations*

Winding Preparation		Position the bobbin item [2] on the mandrel such that the pin side of the bobbin is on the left side. Winding direction is clock-wise direction.
WD1 **Primary**	 	Start at pin 2, wind 39 turns of wire item [4] in 2 layers, with tight tension, spread wire evenly for 2nd layer. At the last turn leave ~1” floating and mark as FL3.

		
Insulation		1 layer of tape item [8].
WD2 & WD3 **Bias & Shield**	 	Start at pin 11, use 4 wires item [5], wind 5 turns, cut 2 wires as No-Connect for WD3. Continue winding other 2 wires 1 more turn and finish at pin 10 for WD2.

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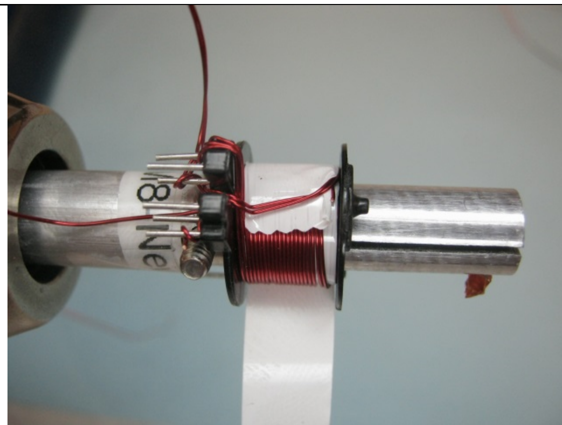
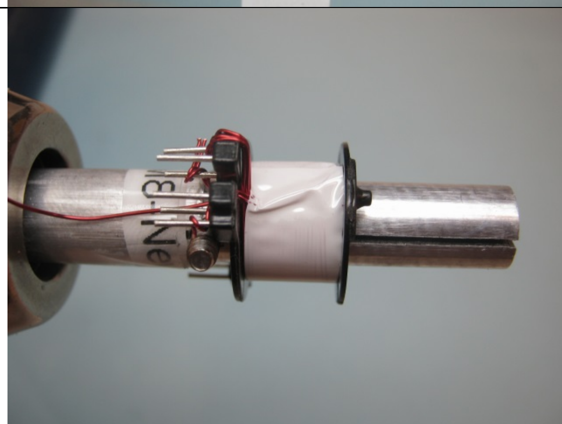
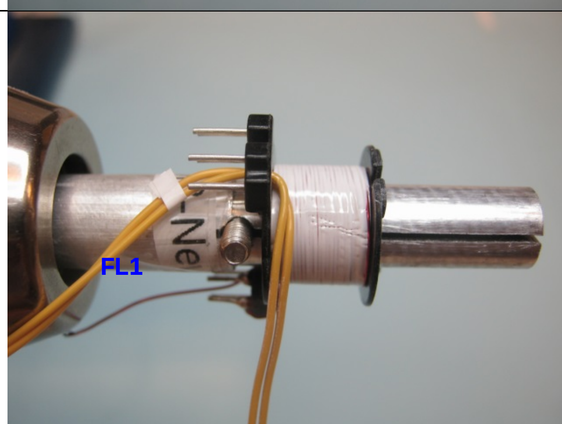
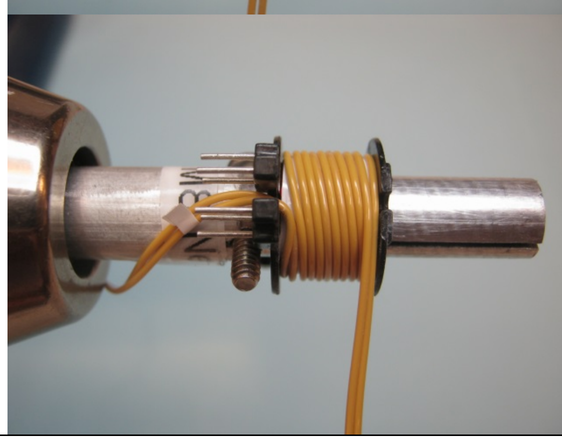
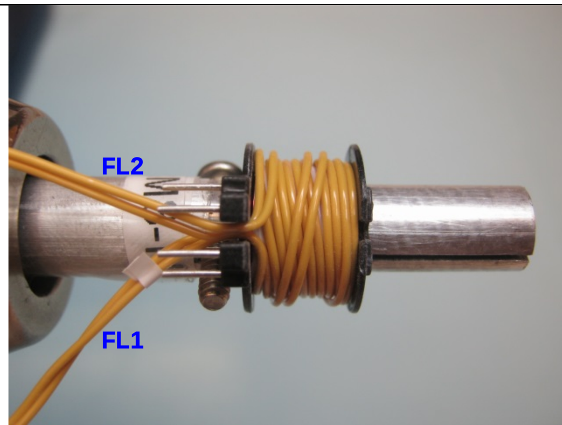
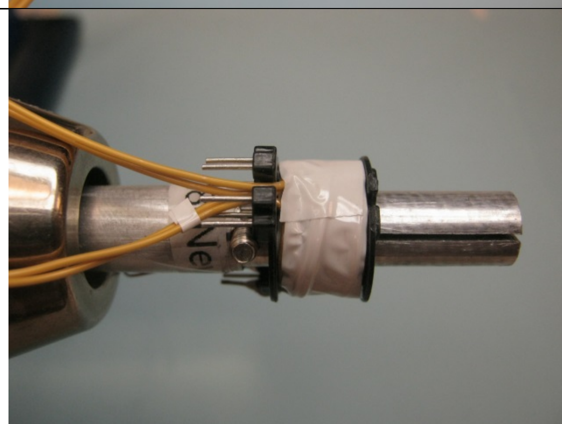
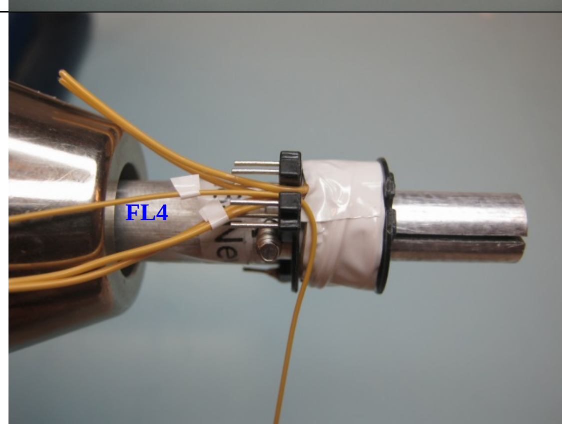
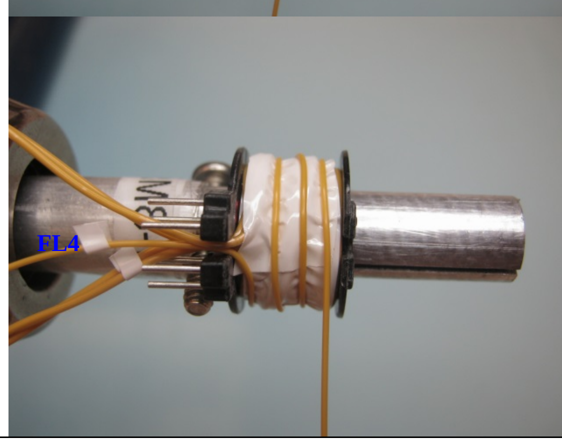
		
Insulation		1 layer of tape item [8].
WD4 **1st Secondary**	 	Use 2 wires item [6], leave ~1” floating for start leads FL1, wind 7 turns in 1 ½ layers and finish with ~1” floating for end leads FL2.

		
Insulation		1 layer of tape item [8].
WD5 **2nd Secondary**	 	Use single wire item [7], leave ~1" floating for start lead FL4, wind 3 turns in 1 layer, spread wire evenly across the bobbin, and finish with ~1" floating for end lead FL5.

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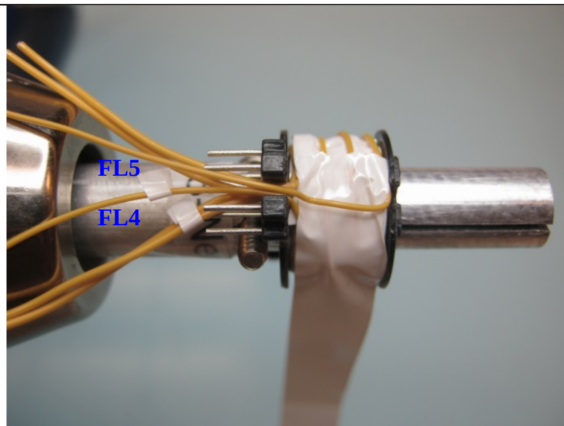
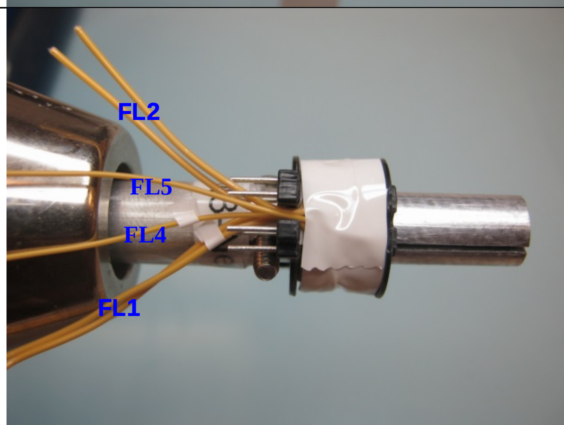
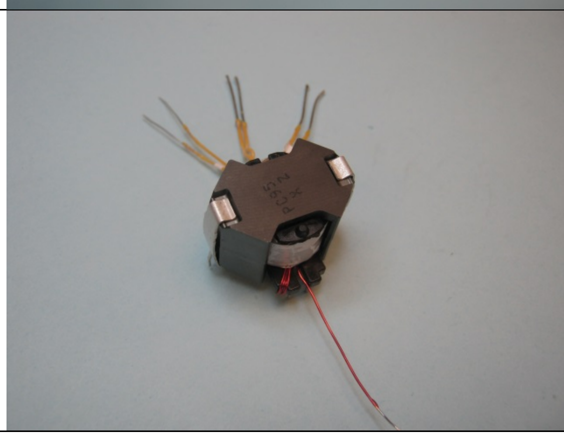
		
Insulation		2 layers of tape item [8] for insulation and secure the windings.
Finish		Gap cores to get 381 μH, assemble cores with tape. Varnish with item [9].

8 Common Mode Choke (L1) Specification

8.1 *Electrical Diagram*

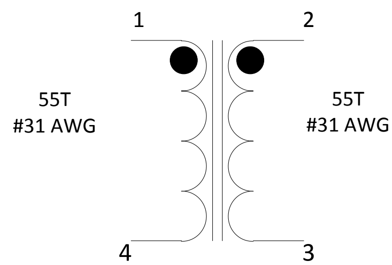


Figure 8 – Inductor Electrical Diagram.

8.2 *Electrical Specifications*

Inductance	Pins 1-4 and pins 2-3 measured at 100 kHz, 0.4 RMS.	16.6 mH ±25%
Core Effective Inductance		5500 nH/N^2
Primary Leakage Inductance	Pins 1-4, with 2-3 shorted.	80 µH

8.3 *Material List*

Item	Description
[1]	Toroid: FERRITE INDUCTR TOROID. 1) JLW Electronics (Hong Kong), T14 x 8 x 5.5C-JL10. 2) TDK, B64290L0658 x 038 material. 3) PI Part number: #32-00286-00
	Divider: Cable-tie, Panduit, PLT.7M-M.
[2]	Magnet Wire: #31 AWG Heavy Nyleze.

8.4 *Winding Instructions*

1) Place 2 pieces of cable tie item [2] onto toroid item [1] to divide 2 equal sections.
2) Use 4 ft of wire item [3], start as pin 1 wind 55 turns in 2 layers in 1 section of toroid, and end at pin 4.
3) Do the same for another section of toroid, start at pin 2 then end at pin 3 symmetrically with last winding.
4) Use hot glue or Epoxy to hold the windings in place.

8.5 *Illustrations*

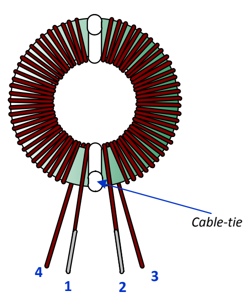


Figure 9 – Inductor Illustration.

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9 Transformer Design Spreadsheet

ACDC_InnoSwitch-EP_052115; Rev.0.1; Copyright Power Integrations 2015	INPUT	INFO	OUTPUT	UNIT	ACDC_InnoSwitch-EP_051915_Rev0-1; InnoSwitch-EP Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85		85	V	Minimum AC Input Voltage
VACMAX	484		484	V	Maximum AC Input Voltage
fL			50	Hz	AC Mains Frequency
VO	5.00		5.00	V	Output Voltage (continuous power at the end of the cable)
IO	3.50		3.50	A	Power Supply Output Current (corresponding to peak power)
Power			17.50	W	Continuous Output Power, including cable drop compensation
n	0.82		0.82		Efficiency Estimate at output terminals. Use 0.8 if no better data available
Z	0.40		0.40		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	36.00		36.00	uFarad	Input Capacitance
ENTER InnoSwitch-EP VARIABLES					
InnoSwitch-EP	**INN2904**		**INN2904**		User defined InnoSwitch
Chose Configuration	**INC**		**Increased Current Limit**		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			1.070	A	Minimum Current Limit
ILIMITTYP			1.150	A	Typical Current Limit
ILIMITMAX			1.231	A	Maximum Current Limit
fSmin			93000	Hz	Minimum Device Switching Frequency
I^2fmin			111.09	A^2kHz	Worst case I2F parameter across the temperature range
VOR	67		67	V	Reflected Output Voltage (VOR <= 100 V Recommended)
VDS			5.00	V	InnoSwitch on-state Drain to Source Voltage
KP			0.981		Ripple to Peak Current Ratio at Vmin, assuming ILIMITMIN, and I2FMIN (KP < 6)
KP_TRANSIENT			0.483		Worst case transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER InnoSwitch-EP PROTECTION VARIABLES					
Line Undervoltage					
BROWN IN			67.0	VRMS	Minimum RMS AC Voltage at which the power supply will BROWN-IN (turn-on). The actual value of this voltage may differ slightly from the desired value due to the V-pin resistor's tolerance
BROWN OUT			54.9	VRMS	Typical RMS AC Voltage at which the power supply will BROWN-OUT (turn-off) under conditions of line-undervoltage
RLS			7.32	MOhms	Theoretical V-pin resistor for the desired UV/OV setup
RLS1/RLS2			3.65	MOhms	Use two 1% resistors in series for line sense (V-Pin) functionality
VBROWNIN VARIATION			0.00	%	Variation between the actual and desired brown-in voltage
Line Overvoltage					
BROWN IN			275.9	VRMS	Typical RMS AC voltage at which the power supply will BROWN-IN (turn-on) after a line overvoltage BROWN-OUT (turn-off) event

BROWN OUT			290.4	VRMS	Typical RMS AC voltage at which the power supply will BROWN-OUT (turn-off) under conditions of line-overvoltage
Load Overcurrent					
IOMAX			2.10	A	Load current beyond which the device will enter into overload protection. By default value consists of the sum of all output currents multiplied by 1.2
RIS			0.017	Ohms	Use a 0.017 Ohm, 1-5% resistor having a minimum power rating of 0.0735W on the IS pin for load overcurrent protection
ENTER BIAS WINDING VARIABLES					
VB			10.00	V	Bias Winding Voltage
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
NB			5.89	V	Bias Winding Number of Turns
PIVB			156.60	V	Bias winding peak reverse voltage at VACmax and assuming VB*1.2
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**RM8**		**RM8**		Enter Transformer Core
Core			PC47RM8Z-12		Enter core part number, if necessary
Bobbin			BRM8-718CPFR		Enter bobbin part number, if necessary
AE			0.64	cm^2	Core Effective Cross Sectional Area
LE			3.80	cm	Core Effective Path Length
AL			1950	nH/T^2	Ungapped Core Effective Inductance
BW			9.05	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2		2		Number of Primary Layers
NS			3		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			78	V	Minimum DC Input Voltage
VMAX			684	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.48		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.26	A	Average Primary Current
IP			1.07	A	Peak Primary Current assuming ILIMITMIN
IR			1.05	A	Primary Ripple Current assuming ILIMITMIN, and LPMIN
IRMS			0.43	A	Primary RMS Current, assuming ILIMITMIN, and LPMIN
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP		**Warning**	381	uHenry	!!! Low primary inductance (LP), Excessive di/dt. Peak drain current may exceed maximum rating. Design for higher output power, or reduce current limit and/or device size
LP_TOLERANCE	10		10	%	Primary inductance tolerance
NP			39		Primary Winding Number of Turns
ALG			250	nH/T^2	Gapped Core Effective Inductance
BM			2649	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			1299	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			921		Relative Permeability of Ungapped Core
LG			0.28	mm	Gap Length (Lg > 0.1 mm)
BWE			18.1	mm	Effective Bobbin Width
OD			0.464	mm	Maximum Primary Wire Diameter including insulation
INS			0.064	mm	Estimated Total Insulation Thickness (= 2 * film thickness)

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DIA			0.401	mm	Bare conductor diameter
AWG			27	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			203	Cmils	Bare conductor effective area in circular mils
CMA			473	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			13.90	A	Peak Secondary Current, assuming ILIMITMIN
ISRMS			5.87	A	Secondary RMS Current
IRIPPLE			4.71	A	Output Capacitor RMS Ripple Current
CMS			1174	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			19	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN		**Warning**	844	V	!!! REDUCE DRAIN VOLTAGE Vdrain<680 Volts. Reduce VOR or Reduce VACMAX
PIVS			79	V	Output Rectifier Maximum Peak Inverse Voltage for 1st output, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
TRANSFORMER SECONDARY DESIGN PARAMETERS					
1st output					
VO1			5.00	V	Main Output Voltage directly after output rectifier
IO1	0.50		0.50	A	Output DC Current
PO1			2.50	W	Output Power
VD1			0.10	V	Output Synchronous Rectification FET Forward Voltage Drop
NS1			3.00	Turns	Output Winding Number of Turns
ISRMS1			0.84	A	Output Winding RMS Current
IRIPPLE1			0.67	A	Output Capacitor RMS Ripple Current
PIVS1			79	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
CMS1			168	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			27	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.36	mm	Minimum Bare Conductor Diameter
ODS1			3.02	mm	Maximum Outside Diameter for Triple Insulated Wire
Recommended MOSFET			**Si7456**		Recommended SR FET for this output
RDSON_HOT			0.042	Ohm	RDSon at 100C
VRATED			100	V	Rated voltage of selected SR FET
2nd output					
VO2	12.00		12.00	V	Output Voltage
IO2	1.25		1.25	A	Output DC Current
PO2			15.00	W	Output Power
VD2			0.70	V	Output Diode Forward Voltage Drop
NS2			7		Output Winding Number of Turns
ISRMS2			2.10	A	Output Winding RMS Current
IRIPPLE2			1.68	A	Output Capacitor RMS Ripple Current
PIVS2			185	V	Output Rectifier Maximum Peak Inverse Voltage
CMS2			419	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			23	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			0.58	mm	Minimum Bare Conductor Diameter
ODS2			1.29	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					

VO3			0.00	V	Output Voltage
IO3			0.00	A	Output DC Current
PO3			0.00	W	Output Power
VD3			0.70	V	Output Diode Forward Voltage Drop
NS3			0		Output Winding Number of Turns
ISRMS3			0.00	A	Output Winding RMS Current
IRIPPLE3			0.00	A	Output Capacitor RMS Ripple Current
PIVS3			0	V	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			17.50	W	Total Power for Multi-output section
Negative Output			N/A		If negative output exists enter Output number; e.g. If VO2 is negative output, select 2

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10 Performance Data

10.1 *Full Load Efficiency vs. Line*

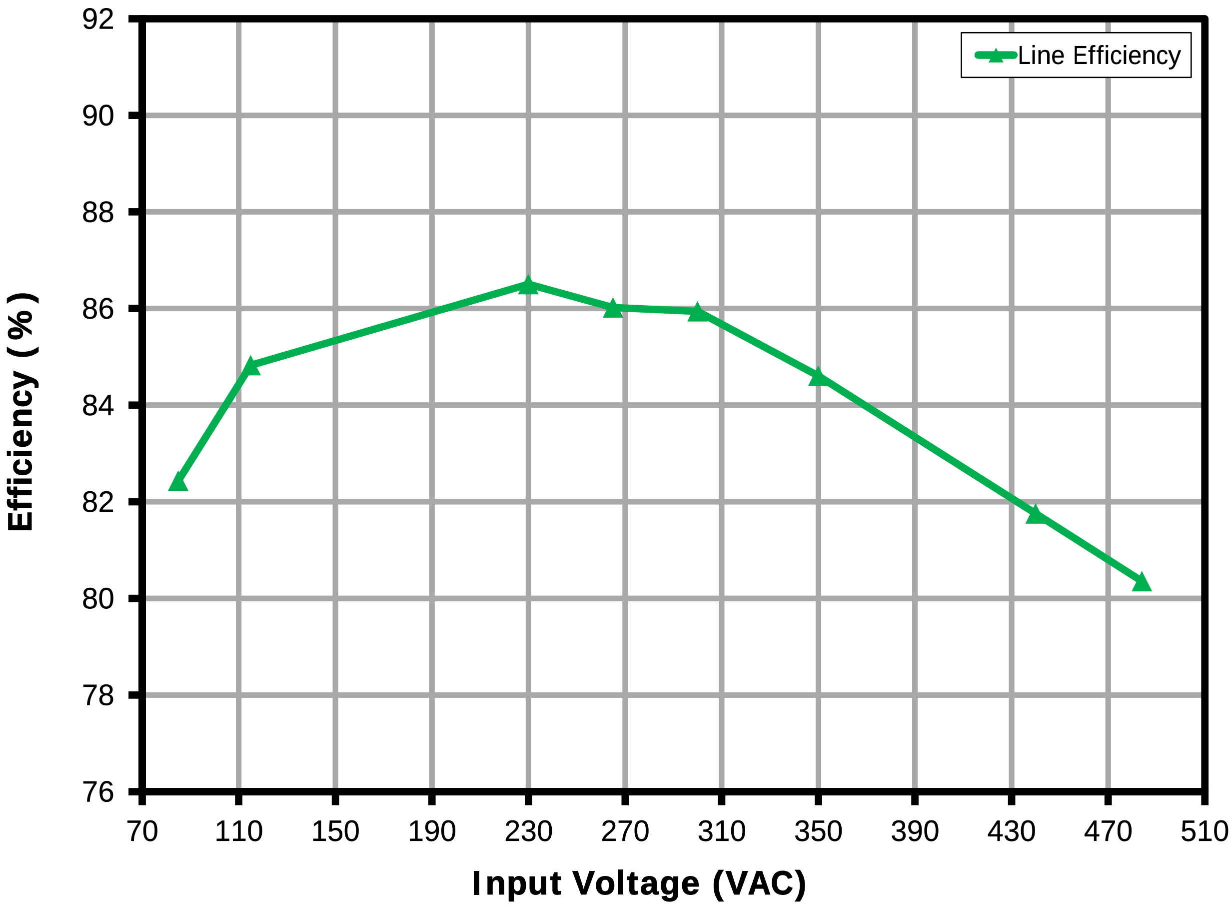

Figure 10 – Full load Efficiency vs. Line Voltage, Room Temperature.

10.2 *No-Load Input Power*

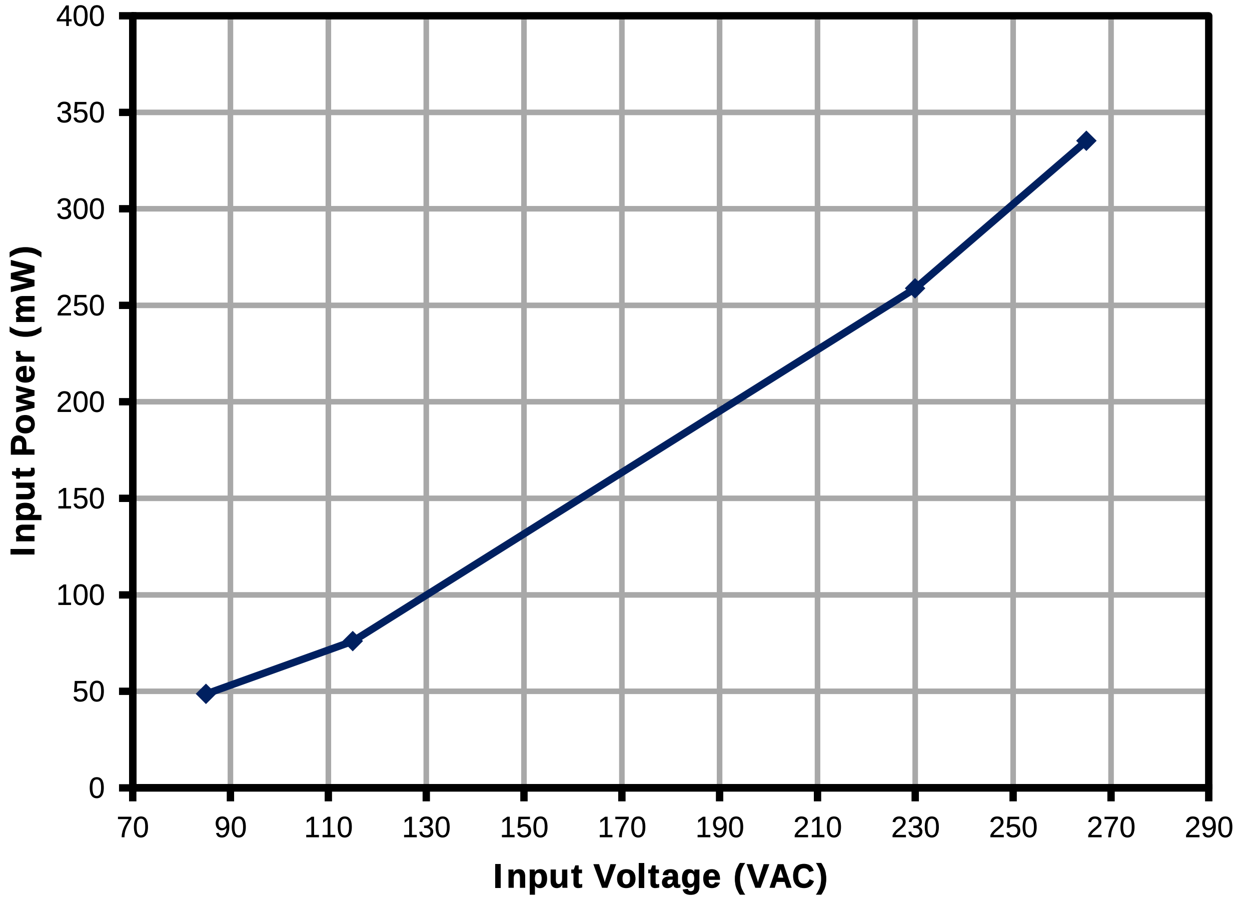

Figure 11 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

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10.3 *Line and Load Regulation*

10.3.1 Line Regulation (Full Load)

VAC	V_{OUT} (12 V)	I_{OUT} (12 V)	V_{OUT} (5V)	I_{OUT} (5 V)
85	12.05	1.243	5.08	0.502
115	12.04	1.243	5.09	0.502
230	12.04	1.243	5.1	0.502
265	12.03	1.243	5.1	0.5
300	12.04	1.243	5.11	0.5
350	12.05	1.243	5.11	0.5
440	12.02	1.243	5.1	0.5
484	12.04	1.243	5.11	0.5

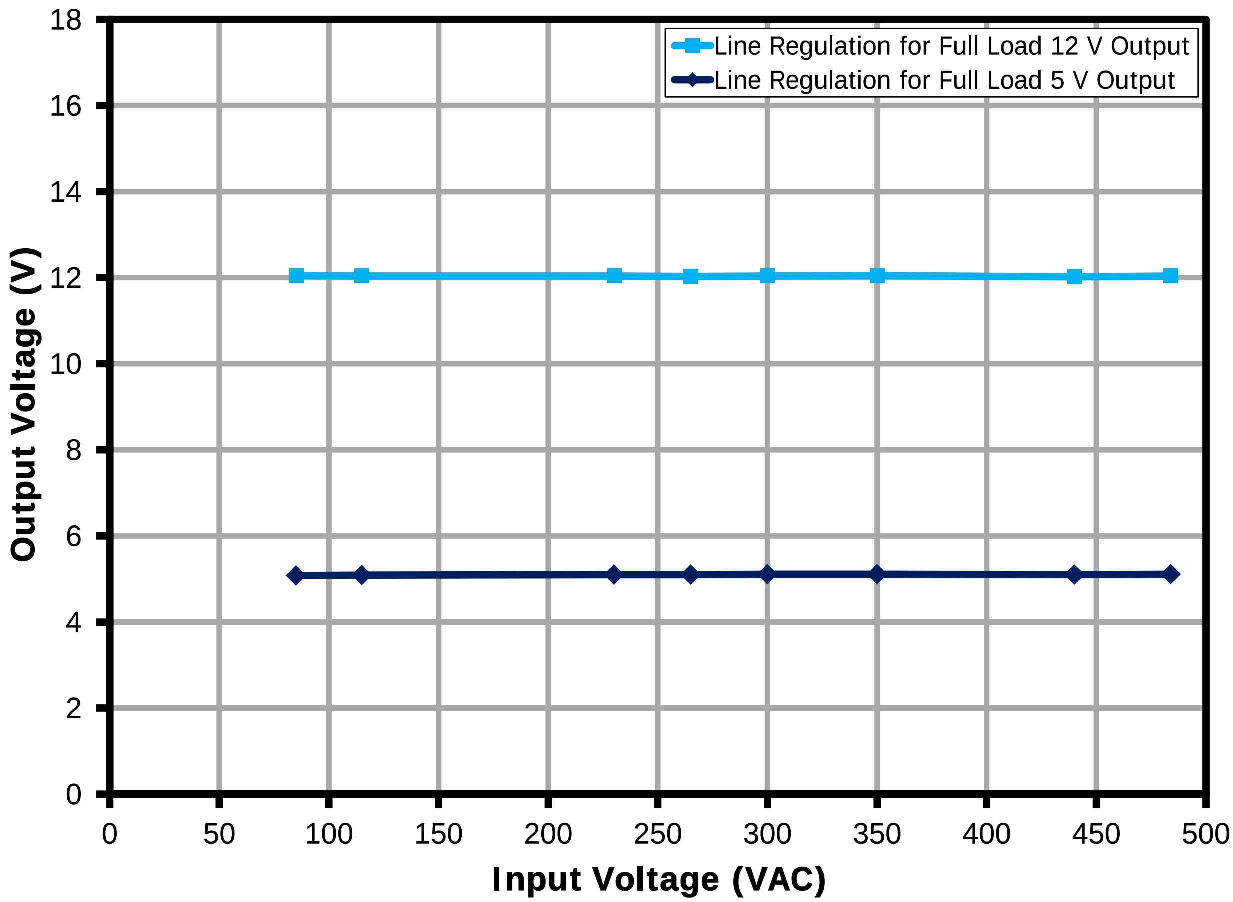

Figure 12 – Output Voltage vs. Input Line Voltage, Room Temperature.

10.3.2 Cross Load Regulation

10.3.2.1 12 V Output (No-Load) Across the Line with Full Load on 5 V

VAC	V_{OUT} (12 V)	I_{OUT} (12 V)	V_{OUT} (5V)	I_{OUT} (5 V)
85	13.6	No Load	5	0.5
115	13.52	No Load	4.99	0.5
230	13.56	No Load	4.99	0.5
265	13.57	No Load	5.01	0.5
300	13.52	No Load	4.98	0.5
350	13.55	No Load	4.99	0.5
440	13.51	No Load	4.98	0.5
484	13.56	No Load	5.01	0.5

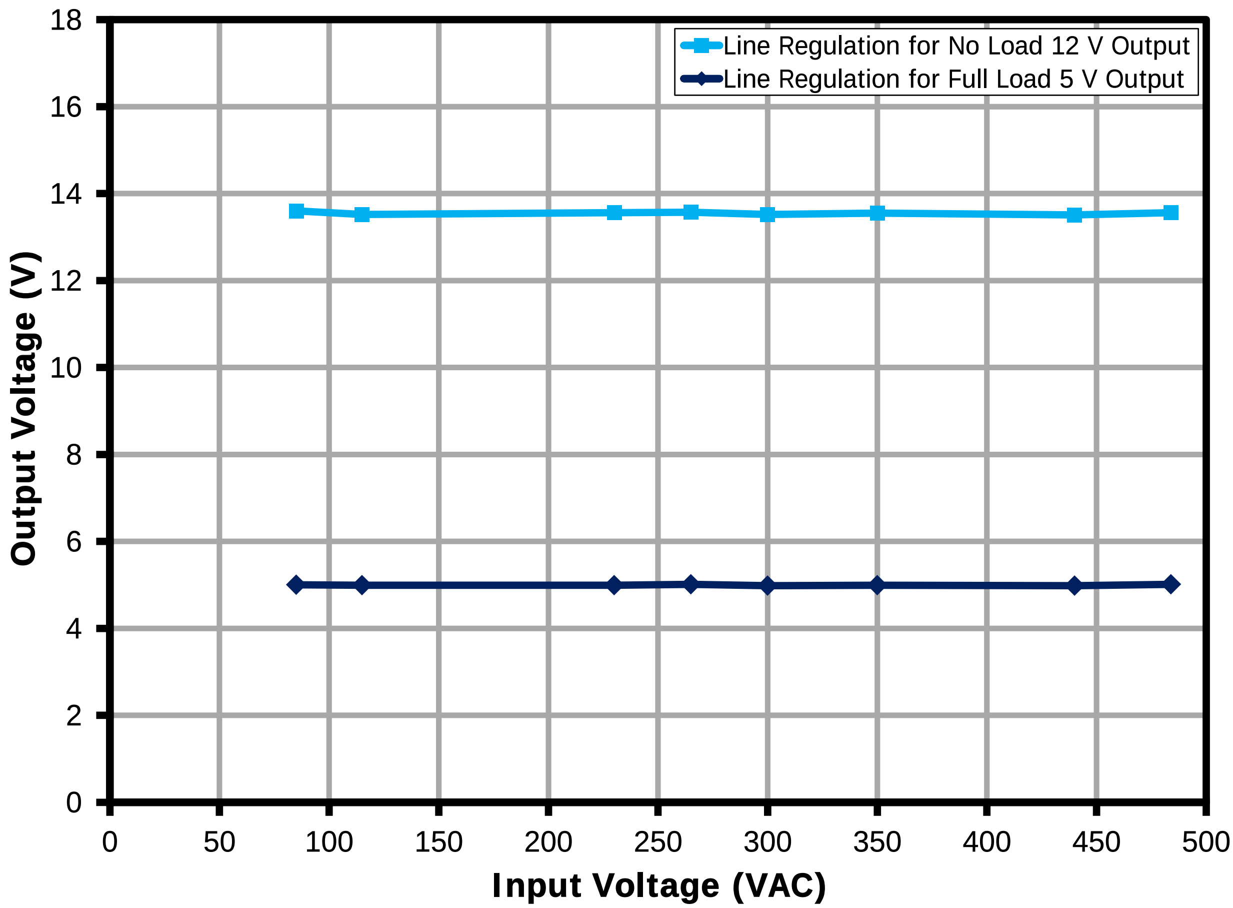

Figure 13 – 12 V Output Voltage vs. No Load, Room Temperature.

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10.3.2.2 12 V Output (No Load) Across the Line with No-Load on 5 V

VAC	V_{OUT} (12 V)	I_{OUT} (12 V)	V_{OUT} (5V)	I_{OUT} (5 V)
85	12.92	No Load	5.07	No Load
115	12.93	No Load	5.07	No Load
230	12.95	No Load	5.07	No Load
265	12.94	No Load	5.05	No Load
300	12.94	No Load	5.05	No Load
350	12.96	No Load	5.06	No Load
440	12.95	No Load	5.06	No Load
484	12.91	No Load	5.06	No Load

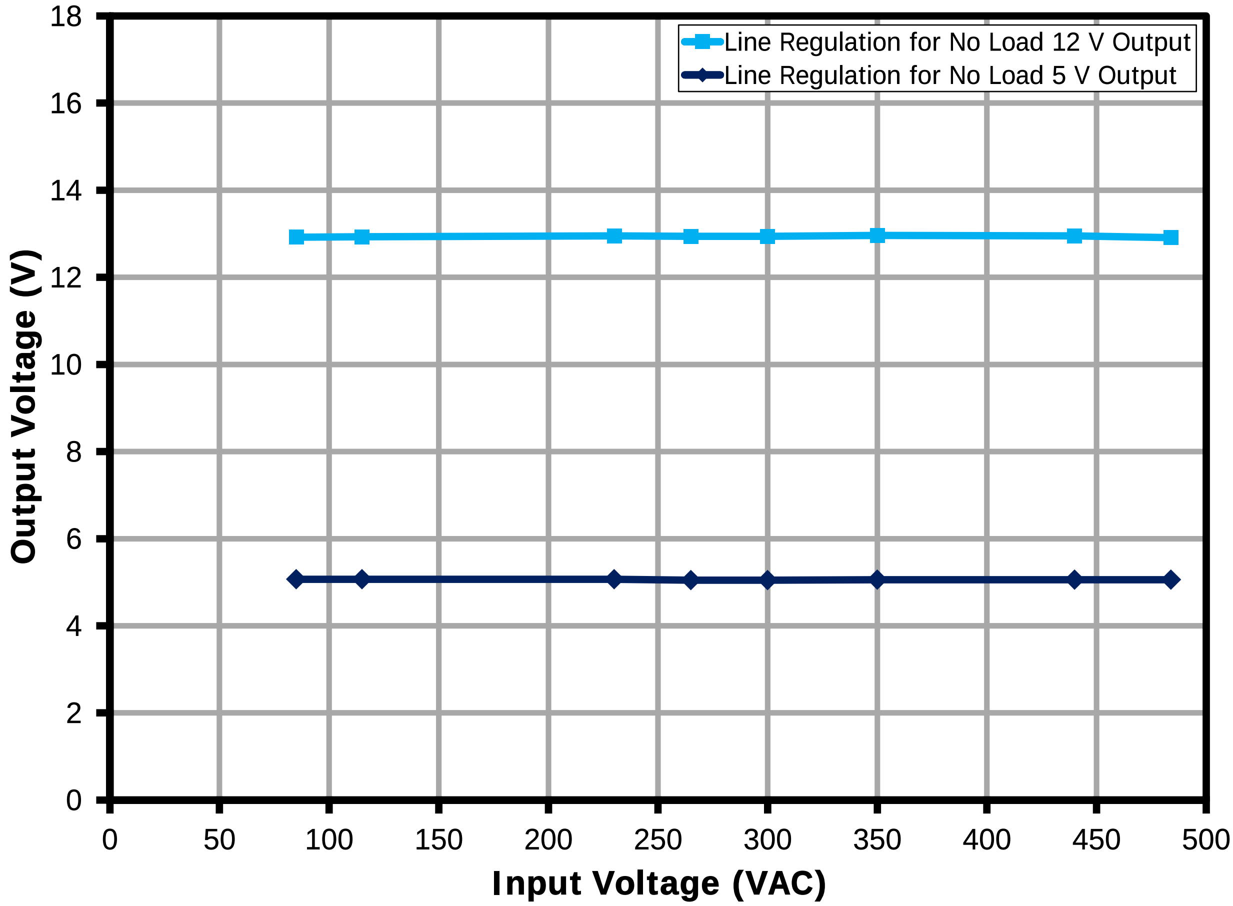

Figure 14 – 12 V Output Voltage vs. Output Load, Room Temperature.

10.3.2.3 12 V Output (Full Load Load) Across the Line with No-Load on 5 V

VAC	V_{OUT} (12 V)	I_{OUT} (12 V)	V_{OUT} (5V)	I_{OUT} (5 V)
85	11.72	1.243	5.15	No Load
115	11.74	1.243	5.15	No Load
230	11.73	1.243	5.17	No Load
265	11.72	1.243	5.18	No Load
300	11.61	1.243	5.16	No Load
350	11.66	1.243	5.14	No Load
440	11.69	1.243	5.18	No Load
484	11.7	1.243	5.18	No Load

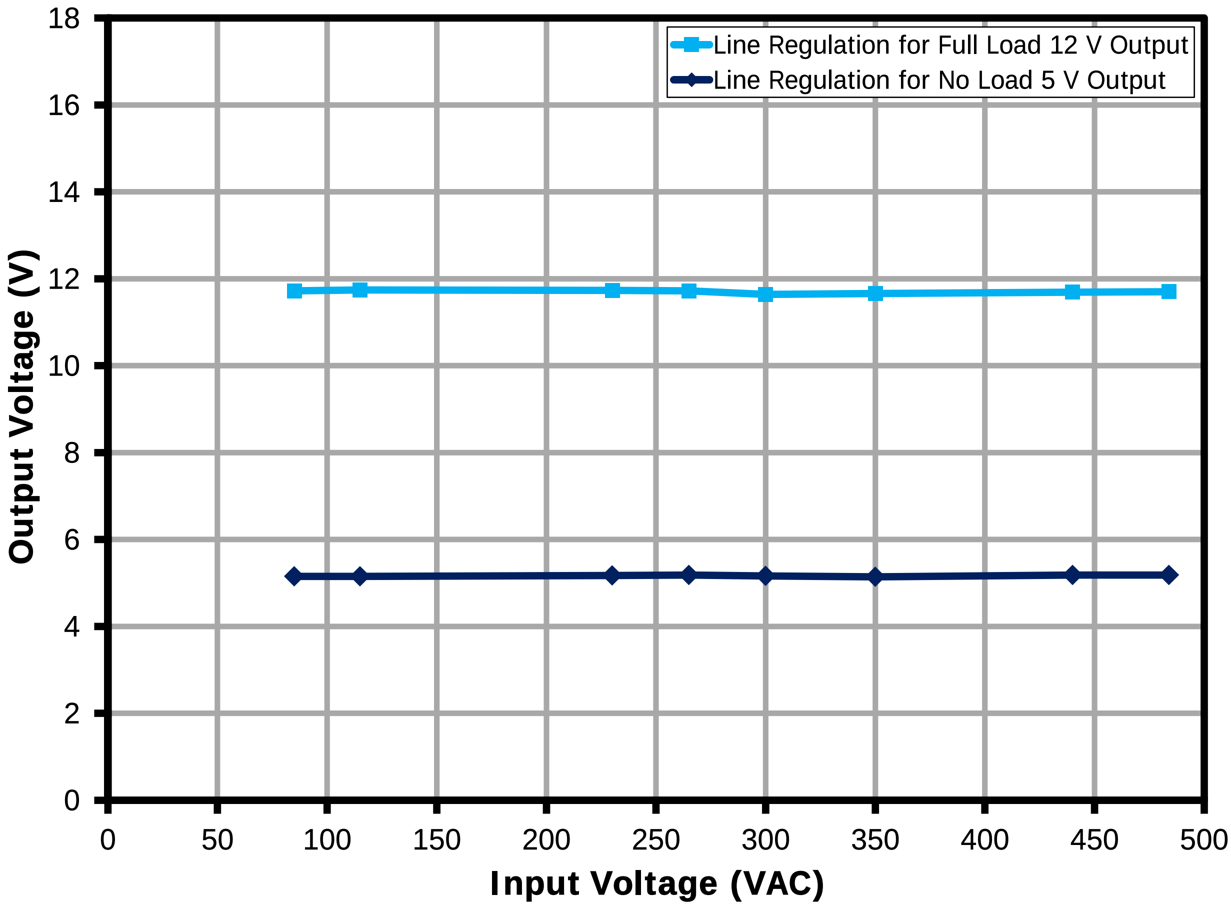

Figure 15 – 12 V Output Voltage vs. Output Load, Room Temperature.

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11 Thermal Performance

11.1 *85 VAC*

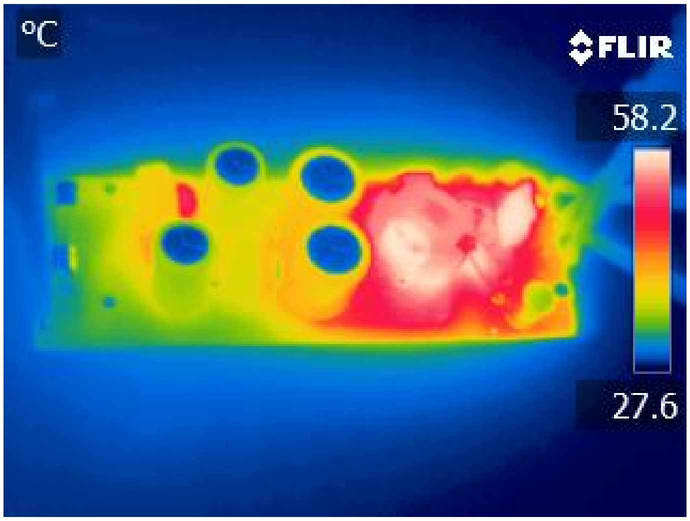

Figure 16 – Transformer Side. 85 VAC, Full Load.

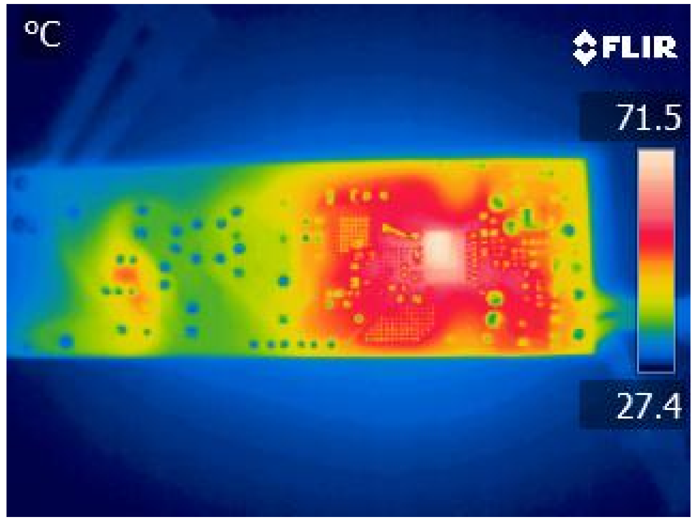

Figure 17 – InnoSwitch-EP Side. 85 VAC, Full Load.

	Reference	°C
Ambient		26.2
Transformer	T1	55.1
Input Capacitor	C17	41
Input Capacitor	C18	40.7
Bridge Rectifier	BR1	51.9
Thermistor	RT1	51.2

	Reference	°C
Ambient		26.2
InnoSwitch-EP	U1	71.5
SR FET Q1	Q1	58
SR FET Q2	Q2	51.5

11.2 *484 VAC*

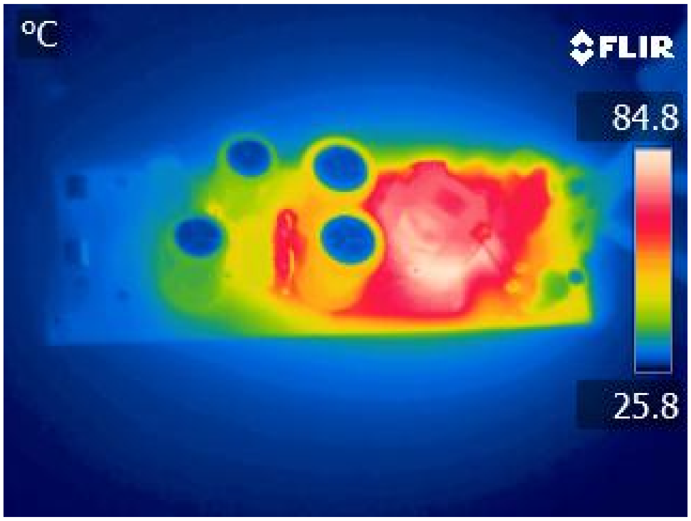

Figure 18 – Transformer Side. 265 VAC, Full Load.

	Reference	°C
Ambient		27.1
Transformer	T1	76.1
Input Capacitor	C17	55.9
Input Capacitor	C18	55.2
Bridge Rectifier	BR1	43.6

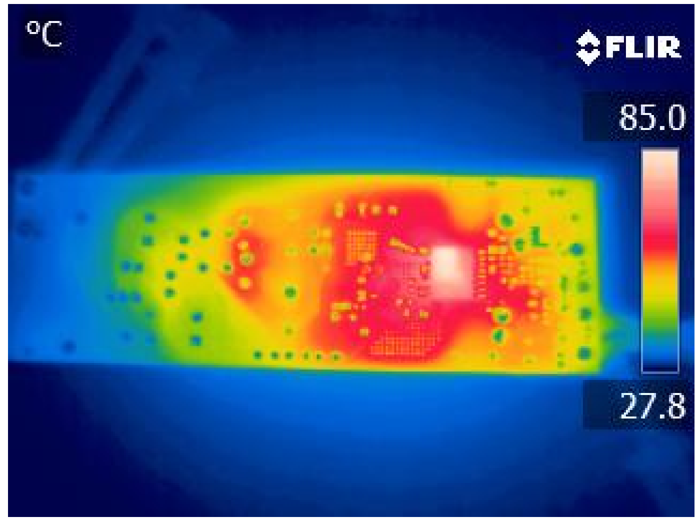

Figure 19 – InnoSwitch-EP Side. 265 VAC, Full Load.

	Reference	°C
Ambient		27.1
InnoSwitch-EP	U1	85
SR FET Q1	Q1	69.2
SR FET Q2	Q2	55.6

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12 Output Power vs. Thermal Rise at 85° Ambient for Different AC Input Voltages

Input Voltage(VAC)	Output Power(W)	T(amb) in (°C)	T(Inno) in (°C)	dT(Rise)
484	5.8	85.5	109.8	24.3
440	6.94	85.2	110.1	24.9
350	9.54	85.1	109.2	24.1
265	11.4	85.2	109	23.8
85	10.12	85.5	109.5	24

Note: All the measurements are done using thermo couples.

13 Waveforms

13.1 *Load Transient Response*

13.1.1 5 V Load Transient (No-Load to Full Load) and No-Load on 12 V Output

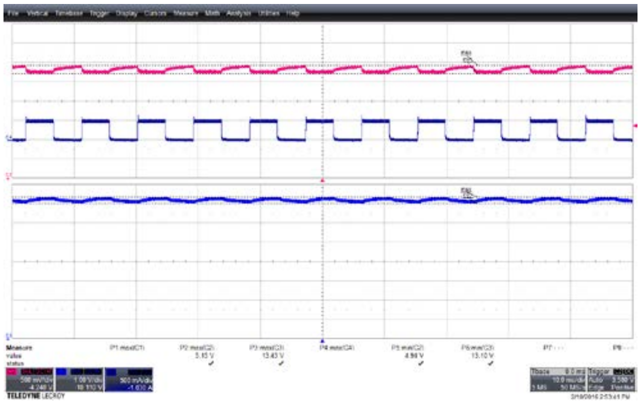

Figure 20 – 0.0 A – 0.5 A, 5 V Load Step Transient Response, 85 VAC.
5 V_{MIN}: 4.94 V.
5 V_{MAX}: 5.15 V.
12 V_{MIN}: 13.10 V.
12 V_{MAX}: 13.43 V.
Upper: 5 V_{OUT}, 0.5 V / div.
Middle: 5 V Load, 0.5 A, 10 ms / div.
Lower: 12 V_{OUT}, 1 V / div.

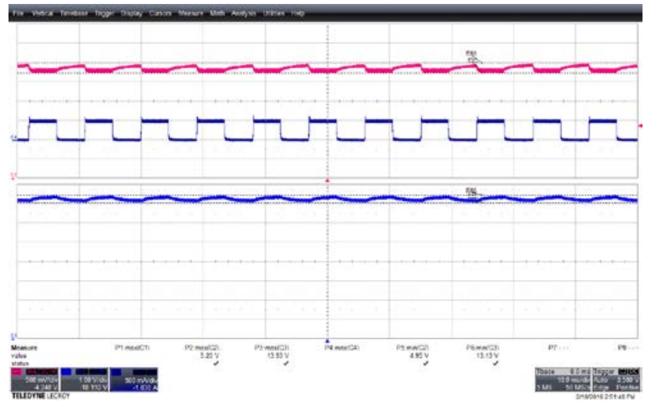

Figure 21 – 0.0 A – 0.5 A, 5 V Load Step Transient Response, 484 VAC.
5 V_{MIN}: 4.95 V.
5 V_{MAX}: 5.20 V.
12 V_{MIN}: 13.13 V.
12 V_{MAX}: 13.53 V.
Upper: 5 V_{OUT}, 0.5 V / div.
Middle: 5 V Load, 0.5 A, 10 ms / div.
Lower: 12 V_{OUT}, 1 V / div.

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13.1.2 5 V Load Transient (No-Load to Full Load) and Full Load on 12 V Output

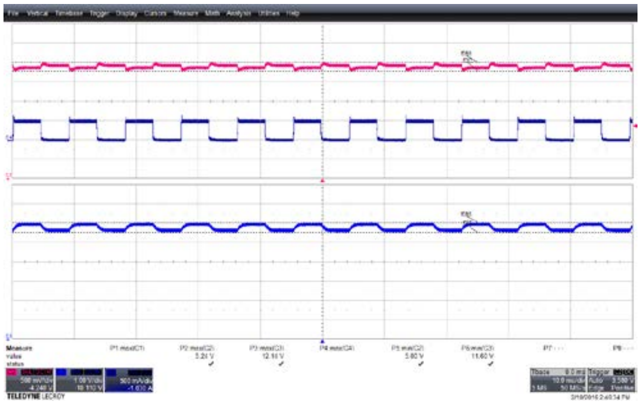

Figure 22 – 0.0 A – 0.5 A, 5 V Load Step Transient Response, 85 VAC.
5 V_{MIN}: 5.00 V.
5 V_{MAX}: 5.24 V.
12 V_{MIN}: 11.60 V.
12 V_{MAX}: 12.14 V.
Upper: 5 V_{OUT}, 0.5 V / div.
Middle: 5 V Load, 0.5 A, 10 ms / div.
Lower: 12 V_{OUT}, 1 V / div.

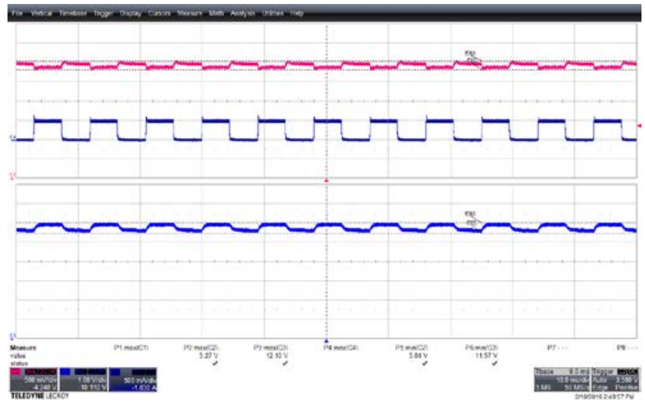

Figure 23 – 0.0 A – 0.5 A, 5 V Load Step Transient Response, 484 VAC.
5 V_{MIN}: 5.04 V.
5 V_{MAX}: 5.27 V.
12 V_{MIN}: 11.57 V.
12 V_{MAX}: 12.10 V.
Upper: 5 V_{OUT}, 0.5 V / div.
Middle: 5 V Load, 0.5 A, 10 ms / div.
Lower: 12 V_{OUT}, 1 V / div.

13.1.3 12 V Load Transient (No-Load to Full Load) and No-Load on 5 V Output

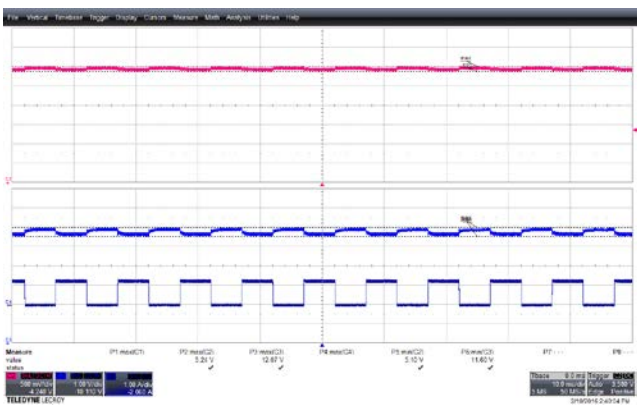

Figure 24 – 0.0 A – 1.25 A, 12 V Load Step Transient Response, 85 VAC.
5 V_{MIN}: 5.10 V.
5 V_{MAX}: 5.24 V.
12 V_{MIN}: 11.64 V.
12 V_{MAX}: 12.07 V.
Upper: 5 V_{OUT}, 0.5 V / div.
Middle: 12 V_{OUT}, 1 V / div.
Lower: 12 V Load, 1 A, 10 ms / div.

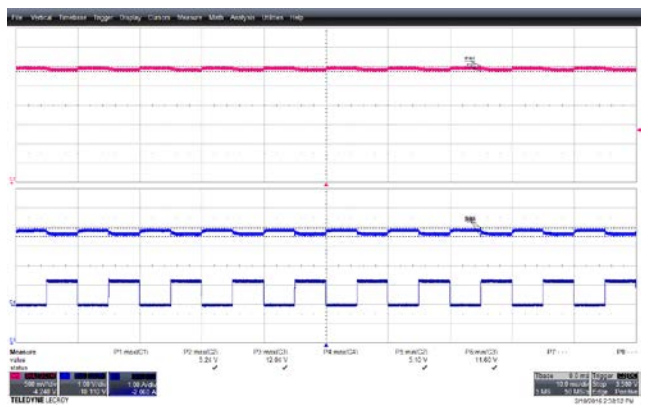

Figure 25 – 0.0 A – 1.25 A, 12 V Load Step Transient Response, 484 VAC.
5 V_{MIN}: 5.10 V.
5 V_{MAX}: 5.24 V.
12 V_{MIN}: 11.60 V.
12 V_{MAX}: 12.04 V.
Upper: 5 V_{OUT}, 0.5 V / div.
Middle: 12 V_{OUT}, 1 V / div.
Lower: 12 V Load, 1 A, 10 ms / div.

13.1.4 12 V Load Transient (No-Load to Full Load) and Full Load on 5 V Output

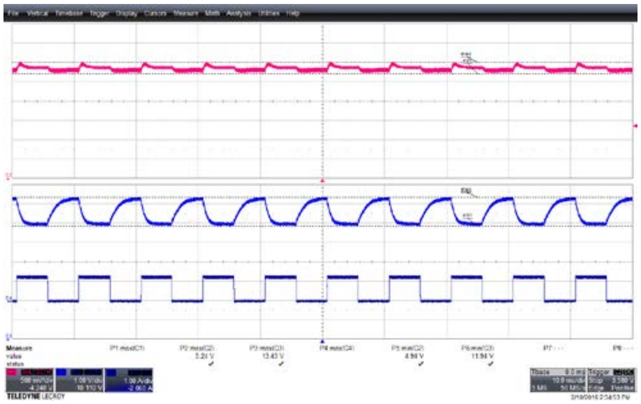

Figure 26 – 0.0 A – 1.25 A, 12 V Load Step Transient Response, 85 VAC.
5 V_{MIN}: 4.94 V.
5 V_{MAX}: 5.24 V.
12 V_{MIN}: 11.94 V.
12 V_{MAX}: 13.43 V.
Upper: 5 V_{OUT}, 0.5 V / div.
Middle: 12 V_{OUT}, 1 V / div.
Lower: 12 V Load, 1 A, 10 ms / div.

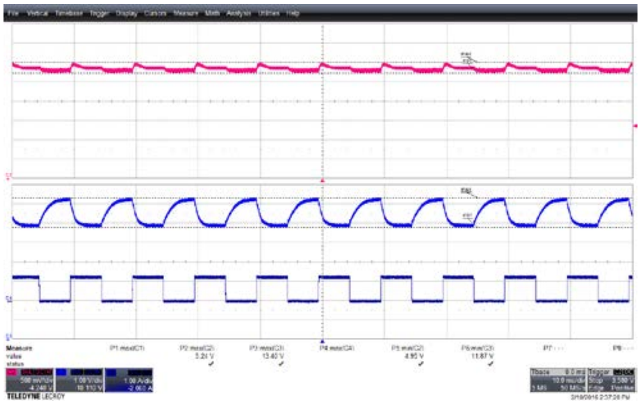

Figure 27 – 0.0 A – 1.25 A, 12 V Load Step Transient Response, 484 VAC.
5 V_{MIN}: 4.95 V.
5 V_{MAX}: 5.24 V.
12 V_{MIN}: 11.87 V.
12 V_{MAX}: 13.40 V.
Upper: 5 V_{OUT}, 0.5 V / div.
Middle: 12 V_{OUT}, 1 V / div.
Lower: 12 V Load, 1 A, 10 ms / div.

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13.2 *Switching Waveforms*

13.2.1 InnoSwitch-EP Waveforms

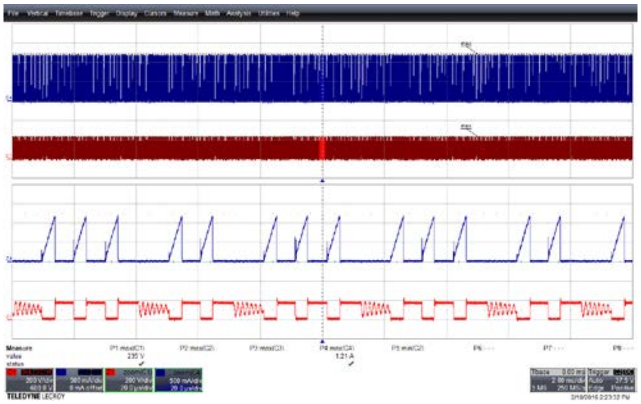

Figure 28 – Drain Voltage and Current Waveforms.
85 VAC Input, Full Load.
Upper: V_{DRAIN}, 200 V, 2 ms, 20 µs / div.
Lower: I_{DRAIN}, 500 mA / div.

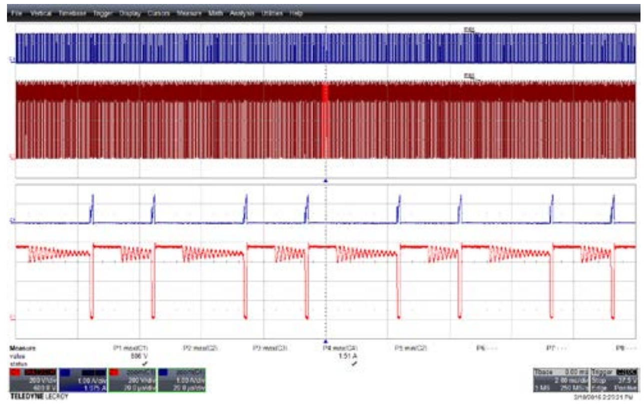

Figure 29 – Drain Voltage and Current Waveforms.
484 VAC Input, Full Load,
(Max V_{DRAIN}: 806 V.)
Upper: V_{DRAIN}, 200 V, 2 ms, 10 µs / div.
Lower: I_{DRAIN}, 1000 mA / div.

13.2.2 SR FET Waveforms

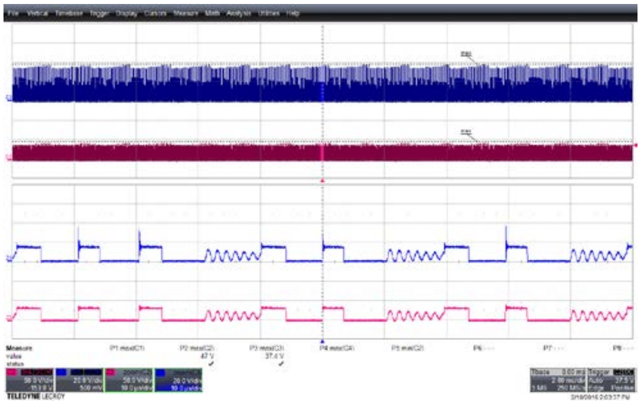

Figure 30 – SR FET Voltage Waveforms.
85 VAC Input, Full Load.
Upper: 5 V, 20 V /, 2 ms, 10 µs / div.
Lower: 12 V, 50 V / div.

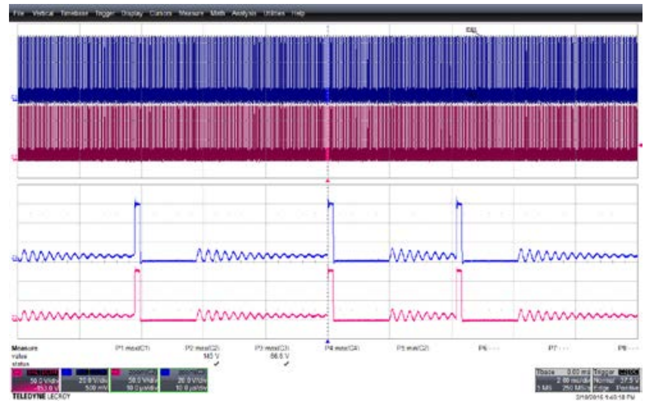

Figure 31 – SR FET Voltage Waveforms.
484 VAC Input, Full Load.
(143 V_{MAX} for 12 V, 66.6 V_{MAX} for 5 V.)
Upper: 5 V, 20 V /, 2 ms, 10 µs / div.
Lower: 12 V, 50 V / div.

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13.2.3 Output Voltage and Current Waveforms During Start-Up

13.2.3.1 Full load

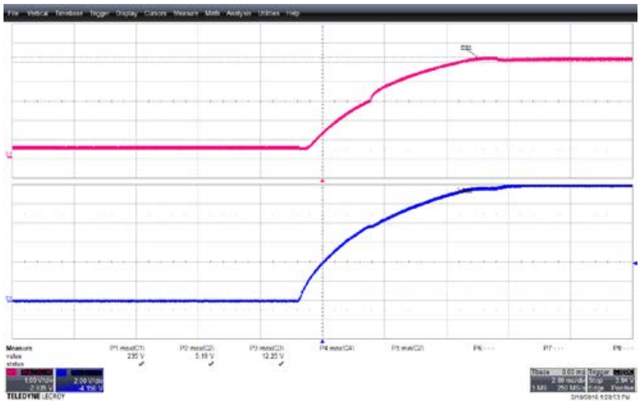

Figure 32 – Output Voltage Waveforms.
85 VAC Input.
Upper: 5 V, 1 V / div.
Lower: 12 V, 2 V / div, 2 ms / div.

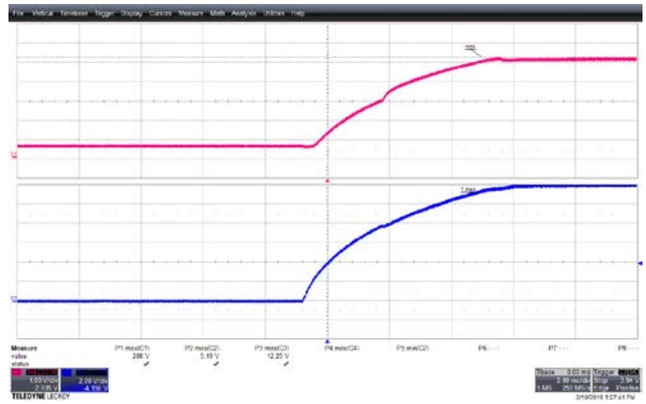

Figure 33 – Output Voltage Waveforms.
484 VAC Input.
Upper: 5 V, 1 V / div.
Lower: 12 V, 2 V / div., 2 ms / div.

13.2.3.2 No-Load

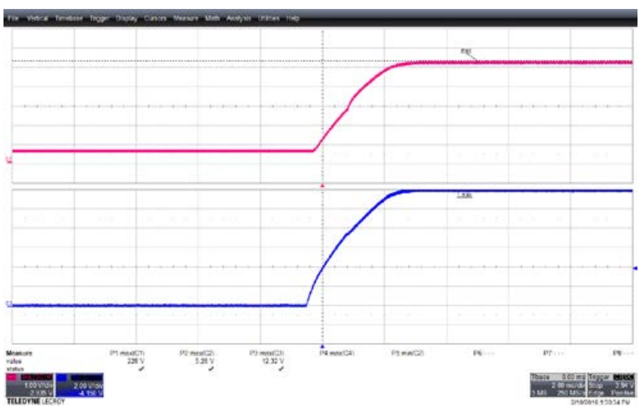

Figure 34 – Output Voltage Waveforms.
85 VAC Input.
Upper: 5 V, 1 V / div.
Lower: 12 V, 2 V / div., 2 ms / div.

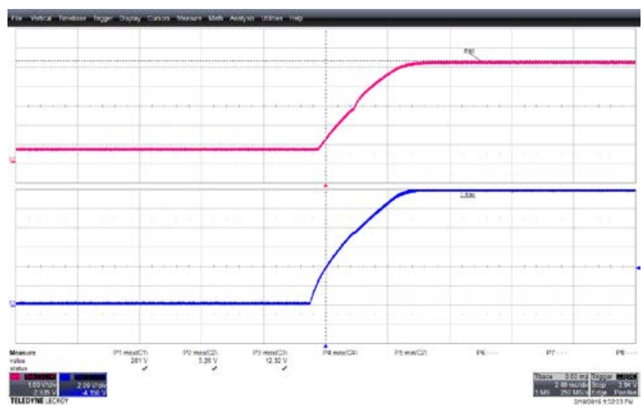

Figure 35 – Output Voltage Waveforms.
484 VAC Input.
Upper: 5 V, 1 V / div.
Lower: 12 V, 2 V / div., 2 ms / div.

13.3 *Output Ripple Measurements*

13.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

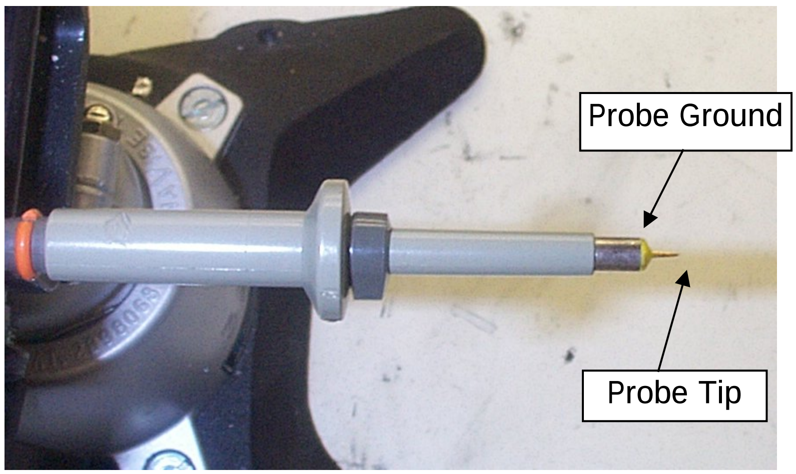

Figure 36 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

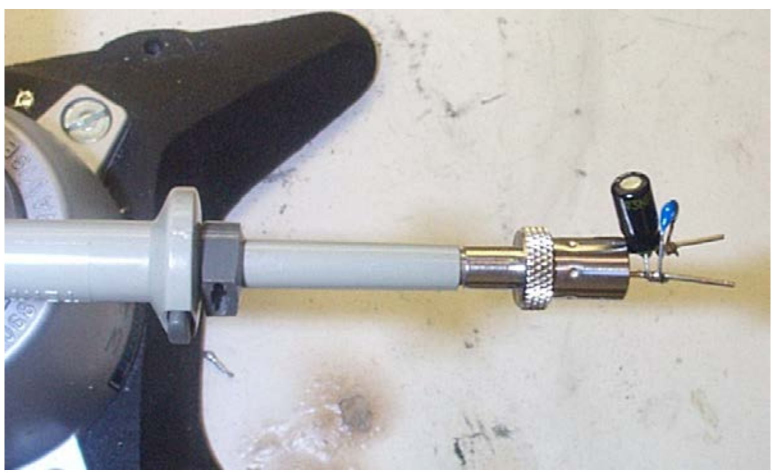

Figure 37 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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13.3.2 Ripple Voltage Waveforms

13.3.2.1 0.5 A Load on 5 V and 1.25 A Load on 12 V

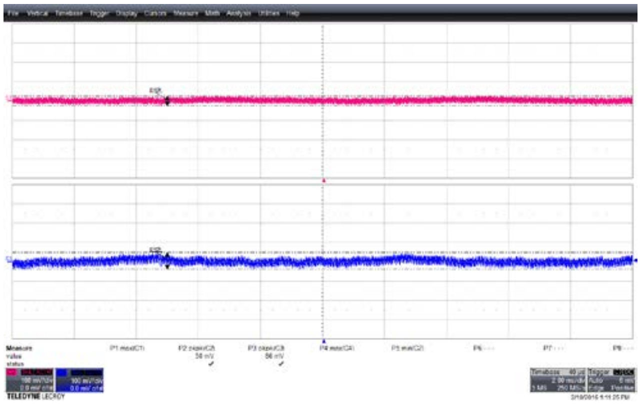

Figure 38 – Output Voltage Ripple Waveforms.
85 VAC Input. 1.25 A on 12 V.
5 V_{PK}: 50 mV, 12 V_{PK}: 86 mV.
Upper: 5 V, 100 mV / div.
Lower: 12 V, 100 mV, 2 ms / div.

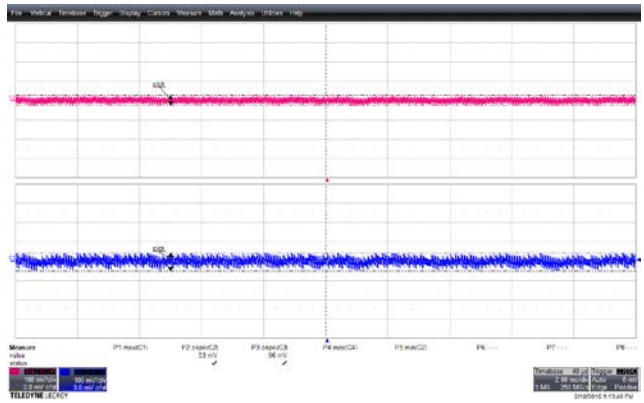

Figure 39 – Output Ripple Voltage Waveforms**.**
265 VAC Input. 1.25 A on 12 V.
5 V_{PK}: 53 mV, 12 V_{PK}: 96 mV.
Upper: 5 V, 100 mV / div.
Lower: 12 V, 100 mV, 2 ms / div.

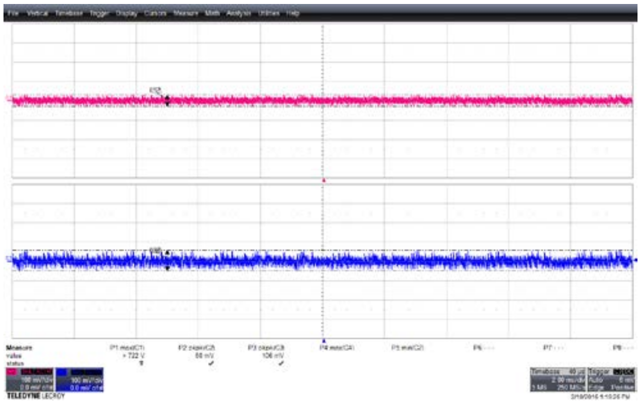

Figure 40 – Output Ripple Voltage Waveforms.
440 VAC Input. 1.25 A on 12 V.
5 V_{PK}: 60 mV, 12 V_{PK}: 106 mV.
Upper: 5 V, 100 mV / div.
Lower: 12 V, 100 mV, 2 ms / div.

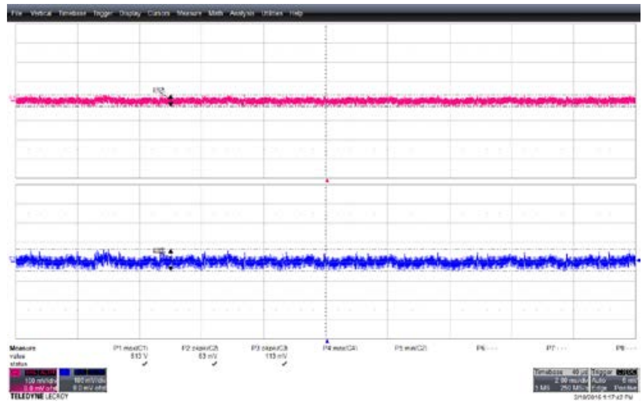

Figure 41 – Output Ripple Voltage Waveforms.
484 VAC Input. 1.25 A on 12 V.
5 V_{PK}: 63 mV, 12 V_{PK}: 113 mV.
Upper: 5 V, 100 mV / div.
Lower: 12 V, 100 mV, 2 ms / div..

13.4 Line Undervoltage and Overvoltage (DC Input)

Figure 42 – Line Undervoltage.
DC Input.
V_{UV+}:84.0 V, V_{UV-}: 70.2 V.
Upper (Output Voltage): 12 V , 5 V / div.
Lower: Voltage across C1& C2, 20 V, 2 s / div.

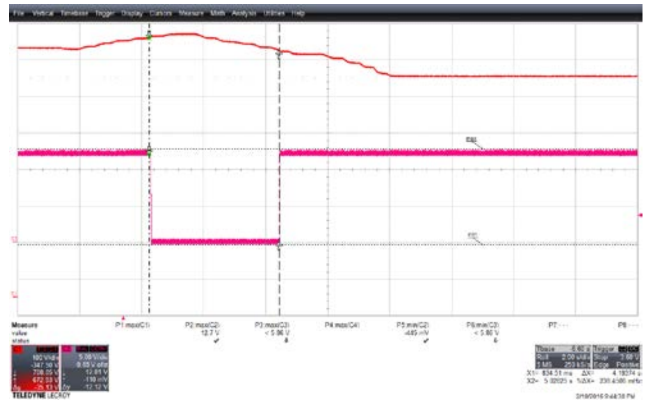

Figure 43 – Line Overvoltage.
DC Input, No-Load.
V_{OV+}: 708 V, V_{OV-}: 673 V.
Upper: 12 V , 5 V / div.
Lower: Voltage across C1& C2, 100 V, 2 s / div.

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14 ESD

Passed ±16.5 kV air discharge and 8 kV contact discharge.

Air discharge (kV)	Number of Strikes	Test Result
+16.5 KV	10	PASS
-16.5 KV	10	PASS

Contact discharge (kV)	Number of Strikes	Test Result
+8 KV	10	PASS
-8 KV	10	PASS

15 EMI

15.1 *Conductive EMI*

15.1.1 Earth Grounded Output (QP / AV)

15.1.1.1 110 VAC Input, Neutral

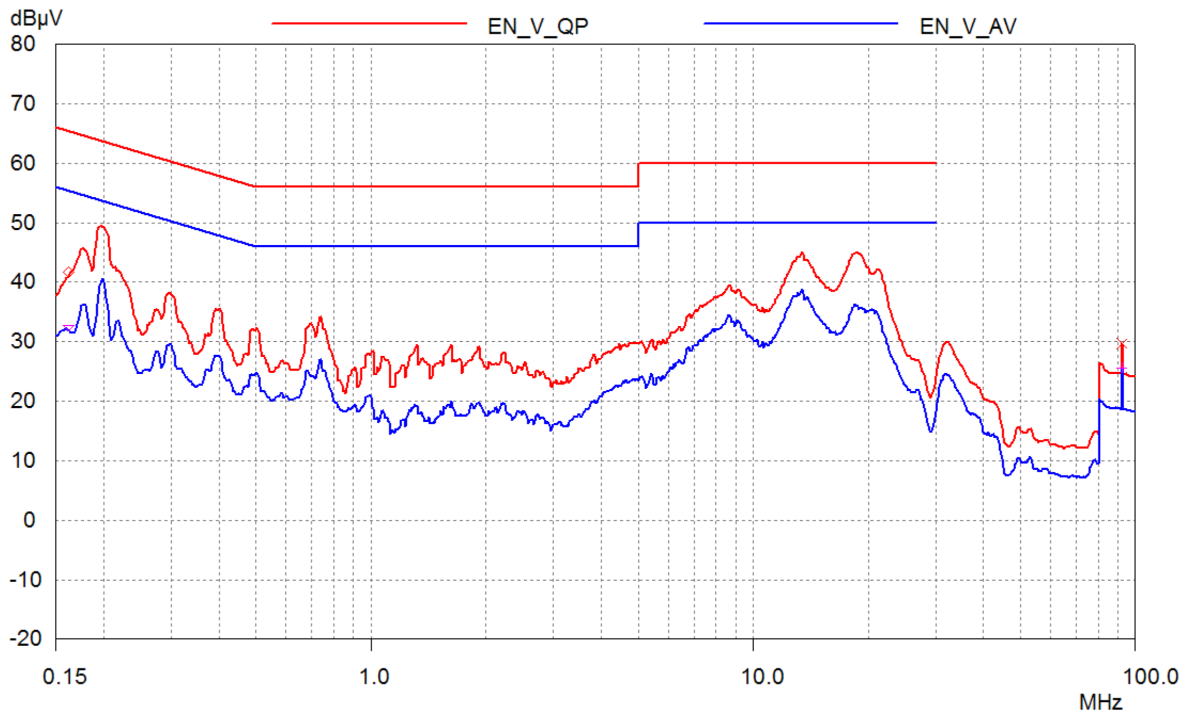

Figure 44 – Earth Ground at 110 VAC, Neutral.

15.1.1.2 110 VAC Input, Line

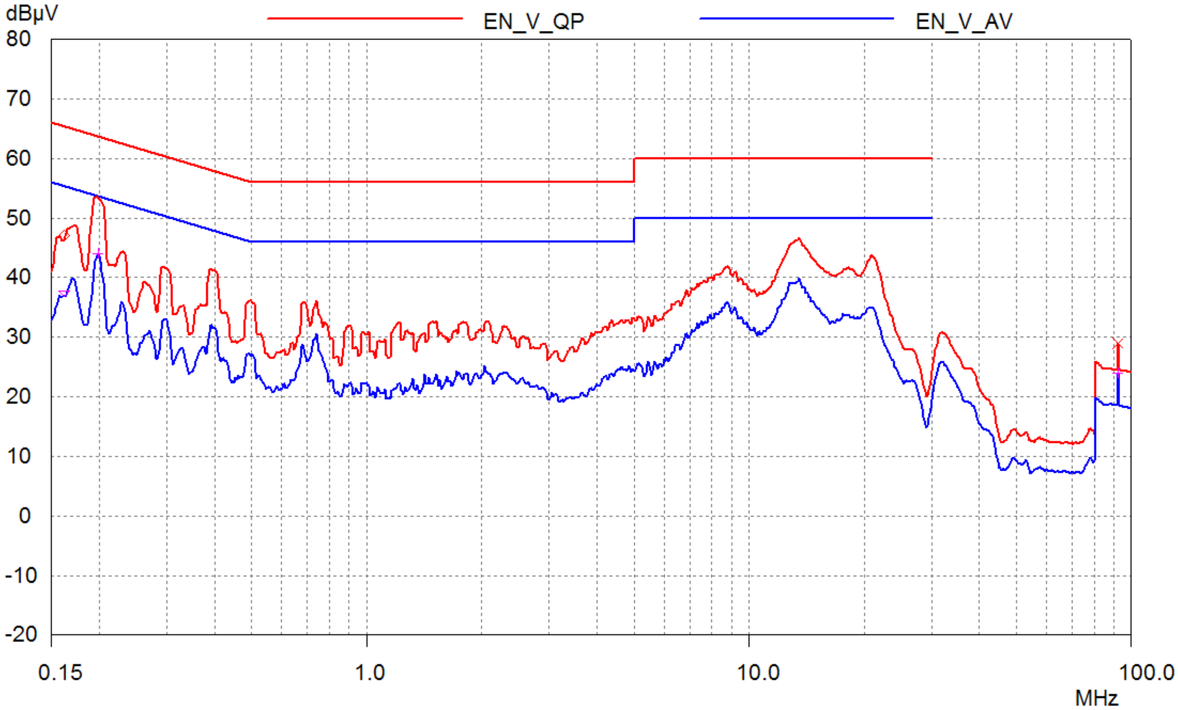

Figure 45 – Earth Ground at 110 VAC, Line.

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15.1.1.3 230 VAC Input, Neutral

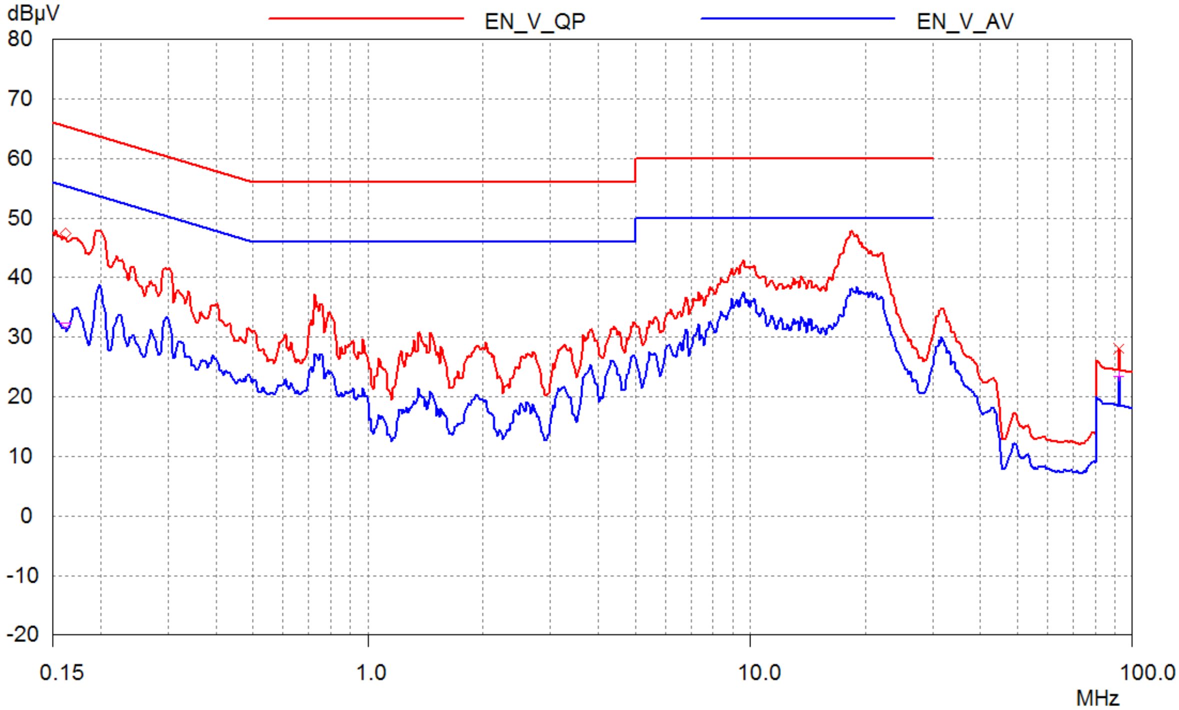

Figure 46 – Earth Ground at 230 VAC, Neutral.

15.1.1.4 230 VAC Input, Line

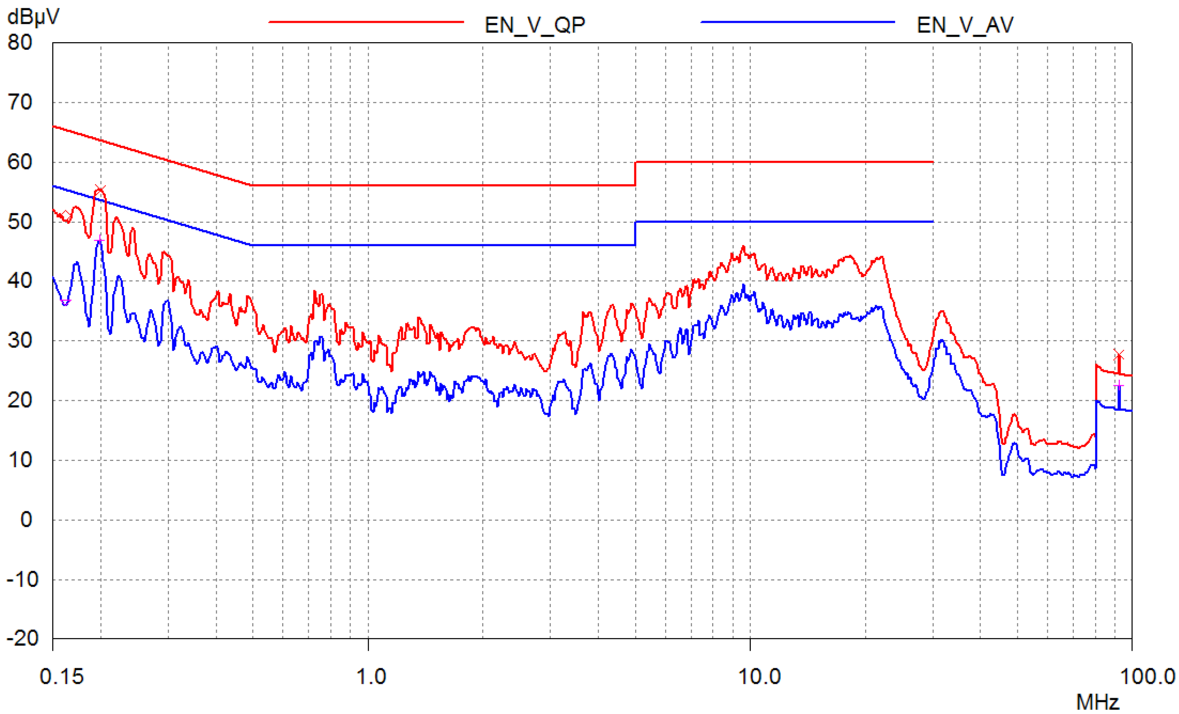

Figure 47 – Earth Ground at 230 VAC, Line.

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16 Lighting Surge Test

16.1 *Combination Wave Differential Mode Test*

Passed ±2 kV.

Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (W)	Number of Strikes	Test Result
±2	0	2	10	PASS
±2	90	2	10	PASS
±2	180	2	10	PASS
±2	270	2	10	PASS

16.2 *Ring Wave Common Mode Test*

Passed ±6 kV.

Ring Wave Voltage (kV)	Phase Angle (°)	Generator Impedance (W)	Number of Strikes	Test Result
±6	0	12	10	PASS
±6	90	12	10	PASS
±6	180	12	10	PASS
±6	270	12	10	PASS

17 Revision History

Date	Author	Revision	Description & Changes	Reviewed
22-Mar-16	SK	1.0	Initial Release.	Apps & Mktg
13-Apr-16	KM	1.1	Updated Schematic.	
12-Jul-16	KM	1.2	Added Magnetics Supplier	
07-Sep-16	KM	1.3	Changed to RDR, Updated Transformer and CMC Documentation	

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