

# MC100LVEL39

## 3.3V ECL $\div 2/4$ , $\div 4/6$ Clock Generation Chip

### Description

The MC100LVEL39 is a low skew  $\div 2/4$ ,  $\div 4/6$  clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended input signal. In addition, by using the  $V_{BB}$  output, a sinusoidal source can be AC coupled into the device.

The common enable ( $\overline{EN}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple LVEL39s, the Master Reset (MR) input must be asserted to ensure synchronization. For systems which only use one LVEL39, the MR pin need not be exercised as the internal divider design ensures synchronization between the  $\div 2/4$  and the  $\div 4/6$  outputs of a single device.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu\text{F}$  capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

### Features

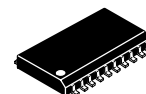
- 50 ps Maximum Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: Human Body Model; >2 kV
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  
 $V_{CC} = 3.0 \text{ V to } 3.8 \text{ V with } V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:  
 $V_{CC} = 0 \text{ V with } V_{EE} = -3.0 \text{ V to } -3.8 \text{ V}$
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



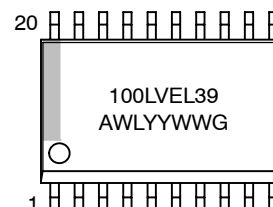
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SO-20 WB  
DW SUFFIX  
CASE 751D

### MARKING DIAGRAM\*



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

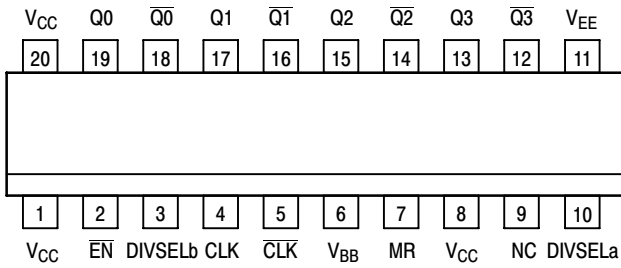
\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

- Moisture Sensitivity Level 1  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 419 devices
- Pb-Free Packages are Available\*

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Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout: SOIC-20 (Top View)

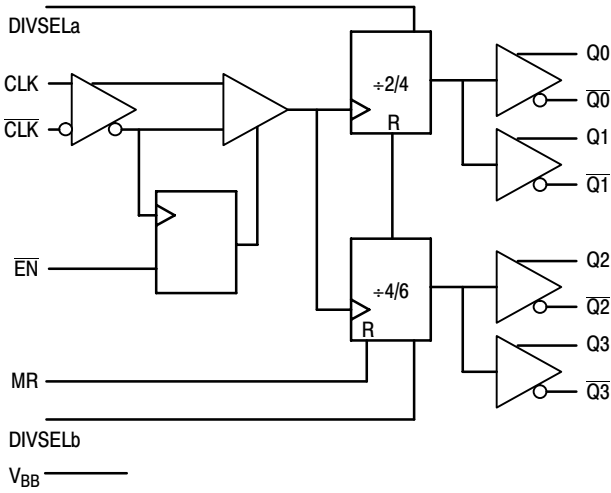


Figure 2. Logic Diagram

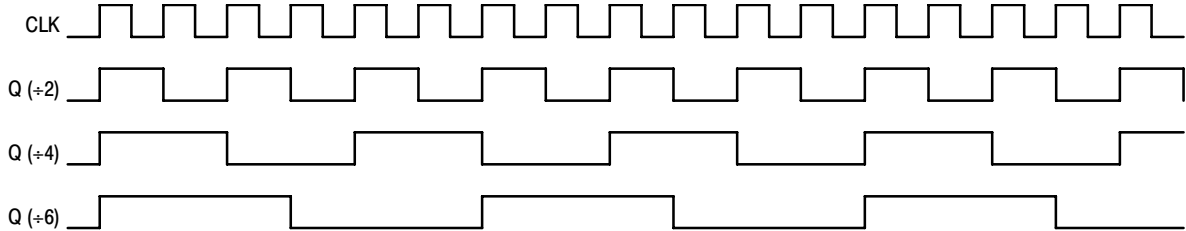


Figure 3. Timing Diagrams

Table 1. PIN DESCRIPTION

Column Head	
CLK, $\overline{\text{CLK}}$	ECL Diff Clock Inputs
$Q_0, Q_1; \overline{Q_0}, \overline{Q_1}$	ECL Diff $\div 2/4$ Outputs
$Q_2, Q_3; \overline{Q_2}, \overline{Q_3}$	ECL Diff $\div 4/6$ Outputs
DIVSELa, DIVSELb	ECL Frequency Select Inputs
$\overline{\text{EN}}$	ECL Sync Enable
MR	ECL Master Reset
$V_{BB}$	Reference Voltage Output
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply
NC	No Connect

Table 2. FUNCTION TABLE

CLK	$\overline{\text{EN}}$	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold $Q_0-3$
X	X	H	Reset $Q_0-3$

Z = Low-to-High Transition  
 ZZ = High-to-Low Transition  
 X = Don't Care

DIVSELa	$Q_0, Q_1$ Outputs
L	Divide by 2
H	Divide by 4

DIVSELb	$Q_2, Q_3$ Outputs
L	Divide by 4
H	Divide by 6

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**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		8 to 0	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-8 to 0	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 to 0 -6 to 0	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-20 SOIC-20	90 60	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-20	30 to 35	°C/W
T <sub>sol</sub>	Wave Solder	Pb Pb-Free	<2 to 3 sec @ 248°C <2 to 3 sec @ 260°C	265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 4. LVPECL DC CHARACTERISTICS** V<sub>CC</sub> = 3.3 V; V<sub>EE</sub> = 0.0 V (Note 1)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		50	59		50	59		54	61	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
V <sub>BB</sub>	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 6) V <sub>PP</sub> < 500 mV V <sub>PP</sub> ≥ 500 mV	1.3		2.9	1.2		2.9	1.2		2.9	V
		1.5		2.9	1.4		2.9	1.4		2.9	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary ±0.3 V.
2. Outputs are terminated through a 50 Ω resistor to V<sub>CC</sub> - 2.0 V.
3. V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>, max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V<sub>PPmin</sub> and 1.0 V.

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**Table 5. LVNECL DC CHARACTERISTICS**  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 4)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		50	59		50	59		54	61	mA
$V_{OH}$	Output HIGH Voltage (Note 5)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 5)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 6) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$	-2.0		-0.4	-2.1		-0.4	-2.1		-0.4	V
		-1.8		-0.4	-1.9		-0.4	-1.9		-0.4	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
- Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ; max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1.0\text{ V}$ .

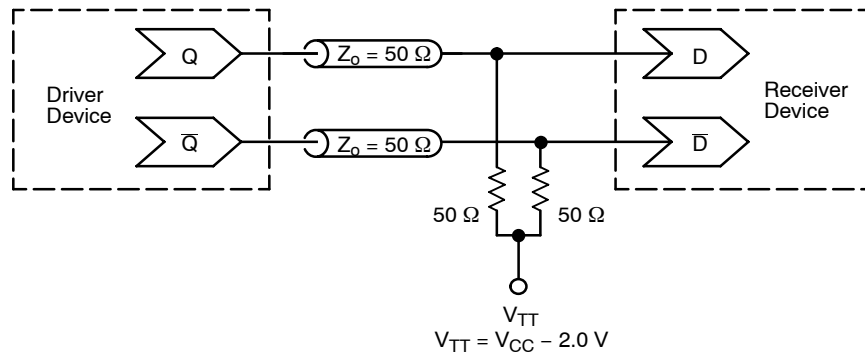
**Table 6. AC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 7)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency	1000			1000			1000			MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delayed Output CLK to Q (Diff) CLK to Q (S.E.) MR to Q	850		1150	900		1200	950		1250	ps
		850		1150	900		1200	950		1250	ps
		600		900	610		910	630		930	ps
$t_{SKEW}$	Within-Device Skew (Note 8) Part-to-Part $Q_0 - Q_3$ (Diff)			50			50			50	ps
				200			200			200	ps
$t_{JITTER}$	Random CLOCK Jitter (RMS) @ 1000 MHz		2.0	3.0		2.0	3.0		2.0	3.0	ps
$t_S$	Setup Time $\overline{EN}$ to $\overline{CLK}$ DIVSEL to CLK	250			250			250			ps
		400			400			400			ps
$t_H$	Hold Time CLK to $\overline{EN}$ CLK to Div_Sel	100			100			100			ps
		150			150			150			ps
$V_{PP}$	Input Swing (Note 9) CLK	250		1000	250		1000	250		1000	mV
$t_{RR}$	Reset Recovery Time			100			100			100	ps
$t_{PW}$	Minimum Pulse Width CLK MR	500			500			500			ps
		700			700			700			ps
$t_r, t_f$	Output Rise/Fall Times Q (20% - 80%)	280		550	280		550	280		550	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- $V_{EE}$  can vary  $\pm 0.3\text{ V}$ . Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
- Skew is measured between outputs under identical transitions.
- $V_{pp(min)}$  is minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to  $100\text{ mV}$ .

## MC100LVEL39



**Figure 4. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC100LVEL39DW	SOIC-20	38 Units / Rail
MC100LVEL39DWG	SOIC-20 (Pb-Free)	38 Units / Rail
MC100LVEL39DWR2	SOIC-20	1000 / Tape & Reel
MC100LVEL39DWR2G	SOIC-20 (Pb-Free)	1000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

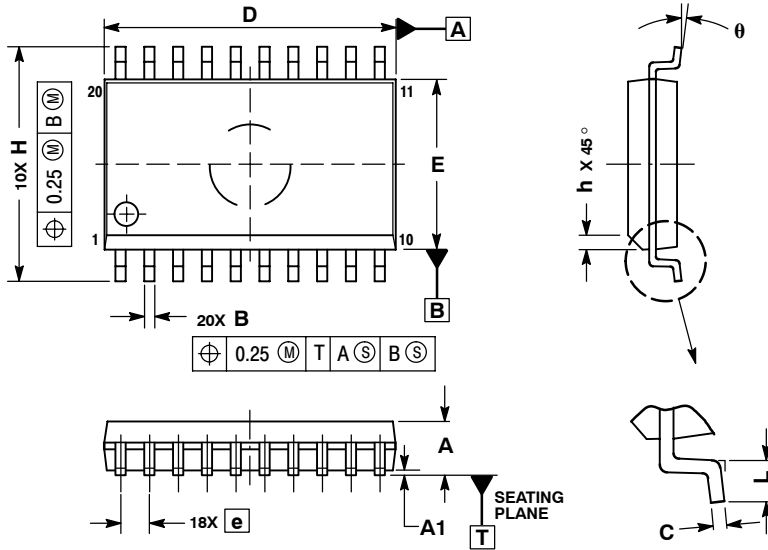
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC100LVEL39

## PACKAGE DIMENSIONS

SO-20 WB  
DW SUFFIX  
CASE 751D-05  
ISSUE G



**NOTES:**

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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