



BUK7240-100A

N-channel TrenchMOS standard level FET

Rev. 2 — 23 February 2011

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

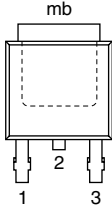
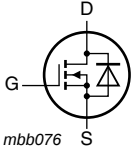
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3	-	-	34	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	114	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 175\text{ °C}$; see Figure 12 ; see Figure 13	-	-	100	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 12 ; see Figure 13	-	34	40	mΩ
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 35\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ Ω}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	-	122.5	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT428 (DPAK)

3. Ordering information

Table 3. Ordering information

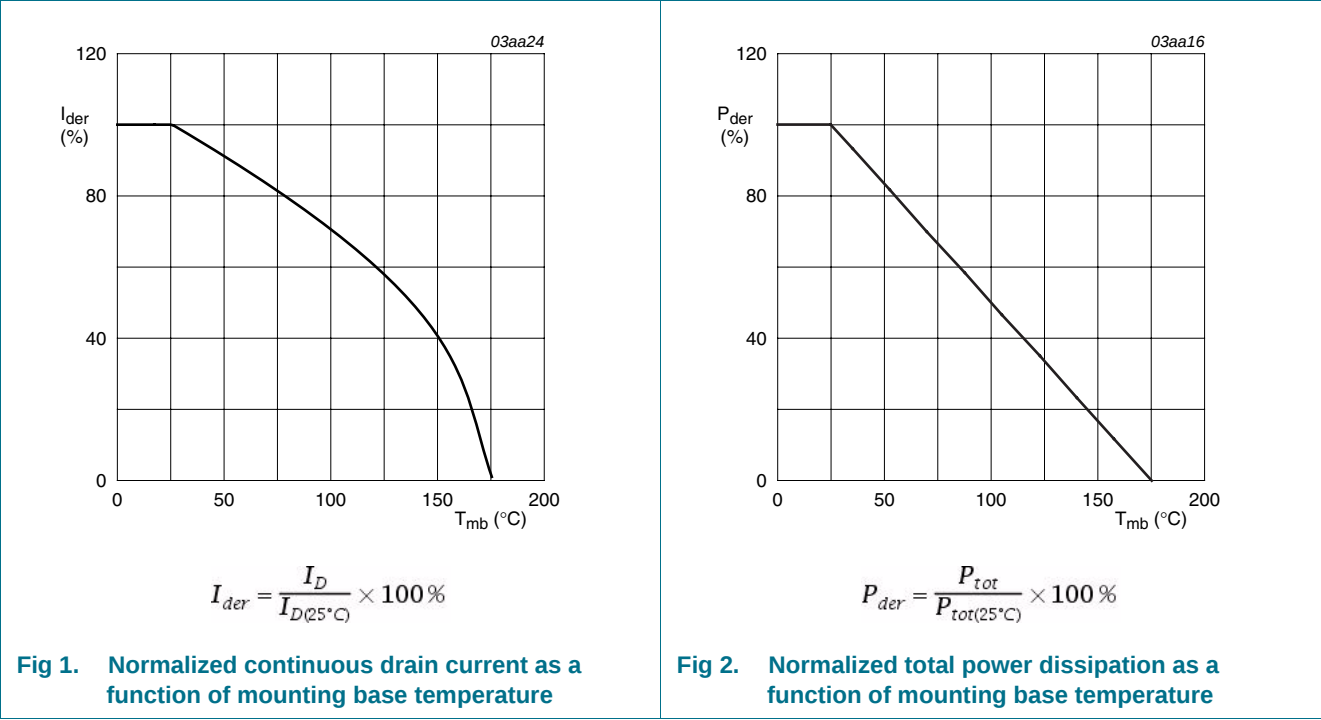
Type number	Package		Version
	Name	Description	
BUK7240-100A	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	100	V
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	100	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	T _{mb} = 100 °C; V _{GS} = 10 V; see Figure 1	-	24	A
		T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1 ; see Figure 3	-	34	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; see Figure 3 [1]	-	136	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	114	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	34	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	136	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 35 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped	-	122.5	mJ

[1] Peak drain current is limited by chip, not package.



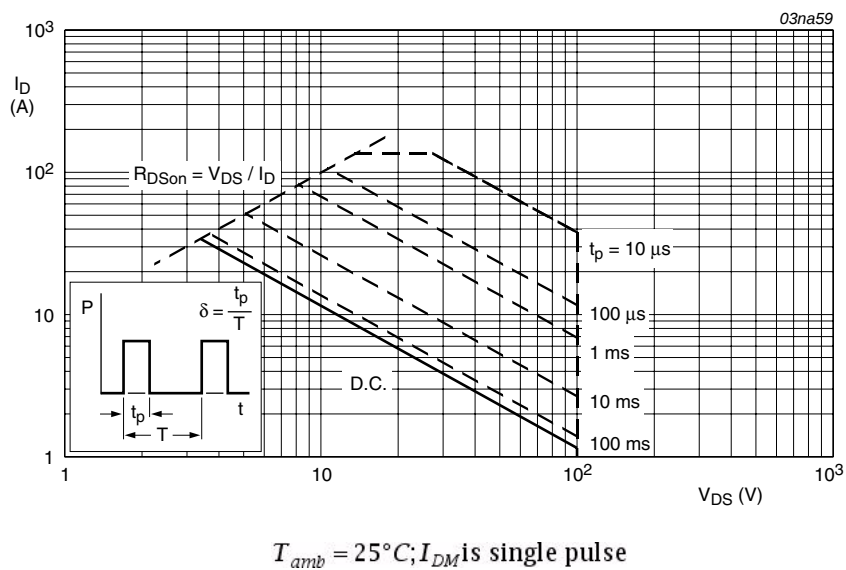


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	71.4	-	K/W

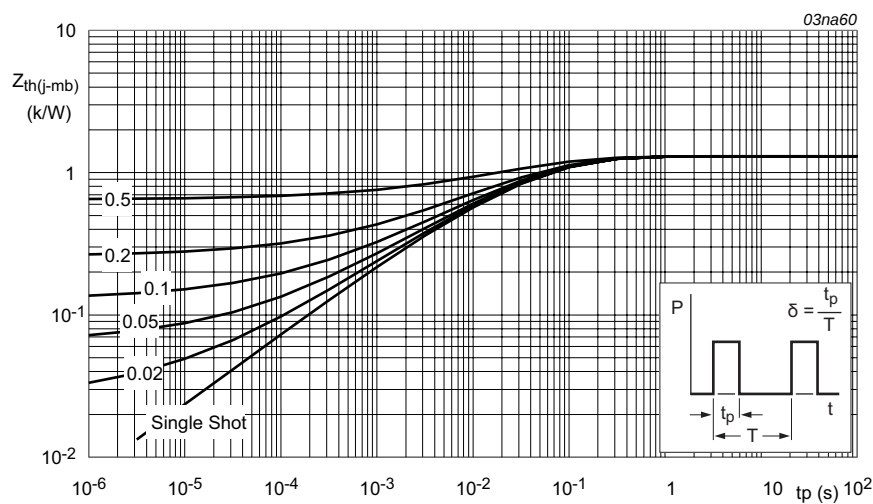


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 A; V _{GS} = 0 V; T _j = 25 °C	100	-	-	V
		I _D = 0.25 A; V _{GS} = 0 V; T _j = -55 °C	89	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 11	1	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 11	2	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 11	-	-	4.4	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	10	µA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	µA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; see Figure 12 ; see Figure 13	-	-	100	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 12 ; see Figure 13	-	34	40	mΩ
Dynamic characteristics						
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; see Figure 14	-	1720	2293	pF
C _{oss}	output capacitance		-	216	259	pF
C _{rss}	reverse transfer capacitance		-	133	182	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 1.5 Ω; V _{GS} = 10 V; R _{G(ext)} = 5.6 Ω; T _j = 25 °C	-	12	-	ns
t _r	rise time		-	55	-	ns
t _{d(off)}	turn-off delay time		-	48	-	ns
t _f	fall time		-	30	-	ns
L _D	internal drain inductance	measured from drain lead from package to centre of die; T _j = 25 °C	-	2.5	-	nH
L _S	internal source inductance	measured from source lead from package to source bond pad; T _j = 25 °C	-	7.5	-	nH
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 15	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 17 A; dI _S /dt = -100 A/µs; V _{GS} = -10 V; V _{DS} = 25 V; T _j = 25 °C	-	70	-	ns
Q _r	recovered charge		-	240	-	nC

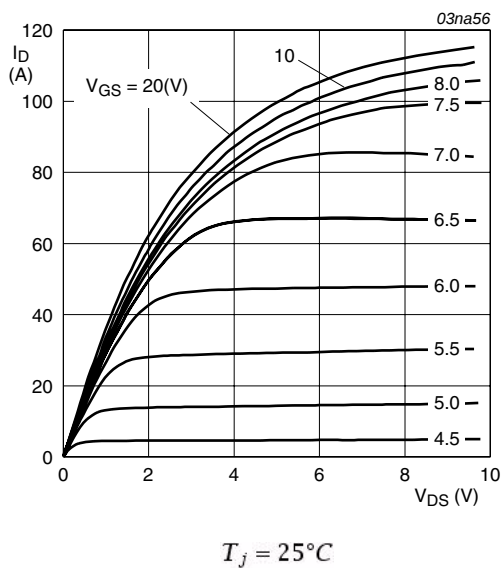


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

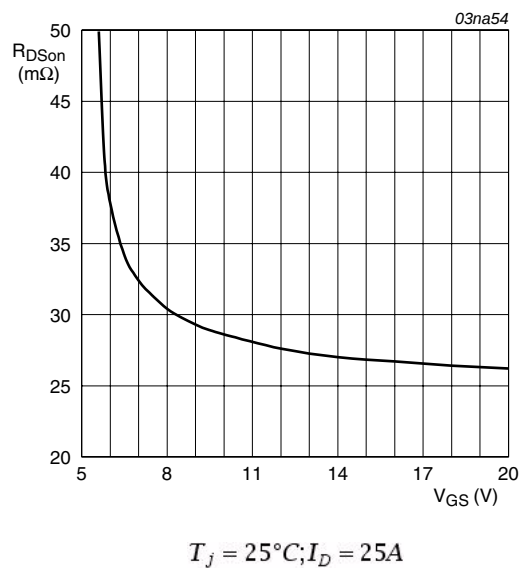


Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

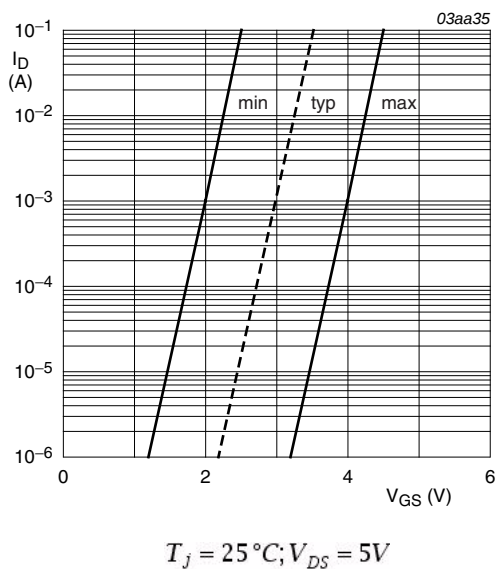


Fig 7. Sub-threshold drain current as a function of gate-source voltage

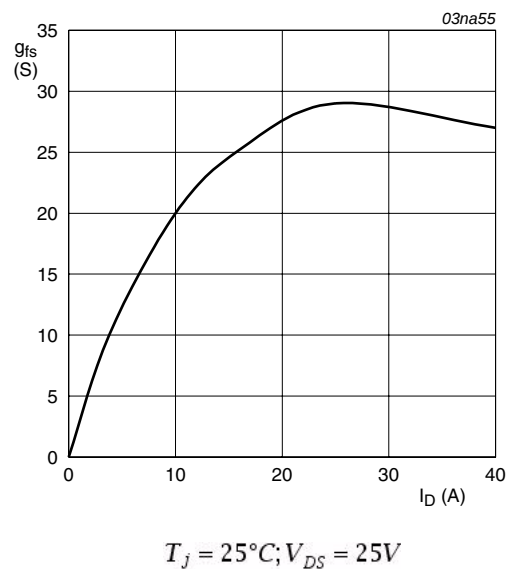


Fig 8. Forward transconductance as a function of drain current; typical values

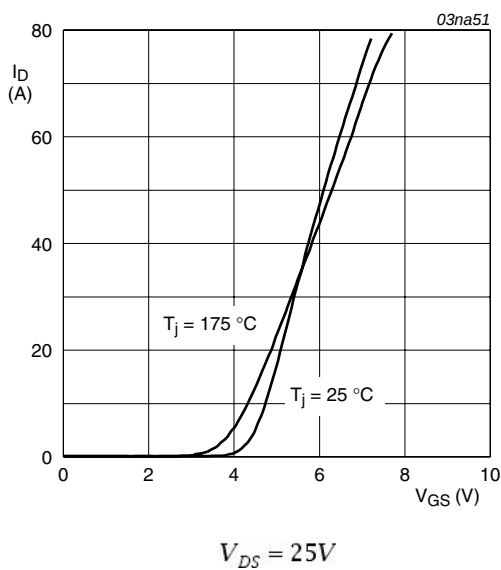


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

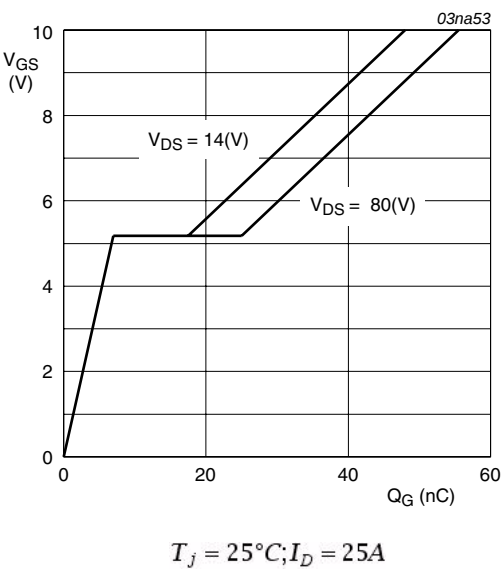


Fig 10. Gate-source voltage as a function of turn-on gate charge; typical values

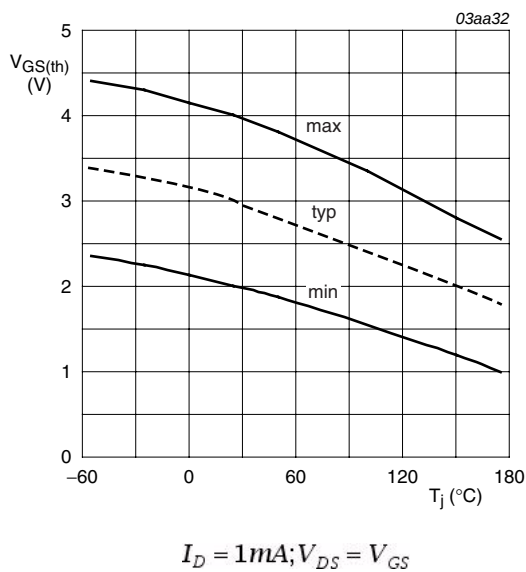


Fig 11. Gate-source threshold voltage as a function of junction temperature

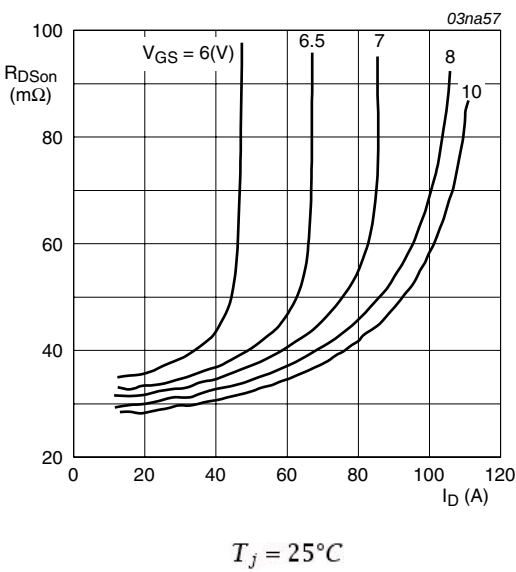
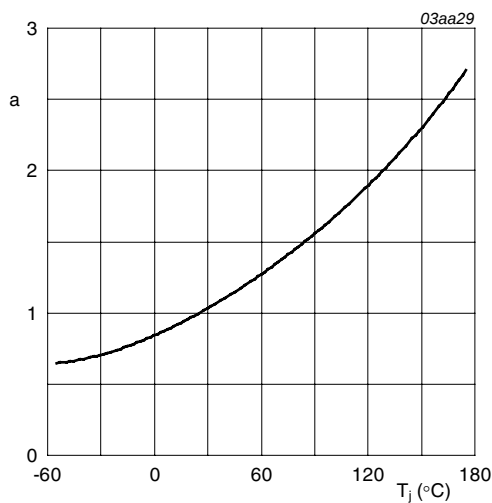
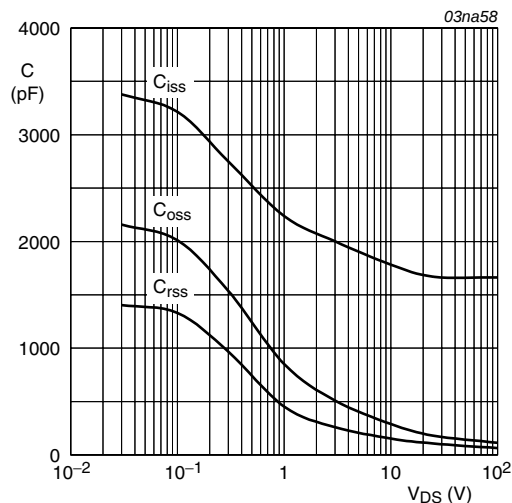


Fig 12. Drain-source on-state resistance as a function of drain current; typical values



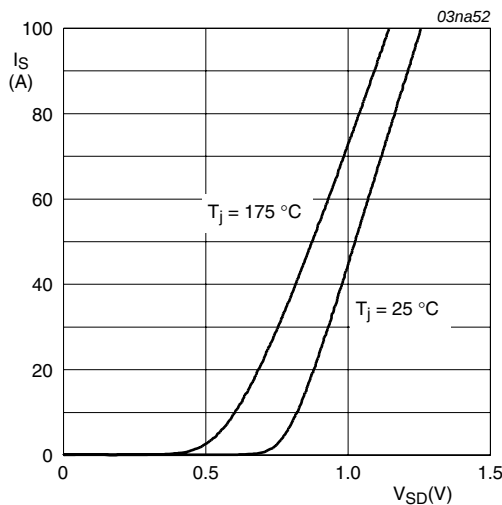
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



$$V_{GS} = 0V; f = 1\text{MHz}$$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$$V_{DS} = 0V$$

Fig 15. Reverse diode current; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

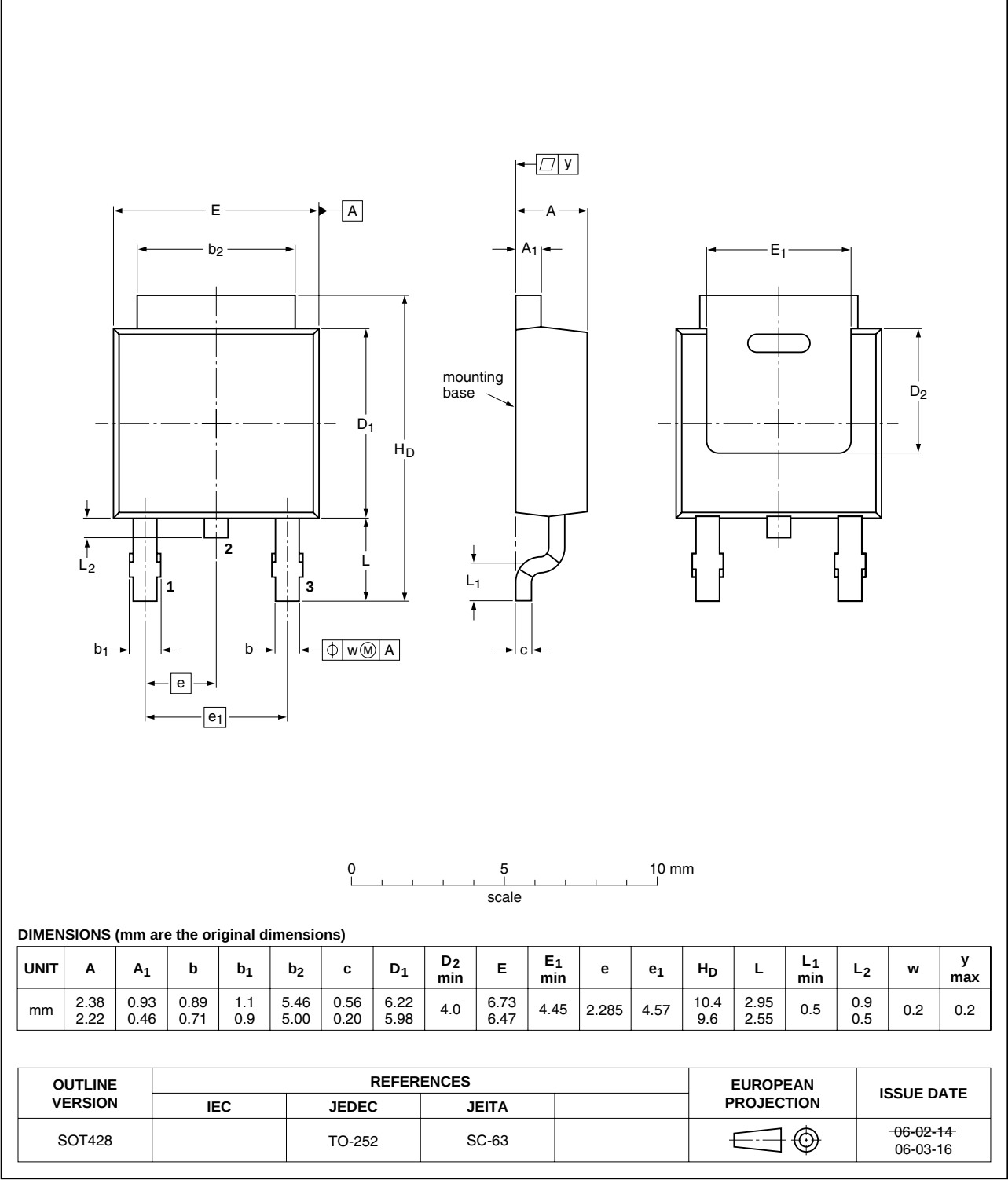


Fig 16. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7240-100A v.2	20110223	Product data sheet	-	BUK7240_100A-01
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.			
BUK7240_100A-01	20001003	Product specification	-	-

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Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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