

Product Description

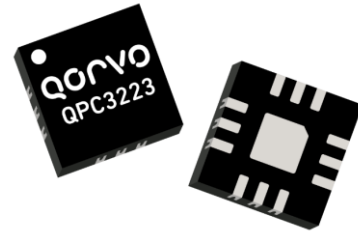
The QPC3223 is a 2-bit digital step attenuator (DSA) that features high linearity over the entire 18 dB gain control range in 6 dB steps. The QPC3223 uses a parallel control interface and has a low insertion loss of 0.8 dB at 2 GHz. The patented circuit architecture provides overshoot-free transient switching performance using a single +3 V to +5 V power supply.

The QPC3223 is available in an industry standard 12 pad 3 mm x 3 mm QFN package that is lead-free and RoHS-compliant

Functional Block Diagram



Top View



12 Pad 3.0 mm x 3.0 mm QFN package

Product Features

- Frequency Range 50 MHz to 6000 MHz
- 2-Bit, 18 dB Range, 6 dB Step
- Overshoot-free Transient Switching Performance
- High Linearity, Input IP3 > +55 dBm
- Parallel Control Interface
- Fast Switching Speed, 80 nsec Typical
- Single Supply +3 V to +5 V Operation
- 1.8V Logic Compatible
- RF Pins Have No DC Voltage, Can be DC Grounded Externally
- Patented Circuit Architecture
- Power-up Default Setting Is Maximum Attenuation

Applications

- 2G through 4G Base Stations
- Point-to-Point
- Wi-Fi
- Test Equipment

Ordering Information

| Part No. | Description |
|---------------|---------------------------------------|
| QPC3223SQ | 25 pieces sample bag |
| QPC3223SR | 100 pieces on a 7" reel |
| QPC3223TR7 | 2500 pieces on a 7" reel |
| QPC3223PCK401 | 50 – 6000 MHz PCBA w/5-pc. sample bag |

Absolute Maximum Ratings

| Parameter | Rating |
|--|----------------|
| Storage Temperature | -40 to +150 °C |
| Supply Voltage (V _{DD}) | -0.5 to +6.0 V |
| All Other DC and Logic Pins (Supply Voltage Must Be Applied Prior to Any Other Pin Voltages) | -0.5 to +6.0 V |
| Input Power (RFIN Pin, +85°C Case Temp.) | +30 dBm |
| Input Power (RFOUT Pin, +85°C Case Temp.) | +27 dBm |

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|-----------------------------------|------|-----|------|-------|
| Supply Voltage (V _{DD}) | +2.7 | | +5.5 | V |
| Case Temperature | -40 | | +105 | °C |
| Operating Junction Temp. | | | +125 | °C |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

| Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------------|--|--------------------------------|-----|------|-------|
| Frequency Range | | 50 | | 6000 | MHz |
| Insertion Loss | 2000 MHz, 0 dB Attenuation Setting | | 0.8 | | dB |
| Attenuation Range | 0.25 dB step size | | 18 | | dB |
| Attenuation Step | | | 6 | | dB |
| Attenuation Accuracy | | ± (0.2 + 4% of Atten. Setting) | | | dB |
| Input IP3 | | | +55 | | dBm |
| Input P0.1dB | | | +30 | | dBm |
| RF Input Power at RFIN Pin | Continuous operation at +85 °C case temperature | | | +27 | dBm |
| RF Input Power at RFOUT Pin | Continuous operation at +85 °C case temperature | | | +20 | dBm |
| Return Loss | | | 15 | | dB |
| Input and Output Impedance | | | 50 | | Ω |
| Switching Speed | 50% CTL to 10% / 90% RF | | 80 | | ns |
| Supply Current, I _{DD} | Steady state operation, current draw during attenuation state transitions is higher. | | 180 | | μA |
| Thermal Resistance | At maximum attenuation state with RF power applied to the RFIN pin | | 62 | | °C/W |

Notes:

1. Test conditions unless otherwise noted: V_{DD}=+5 V, Temp= +25 °C, Freq.=2000 MHz, 50 Ω system,

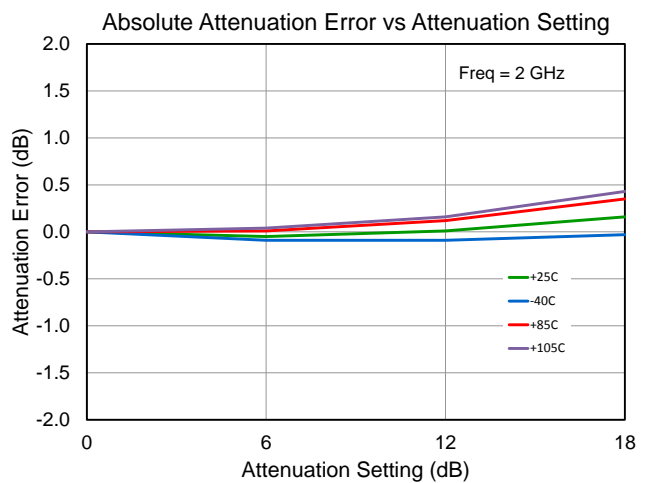
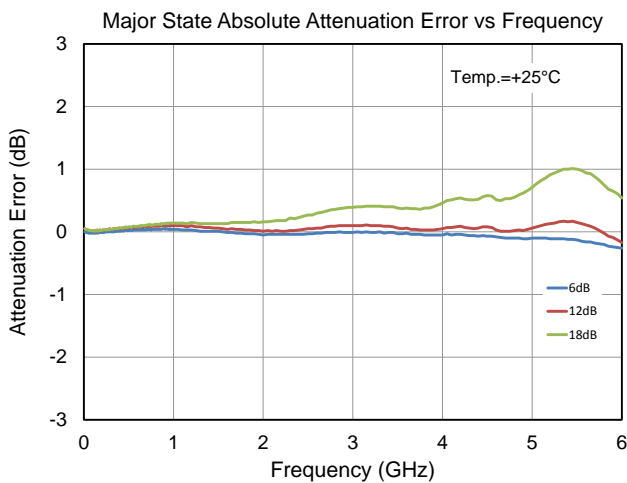
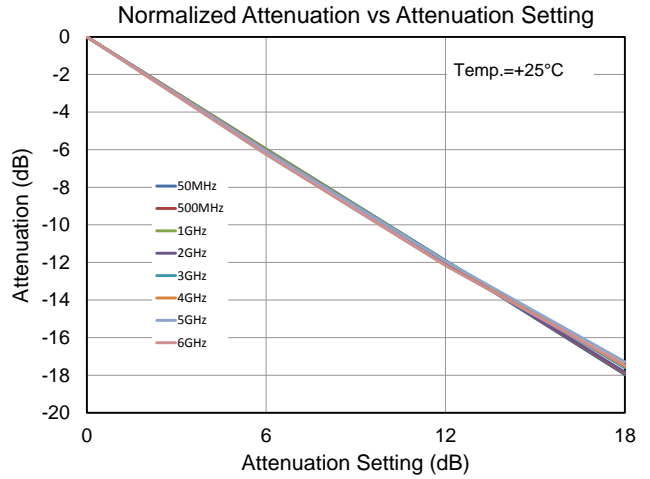
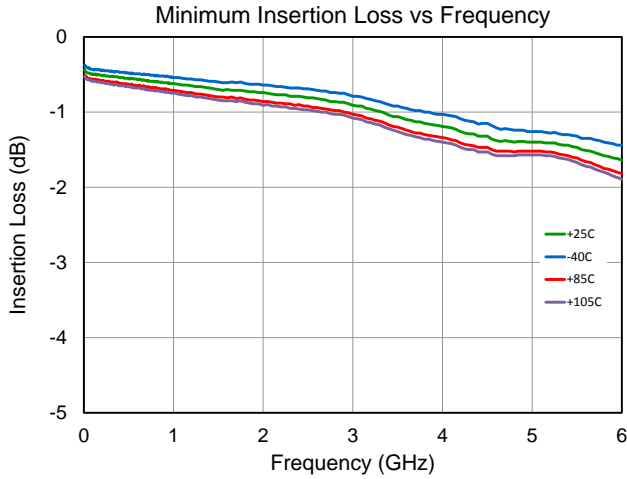
Control Logic Requirements

| Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------|------------|-------|-----|-----------------|-------|
| Low State Input Voltage | | -0.2 | | +0.63 | V |
| High State Input Voltage | | +1.17 | | V _{DD} | V |

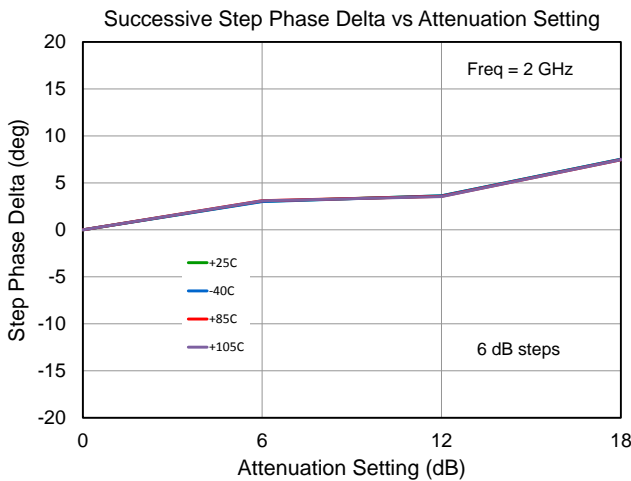
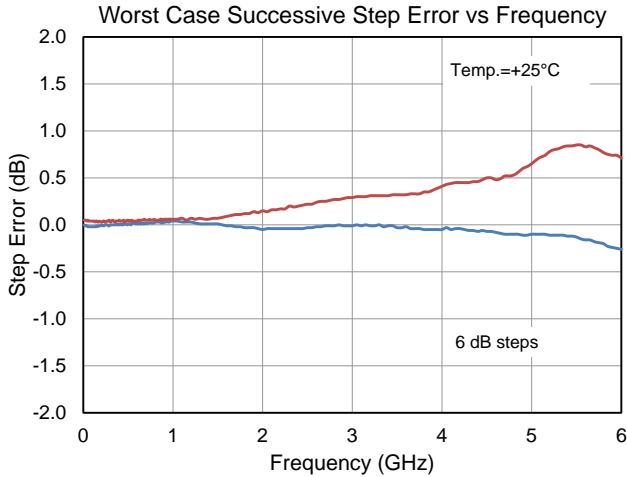
Notes:

1. Test conditions unless otherwise noted: V_{DD}=+5 V, Temp= +25 °C, Freq.=2000 MHz, 50 Ω system,

Typical Performance Plots



Typical Performance Plots



Typical Performance Plots



Typical Application Schematic – 50 MHz to 6000 MHz



Evaluation Board Schematic – 50 MHz to 6000 MHz



Evaluation Board Assembly Drawing



Bill of Material – Evaluation Board

| Reference Des. | Value | Description | Manufacturer | Part Number |
|----------------|--------|---|------------------------|--------------------|
| N/A | N/A | Printed Circuit Board | Qorvo | QPC3213-410(A) |
| U1 | N/A | Digital Step Attenuator, 50MHz to 6000MHz | Qorvo | QPC3223SB |
| C14 | 1 uF | CAP, 1µF, 10%, 25V, X7R, 1206 | Taiyo Yuden | CE TMK316BJ105KL-T |
| J1-J4 | N/A | CONN, SMA, END LNCH, UNIV, HYB MNT, FLT | Molex | SD-73251-4000 |
| P3 | N/A | CONN, HDR, ST, PLRZD, 2-PIN, 0.100" | ITW Pancon | MPSS100-2-C |
| P2 | N/A | CONN, SKT, 24-PIN DIP, 0.600", T/H | Aries Electronics Inc. | 24-6518-10 |
| P1 | N/A | CONN, HDR, ST, 9-PIN, 0.100", T/H | Samtec Inc. | TSW-109-07-G-S |
| M1 (See Note) | N/A | MOD, USB TO SERIAL UART, SSOP-28 | Future Technology | UM232R |
| C11 | 470 pF | CAP, 470pF, 5%, 50V, C0G, 0402 | Murata Electronics | GRM1555C1H471JA01D |
| C12-C13 | N/A | DNP | N/A | N/A |

Notes:

1. M1 should be mounted into P2 with respect to the Pin 1 alignment of M1 and P2.

Evaluation Board Programming Using USB Interface

Parallel Mode

Refer to the Control Bit Generator (CBG) Software Reference Manual for detailed instructions on how to setup the software for use. Apply the supply voltage to P3. Select 'QPC3223' from the Parts List of the CBG user interface. Set the attenuation value using the CBG user interface. The attenuator is set to the desired state and measurements can be taken.

Evaluation Board Programming Using External Bus

Parallel Mode

This configuration allows the user to control the attenuator through the P1 connector using an external harness. Remove the USB interface if it is currently installed on the evaluation board. Connect a user-supplied harness to the P1 connector. The parallel bus signal names for P1 are indicated on the evaluation board. Cross reference for device pins names to P1 connector signals is as follows: C1 = D0, C2 = D1. Apply the supply voltage to P3. Send the appropriate signals onto the parallel bus lines in accordance with the Parallel Interface Attenuation Truth Table. The attenuator is set to the desired state and measurements can be taken.

Default Power-up State

The default attenuation state is maximum (18dB) when supply voltage is applied to the attenuator. If a different attenuation state is desired during power up, this can be accomplished by applying signals according to the Parallel Interface Attenuation Truth Table. The attenuator will power up to the state applied to the parallel bus during turn on.

Parallel Interface Attenuation Truth

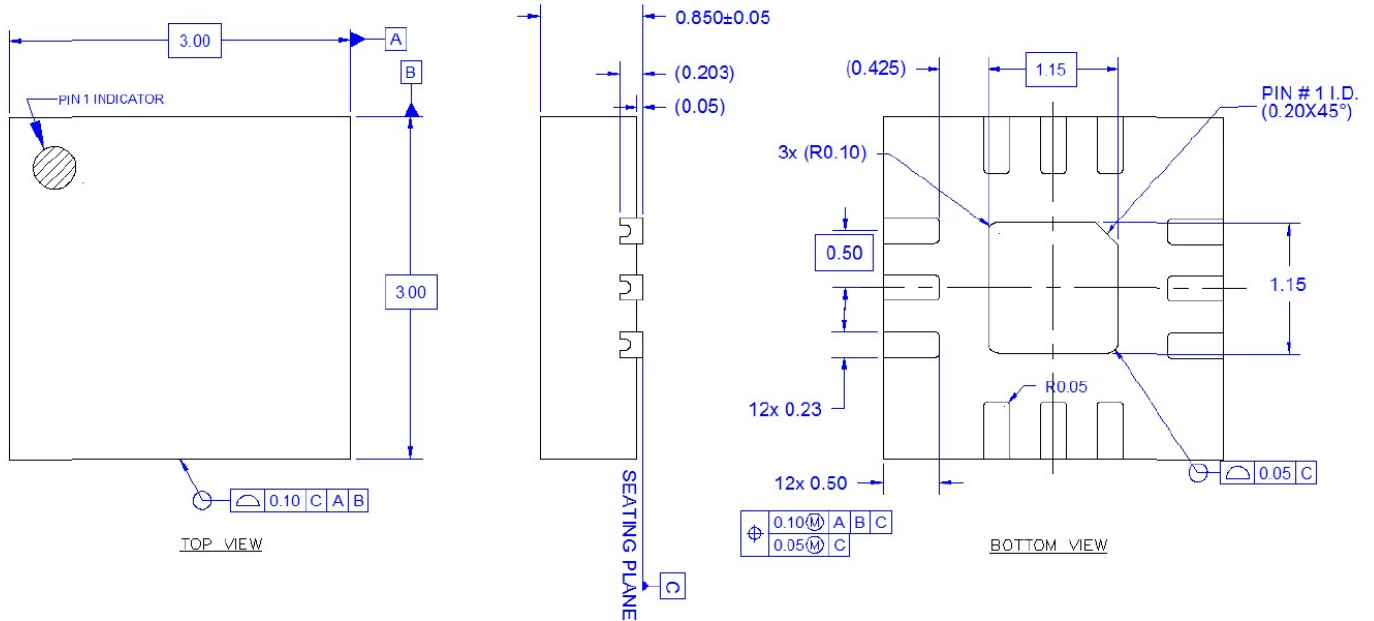
| Attenuation Word | | Attenuation State |
|------------------|---------|--------------------------------|
| C1 (D0) | C2 (D1) | |
| L | L | 0dB / Reference Insertion Loss |
| H | L | 6 dB |
| L | H | 12 dB |
| H | H | 18 dB |

Pad Configuration and Description



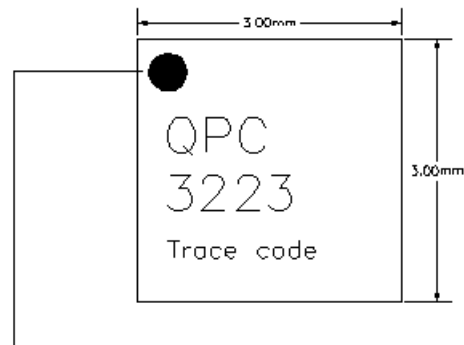
| Pad No. | Label | Description |
|--------------|-----------------|--|
| 1 | GND | Ground Pin; Connect to PCB ground |
| 2 | RFIN | RF Input Pin; Incident RF power must enter this pin for rated thermal performance and reliability. Do not apply DC power to this pin. Pin may be DC grounded externally and is grounded thru resistors internal to the part. |
| 3 | NC | Open in package. Connect to PCB ground or leave floating |
| 4 | NC | Open in package. Connect to PCB ground or leave floating |
| 5 | NC | Open in package. Connect to PCB ground or leave floating |
| 6 | NC | Open in package. Connect to PCB ground or leave floating |
| 7 | NC | Open in package. Connect to PCB ground or leave floating |
| 8 | RFOUT | RF Output Pin; Pin may be DC grounded externally and is grounded thru resistors internal to the part. |
| 9 | GND | Ground Pin; Connect to PCB ground |
| 10 | C2 | 12dB bit parallel logic input; 1.8V CMOS compatible logic |
| 11 | C1 | 6dB bit parallel logic input; 1.8V CMOS compatible logic |
| 12 | V _{DD} | Supply Voltage |
| Backside Pad | GND | RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint. |

Package Dimensions



- Notes:
1. All Dimensions in millimeters

Branding Diagram



Pin 1 Indicator
Trace code to be assigned by SubCon

Handling Precautions

| Parameter | Rating | Standard |
|----------------------------------|----------|---------------------------------|
| ESD – Human Body Model (HBM) | Class 1C | ANSI / ESDA / JEDEC JS-001-2014 |
| ESD – Human Body Model (CDM) | Class C3 | ANSI / ESDA / JEDEC JS-002-2014 |
| MSL – Moisture Sensitivity Level | Level 2 | IPC / JEDEC J-STD-020 |



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: Matte Tin

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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