



SY89833AL

3.3V Low Noise Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination

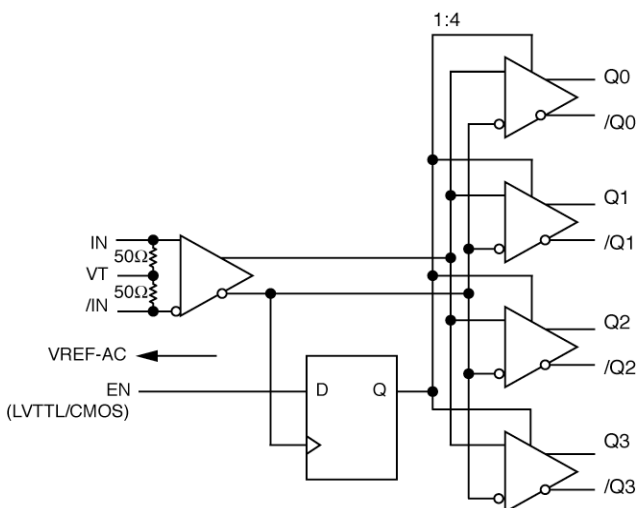
General Description

The SY89833AL is a lower noise version of the SY89833L 3.3V, high-speed 2GHz Low Voltage Differential Swing (LVDS) 1:4 fanout buffer. Within device skew is guaranteed to be less than 20ps over supply voltage and temperature.

The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A VREF-AC reference is included for AC-coupled applications.

The SY89833AL is part of Micrel's high-speed clock synchronization family. For 2.5V applications, the SY89832U provides similar functionality while operating from a 2.5V $\pm 5\%$ supply. For applications that require a different I/O combination, consult the Micrel website at: www.micrel.com, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators and clock generators. Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



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Features

- Guaranteed AC performance over temperature and voltage:
 - DC-to > 2GHz throughput
 - <470ps propagation delay (IN-to-Q)
 - <20ps within-device skew
 - <190ps rise/fall times
- Improved Ultra-low jitter design:
 - <1ps_{RMS} cycle-to-cycle jitter
 - <10ps_{PP} total jitter
 - <1ps_{RMS} random jitter
 - <10ps_{PP} deterministic jitter
 - <0.635ps @ 156.25MHz (Integrated from 12kHz to 20MHz)
- Unique input termination and VT pin accepts DC- and AC-coupled inputs
- High-speed LVDS outputs
- 3.3V power supply operation
- Industrial temperature range: -40°C to +85°C
- Available in 16-pin (3mm x 3mm) QFN package

Applications

- Processor clock distribution
- SONET clock distribution
- Fibre Channel clock distribution
- Gigabit Ethernet clock distribution

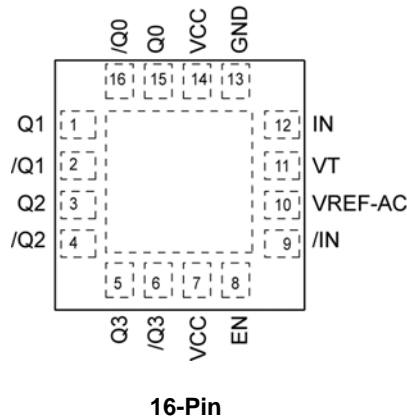
Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89833ALMI	QFN-16	Industrial	833A	Sn-Pb
SY89833ALMITR ⁽²⁾	QFN-16	Industrial	833A	Sn-Pb
SY89833ALMG ⁽³⁾	QFN-16	Industrial	833A with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89833ALMGTR ^(2,3)	QFN-16	Industrial	833A with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

Pin Configuration



Truth Table

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0 ⁽¹⁾	1 ⁽¹⁾

Note:

1. On next negative transition of the input signal (IN).

Pin Description

Pin Number	Pin Name	Pin Function
15, 16 1, 2 3, 4 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVDS Differential Outputs: Normally terminated with 100Ω across the pair (Q, /Q). See "LVDS Outputs" section, Figure 2a. Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
9, 12	/IN, IN	Differential Input: This input pair is the differential signal input to the device. Input accepts AC- or DC-Coupled differential signals as small as 100mV. Each pin of the pair internally terminates to a VT pin through 50Ω. Note that this input will default to an intermediate state if left open. Please refer to the "Input Interface Applications" section for more details.
10	VREF-AC	Reference Voltage: This output biases to $V_{CC}-1.4V$. It is used when AC-Coupling the input (IN, /IN). For AC-Coupled applications, connect VREF-AC to VT pin and bypass with 0.1μF low ESR capacitor to V_{CC} . See "Input Interface Applications" section for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, each VREF-AC pin is only intended to drive its respective VT pin.
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to the VT pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
13	GND	Ground. GND pin and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors and place as close to each VCC pin as possible.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC})	-0.5V to +4.0V
Input Voltage (V_{IN})	-0.5V to $V_{CC} + 0.3V$
LVDS Output Current (I_{OUT})	$\pm 10mA$
Input Current	
Source or Sink Current on (IN, /IN)	$\pm 50mA$
V_T Current	
Source or Sink Current on (V_T)	$\pm 100mA$
V_{REF-AC} Current	
Source or Sink Current on (V_{REF-AC})	$\pm 2mA$
Maximum Operating Junction Temperature	125°C
Lead Temperature (soldering, 20sec.)	260°C
Storage Temperature (T_s)	-65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC})	+3.0V to +3.60V
Ambient Temperature (T_A)	-40°C to +85°C
Junction Thermal Resistance ⁽³⁾	
QFN (θ_{JA})	
Still-Air	75°C/W
QFN (ψ_{JB})	33°C/W

Electrical Characteristics⁽⁴⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC} .		75	100	mA
R_{IN}	Input Resistance (IN-to- V_T)		45	50	55	Ω
$R_{DIFF-IN}$	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN-to-/IN)		1.2		V_{CC}	V
V_{IL}	Input LOW Voltage (IN-to-/IN)		0		$V_{IH}-0.1$	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	See Figure 2c.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage	See Figure 2d.	0.2			V
$ I_{IN} $	Input Current (IN, /IN)	Note 5			45	mA
V_{REF-AC}	Reference Voltage		$V_{CC}-1.525$	$V_{CC}-1.425$	$V_{CC}-1.325$	V

Notes:

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
- The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- Due to the internal termination (see "Input Stage" section) the input current depends on the applied voltages at IN, /IN and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!

LVDS Outputs DC Electrical Characteristics⁽⁶⁾

$V_{CC} = 3.3V \pm 10\%$, $R_L = 100\Omega$ across the output, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing	See Figure 2c.	250	325		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 2d.	500	650		mV
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage		-50		50	mV

LVTTL/CMOS DC Electrical Characteristics⁽⁶⁾

$V_{CC} = 3.3V \pm 10\%$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		-125		30	μA
I_{IL}	Input LOW Current		-300			μA

Notes:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics⁽⁷⁾

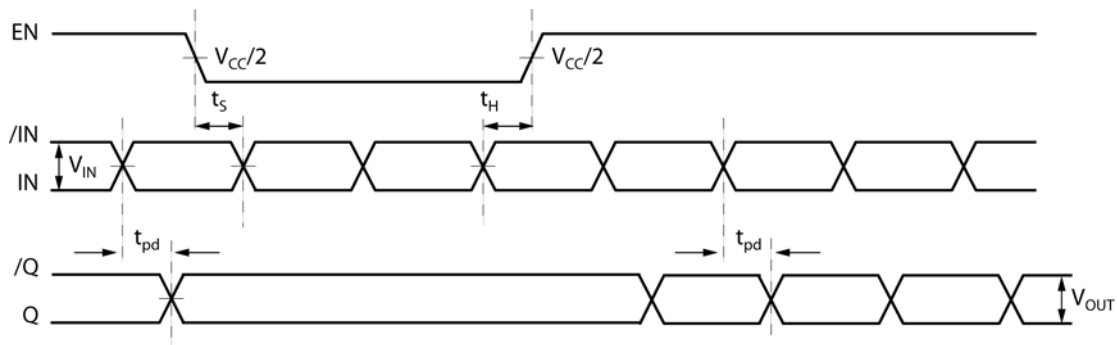
$V_{CC} = 3.3V \pm 10\%$, $R_L = 100\Omega$ across the output, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	$V_{OUT} \geq 200mV$	2.0			GHz
t_{PD}	Propagation Delay		250		470	ps
t_{SKEW}	Within-Device Skew	Note 8		5	20	ps
	Part-to-Part Skew	Note 9			200	ps
t_S	Set-Up Time	Note 10	400			ps
t_H	Hold Time	Note 10	400			ps
t_{JITTER}	Data Random Jitter (RJ) Deterministic Jitter (DJ)	Note 11 Note 12			1 10	μs_{RMS} μs_{PP}
	Clock Cycle-to-Cycle Jitter Total Jitter (TJ)	Note 13 Note 14			1 10	μs_{RMS} μs_{PP}
	Additive Phase Jitter	$f = 622.08MHz$, Note 15 $f = 156.25MHz$, Note 15		0.07		μs_{RMS} μs_{RMS}
t_r, t_f	Output Rise/Fall Times (20% to 80%)	At full output swing.	60	110	190	ps
	Duty Cycle	Differential I/O	47		53	%

Notes:

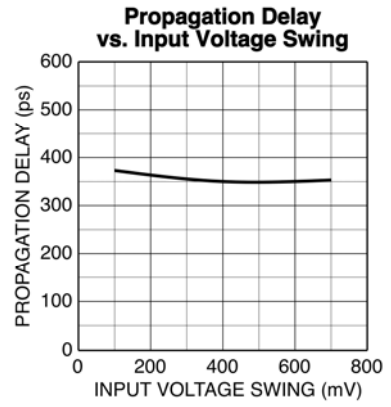
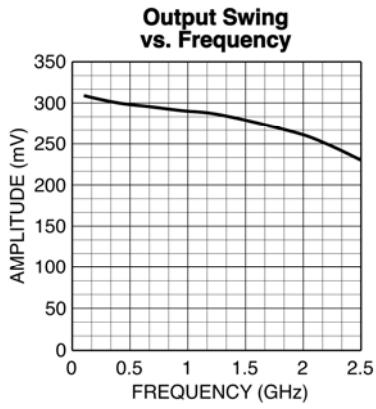
- High-frequency AC parameters are guaranteed by design and characterization.
- Within device skew is measured between two different outputs under identical input transitions.
- Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
- Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.
- Random jitter is measured with a K28.7 pattern, measured at $\leq f_{MAX}$.
- Deterministic jitter is measured at 2.5Gbps with both K28.5 and $2^{23}-1$ PRBS pattern.
- Cycle-to-cycle jitter definition: The variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
- Total jitter definition: with an ideal clock input frequency of $\leq f_{MAX}$ (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
- Integrated over the range of 12kHz to 20MHz.

Timing Diagrams



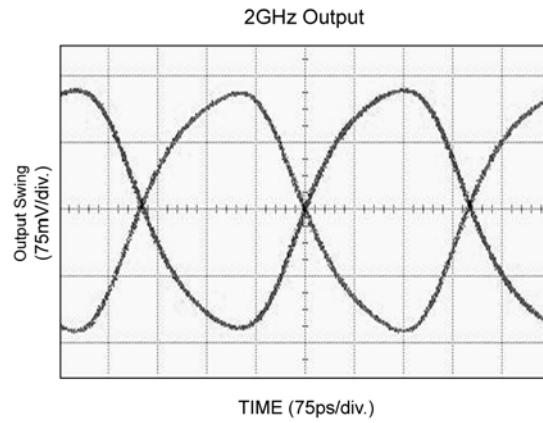
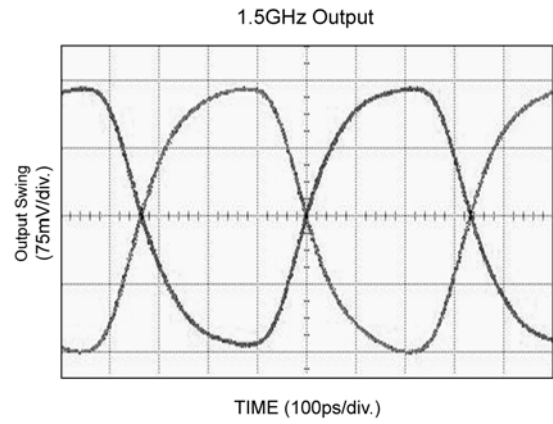
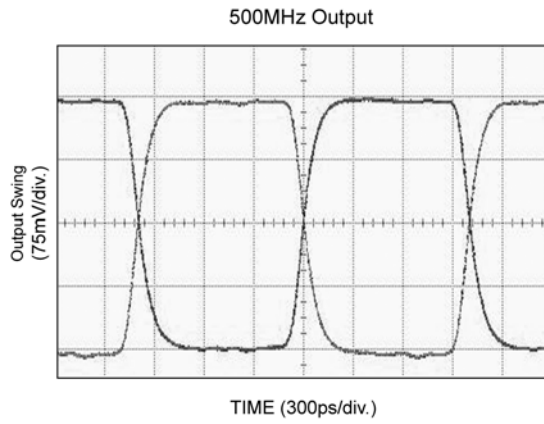
Typical Characteristics

$V_{CC} = 3.3V$, $GND = 0V$, $V_{IN} = 400mV$, $R_L = 100\Omega$ across the outputs, $T_A = 25^\circ C$, unless otherwise stated.



Functional Characteristics

$V_{CC} = 3.3V$, $GND = 0V$, $V_{IN} = 400mV$, $R_L = 100\Omega$ across the outputs, $T_A = 25^\circ C$, unless otherwise stated.



Input Stage

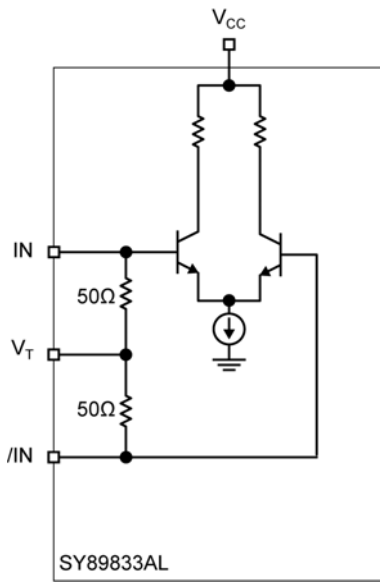


Figure 1. Simplified Differential Input Buffer

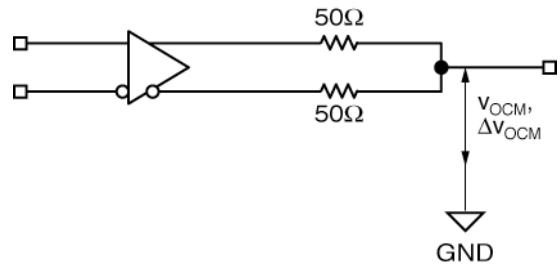


Figure 2b. LVDS Common Mode Measurement

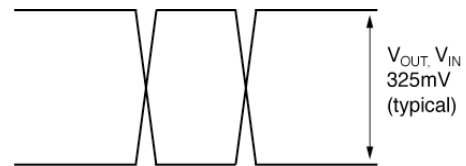


Figure 2c. Single-Ended Swing

LVDS Outputs

LVDS specifies a small swing of 325mV typical, on a nominal 1.20V common mode above ground. The common mode voltage has tight limits to permit large variations in ground noise between an LVDS driver and receiver.

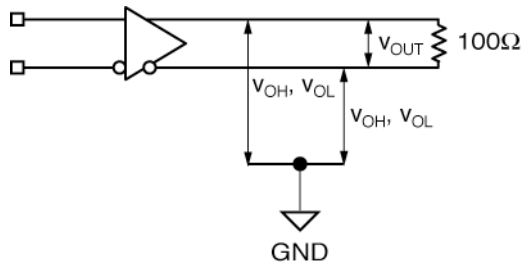


Figure 2a. LVDS Differential Measurement

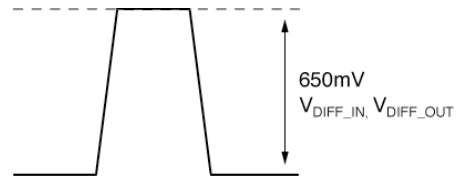


Figure 2d. Differential Swing

Input Interface Applications

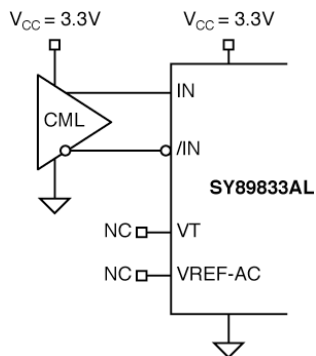


Figure 3a. DC-Coupled CML Input Interface
Option: May connect V_T to V_{CC}

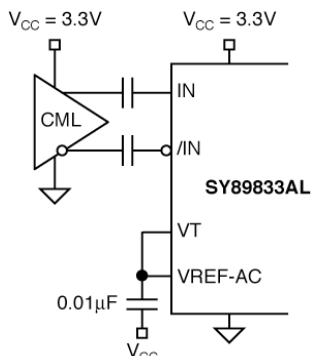


Figure 3b. AC-Coupled CML Input Interface

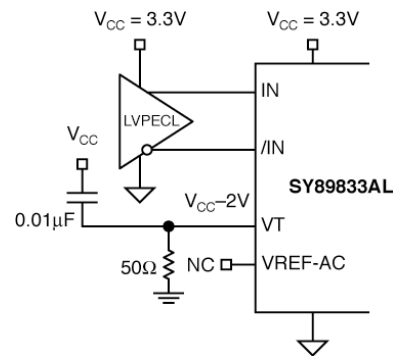


Figure 3c. DC-Coupled LVPECL Input Interface

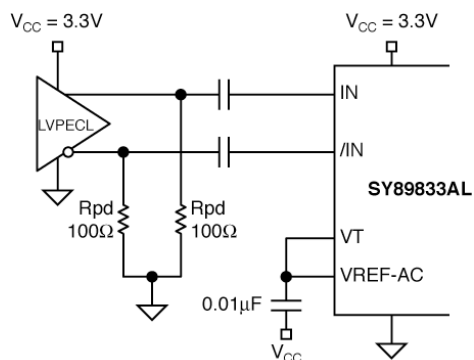


Figure 3d. AC-Coupled LVPECL Input Interface

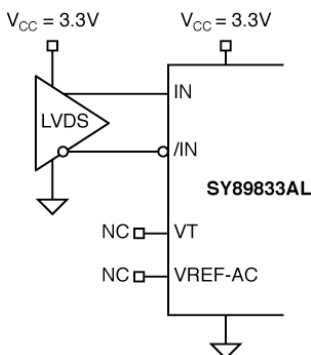
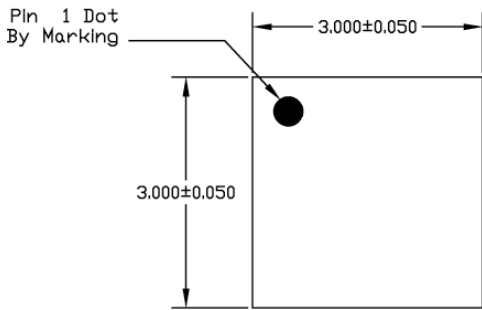


Figure 3e. LVDS Input Interface

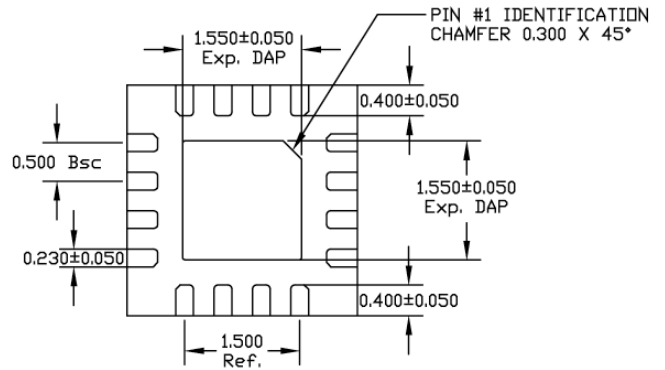
Related Product and Support Documentation

Part Number	Function	Datasheet Link
SY89830U	2.5V/3.3V/5V 2.5GHz 1:4 PECL/ECL Clock Driver with 2:1 Differential Input MUX	http://www.micrel.com/product-info/products/sy89830u.shtml
SY89831U	Ultra-Precision 1:4 LVPECL Fanout Buffer/Translator with Internal Termination	http://www.micrel.com/product-info/products/sy89831u.shtml
SY89832U	2.5V Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination	http://www.micrel.com/product-info/products/sy89832u.shtml
SY89834U	2.5/3.3V Two Input, 1GHz LVTTTL/CMOS-to-LVPECL 1:4 Fanout Buffer/Translator	http://www.micrel.com/product-info/products/sy89834u.shtml
SY89833L	3.3V Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination	http://www.micrel.com/page.do?page=/product-info/products/sy89833l.shtml
HBW Solutions	New Products and Termination App. Note	http://www.micrel.com/product-info/as/solutions.shtml

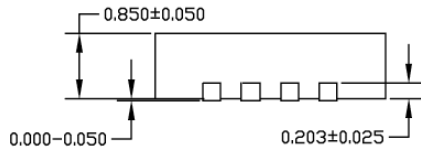
Package Information



TOP VIEW



BOTTOM VIEW

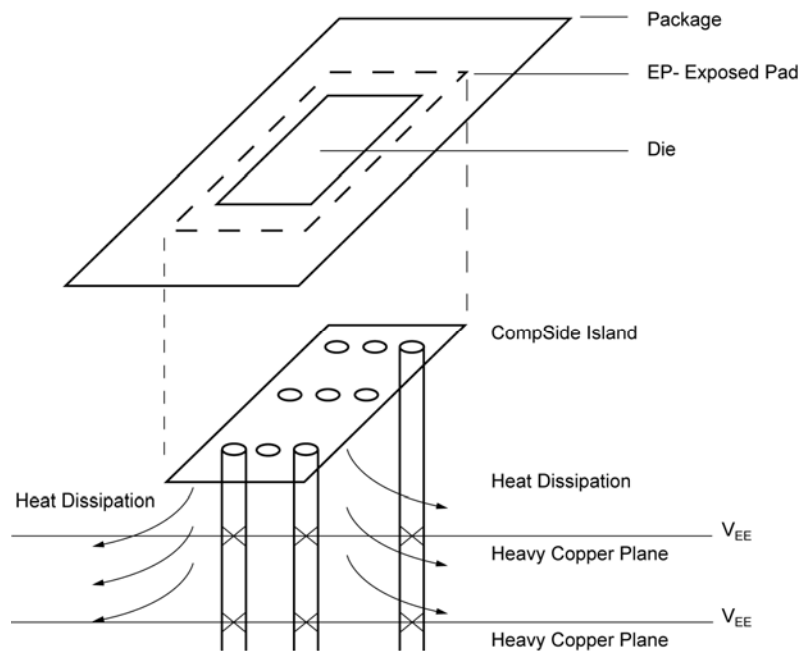


SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

16-Pin QFN



**PCB Thermal Consideration for 16-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)**

Package Notes:

1. Package meets Level 2 moisture sensitivity classification, and are shipped in dry-pack form.
2. Exposed pads must be soldered to a ground for proper thermal management.

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«JONHON» (основан в 1970 г.)

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