

Operational Amplifiers / Comparators

# High Speed with Low Voltage CMOS Operational Amplifiers



**Input-Output Full Swing**  
BU7291G, BU7291SG, BU7255HFV, BU7255SHFV

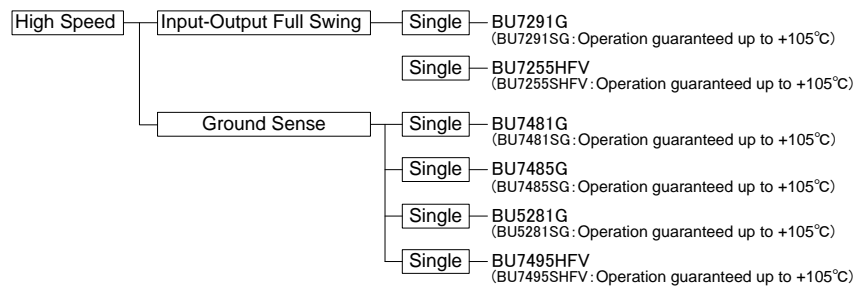
**Ground sense**  
BU7495HFV, BU7495SHFV, BU7481G, BU7481SG  
BU7485G, BU7485SG, BU5281G, BU5281SG

No.10049EAT20

## ●Description

Low Voltage with High Speed CMOS Op-Amp integrates one independent output full swing Op-Amps and phase compensation capacitors on a single chip. Especially, this series is operable with low voltage, low supply current, high speed and low input bias current.

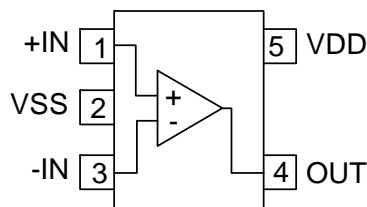
- Input-Output Full Swing  
BU7291 family, BU7255 family
- Ground sense  
BU7495 family, BU7481 family,  
BU7485 family, BU5281 family



## ●Features

- |   |  |
|---|--|
| <ol style="list-style-type: none"> <li>1) Low operating supply voltage<br/>+2.4 [V] ~ +5.5 [V] (single supply): BU7291 family<br/>BU7255 family<br/>+1.8 [V] ~ +5.5 [V] (single supply): BU7495 family<br/>BU7481 family<br/>BU5281 family<br/>+3.0 [V] ~ +5.5 [V] (single supply): BU7485 family</li> <li>2) High large signal voltage gain</li> <li>3) Internal ESD protection<br/>Human body model (HBM) ±4000 [V] (Typ.)</li> <li>4) Low input bias current 1[pA] (Typ.)</li> </ol> | <ol style="list-style-type: none"> <li>5) High slew rate<br/>3.0 [V/μs]: BU7291 family<br/>3.4 [V/μs]: BU7255 family<br/>5.0 [V/μs]: BU7495 family<br/>3.2 [V/μs]: BU7481 family<br/>2.0 [V/μs]: BU5281 family<br/>10.0 [V/μs]: BU7485 family</li> </ol> |
|---|--|

## ●Pin Assignments



### SSOP5

BU7291G BU7291SG  
BU7485G BU7485SG  
BU7481G BU7481SG  
BU5281G BU5281SG

### HVSO5

BU7255HFV BU7255SHFV  
BU7495HFV BU7495SHFV

● Absolute Maximum Ratings (Ta=25[°C])

Parameter	Symbol	Ratings		Unit
		BU7291G, BU7255HFV BU7495HFV, BU7481G BU7485G, BU5281G	BU7291SG, BU7255SHFV BU7495SHFV, BU7481SG BU7485SG, BU5281SG	
Supply Voltage	VDD - VSS	+7		V
Differential Input Voltage <sup>(*)</sup>	Vid	VDD - VSS		V
Input Common-mode Voltage Range	Vicm	(VSS - 0.3) ~ (VDD + 0.3)		V
Operating Temperature	Topr	- 40 ~ +85	- 40 ~ +105	°C
Storage Temperature	Tstg	- 55 ~ +125		°C
Maximum Junction Temperature	Tjmax	+125		°C

Note: Absolute maximum rating item indicates the condition which must not be exceeded.

Application of voltage in excess of absolute maximum rating or use out absolute maximum rated temperature environment may cause deterioration of characteristics.

(\*) The voltage difference between inverting input and non-inverting input is the differential input voltage. Then input terminal voltage is set to more than VSS.

● Electrical characteristics: Input-Output Full Swing

OBU7291 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7291G, BU7291SG				
			Min.	Typ.	Max.		
Input Offset Voltage <sup>(*)2</sup>	Vio	25°C	—	1	9	mV	—
Input Offset Current <sup>(*)2</sup>	Iio	25°C	—	1	—	pA	—
Input Bias Current <sup>(*)2</sup>	Ib	25°C	—	1	—	pA	—
Supply Current <sup>(*)3</sup>	IDD	25°C	—	470	800	µA	RL=∞ All Op-Amps AV=0[dB], VIN=1.5[V]
		Full range	-	—	1100		
High Level Output Voltage	VOH	25°C	VDD-0.1	—	—	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	—	—	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	70	105	—	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	—	3	V	VSS ~ VDD
Common-mode Rejection Ratio	CMRR	25°C	40	60	—	dB	—
Power Supply Rejection Ratio	PSRR	25°C	45	80	—	dB	—
Output Source Current <sup>(*)4</sup>	IOH	25°C	5	8	—	mA	VDD-0.4[V]
Output Sink Current <sup>(*)4</sup>	IOL	25°C	9	16	—	mA	VSS+0.4[V]
Slew Rate	SR	25°C	—	3.0	—	V/µs	CL=25[pF]
Gain Band width	FT	25°C	—	2.8	—	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	—	50	—	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25°C	—	0.03	—	%	VOUT=0.8[Vp-p], f=1[kHz]

(\*)2 Absolute value

(\*)3 Full range BU7291: Ta=-40[°C]~+85[°C] BU7291S: Ta=-40[°C]~+105[°C]

(\*)4 Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

OBU7255 (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7255HFV, BU7255SHFV				
			Min.	Typ.	Max.		
Input Offset Voltage <sup>(*5)</sup>	Vio	25°C	—	1	9	mV	—
Input Offset Current <sup>(*5)</sup>	Iio	25°C	—	1	—	pA	—
Input Bias Current <sup>(*5)</sup>	Ib	25°C	—	1	—	pA	—
Supply Current <sup>(*6)</sup>	IDD	25°C	—	540	900	μA	RL=∞ All Op-Amps AV=0[dB], VIN=1.5[V]
		Full range	—	—	1200		
High Level Output Voltage	VOH	25°C	VDD-0.1	—	—	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	—	—	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	60	105	—	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	-	3	V	VSS ~ VDD
Common-mode Rejection Ratio	CMRR	25°C	40	60	—	dB	—
Power Supply Rejection Ratio	PSRR	25°C	45	80	—	dB	—
Output Source Current <sup>(*7)</sup>	IOH	25°C	2	4	—	mA	VDD - 0.4[V]
Output Sink Current <sup>(*7)</sup>	IOL	25°C	4	8	—	mA	VSS + 0.4[V]
Slew Rate	SR	25°C	—	3.4	—	V/μs	CL=25[pF]
Gain Band width	FT	25°C	—	4	—	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	—	40	—	°	CL=25[pF], AV=40[dB]

(\*5) Absolute value

(\*6) Full range BU7255: Ta=-40[°C]~+85[°C] BU7255S: Ta=-40[°C]~+105[°C]

(\*7) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

OBU7495 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7495HFV, BU7495SHFV				
			Min.	Typ.	Max.		
Input Offset Voltage <sup>(*8)</sup>	Vio	25°C	—	1	6	mV	—
Input Offset Current <sup>(*8)</sup>	Iio	25°C	—	1	—	pA	—
Input Bias Current <sup>(*8)</sup>	Ib	25°C	—	1	—	pA	—
Supply Current <sup>(*9)</sup>	IDD	25°C	—	650	1150	µA	RL=∞ All Op-Amps AV=0[dB], VIN=0.9[V]
		Full range	—	—	1350		
High Level Output Voltage	VOH	25°C	VDD-0.1	—	—	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	-	-	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	60	100	—	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	-	1.8	V	VSS ~ VDD-1.2[V]
Common-mode Rejection Ratio	CMRR	25°C	45	60	—	dB	—
Power Supply Rejection Ratio	PSRR	25°C	60	80	—	dB	—
Output Source Current <sup>(*10)</sup>	IOH	25°C	4	7	—	mA	VDD - 0.4[V]
Output Sink Current <sup>(*10)</sup>	IOL	25°C	9	14	—	mA	VSS + 0.4[V]
Slew Rate	SR	25°C	—	5.0	—	V/µs	CL=25[pF]
Gain Band width	FT	25°C	—	4	—	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	—	50	—	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25°C	—	0.03	—	%	VOUT=0.8[Vp-p], f=1[kHz]

(\*8) Absolute value

(\*9) Full range BU7495: Ta=-40[°C]~+85[°C] BU7495S: Ta=-40[°C]~+105[°C]

(\*10) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC

OBU7481 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7481G, BU7481SG				
			Min.	Typ.	Max.		
Input Offset Voltage <sup>(*11)</sup>	Vio	25°C	—	1	8	mV	—
Input Offset Current <sup>(*11)</sup>	Iio	25°C	—	1	—	pA	—
Input Bias Current <sup>(*11)</sup>	Ib	25°C	—	1	—	pA	—
Supply Current <sup>(*12)</sup>	IDD	25°C	—	420	750	µA	RL=∞ All Op-Amps AV=0[dB], VIN=0.9[V]
		Full range	—	—	900		
High Level Output Voltage	VOH	25°C	VDD-0.1	—	—	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	—	—	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	70	105	—	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	—	1.8	V	VSS ~ VDD-1.2[V]
Common-mode Rejection Ratio	CMRR	25°C	45	60	—	dB	—
Power Supply Rejection Ratio	PSRR	25°C	60	80	—	dB	—
Output Source Current <sup>(*13)</sup>	IOH	25°C	5	8	—	mA	VDD - 0.4[V]
Output Sink Current <sup>(*13)</sup>	IOL	25°C	9	16	—	mA	VSS + 0.4[V]
Slew Rate	SR	25°C	—	3.2	—	V/µs	CL=25[pF]
Gain Band width	FT	25°C	—	2.8	—	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	—	50	—	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25°C	—	0.03	—	%	VOUT=0.8[Vp-p], f=1[kHz]

(\*11) Absolute value

(\*12) Full range BU7481: Ta=-40[°C]~+85[°C] BU7481S: Ta=-40[°C]~+105[°C]

(\*13) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

OBU7485 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU7485G, BU7485SG				
			Min.	Typ.	Max.		
Input Offset Voltage <sup>(*14)</sup>	Vio	25°C	—	1	9.5	mV	—
Input Offset Current <sup>(*14)</sup>	Iio	25°C	—	1	—	pA	—
Input Bias Current <sup>(*14)</sup>	Ib	25°C	—	1	—	pA	—
Supply Current <sup>(*15)</sup>	IDD	25°C	—	1500	2000	µA	RL=∞ All Op-Amps AV=0[dB], VIN=0.8[V]
		Full range	—	—	2400		
High Level Output Voltage	VOH	25°C	VDD-0.1	—	—	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	—	—	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	70	105	—	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	—	1.6	V	VSS ~ VDD-1.4[V]
Common-mode Rejection Ratio	CMRR	25°C	45	60	—	dB	—
Power Supply Rejection Ratio	PSRR	25°C	60	80	—	dB	—
Output Source Current <sup>(*16)</sup>	IOH	25°C	4	8	—	mA	VDD-0.4[V]
Output Sink Current <sup>(*16)</sup>	IOL	25°C	7	12	—	mA	VSS + 0.4[V]
Slew Rate	SR	25°C	—	10	—	V/µs	CL=25[pF]
Gain Band width	FT	25°C	—	10	—	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25°C	—	50	—	°	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25°C	—	0.03	—	%	VOUT=0.7[Vp-p], f=1[kHz]

(\*14) Absolute value

(\*15) Full range BU7485: Ta=-40[°C]~+85[°C] BU7485S: Ta=-40[°C]~+105[°C]

(\*16) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

OBU5281 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Limits			Unit	Condition
			BU5281G, BU5281SG				
			Min.	Typ.	Max.		
Input Offset Voltage <sup>(*17)</sup>	Vio	25°C	—	0.1	2.5	mV	—
Input Offset Voltage drift <sup>(*17)</sup>	$\Delta V_{io}/\Delta T$	-	—	0.8	—	$\mu V/^{\circ}C$	—
Input Offset Current <sup>(*17)</sup>	Iio	25°C	—	1	—	pA	—
Input Bias Current <sup>(*17)</sup>	Ib	25°C	—	1	—	pA	—
Supply Current <sup>(*18)</sup>	IDD	25°C	—	750	1000	$\mu A$	RL=∞ All Op-Amps AV=0[dB], VIN=0.9[V]
		Full range	—	—	1200		
High Level Output Voltage	VOH	25°C	VDD-0.1	—	—	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25°C	—	—	VSS+0.1	V	RL=10[kΩ]
Large Signal Voltage Gain	AV	25°C	70	110	—	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25°C	0	—	1.8	V	VSS ~ VDD - 1.2[V]
Common-mode Rejection Ratio	CMRR	25°C	45	60	—	dB	—
Power Supply Rejection Ratio	PSRR	25°C	60	80	—	dB	—
Output Source Current <sup>(*19)</sup>	IOH	25°C	5	8	—	mA	VDD-0.4[V]
Output Sink Current <sup>(*19)</sup>	IOL	25°C	10	16	—	mA	VSS+0.4[V]
Slew Rate	SR	25°C	—	2.0	—	V/ $\mu s$	CL=25[pF]
Gain Band width	FT	25°C	—	3	—	MHz	CL=25[pF], AV=40[dB]
Phase Margin	$\theta$	25°C	—	40	—	°	CL=25[pF], AV=40[dB]
Input Referred Noise Voltage	Vin	25°C	—	18	—	nV/(Hz) <sup>1/2</sup>	AV=40[dB], f=1[kHz]
			—	3.2	—	$\mu V_{rms}$	AV=40[dB], DINAUDIO
Total Harmonic Distortion	THD	25°C	—	0.003	—	%	VOUT=0.4[Vp-p], f=1[kHz]

(\*17) Absolute value

(\*18) Full range BU5281: Ta=-40[°C]~+85[°C] BU5281S: Ta=-40[°C]~+105[°C]

(\*19) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

● Reference Data (BU7291 family)

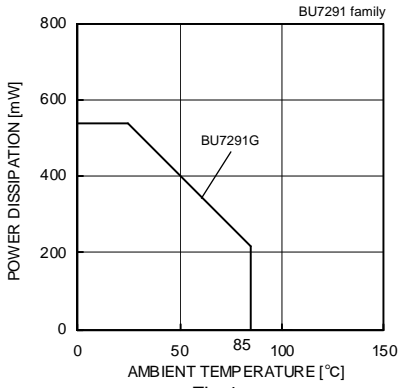


Fig.1

Derating curve

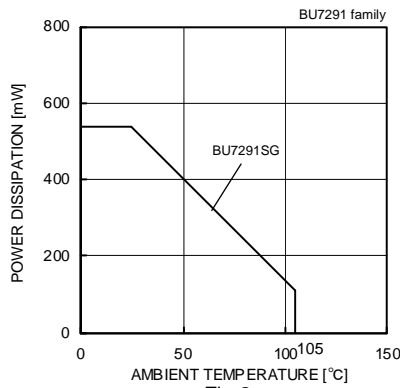


Fig.2

Derating curve

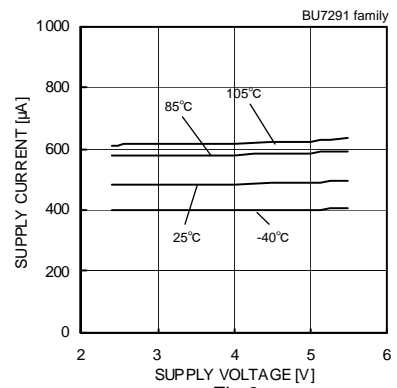


Fig.3

Supply Current - Supply Voltage

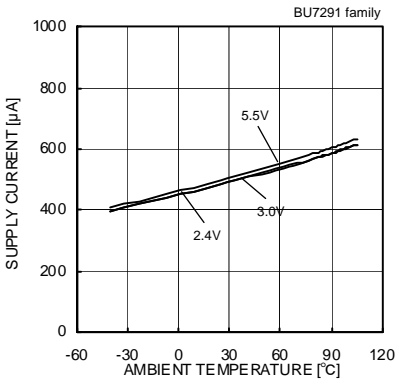


Fig.4

Supply Current - Ambient Temperature

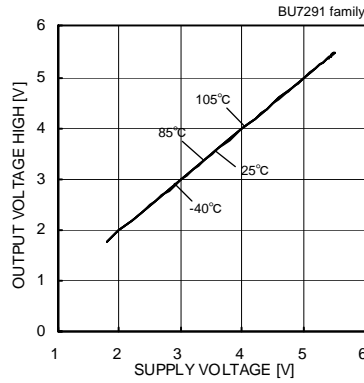


Fig.5

Output Voltage High - Supply Voltage (RL=10[kΩ])

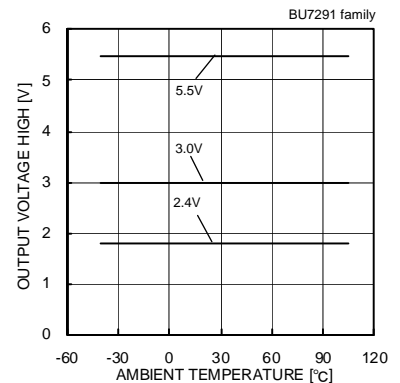


Fig.6

Output Voltage High - Ambient Temperature (RL=10[kΩ])

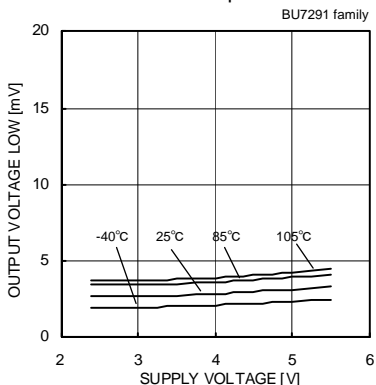


Fig.7

Output Voltage Low - Supply Voltage (RL=10[kΩ])

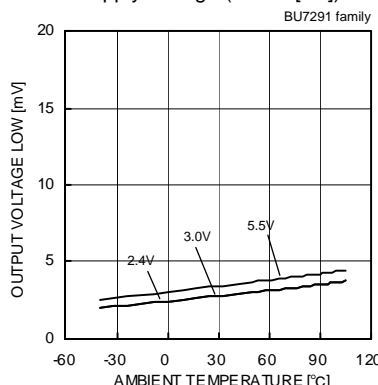


Fig.8

Output Voltage Low - Ambient Temperature (RL=10[kΩ])

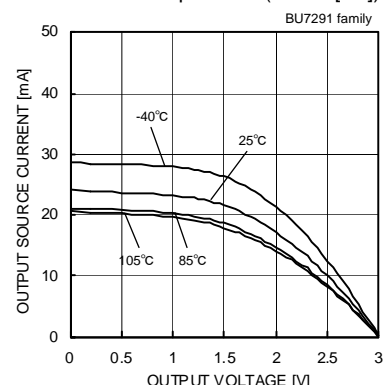


Fig.9

Output Source Current - Output Voltage (VDD=3[V])

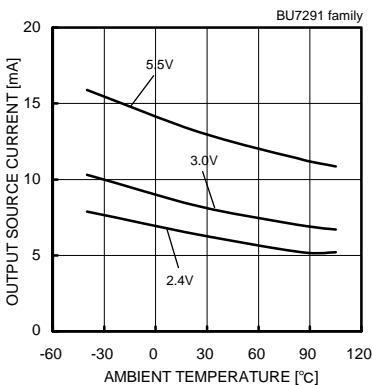


Fig.10

Output Source Current - Ambient Temperature (VOUT=VDD-0.4[V])

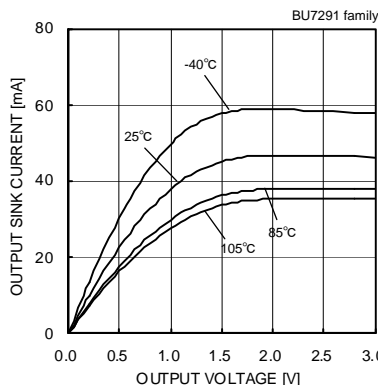


Fig.11

Output Sink Current - Output Voltage (VDD=3[V])

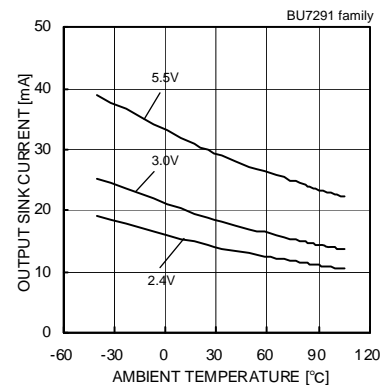


Fig.12

Output Sink Current - Ambient Temperature (VOUT=VSS+0.4[V])

(\*)The above data is ability value of sample, it is not guaranteed. BU7291G: -40[°C] ~ +85[°C] BU7291SG: -40[°C] ~ +105[°C]



● Reference Data (BU7291 family)

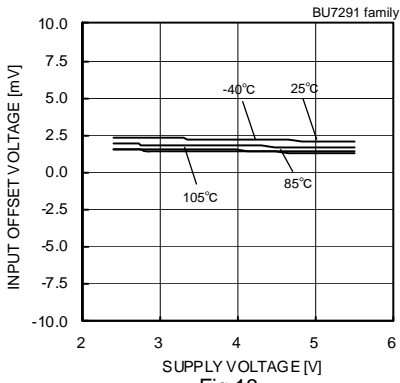


Fig. 13  
 Input Offset Voltage – Supply Voltage  
 (Vicm=VDD, VOUT=1.5[V])

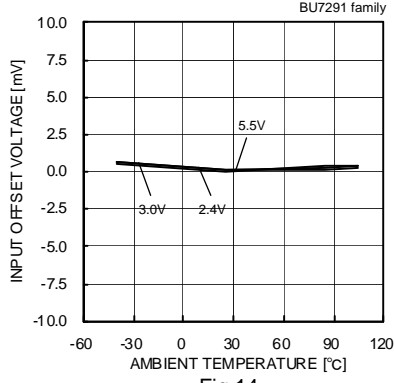


Fig. 14  
 Input Offset Voltage – Ambient Temperature  
 (Vicm=VDD, VOUT=1.5[V])

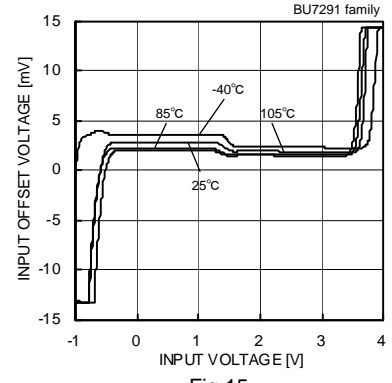


Fig. 15  
 Input Offset Voltage – Input Voltage  
 (VDD=3[V])

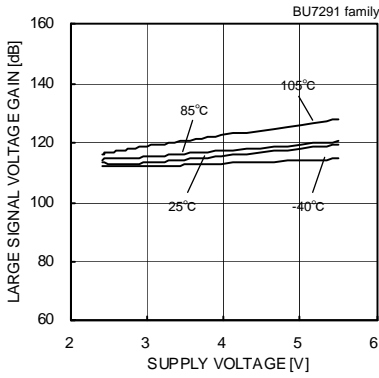


Fig. 16  
 Large Signal Voltage Gain  
 – Supply Voltage

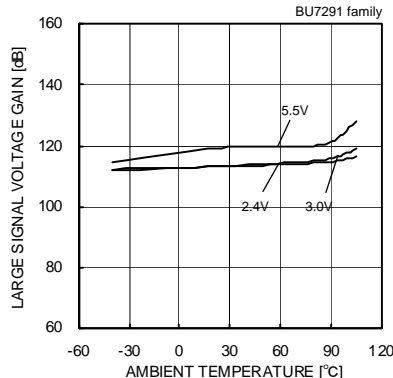


Fig. 17  
 Large Signal Voltage Gain  
 – Ambient Temperature

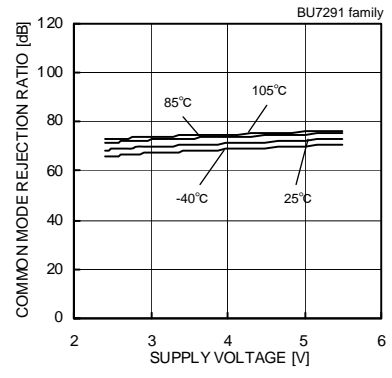


Fig. 18  
 Common Mode Rejection Ratio  
 – Supply Voltage (VDD=3[V])

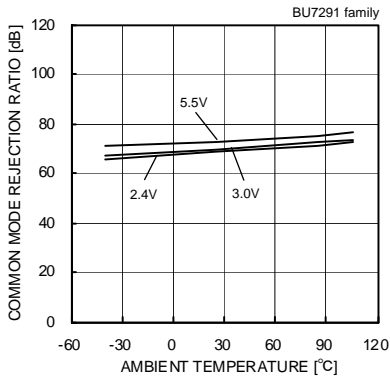


Fig. 19  
 Common Mode Rejection Ratio  
 – Ambient Temperature

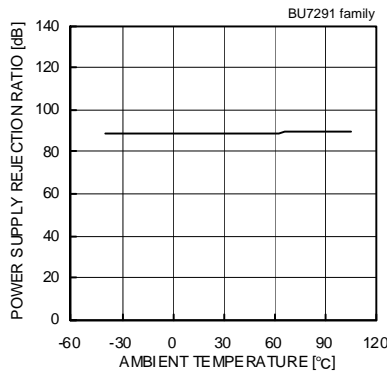


Fig. 20  
 Power Supply Rejection Ratio  
 – Ambient Temperature

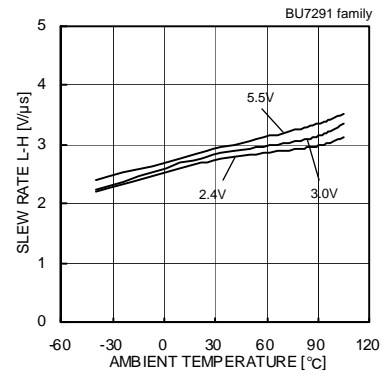


Fig. 21  
 Slew Rate L-H  
 – Ambient Temperature

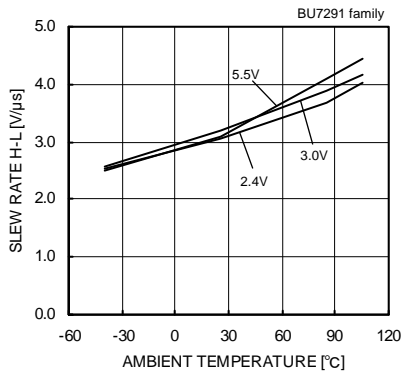


Fig. 22  
 Slew Rate H-L – Ambient Temperature

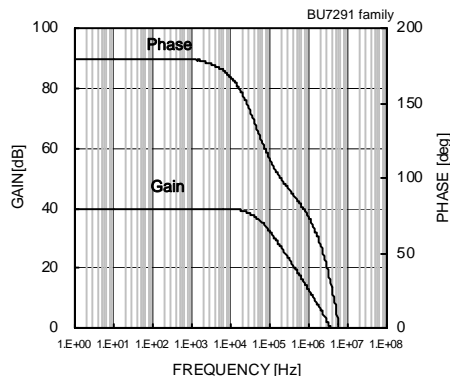


Fig. 23  
 Voltage Gain – Frequency

(\*)The above data is ability value of sample, it is not guaranteed. BU7291G: -40[°C] ~ +85[°C] BU7291SG: -40[°C] ~ +105[°C]

● Reference Data (BU7255 family)

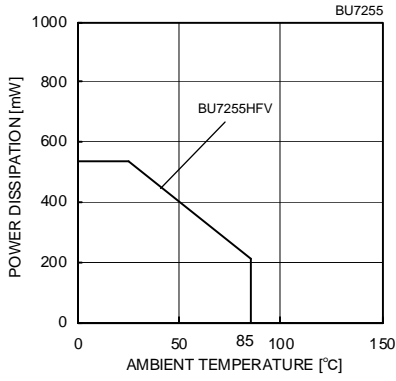


Fig.24  
Derating curve



Fig.25  
Derating curve

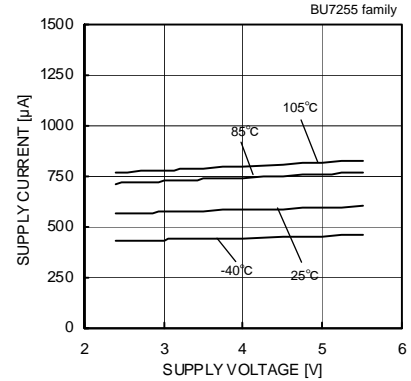


Fig.26  
Supply Current - Supply Voltage

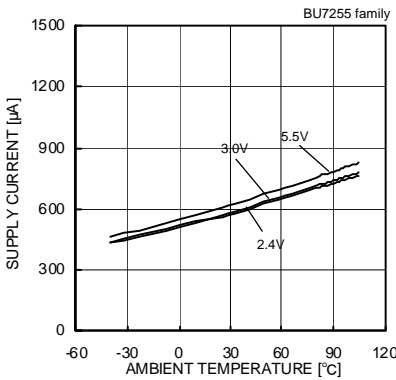


Fig.27  
Supply Current  
- Ambient Temperature



Fig.28  
Output Voltage High  
- Supply Voltage (RL=10[kΩ])

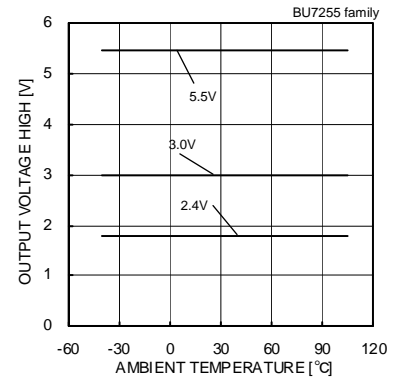


Fig.29  
Output Voltage High  
- Ambient Temperature (RL=10[kΩ])

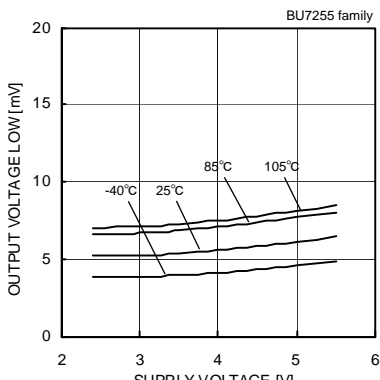


Fig.30  
Output Voltage Low  
- Supply Voltage (RL=10[kΩ])

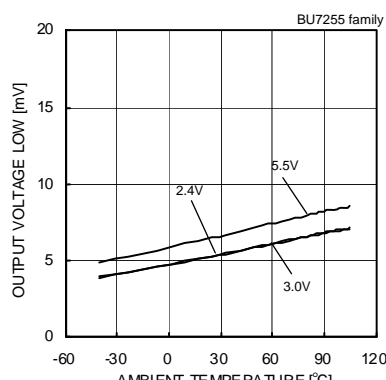


Fig.31  
Output Voltage Low  
- Ambient Temperature (RL=10[kΩ])

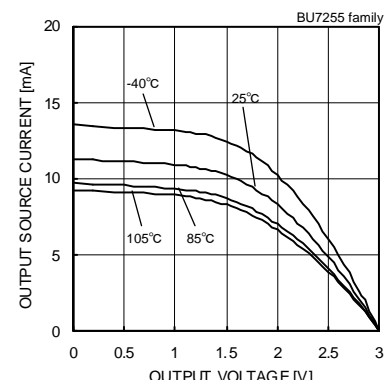


Fig.32  
Output Source Current  
- Output Voltage (VDD=3[V])

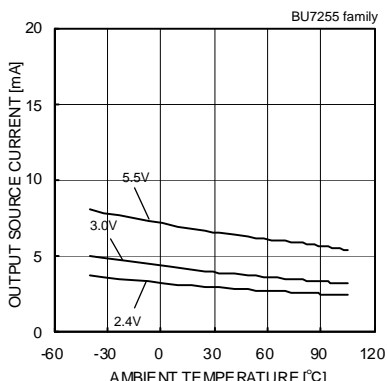


Fig.33  
Output Source Current - Ambient Temperature  
(VOUT=VDD-0.4[V])

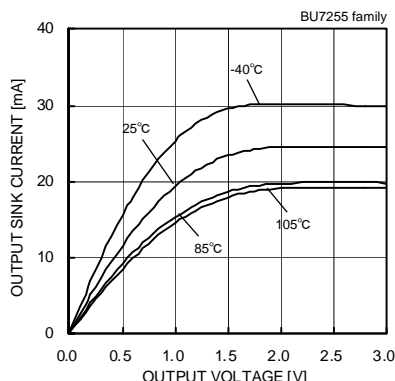


Fig.34  
Output Sink Current - Output Voltage  
(VDD=3[V])

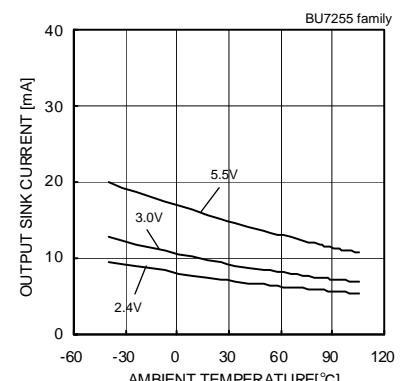


Fig.35  
Output Sink Current - Ambient Temperature  
(VOUT=VSS+0.4[V])

(\*)The above data is ability value of sample, it is not guaranteed. BU7255HFV: -40[°C] ~ +85[°C] BU7255SHFV: -40[°C] ~ +105[°C]

● Reference Data (BU7255 family)

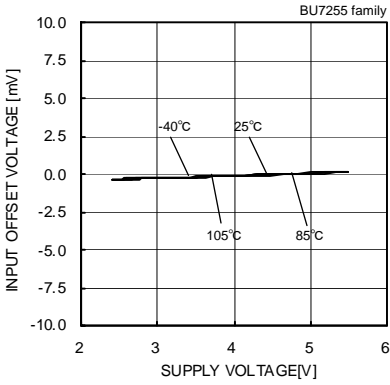


Fig.36  
 Input Offset Voltage – Supply Voltage  
 (Vicm=VDD, VOUT=1.5[V])

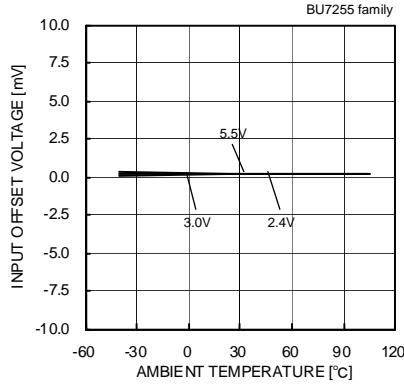


Fig.37  
 Input Offset Voltage – Ambient Temperature  
 (Vicm=VDD, VOUT=1.5[V])

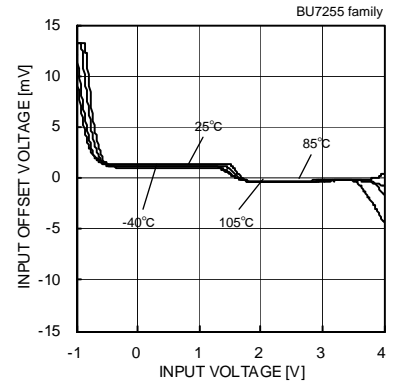


Fig.38  
 Input Offset Voltage – Input Voltage  
 (VDD=3[V])

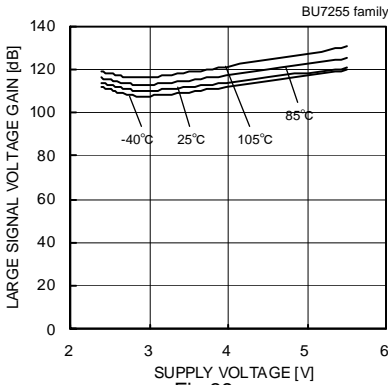


Fig.39  
 Large Signal Voltage Gain  
 – Supply Voltage

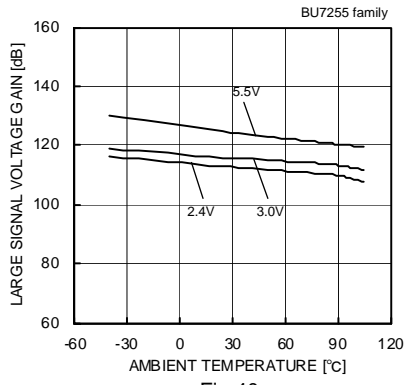


Fig.40  
 Large Signal Voltage Gain  
 – Ambient Temperature

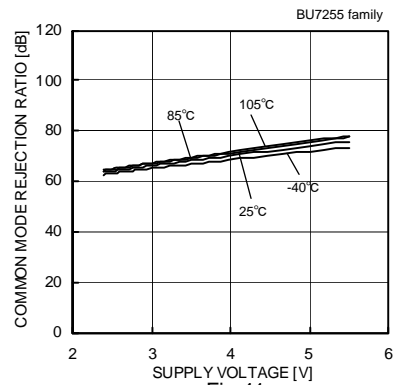


Fig.41  
 Common Mode Rejection Ratio  
 – Supply Voltage (VDD=3[V])

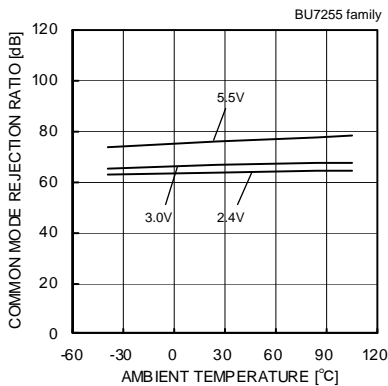


Fig.42  
 Common Mode Rejection Ratio  
 – Ambient Temperature

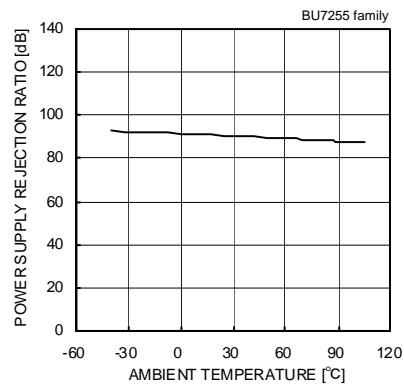


Fig.43  
 Power Supply Rejection Ratio  
 – Ambient Temperature

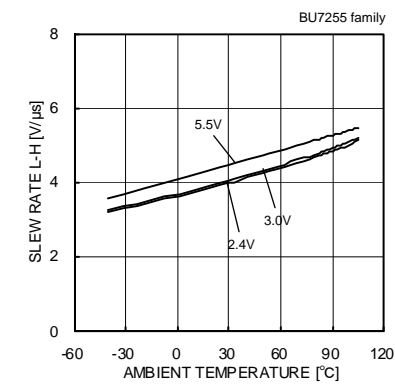


Fig.44  
 Slew Rate L-H  
 – Ambient Temperature

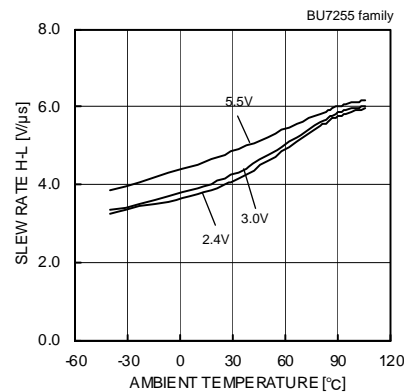


Fig.45  
 Slew Rate H-L – Ambient Temperature

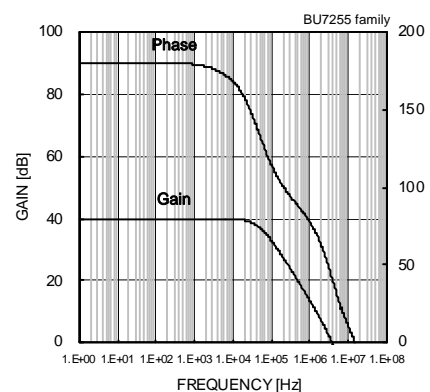


Fig.46  
 Voltage Gain – Frequency

(\*)The above data is ability value of sample, it is not guaranteed. BU7255HFV: -40[°C] ~ +85[°C] BU7255SHFV: -40[°C] ~ +105[°C]

● Reference Data (BU7495 family)

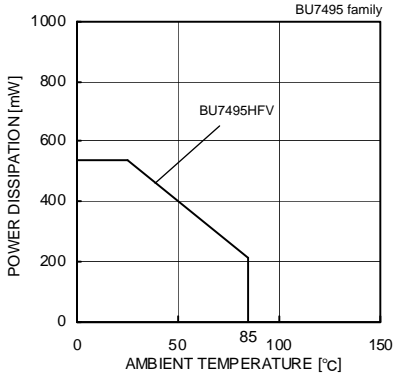


Fig.47

Derating curve

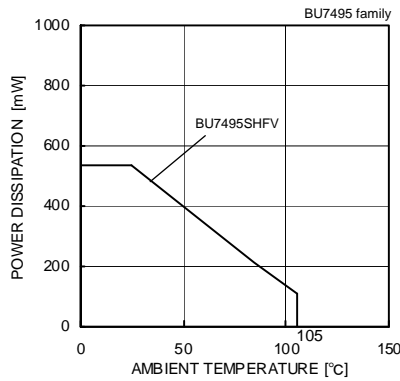


Fig.48

Derating curve

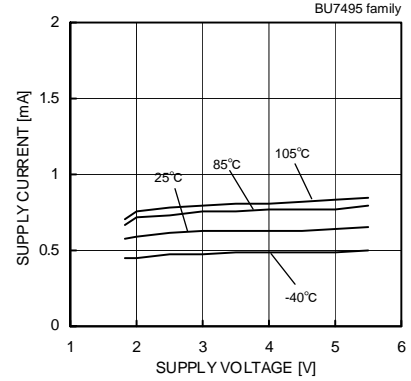


Fig.49

Supply Current - Supply Voltage

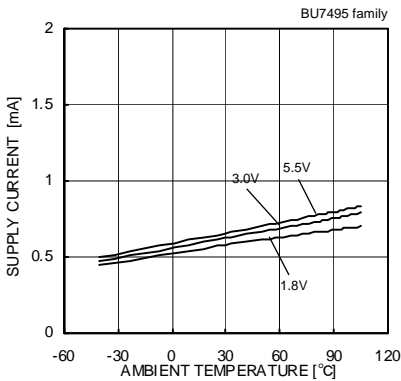


Fig.50

Supply Current - Ambient Temperature



Fig.51

Output Voltage High - Supply Voltage (RL=10[kΩ])



Fig.52

Output Voltage High - Ambient Temperature (RL=10[kΩ])

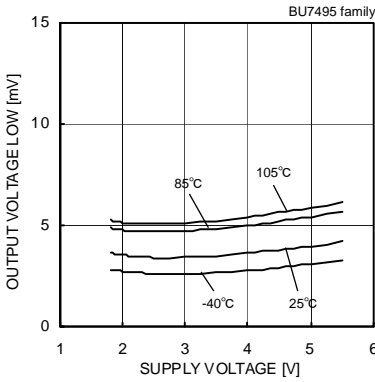


Fig.53

Output Voltage Low - Supply Voltage (RL=10[kΩ])

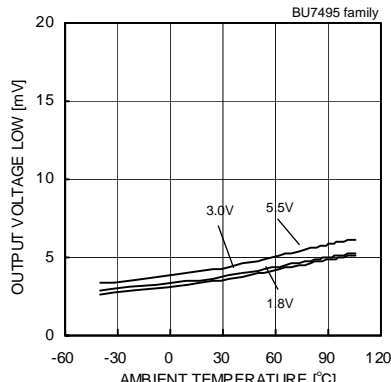


Fig.54

Output Voltage Low - Ambient Temperature (RL=10[kΩ])

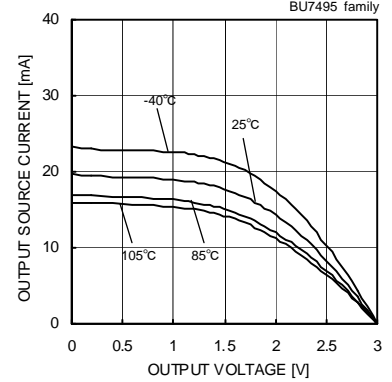


Fig.55

Output Source Current - Output Voltage (VDD=3[V])

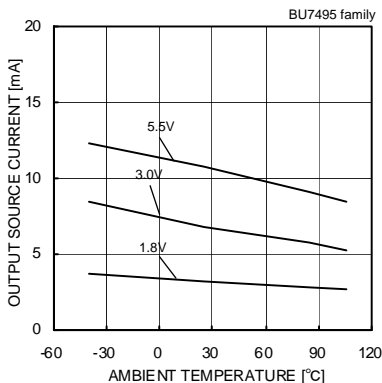


Fig.56

Output Source Current - Ambient Temperature (VOUT=VDD-0.4[V])

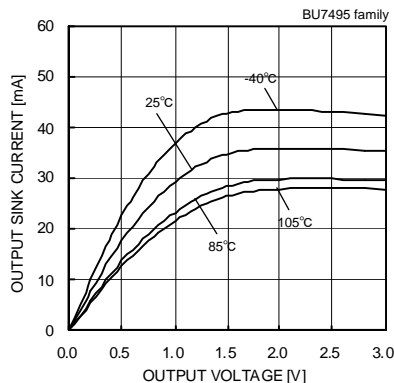


Fig.57

Output Sink Current - Output Voltage (VDD=3[V])

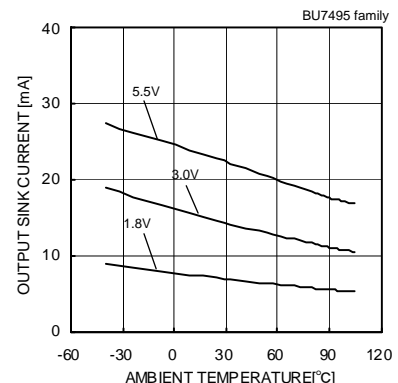
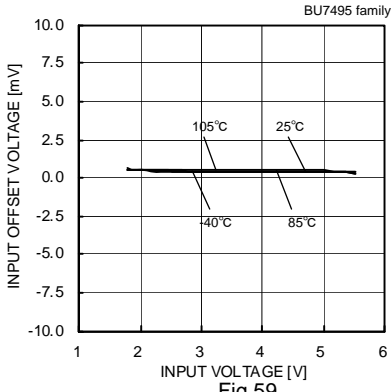


Fig.58

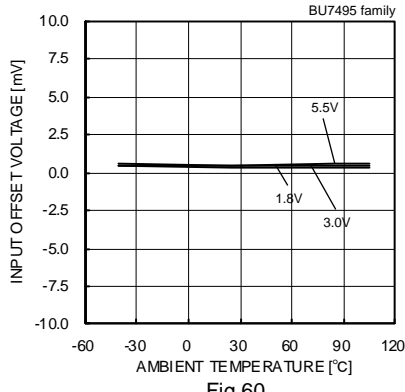
Output Sink Current - Ambient Temperature (VOUT=VSS+0.4[V])

(\*The above data is ability value of sample, it is not guaranteed. BU7495HFV: -40[°C] ~ +85[°C] BU7495SHFV: -40[°C] ~ +105[°C]

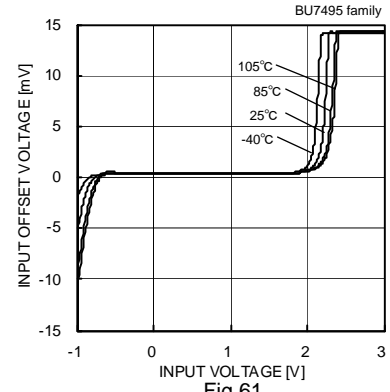
● Reference Data (BU7495 family)



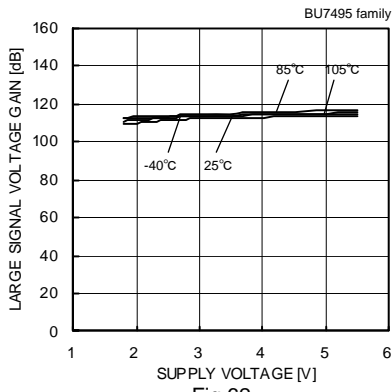
Input Offset Voltage – Supply Voltage  
 (Vicm=VDD-1.2[V], VOUT=1.5[V])



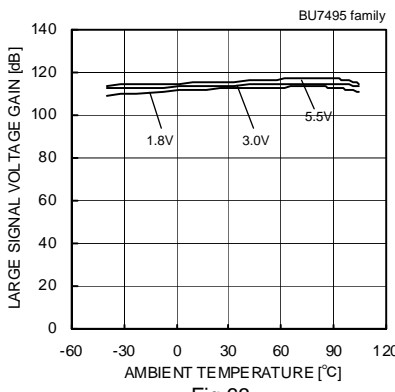
Input Offset Voltage – Ambient Temperature  
 (Vicm=VDD, VOUT=1.5[V])



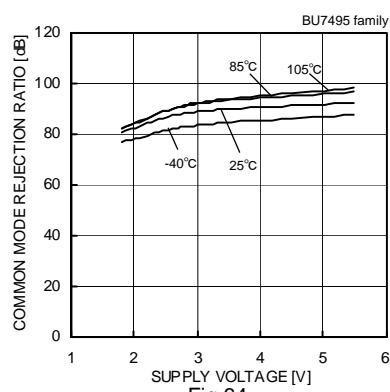
Input Offset Voltage – Input Voltage  
 (VDD=3[V])



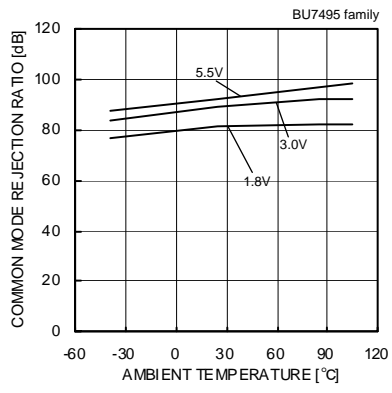
Large Signal Voltage Gain  
 – Supply Voltage



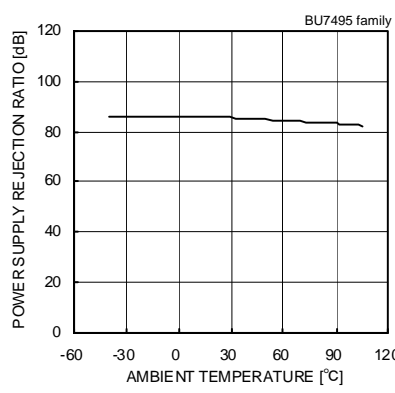
Large Signal Voltage Gain  
 – Ambient Temperature



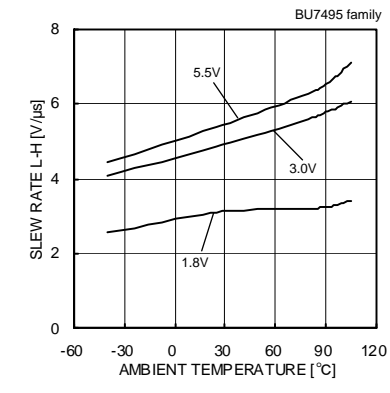
Common Mode Rejection Ratio  
 – Supply Voltage (VDD=3[V])



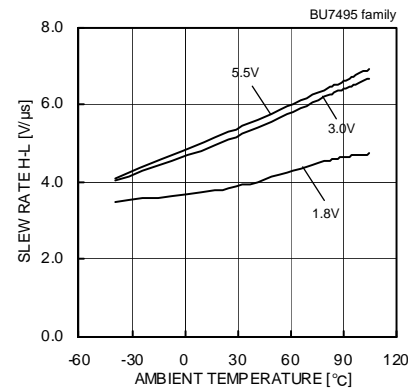
Common Mode Rejection Ratio  
 – Ambient Temperature



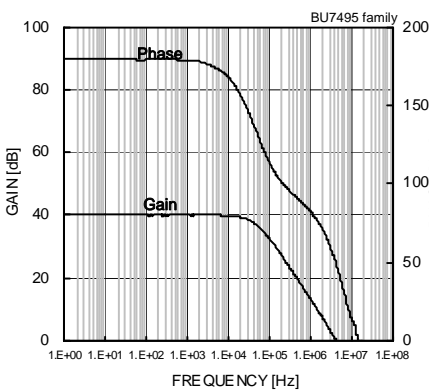
Power Supply Rejection Ratio  
 – Ambient Temperature



Slew Rate L-H  
 – Ambient Temperature



Slew Rate H-L – Ambient Temperature



Voltage Gain – Frequency

(\*)The above data is ability value of sample, it is not guaranteed. BU7495HFV: -40[°C] ~ +85[°C] BU7495SHFV: -40[°C] ~ +105[°C]

● Reference Data (BU7481 family)

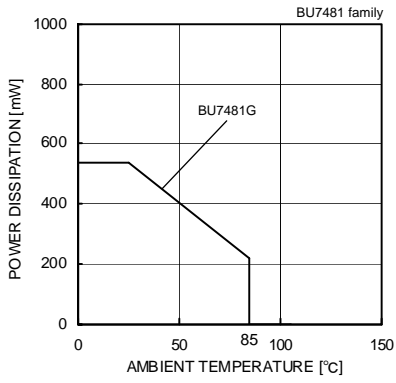


Fig.70  
Derating curve

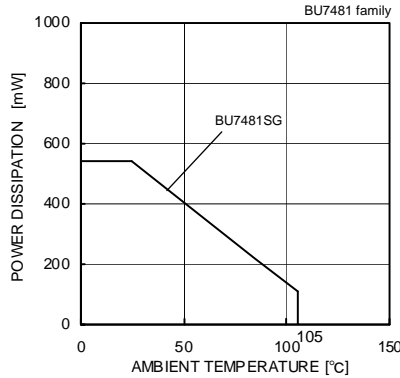


Fig.71  
Derating curve

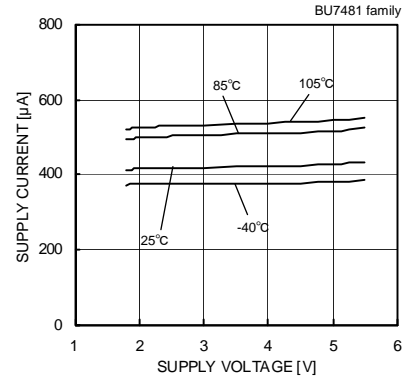


Fig.72  
Supply Current – Supply Voltage

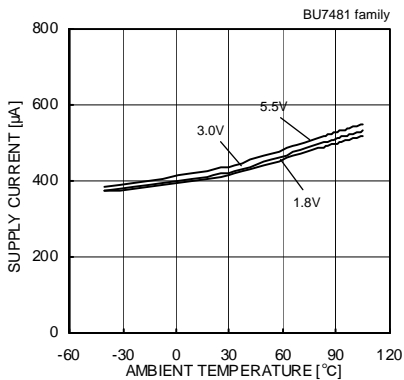


Fig.73  
Supply Current  
– Ambient Temperature

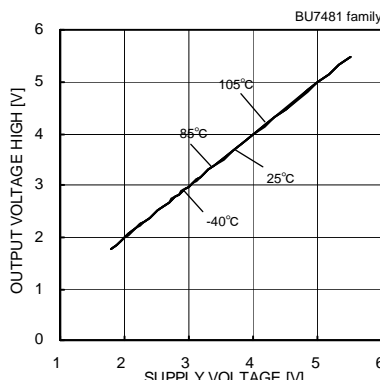


Fig.74  
Output Voltage High  
– Supply Voltage (RL=10[kΩ])

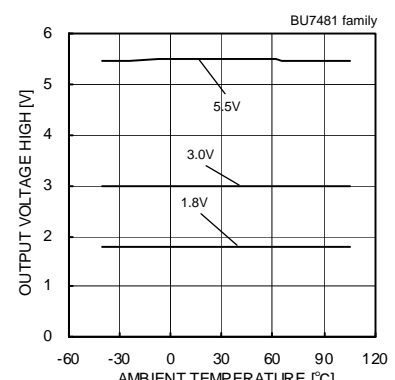


Fig.75  
Output Voltage High  
– Ambient Temperature (RL=10[kΩ])

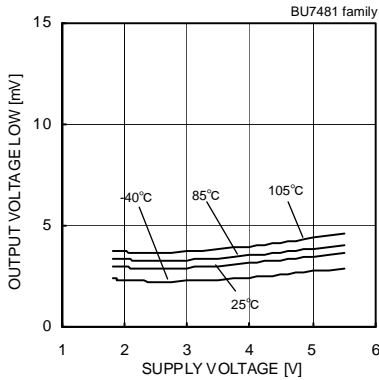


Fig.76  
Output Voltage Low  
– Supply Voltage (RL=10[kΩ])

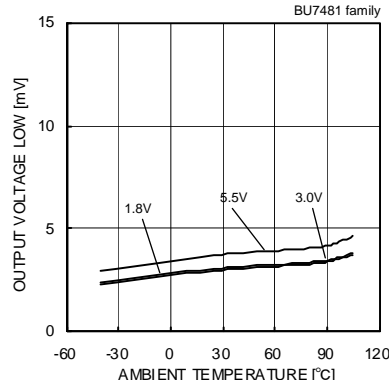


Fig.77  
Output Voltage Low – Ambient  
Temperature (RL=10[kΩ])

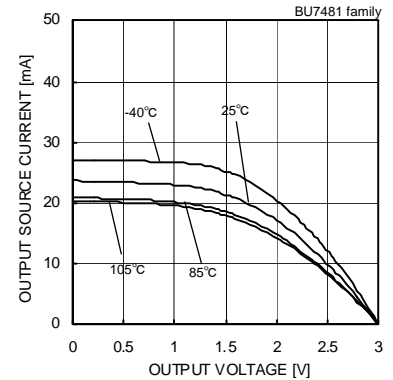


Fig.78  
Output Source Current – Output  
Voltage (VDD=3[V])

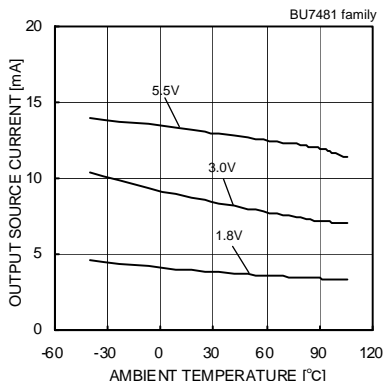


Fig.79  
Output Source Current – Ambient Temperature  
(VOUT=VDD-0.4[V])

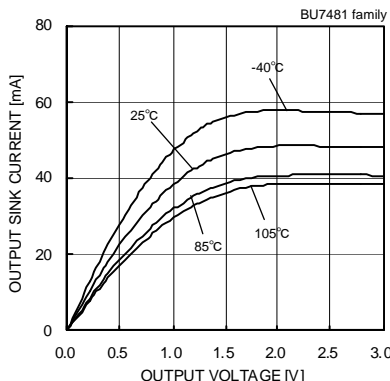


Fig.80  
Output Sink Current – Output Voltage  
(VDD=3[V])

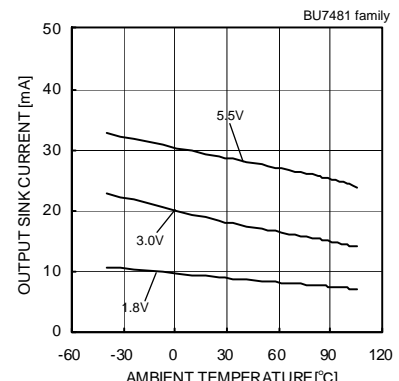


Fig.81  
Output Sink Current – Ambient Temperature  
(VOUT=VSS+0.4[V])

(\*The above data is ability value of sample, it is not guaranteed. BU7481G: -40[°C] ~ +85[°C] BU7481SG: -40[°C] ~ +105[°C])

●Reference Data (BU7481 family)

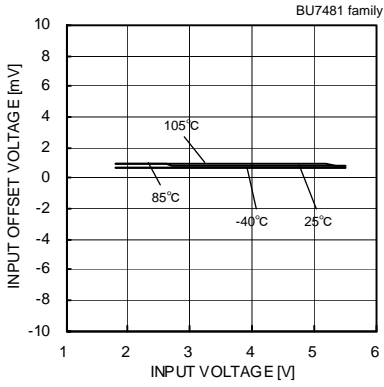


Fig.82  
 Input Offset Voltage – Supply Voltage  
 (Vicm=VDD-1.2[V], VOUT=1.5[V])

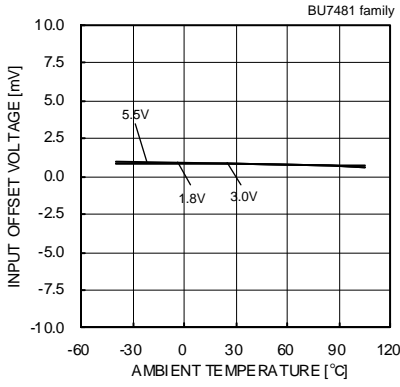


Fig.83  
 Input Offset Voltage – Ambient Temperature  
 (Vicm=VDD-1.2[V], VOUT=1.5[V])

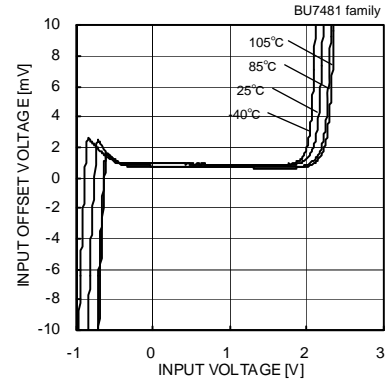


Fig.84  
 Input Offset Voltage – Input Voltage  
 (VDD=3[V])



Fig.85  
 Large Signal Voltage Gain  
 – Supply Voltage

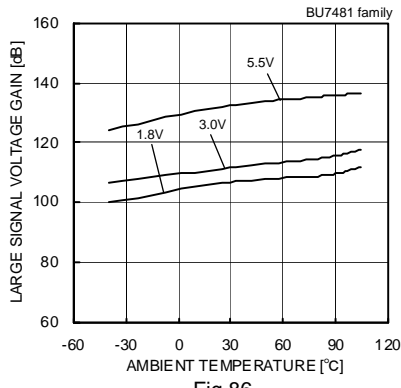


Fig.86  
 Large Signal Voltage Gain  
 – Ambient Temperature

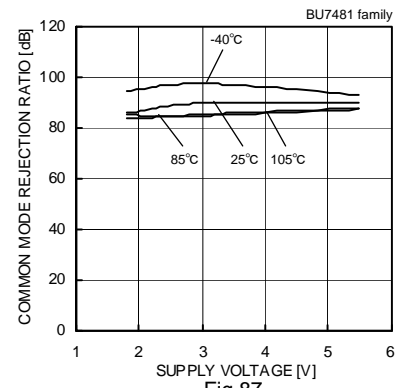


Fig.87  
 Common Mode Rejection Ratio  
 – Supply Voltage (VDD=3[V])



Fig.88  
 Common Mode Rejection Ratio  
 – Ambient Temperature

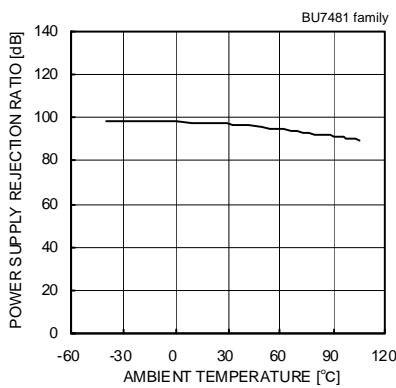


Fig.89  
 Power Supply Rejection Ratio  
 – Ambient Temperature

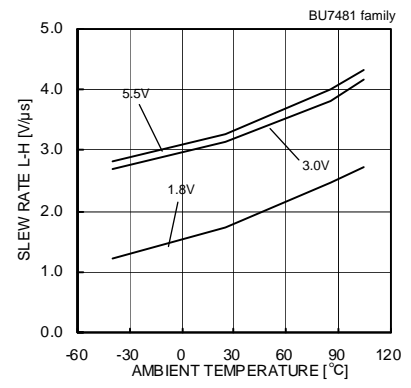


Fig.90  
 Slew Rate L-H  
 – Ambient Temperature

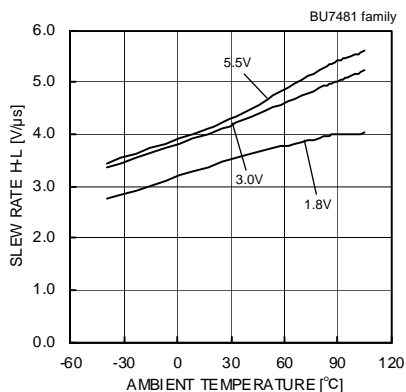


Fig.91  
 Slew Rate H-L – Ambient Temperature

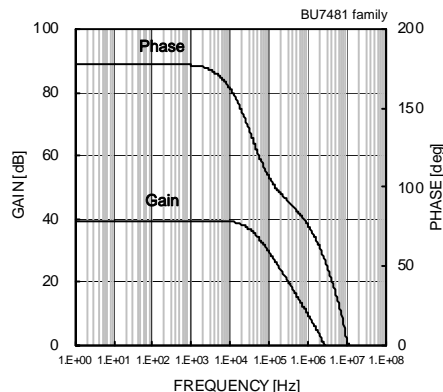


Fig.92  
 Voltage Gain – Frequency

(\*)The above data is ability value of sample, it is not guaranteed. BU7481G: -40[°C] ~ +85[°C] BU7481SG: -40[°C] ~ +105[°C]

● Reference Data (BU7485 family)



Fig.93  
Derating curve



Fig.94  
Derating curve

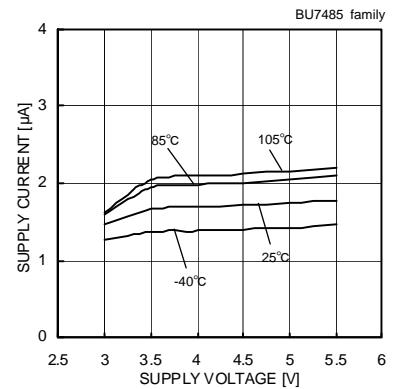


Fig.95  
Supply Current - Supply Voltage

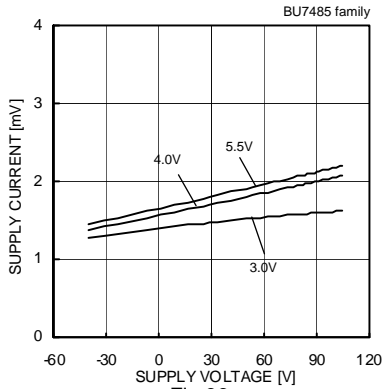


Fig.96  
Supply Current  
- Ambient Temperature



Fig.97  
Output Voltage High  
- Supply Voltage (RL=10[kΩ])

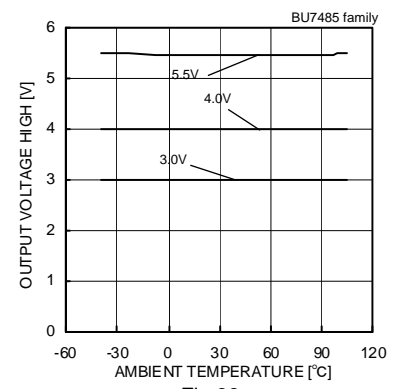


Fig.98  
Output Voltage High  
- Ambient Temperature (RL=10[kΩ])

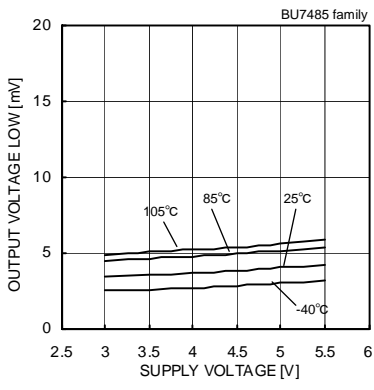


Fig.99  
Output Voltage Low  
- Supply Voltage (RL=10[kΩ])

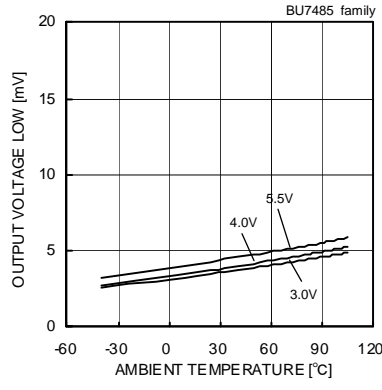


Fig.100  
Output Voltage Low  
- Ambient Temperature (RL=10[kΩ])

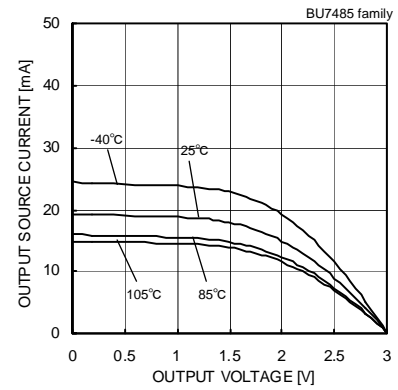


Fig.101  
Output Source Current  
- Output Voltage (VDD=3[V])

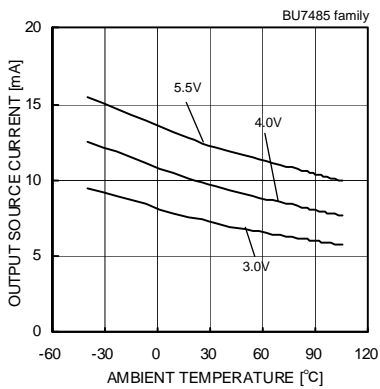


Fig.102  
Output Source Current - Ambient Temperature  
(VOUT=VDD-0.4[V])

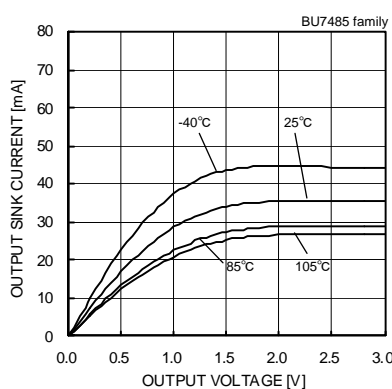


Fig.103  
Output Sink Current - Output Voltage  
(VDD=3[V])

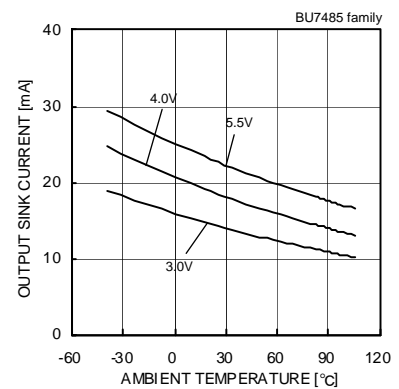


Fig.104  
Output Sink Current - Ambient Temperature  
(VOUT=VSS+0.4[V])

(\*)The above data is ability value of sample, it is not guaranteed. BU7485G: -40[°C] ~ +85[°C] BU7485SG: -40[°C] ~ +105[°C]



● Reference Data (BU7485 family)

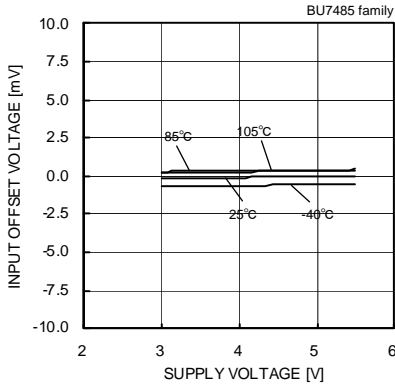


Fig.105  
 Input Offset Voltage – Supply Voltage  
 (Vicm=VDD-1.4[V], VOUT=1.5[V])

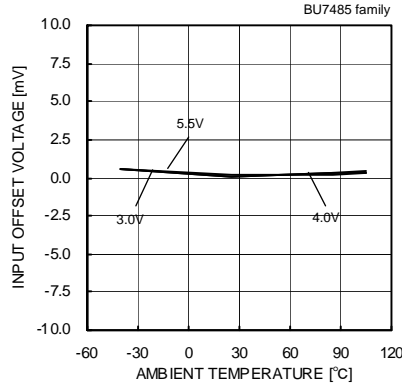


Fig.106  
 Input Offset Voltage – Ambient Temperature  
 (Vicm=VDD-1.4[V], VOUT=1.5[V])

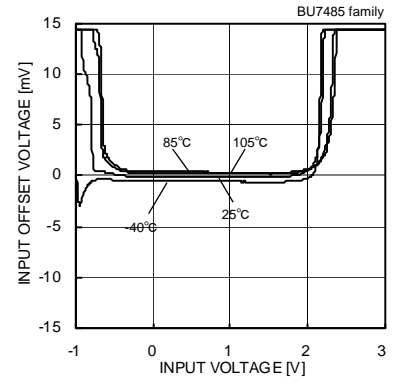


Fig.107  
 Input Offset Voltage – Input Voltage  
 (VDD=3[V])

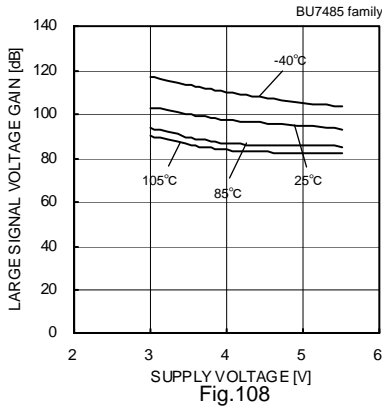


Fig.108  
 Large Signal Voltage Gain  
 – Supply Voltage

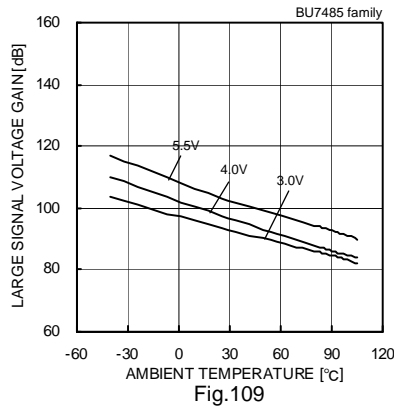


Fig.109  
 Large Signal Voltage Gain  
 – Ambient Temperature

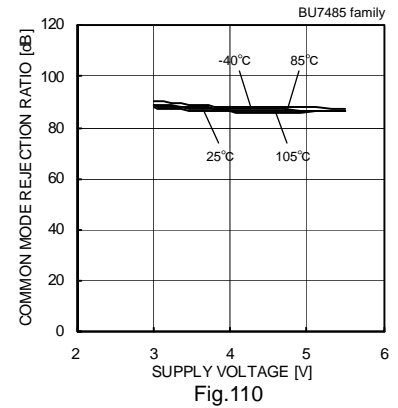


Fig.110  
 Common Mode Rejection Ratio  
 – Supply Voltage (VDD=3[V])

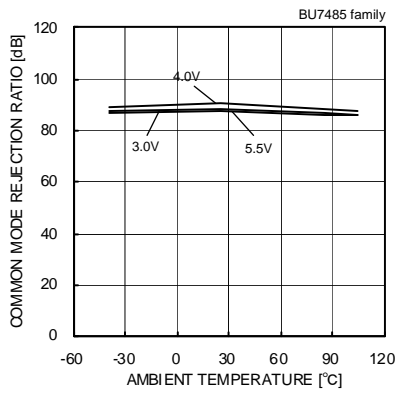


Fig.111  
 Common Mode Rejection Ratio  
 – Ambient Temperature

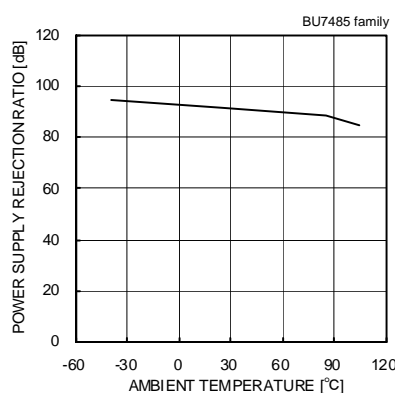


Fig.112  
 Power Supply Rejection Ratio  
 – Ambient Temperature

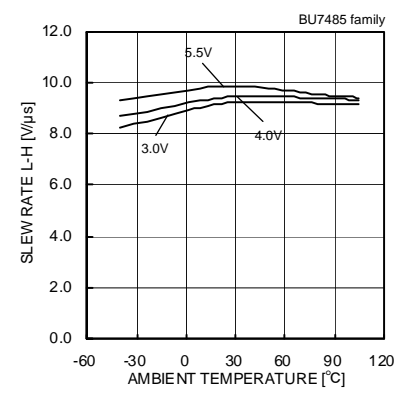


Fig.113  
 Slew Rate L-H  
 – Ambient Temperature

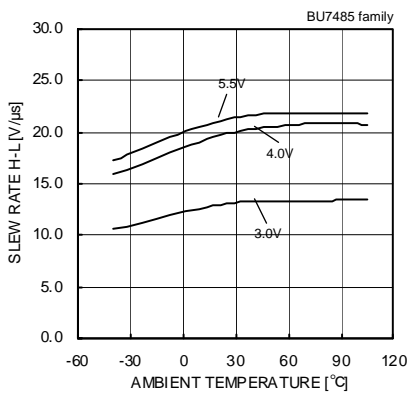


Fig.114  
 Slew Rate H-L – Ambient Temperature

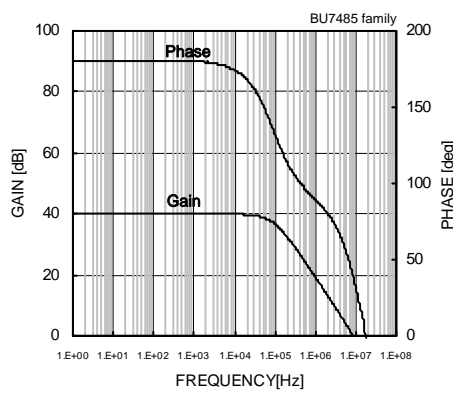


Fig.115  
 Voltage Gain – Frequency

(\*The above data is ability value of sample, it is not guaranteed. BU7485G: -40[°C] ~ +85[°C] BU7485SG: -40[°C] ~ +105[°C]

● Reference Data (BU5281 family)

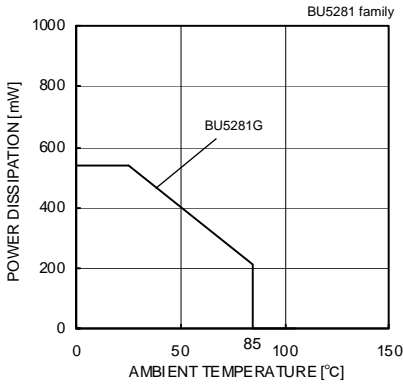


Fig. 116

Derating curve

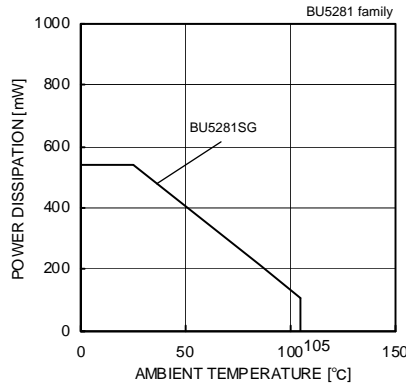


Fig. 117

Derating curve

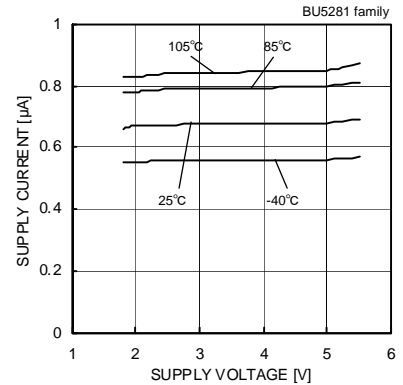


Fig. 118

Supply Current - Supply Voltage

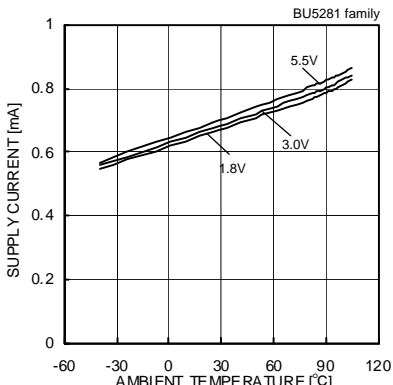


Fig. 119

Supply Current  
 - Ambient Temperature

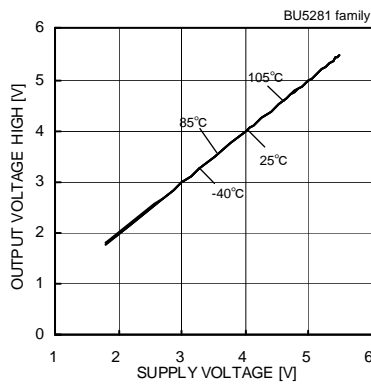


Fig. 120

Output Voltage High  
 - Supply Voltage (RL=10[kΩ])

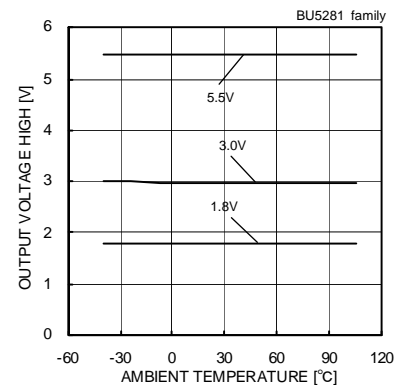


Fig. 121

Output Voltage High  
 - Ambient Temperature (RL=10[kΩ])



Fig. 122

Output Voltage Low  
 - Supply Voltage (RL=10[kΩ])



Fig. 123

Output Voltage Low  
 - Ambient Temperature (RL=10[kΩ])

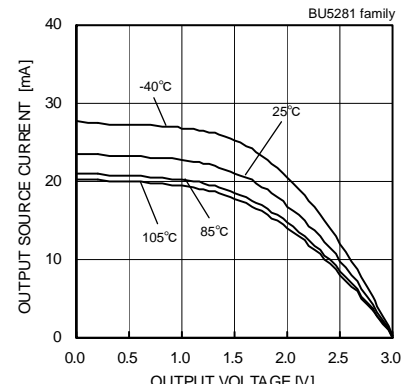


Fig. 124

Output Source Current  
 - Output Voltage (VDD=3[V])

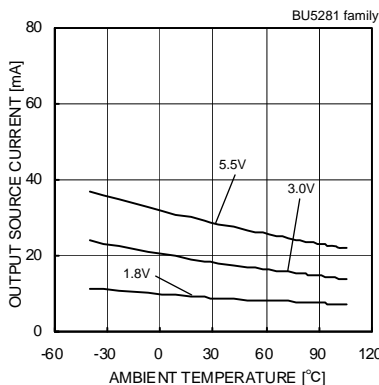


Fig. 125

Output Source Current - Ambient Temperature  
 (VOUT=VDD-0.4[V])

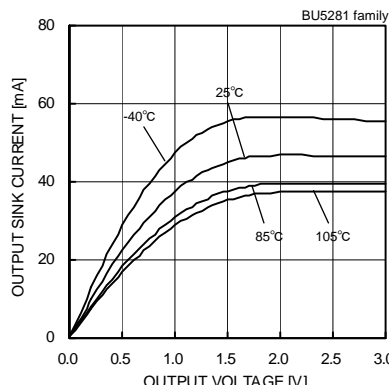


Fig. 126

Output Sink Current - Output Voltage  
 (VDD=3[V])

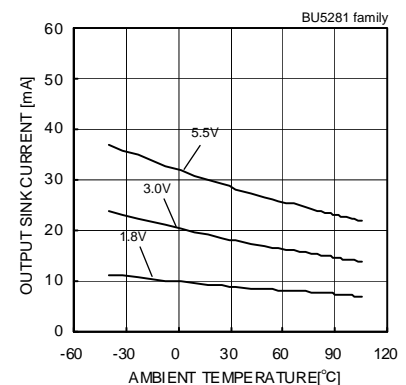


Fig. 127

Output Sink Current - Ambient Temperature  
 (VOUT=VSS+0.4[V])

(\*)The above data is ability value of sample, it is not guaranteed. BU5281G: -40[°C] ~ +85[°C] BU5281SG: -40[°C] ~ +105[°C]

●Reference Data (BU5281 family)



Fig.128  
 Input Offset Voltage – Supply Voltage  
 (Vicm=VDD-1.2[V], VOUT=1.5[V])



Fig.129  
 Input Offset Voltage – Ambient Temperature  
 (Vicm=VDD-1.2[V], VOUT=1.5[V])

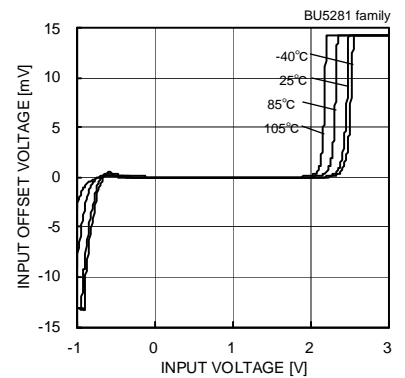


Fig.130  
 Input Offset Voltage – Input Voltage  
 (VDD=3[V])



Fig.131  
 Large Signal Voltage Gain  
 – Supply Voltage



Fig.132  
 Large Signal Voltage Gain  
 – Ambient Temperature

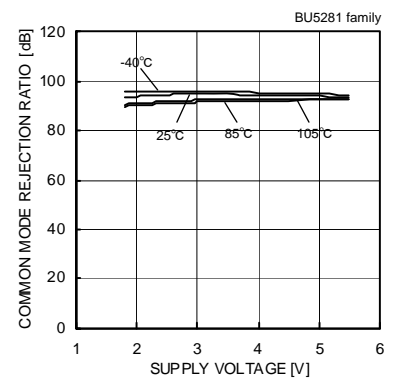


Fig.133  
 Common Mode Rejection Ratio  
 – Supply Voltage (VDD=3[V])



Fig.134  
 Common Mode Rejection Ratio  
 – Ambient Temperature



Fig.135  
 Power Supply Rejection Ratio  
 – Ambient Temperature

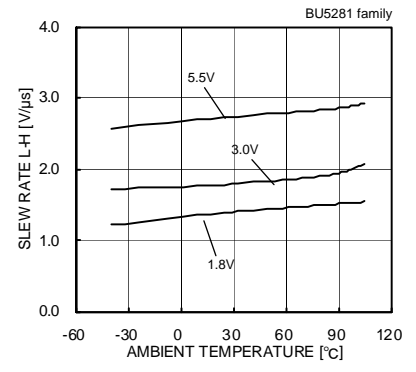


Fig.136  
 Slew Rate L-H –  
 Ambient Temperature

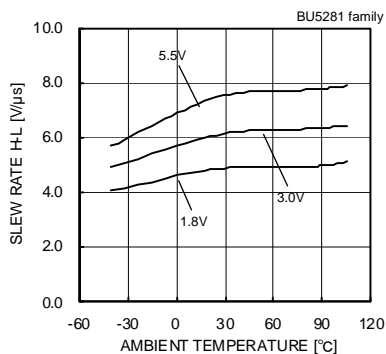


Fig.137  
 Slew Rate H-L – Ambient Temperature



Fig.138  
 Voltage Gain – Frequency

(\*)The above data is ability value of sample, it is not guaranteed. BU5281G: -40[°C] ~ +85[°C] BU5281SG: -40[°C] ~ +105[°C]

● Test circuit 1 NULL method

○ Input-Output Full Swing BU7291/BU7255 family

VDD, VSS, EK, Vicm Unit:[V]

Parameter	VF	S1	S2	S3	VDD	VSS	EK	Vicm	Calculation
Input Offset Voltage	VF1	ON	ON	OFF	3	0	-1.5	3	1
Large Signal Voltage Gain	VF2	ON	ON	ON	3	0	-0.5	1.5	2
	VF3						-2.5		
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	VF4	ON	ON	OFF	3	0	-1.5	0	3
	VF5						-1.5	3	
Power Supply Rejection Ratio	VF6	ON	ON	OFF	2.4	0	-1.2	0	4
	VF7				5.5				

○ Ground Sense BU7495/BU7481/BU7485/BU5281 family

VDD, VSS, EK, Vicm Unit:[V]

Parameter	VF	S1	S2	S3	VDD	VSS	EK	Vicm	Calculation	
Input Offset Voltage	VF1	ON	ON	OFF	3	0	-1.5	1.8	1	
Large Signal Voltage Gain	VF2	ON	ON	ON	3	0	-0.5	0.9	2	
	VF3						-2.5			
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	VF4	ON	ON	OFF	3	0	-1.5	0	3	
	VF5						-1.5	1.8		
Power Supply Rejection Ratio	VF6	ON	ON	OFF	1.8	0	-0.9	0	4	
					BU7495/BU7481/BU5281					3.0
					BU7485					5.5

— Calculation —

1. Input Offset Voltage (Vio)

$$V_{io} = \frac{|VF1|}{1+R_f/R_s} \text{ [V]}$$

2. Large Signal Voltage Gain (Av)

$$A_v = 20 \text{Log} \frac{2x(1+R_f/R_s)}{|VF2-VF3|} \text{ [dB]}$$

3 Common-mode Rejection Ratio (CMRR)

$$\text{CMRR} = 20 \text{Log} \frac{\Delta V_{icm} x (1+R_f/R_s)}{|VF4-VF5|} \text{ [dB]}$$

4. Power Supply Rejection Ratio (PSRR)

$$\text{PSRR} = 20 \text{Log} \frac{\Delta V_{DD} x (1+R_f/R_s)}{|VF6-VF7|} \text{ [dB]}$$

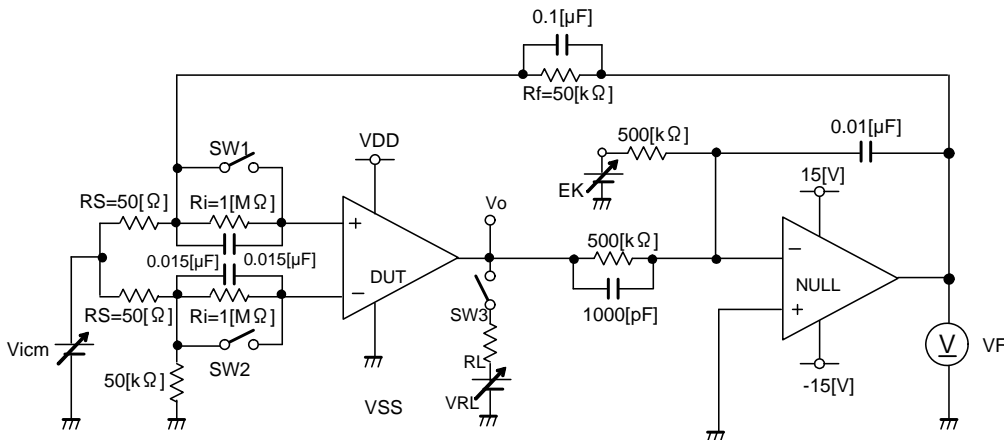


Fig.139 Test circuit 1 (one channel only)

● Test circuit 2 switch condition

SW No.	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage (RL=10[kΩ])	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Maximum Frequency	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

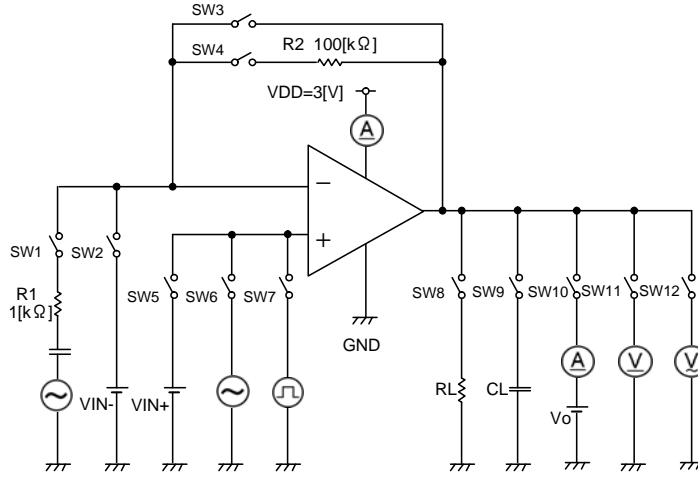


Fig.140 Test circuit 2



Fig.141 Slew rate input output wave  
 (Input-Output Full Swing BU7291/BU7255 family)

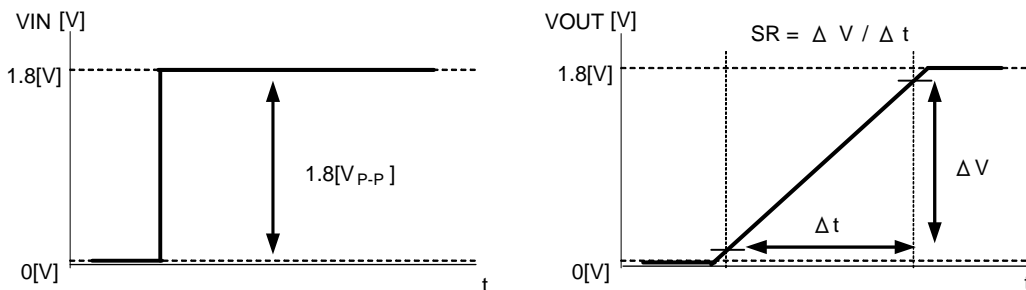


Fig.142 Slew rate input output wave  
 (Ground Sense BU7495/BU7481/BU7485/BU5281 family)

● Test circuit 3 Channel Separation

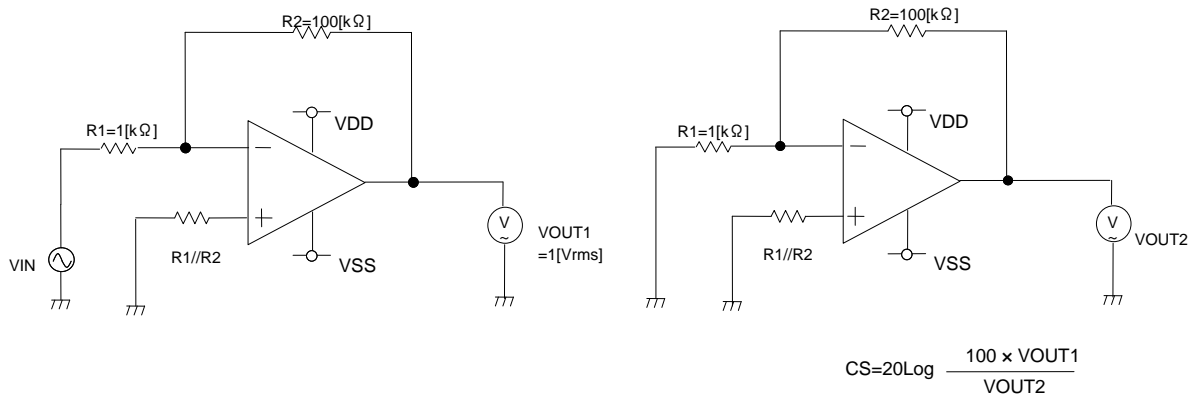


Fig.143 Test circuit 3

● Schematic Diagram

○ Input-Output Full Swing BU7291/BU7255 family

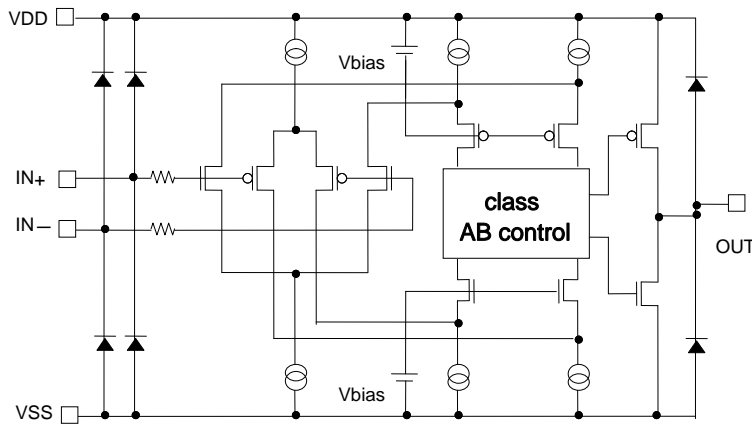


Fig.144 Input-Output Full Swing Schematic Diagram

○ Ground Sense BU7495/BU7481/BU7485/BU5281 family

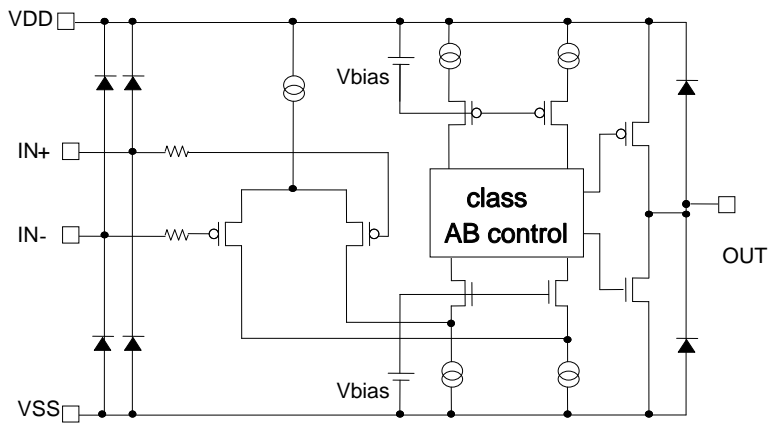


Fig.145 Ground Sense Schematic Diagram

● Examples of circuit

○ Voltage follower

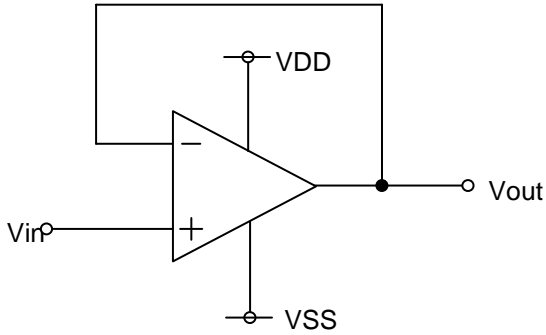


Fig.146 Voltage follower

Voltage gain is 0 [dB].

This circuit controls output voltage ( $V_{out}$ ) equal input voltage ( $V_{in}$ ), and keeps  $V_{out}$  with stable because of high input impedance and low output impedance.

$V_{out}$  is shown next formula.

$$V_{out} = V_{in}$$

○ Inverting amplifier

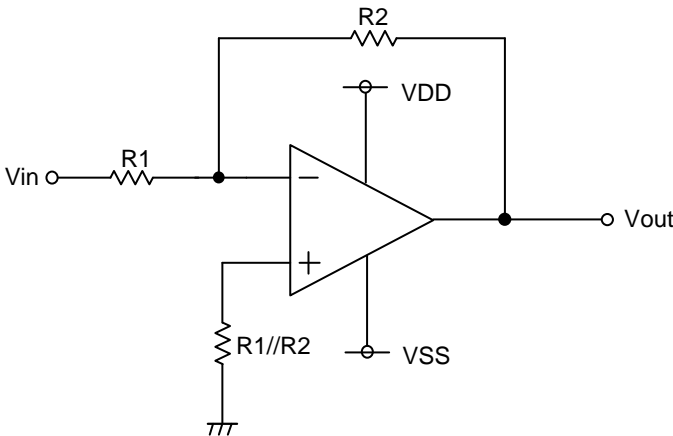


Fig.147 Inverting amplifier circuit

For inverting amplifier,  $V_{in}$  is amplified by voltage gain decided  $R_1$  and  $R_2$ , and phase reversed voltage is outputted.  $V_{out}$  is shown next formula.

$$V_{out} = -(R_2/R_1) \cdot V_{in}$$

Input impedance is  $R_1$ .

○ Non-inverting amplifier

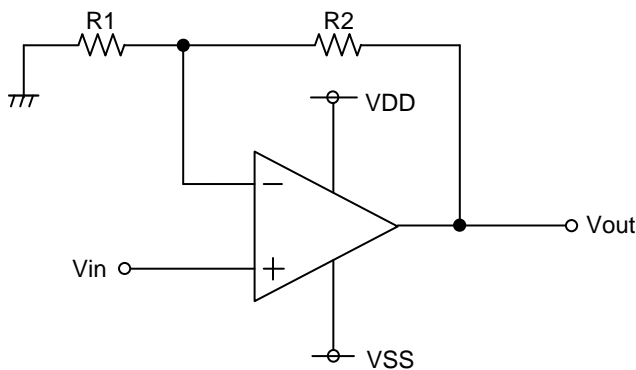


Fig.148 Non-inverting amplifier circuit

For non-inverting amplifier,  $V_{in}$  is amplified by voltage gain decided  $R_1$  and  $R_2$ , and phase is same with  $V_{in}$ .

$V_{out}$  is shown next formula.

$$V_{out} = (1 + R_2/R_1) \cdot V_{in}$$

This circuit realizes high input impedance because Input impedance is operational amplifier's input Impedance.

● Derating Curve

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25°C (normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol  $\theta_{j-a}$  [°C/W]. The temperature of IC inside the package can be estimated by this thermal resistance.

Fig.149 (a) shows the model of thermal resistance of the package. Thermal resistance  $\theta_{j-a}$ , ambient temperature Ta, junction temperature Tj, and power dissipation Pd can be calculated by the equation below:

$$\theta_{j-a} = (T_j - T_a) / P_d \quad [^{\circ}\text{C}/\text{W}] \quad \dots \dots \dots (I)$$

Derating curve in Fig.149 (b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance  $\theta_{j-a}$ . Thermal resistance  $\theta_{j-a}$  depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Fig.150(c)-(d) show a derating curve for an example of BU7291 family, BU7255 family, BU7495 family, BU7481 family, BU7485 family, BU5281 family.

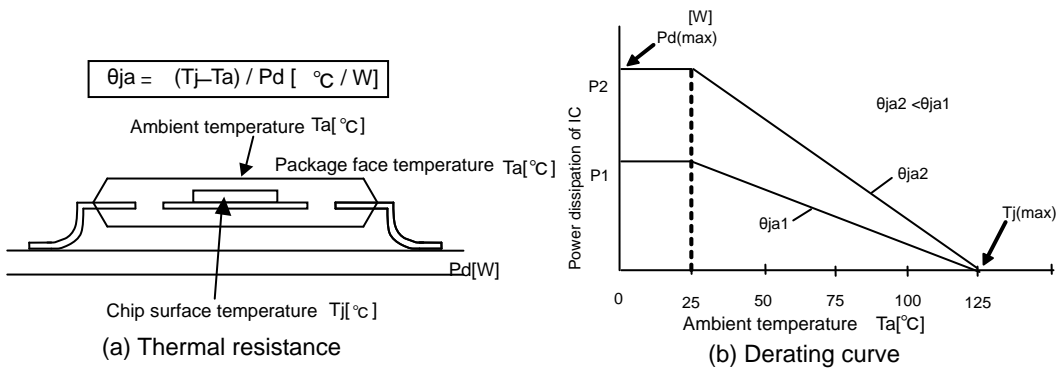
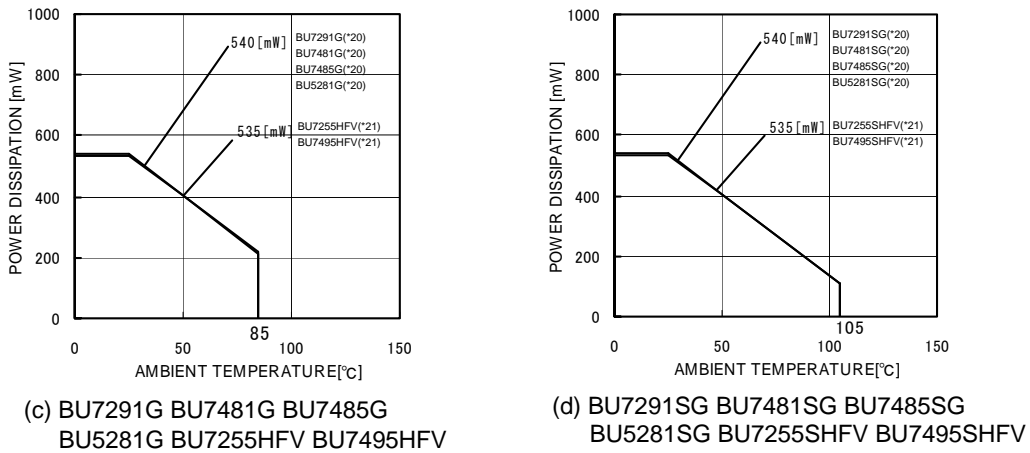


Fig.149 Thermal resistance and derating



(*20)	(*21)	Unit
5.4	5.35	[mW/°C]

When using the unit above Ta=25[°C], subtract the value above per degree[°C]. Permissible dissipation is the value when FR4 glass epoxy board 70[mm] × 70[mm] × 1.6[mm] (cooper foil area below 3[%]) is mounted

Fig.150 Derating Curve



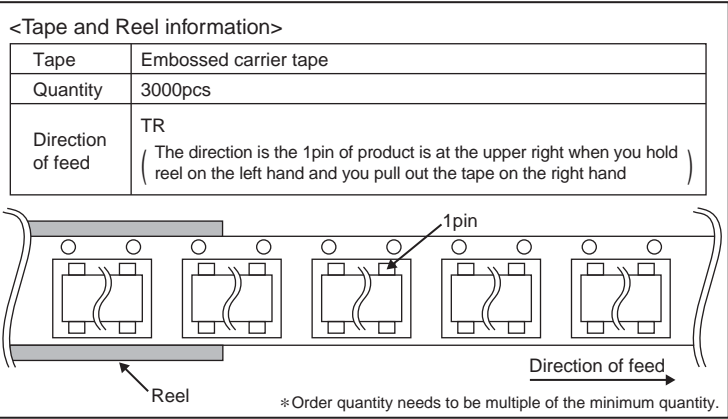
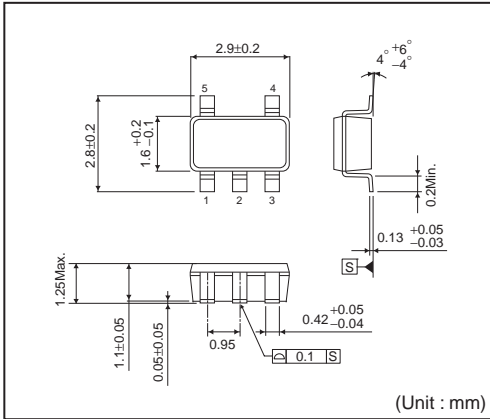
**●Notes for Use**

- 1) Absolute maximum ratings  
Absolute maximum ratings are the values which indicate the limits, within which the given voltage range can be safely charged to the terminal. However, it does not guarantee the circuit operation.
- 2) Applied voltage to the input terminal  
For normal circuit operation of voltage comparator, please input voltage for its input terminal within input common mode voltage  $VDD + 0.3[V]$ . Then, regardless of power supply voltage,  $VSS - 0.3[V]$  can be applied to input terminals without deterioration or destruction of its characteristics.
- 3) Operating power supply (split power supply/single power supply)  
The operational amplifier operates if a given level of voltage is applied between VDD and VSS. Therefore, the operational amplifier can be operated under single power supply or split power supply.
- 4) Power dissipation (Pd)  
If the IC is used under excessive power dissipation. An increase in the chip temperature will cause deterioration of the radical characteristics of IC. For example, reduction of current capability. Take consideration of the effective power dissipation and thermal design with a sufficient margin. Pd is reference to the provided power dissipation curve.
- 5) Output short circuit  
If short circuit occurs between the output terminal and VDD terminal, excessive in output current may flow and generate heat, causing destruction of the IC. Take due care.
- 6) Using under strong electromagnetic field  
Be careful when using the IC under strong electromagnetic field because it may malfunction.
- 7) Usage of IC  
When stress is applied to the IC through warp of the printed circuit board, The characteristics may fluctuate due to the piezo effect. Be careful of the warp of the printed circuit board.
- 8) Testing IC on the set board  
When testing IC on the set board, in cases where the capacitor is connected to the low impedance, make sure to discharge per fabrication because there is a possibility that IC may be damaged by stress. When removing IC from the set board, it is essential to cut supply voltage. As a countermeasure against the static electricity, observe proper grounding during fabrication process and take due care when carrying and storage it.
- 9) The IC destruction caused by capacitive load  
The transistors in circuits may be damaged when VDD terminal and VSS terminal is shorted with the charged output terminal capacitor. When IC is used as a operational amplifier or as an application circuit, where oscillation is not activated by an output capacitor, the output capacitor must be kept below  $0.1[\mu F]$  in order to prevent the damage mentioned above.
- 10) Decoupling capacitor  
Insert the decoupling capacitance between VDD and VSS, for stable operation of operational amplifier.
- 11) Latch up  
Be careful of input voltage that exceed the VDD and VSS. When CMOS device have sometimes occur latch up operation. And protect the IC from abnormaly noise.

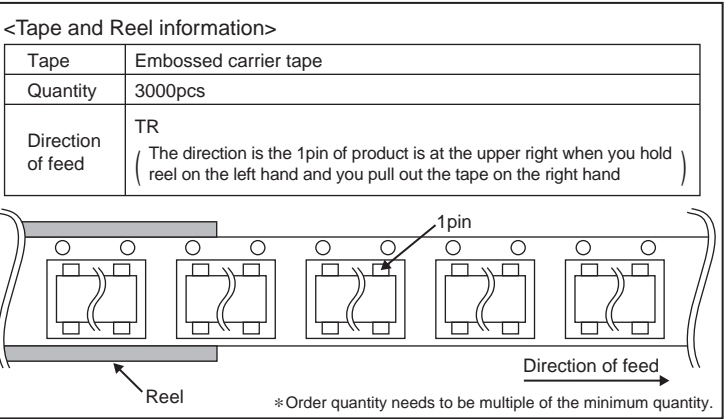
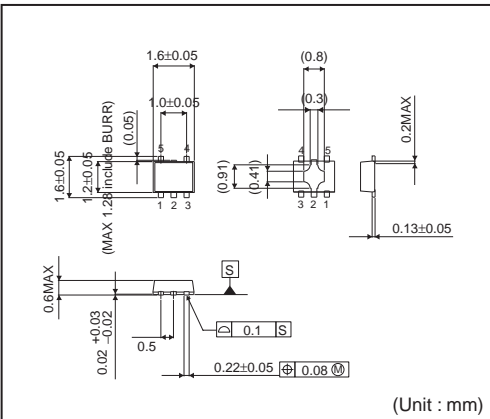
● Ordering Part Number

B	U	7	4	9	5	S	H	F	V	-	T	R
Part No.		Part No. <b>Input-Output Full Swing</b> 7291 , 7291S , 7255 , 7255S <b>Ground Sense</b> 7495 , 7495S , 7481 , 7481S 7485 , 7485S , 5281 , 5281S					Package G: SSOP5 HFV: HVSO5F5			Packaging and forming specification TR: Embossed tape and reel		

SSOP5



HVSO5F5



## Notes

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