# 1 GBPS TO 4.25 GBPS MULTI-RATE VCSEL DRIVER

## FEATURES

- **Multi-Rate Operation from 1 Gbps Up To 4.25 Gbps**
- **2-Wire Digital Interface**
- **Digitally Selectable Modulation Current**
- **Digitally Selectable Bias Current**
- **Automatic Power Control (APC) Loop**
- **Supports Transceiver Management System (TMS)**
- **Includes Laser Safety Features**
- **Analog Temperature Sensor Output**
- **Single 3.3-V Supply**
- **Operating Temperature –40°C to 85°C**
- **Small Footprint Surface Mount 4 mm × 4 mm, 20-Pin QFN Package**

## APPLICATIONS

- **Multirate SFP/SFF Modules**
- **1.0625 Gbps, 2.125 Gbps, and 4.25 Gbps Fibre Channel Transmitters**
- **Gigabit Ethernet Transmitters**

## DESCRIPTION

The ONET4291VA is a versatile high-speed multi-rate VCSEL driver for fiber optic applications with data rates up to 4.25 Gbps.

The device provides a 2-wire interface which allows digital control of the modulation and bias currents, eliminating the need for of external components.

The ONET4291VA includes an integrated automatic power control loop as well as circuitry to support laser safety and transceiver management systems.

The part is available in a small footprint 4 mm × 4 mm 20-pin QFN package and it requires a single 3.3-V supply.

This power efficient multi-rate VCSEL driver is characterized for operation from –40°C to 85°C ambient temperature.

## BLOCK DIAGRAM

A simplified block diagram of the ONET4291VA is shown in Figure 1.

This compact, low power 1-Gbps to 4.25-Gbps multi-rate VCSEL driver consists of a high-speed current modulator, a modulation current generator, power-on reset circuitry, a 2-wire interface and control logic block, a bias current generator and automatic power control loop, and an analog reference block.

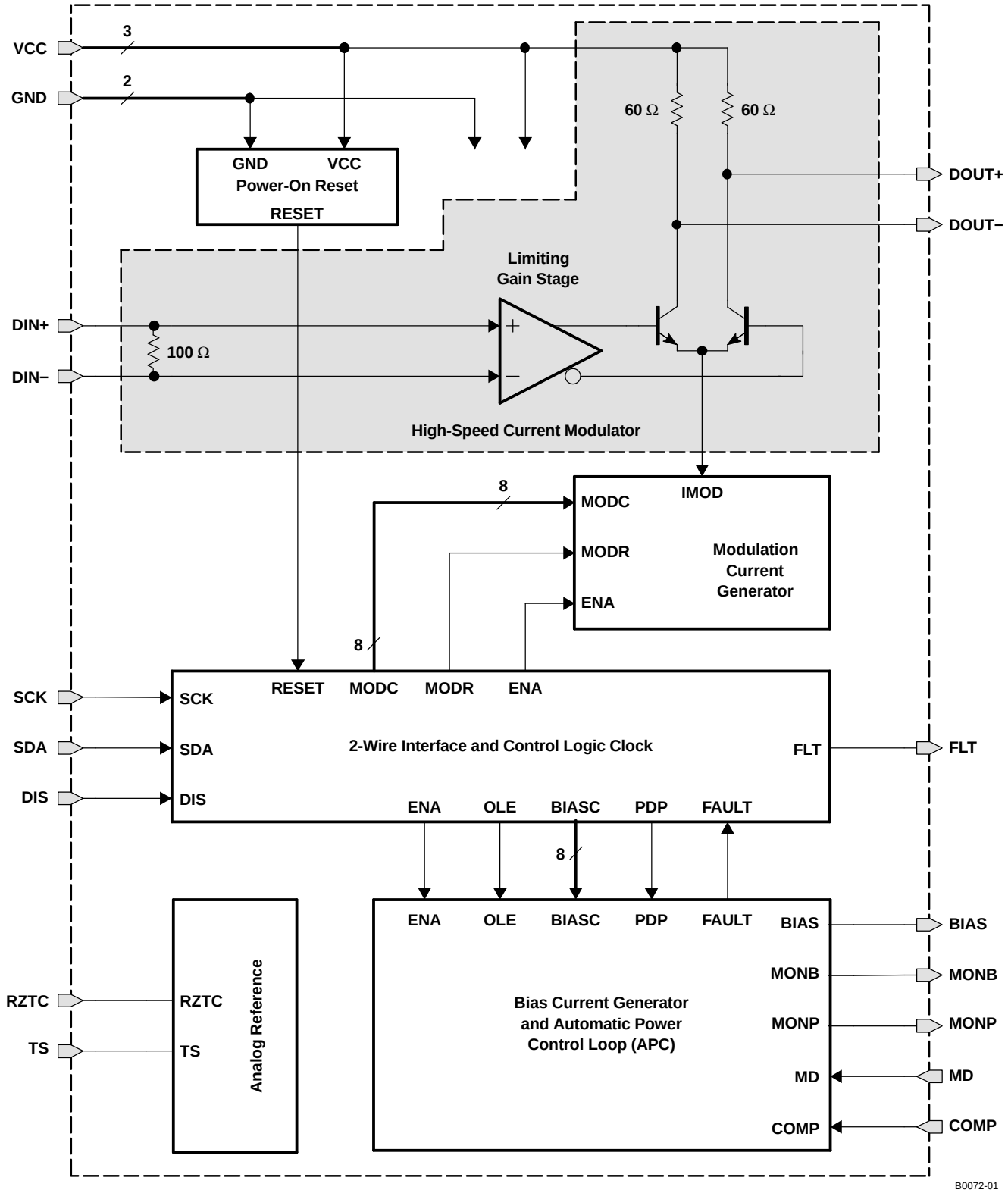



**Figure 1. Simplified Block Diagram of the ONET4291VA**

## HIGH-SPEED CURRENT MODULATOR

The data signal is applied to the high-speed current modulator by means of the input signal pins DIN+/DIN–, which provide on-chip differential 100-Ω line-termination. The succeeding limiting gain stage ensures sufficient drive amplitude and edge-speed for driving the current modulator differential pair.

The modulation current is sunk from the common emitter node of the differential pair by means of a modulation current generator, which is digitally controlled by the 2-wire interface and control logic block.

The collector nodes of the differential pair are connected to the output pins DOUT+/DOUT–, which include on-chip 2 × 60-Ω back-termination to VCC. The 60-Ω back-termination helps to sufficiently suppress signal distortion caused by double reflections for VCSEL diodes with impedances ranging from 50 Ω through 75 Ω.

## MODULATION CURRENT GENERATOR

The modulation current generator provides the current for the current modulator described above. The circuit is digitally controlled by the 2-wire interface and control logic block.

An 8-bit wide control bus, MODC, is used to set the desired modulation current.

Furthermore, two modulation current ranges are selected by means of the MODR signal.

The ENA signal enables or disables the modulation current generator.

The modulation current can be disabled by setting the DIS input pin to a high level. The modulation current is also disabled in a fault condition if the fault detection enable register flag FLTEN is set.

For more information about the register functionality, see the register mapping description.

## 2-WIRE SERIAL INTERFACE AND CONTROL LOGIC

The ONET4291VA uses a 2-wire serial interface for digital control. A simplified block diagram of this interface is shown in Figure 2.

The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microprocessor, for example. Both inputs include 100-kΩ pullup resistors to VCC. For driving these inputs, an open drain output is recommended.

A write cycle consists of a START command, three address bits with MSB first, eight data bits with MSB first, and a STOP command. In idle mode, both SDA and SCK lines are at a high level.

A START command is initiated by the falling edge of SDA with SCK at a high level, transitioning to a low level.

Bits are clocked into an 11-bit wide shift register during the high level of the system clock SCK.

A STOP command is detected on the rising edge of SDA after SCK has changed from a low to a high level.

At the time of detection of a STOP command, the eight data bits from the shift register are copied to a selected 8-bit register. Register selection occurs according to the three address bits in the shift register, which are decoded to eight independent select signals using a 3 to 8 decoder block.

In the ONET4291VA, only addresses 0 (000b) through 3 (011b) are used.

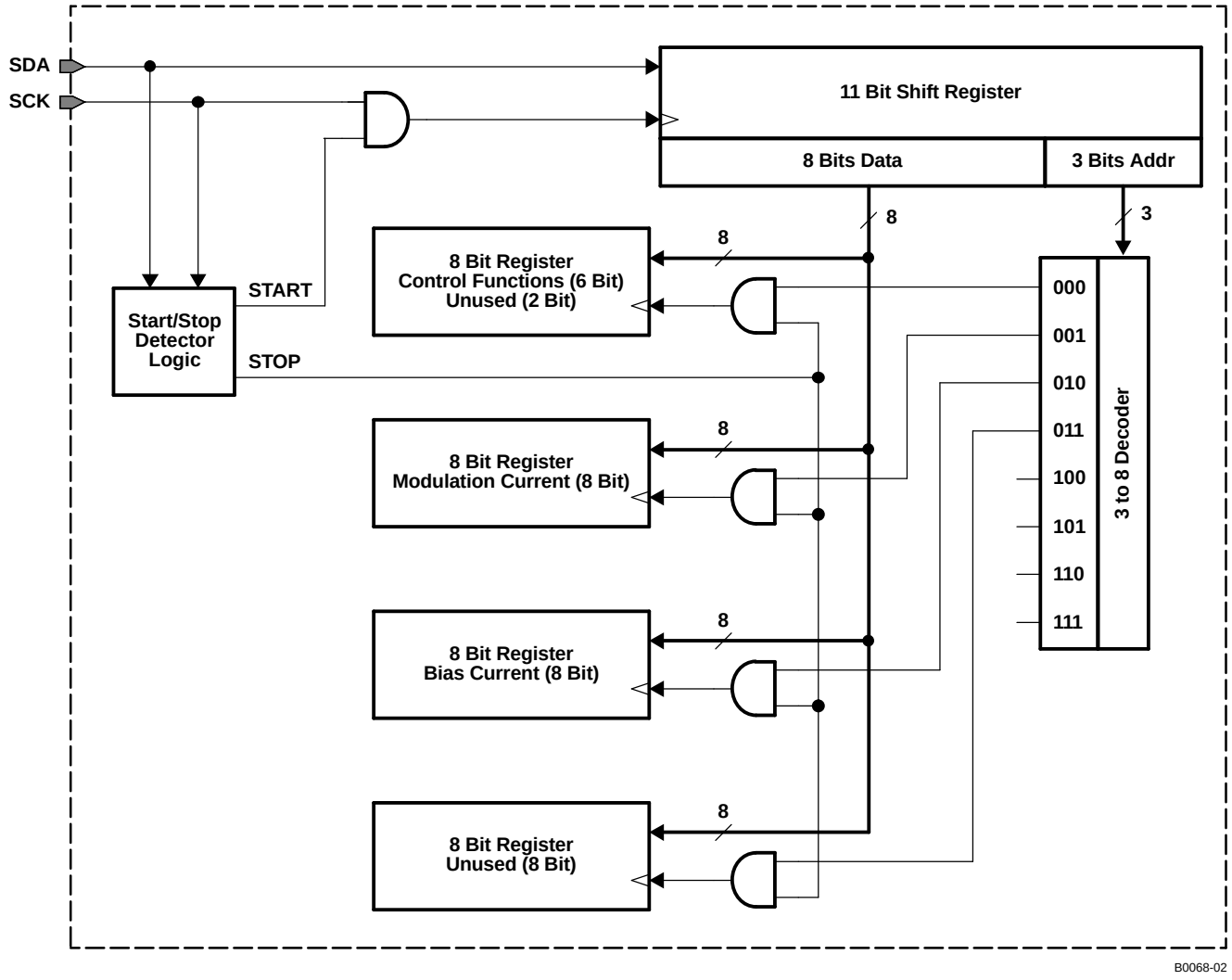



**Figure 2. Simplified 2-Wire Interface Block Diagram**

The timing definition for the serial data signal SDA and the serial clock signal SCK is shown in Figure 3. The corresponding timing requirements are listed in Table 1.

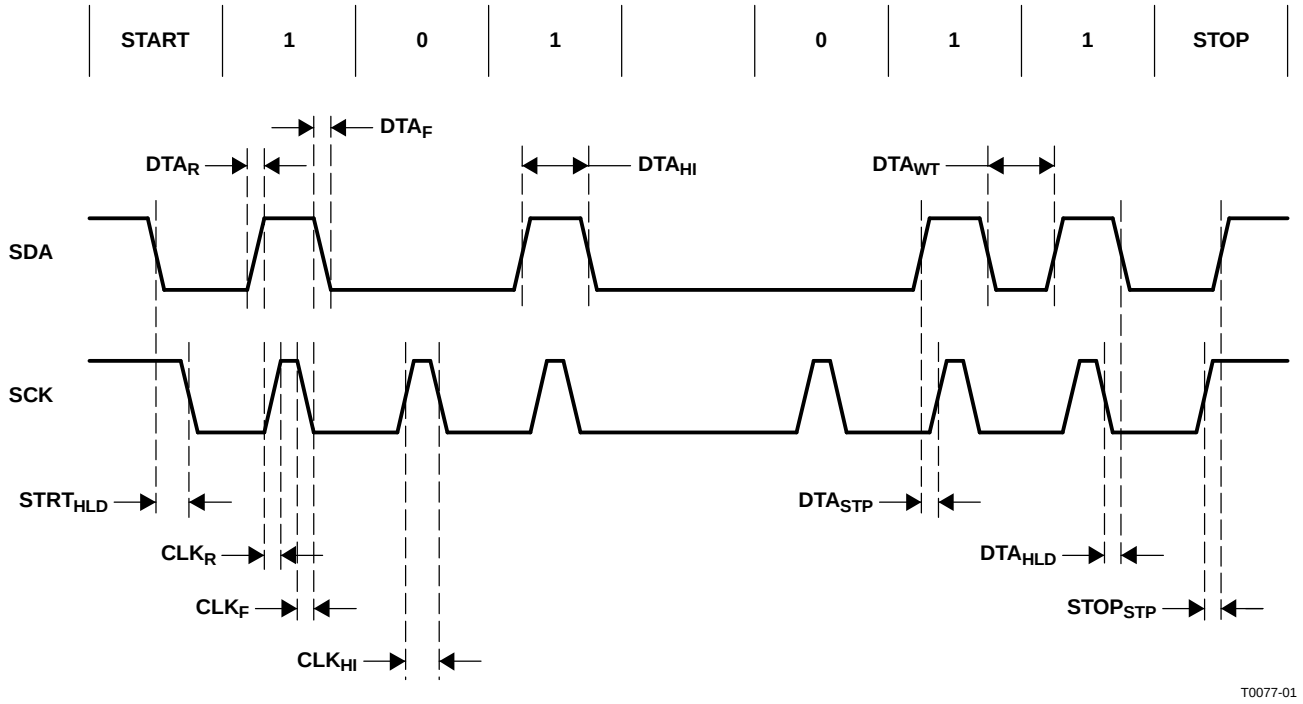



**Figure 3. 2-Wire Interface Timing Diagram**

**Table 1. 2-Wire Interface Timing**

| PARAMETER | | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $STRT_{HLD}$ | START hold time | Time required from data falling edge to clock falling edge at START | 10 | | ns |
| $CLK_R$, $DTA_R$ | Clock and data rise time | Clock and data rise time | | 10 | ns |
| $CLK_F$, $DTA_F$ | Clock and data fall time | Clock and data fall time | | 10 | ns |
| $CLK_{HI}$ | Clock high time | Minimum clock high period | 50 | | ns |
| $DTA_{HI}$ | Data high time | Minimum data high period | 100 | | ns |
| $DTA_{STP}$ | Data setup time | Minimum time from data rising edge to clock rising edge | 10 | | ns |
| $DTA_{WT}$ | Data wait time | Minimum time from data falling edge to data rising edge | 50 | | ns |
| $DTA_{HLD}$ | Data hold time | Minimum time from clock falling edge to data falling edge | 10 | | ns |
| $STOP_{STP}$ | STOP setup time | Minimum time from clock rising edge to data rising edge at STOP | 10 | | ns |

## REGISTER MAPPING

The register mapping for the register addresses 0 (000b) through 3 (011b) are shown in Table 2 to Table 5. Register 3 is included for future enhancements. It is not used in the current device.

Table 6 describes the circuit functionality based on the register settings.

**Table 2. Register 0 (000b) Mapping**

| address 0 (000b) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **bit 7** | **bit 6** | **bit 5** | **bit 4** | **bit 3** | **bit 2** | **bit 1** | **bit 0** |
| ENA | PDP | PDR | OLE | FLTEN | MODR | – | – |

**Table 3. Register 1 (001b) Mapping**

| address 1 (001b) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **bit 7** | **bit 6** | **bit 5** | **bit 4** | **bit 3** | **bit 2** | **bit 1** | **bit 0** |
| MODC7 | MODC6 | MODC5 | MODC4 | MODC3 | MODC2 | MODC1 | MODC0 |

**Table 4. Register 2 (010b) Mapping**

| address 2 (010b) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **bit 7** | **bit 6** | **bit 5** | **bit 4** | **bit 3** | **bit 2** | **bit 1** | **bit 0** |
| BIASC7 | BIASC6 | BIASC5 | BIASC4 | BIASC3 | BIASC2 | BIASC1 | BIASC0 |

**Table 5. Register 3 (011b) Mapping**

| address 3 (011b) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **bit 7** | **bit 6** | **bit 5** | **bit 4** | **bit 3** | **bit 2** | **bit 1** | **bit 0** |
| – | – | – | – | – | – | – | – |

**Table 6. Register Functionality**

| Symbol | Register | Function |
|---|---|---|
| ENA | Enable | Enables chip when set to 1. Can be toggled to reset a fault condition. |
| PDP | Photodiode polarity | Photodiode polarity bit:<br>1 = common anode<br>0 = common cathode |
| PDR | Photodiode current range | Photodiode current range bit:<br>1 = 0 µA – 500 µA with 2-µA resolution<br>0 = 0 µA – 250 µA with 1-µA resolution |
| OLE | Open loop enable | Open loop enable bit:<br>1 = open loop bias current control<br>0 = closed loop bias current control |
| FLTEN | Fault detection enable | Fault detection enable bit:<br>1 = fault detection on<br>0 = fault detection off |
| MODR | Modulation current range | Laser modulation current range:<br>1 = 0 mA – 15 mA<br>0 = 0 mA – 12 mA |
| MODC7 | Modulation current bit 7 (MSB) | Modulation current setting: |
| MODC6 | Modulation current bit 6 | |
| MODC5 | Modulation current bit 5 | MODR = 1 (see above): |
| MODC4 | Modulation current bit 4 | Modulation current: 100 µA – 15.4 mA with 68 µA step size |
| MODC3 | Modulation current bit 3 | |
| MODC2 | Modulation current bit 2 | MODR = 0 (see above): |
| MODC1 | Modulation current bit 1 | Modulation current: 100 µA – 12 mA with 51 µA step size |
| MODC0 | Modulation current bit 0 (LSB) | |
| BIASC7 | Bias current bit 7 (MSB) | **closed loop (APC):** |
| BIASC6 | Bias current bit 6 | Coupling ratio CR between VCSEL bias current and photodiode current is: |
| BIASC5 | Bias current bit 5 | CR = $I_{BIAS-VCSEL}$ / $I_{PD}$ |
| BIASC4 | Bias current bit 4 | PDR = 0 (see above), BIASC = 0 .. 255, $I_{BIAS-VCSEL} \leq$ 12 mA: |
| BIASC3 | Bias current bit 3 | $I_{BIAS-VCSEL}$ = 100 µA + (1 µA × CR × BIASC) |
| BIASC2 | Bias current bit 2 | PDR = 1 (see above), BIASC = 0 .. 255, $I_{BIAS-VCSEL} \leq$ 12 mA: |
| BIASC1 | Bias current bit 1 | $I_{BIAS-VCSEL}$ = 100 µA + (2 µA × CR × BIASC) |
| BIASC0 | Bias current bit 0 (LSB) | **open loop:** $I_{BIAS-VCSEL}$ = 100 µA + (47 µA × BIASC) |

## BIAS CURRENT GENERATION AND APC LOOP

The bias current generation and APC loop are controlled by means of the 2-wire interface.

In open loop operation, selected by setting OLE = 1 (bit 4 of register 0), the bias current is set directly by the 8-bit wide control word BIASC[0..7] (register 2).

In automatic power control mode, selected by setting OLE = 0, the bias current depends on the register settings BIASC[0..7] and the coupling ratio (CR) between the VCSEL bias current and the photodiode current. $CR = I_{BIAS\text{-}VCSEL} / I_{PD}$.

Two photodiode current ranges can be selected by means of the PDR register (bit 5 of register 0). The photodiode range should be chosen to keep the laser bias control DAC close to the center of its range. This keeps the laser bias current setpoint resolution high and the loop settling time constant within specification.

For details regarding the bias current setting in open loop as well as in closed loop mode, see Table 6.

In closed loop mode, the photodiode polarity bit, PDP, must be set for common anode or common cathode configuration to ensure proper operation. In open loop mode if a photodiode is still present, the photodiode polarity bit must be set to the opposite setting.

## ANALOG REFERENCE

The ONET4291VA is supplied by a single 3.3-V ±10% supply voltage connected to the VCC pins. This voltage is referenced to ground (GND).

On-chip bandgap voltage circuitry generates a reference voltage, independent of the supply voltage, from which all other internally required voltages and bias currents are derived.

An external zero temperature coefficient resistor must be connected from the RZTC pin of the device to ground (GND). This resistor is used to generate a precise zero TC current which is used as a reference current for the on-chip DACs.

In order to minimize the module component count, the ONET4291VA VCSEL driver provides an on-chip temperature sensor. The output voltage of the temperature sensor is available at the TS pin.

The voltage is $V_{TS}$ = 9.4 mV × TEMP + 1337 mV with TEMP given in °C.

Note that the voltage at TS is not buffered. As a result, TS can only drive capacitive loads.

## POWER-ON RESET AND REGISTER LOADING SEQUENCE

The ONET4291VA has power on reset circuitry which ensures that all registers are reset to zero during startup. After the power-on to initialize time ($T_{INIT1}$), the internal registers are ready to be loaded. It is important that the registers are loaded in the following order:

1. Bias current register (register 2, 010b),
2. Modulation current register (register 1, 001b),
3. Control register (register 0, 000b).

The part will be ready to transmit data after the initialize to transmit time $T_{INIT2}$, assuming that the control register enable bit ENA is 1 and the disable pin DIS is low.

The ONET4291VA can be disabled using either the ENA control register bit or the disable pin DIS. In both cases the internal registers are not reset. After the disable pin DIS is de-asserted and/or the enable bit ENA is re-asserted the part returns to its prior output settings.

## LASER SAFETY FEATURES AND FAULT RECOVERY PROCEDURE

The ONET4291VA provides built in laser safety features. The following fault conditions are detected:

1. Voltage at MONB exceeds 1.2 V,
2. Photodiode current exceeds 150% of its target value,
3. Bias control DAC drops in value by more than 33% in one step.

If one or more fault conditions occur and the fault enable bit FLTEN is set to 1, the ONET4192VA responds by:

1. Setting the VCSEL bias current to zero.

2. Setting the modulation current to zero.
3. Asserting and latching the FLT pin.

Fault recovery is performed by the following procedure:

1. The disable pin DIS and/or the enable control bit ENA are toggled for at least the fault latch reset time $T_{RESET}$.
2. The FLT pin de-asserts while the disable pin DIS is asserted or the enable bit ENA is de-asserted.
3. If the fault condition is no longer present, the part will return to normal operation with its prior output settings after the disable negate time $T_{ON}$.
4. If the fault condition is still present, FLT re-asserts once DIS is set to low level and the part will not return to normal operation.

## PACKAGE

For the ONET4291VA, a small footprint 4 mm × 4 mm 20-pin QFN package with a lead pitch of 0,5 mm is used. The pin out is shown in Figure 4.

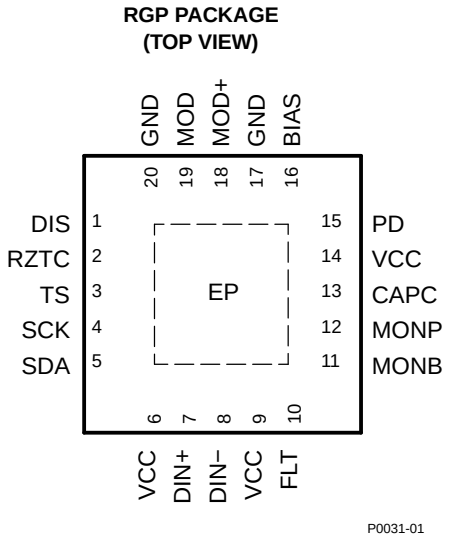



**Figure 4. Pinout of ONET4291VA in a 4 mm × 4 mm 20-Pin QFN Package**

### TERMINAL FUNCTIONS

| TERMINAL | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | DIS | CMOS-in | Disables both bias and modulation current when set to high state. Toggle to reset a fault condition |
| 2 | RZTC | Analog | Connect external zero TC 30-kΩ to ground (GND). Used to generate a defined zero TC reference current for internal DACs. |
| 3 | TS | Analog-out | Temperature sensor output. Not buffered, capacitive load only. |
| 4 | SCK | CMOS-in | 2-wire interface serial clock. Includes a 100-kΩ pullup resistor to VCC. |
| 5 | SDA | CMOS-in | 2-wire interface serial data input. Includes a 100-kΩ pullup resistor to VCC. |
| 6, 9, 14 | VCC | Supply | 3.3-V ±10% supply voltage |
| 7 | DIN+ | Analog-in | Non-inverted data input. On-chip differentially 100-Ω terminated to DIN–. Must be ac coupled. |
| 8 | DIN– | Analog-in | Inverted data input. On-chip differentially 100-Ω terminated to DIN+. Must be ac coupled. |
| 10 | FLT | CMOS-out | Fault detection flag |
| 11 | MONB | Analog-out | Bias current monitor. Sources an 8.3% replica of the bias current. Connect an external resistor to ground (GND). If the voltage at this pin exceeds 1.2 V a fault is triggered. |

### TERMINAL FUNCTIONS (continued)

| TERMINAL | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 12 | MONP | Analog-out | Photodiode current monitor. Sources a 50% replica of the photodiode current. Connect an external resistor to ground (GND). |
| 13 | CAPC | Analog | Compensation pin used to control the bandwidth of the APC loop. Connect a 0.01-μF capacitor to ground. |
| 15 | PD | Analog | Monitor photodiode input. The pin can source or sink current dependent on PDP register setting. Pin supplies >1.5-V reverse bias. |
| 16 | BIAS | Analog | VCSEL diode bias current source. Connect to laser anode through inductor. Murata BLM15HG102SN1 is recommended. |
| 17, 20, EP | GND | Supply | Circuit ground. The exposed die pad (EP) must be grounded. |
| 18 | MOD+ | CML-out | Non-inverted modulation current output. AC coupled to anode of common cathode VCSEL. On-chip 60-Ω back-terminated to VCC. |
| 19 | MOD– | CML-out | Inverted modulation current output. AC coupled through VCSEL matching resistor to ground (GND). On-chip 60-Ω back-terminated to VCC. |

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | VALUE / UNIT |
|---|---|---|
| $V_{CC}$ | Supply voltage | –0.3 V to 4 V |
| $V_{DIS}$, $V_{RZTC}$, $V_{TS}$, $V_{SCK}$, $V_{SDA}$, $V_{DIN+}$, $V_{DIN–}$, $V_{FLT}$, $V_{MONB,}$ $V_{MONP}$, $V_{CAPC}$, $V_{PD}$, $V_{BIAS}$, $V_{MOD+}$, $V_{MOD–}$ | Voltage at DIS, RZTC, TS, SCK, SDA, DIN+, DIN–, FLT, MONB, MONP, CAPC, PD, BIAS, MOD+, MOD–(2) | –0.3 V to 4 V |
| ESD | ESD rating at all pins | 3 kV (HBM) |
| $T_{J,max}$ | Maximum junction temperature | 125°C |
| $T_{STG}$ | Storage temperature range | –65°C to 85°C |
| $T_A$ | Characterized free-air operating temperature range | –40°C to 85°C |
| $T_{LEAD}$ | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.9 | 3.3 | 3.6 | V |
| $V_{IH}$ | CMOS input high voltage | DIS, SCK, SDA | 2 | | | V |
| $V_{IL}$ | CMOS input low voltage | DIS, SCK, SDA | | | 0.8 | V |
| | Bias output headroom voltage | $V_{CC}$– $V_{BIAS}$, $I_{BIAS}$ = 10 mA | 500 | | | mV |
| | Photodiode current range | Control bit PDR = 1, step size = 2 μA | 10 | | 500 | μA |
| | | Control bit PDR = 0, step size = 1 μA | 5 | | 250 | |
| $R_{RZTC}$ | Zero TC resistor value(1) | 1.22-V bias across resistor | 29.7 | 30 | 30.3 | kΩ |
| $V_{IN}$ | Differential input voltage swing | | 200 | 800 | 2400 | mVp-p |
| $t_{R-IN}$ | Input rise time | 20%–80%, $f_{BIT}$ = 1.25 Gbps | | | 160 | ps |
| | | 20%–80%, $f_{BIT}$≥ 2.125 Gbps | | | 100 | |
| $t_{F-IN}$ | Input fall time | 20%–80%, $f_{BIT}$ = 1.25 Gbps | | | 160 | ps |
| | | 20%–80%, $f_{BIT}$≥ 2.125 Gbps | | | 100 | |
| $T_A$ | Operating free-air temperature | | –40 | | 85 | °C |

(1) Changing the value alters DAC ranges.

## DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, all values are for open loop operation, $I_{MOD}$ = 6 mA, $I_{BIAS}$ = 5 mA, and $R_{RZTC}$ = 30 kΩ, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.9 | 3.3 | 3.6 | V |
| $I_{VCC}$ | Supply current | $I_{MOD}$ = 6 mA, $I_{BIAS}$ = 5 mA, including $I_{MOD}$ and $I_{BIAS}$ | | 40 | 45 | mA |
| | | Disabled, DIS = high and/or control bit ENA = low | | 22 | | |
| $R_{IN}$ | Data input/output resistance | Differential between DIN+/DIN– | 85 | 100 | 115 | Ω |
| $R_{OUT}$ | Data output/output resistance | Single-ended to VCC | 50 | 60 | 70 | Ω |
| | CMOS input current | SCK, SDA, 100-kΩ pullup to VCC | –50 | | 10 | µA |
| | CMOS input current | DIS | –10 | | 10 | µA |
| $V_{OH}$ | CMOS output high voltage | FLT, $I_{SINK}$ = 1 mA | 2.5 | | | V |
| $V_{OL}$ | CMOS output low voltage | FLT, $I_{SOURCE}$ = 1 mA | | | 0.5 | V |
| $I_{BIAS-DIS}$ | Bias current during disable | | | | 100 | µA |
| $I_{BIAS-MIN}$ | Minimum bias current | See (1) | | | 0.2 | mA |
| $I_{BIAS-MAX}$ | Maximum bias current | DAC set to maximum, closed loop | 8.5 | | | mA |
| | | DAC set to maximum, open loop | 11 | | | |
| $V_{PD}$ | Photodiode reverse bias voltage | APC active, $I_{PD}$ = max | 1.5 | 2.1 | | V |
| | Photodiode fault current level | Percent of target $I_{PD}$ (2) | | 150% | | |
| $V_{TS}$ | Temperature sensor voltage range | –40°C to 120°C junction temperature. Capacitive load only. After mid-scale calibration. | 0.8 | | 2.5 | V |
| | Temperature sensor accuracy | Mid scale calibration | | ±3 | | °C |
| $I_{TS}$ | Temperature sensor drive current | Source or sink (2) | –10 | | 10 | µ A |
| | Photodiode current monitor ratio | $I_{MONP}$ / $I_{PD}$, $I_{BIAS}$ > 100 µA | 45% | 60% | 80% | |
| | Bias current monitor ratio | $I_{MONB}$ / $I_{BIAS}$ (nominal 1/12 = 8.3%) | 6.7% | 8.3% | 10% | |
| $V_{CC-RST}$ | $V_{CC}$ reset threshold voltage | VCC voltage level which triggers power-on reset | 2.4 | 2.6 | 2.85 | V |
| $V_{CC-RSTHYS}$ | VCC reset threshold voltage hysteresis | | | 120 | | mV |
| $V_{MONB-FLT}$ | Fault voltage at MONB | Fault occurs if voltage at MONB exceeds value | 1.05 | 1.2 | 1.45 | V |

(1) The bias current can be set below the specified minimum according to the corresponding register setting described in the register mapping section above, however in closed loop operation settings below the specified value may trigger a fault.
(2) Assured by simulation over process, supply, and temperature variation.

## AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions with 50-Ω output load, open loop operation, $I_{MOD}$ = 6 mA, $I_{BIAS}$ = 5 mA, and $R_{RZTC}$ = 30 kΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP (1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{R-OUT}$ | Output rise time | 20%–80%, $t_{R-IN}$ = 160 ps, single-ended $V_{IN}$ > 400 $mV_{pp}$ | | 60 | 125 | ps |
| | | 20%–80%, $t_{R-IN}$ = 100 ps, single-ended $V_{IN}$ > 400 $mV_{pp}$ | | 35 | 100 | |
| $t_{F-OUT}$ | Output fall time | 20%–80%, $t_{F-IN}$ = 160 ps, single-ended $V_{IN}$ > 400 $mV_{pp}$ | | 60 | 125 | ps |
| | | 20%–80%, $t_{F-IN}$ = 100 ps, single-ended $V_{IN}$ > 400 $mV_{pp}$ | | 35 | 100 | |
| $I_{MOD-MAX}$ | Maximum modulation current | Control bit MODR = 1, 50-Ω load | 11.5 | | | mA |
| | | Control bit MODR = 0, 50-Ω load | 9 | | | |
| $I_{MOD-STEP}$ | Modulation current step size | Control bit MODR = 1, 50-Ω load | | 68 | | µA |
| | | Control bit MODR = 0, 50-Ω load | | 51 | | |
| DJ | Deterministic output jitter | $f_{BIT}$ = 4.25 Gbps, excluding DJ caused by duty cycle distortion | | 7 | 20 | $ps_{p-p}$ |
| DCD | Duty cycle distortion | $f_{BIT}$ = 4.25 Gbps | | 8 | | $ps_{p-p}$ |

(1) Typical operating condition is at $V_{CC}$ = 3.3 V and $T_A$ = 25°C.

## AC ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions with 50-Ω output load, open loop operation, $I_{MOD}$ = 6 mA, $I_{BIAS}$ = 5 mA, and $R_{RZTC}$ = 30 kΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\tau_{APC}$ | APC time constant | $C_{APC}$ 0.01 µF, $I_{PD}$ = 100 µA, PD coupling ratio CR = 1/40(2) | | 200 | | µs |
| $T_{OFF}$ | Transmitter disable time | Rising edge of DIS to $I_{BIAS} \leq 0.1 \times I_{BIAS\text{-}NOMINAL}$(2) | | 2.4 | 5 | µs |
| $T_{ON}$ | Disable negate time | Falling edge of DIS to $I_{BIAS} \geq 0.9 \times I_{BIAS\text{-}NOMINAL}$(2) | | | 1 | ms |
| $T_{INIT1}$ | Power-on to initialize | Power-on to registers ready to be loaded | | 20 | 250 | ms |
| $T_{INIT2}$ | Initialize to transmit | Register load STOP command to part ready to transmit valid data(2) | | | 2 | ms |
| $T_{RESET}$ | DIS pulse width | Time DIS must held high to reset part(2) | 100 | | | ns |
| $T_{FAULT}$ | Fault assert time | Time from fault condition to FLT high(2) | | | 50 | µs |

(2) Assured by simulation over process, supply, and temperature variation.

## TYPICAL CHARACTERISTICS

Typical operating condition is at $V_{CC}$ = 3.3 V and $T_A$ = 25°C (unless otherwise noted)

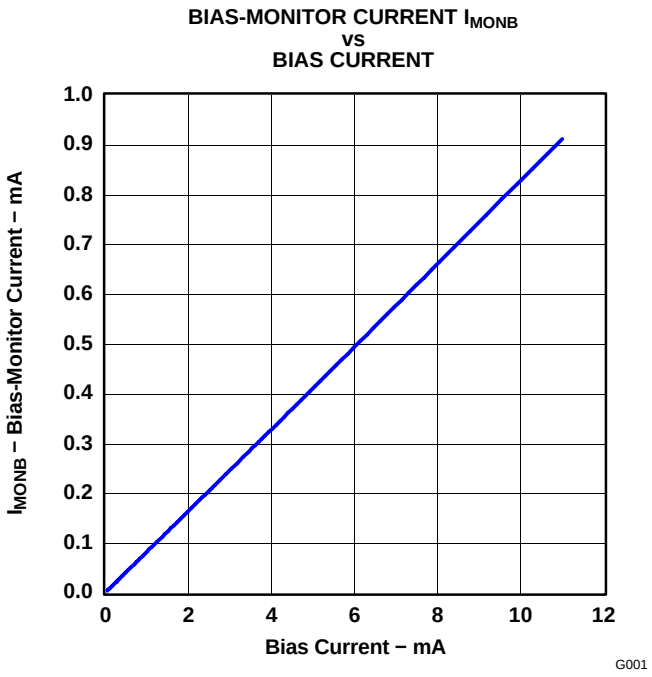
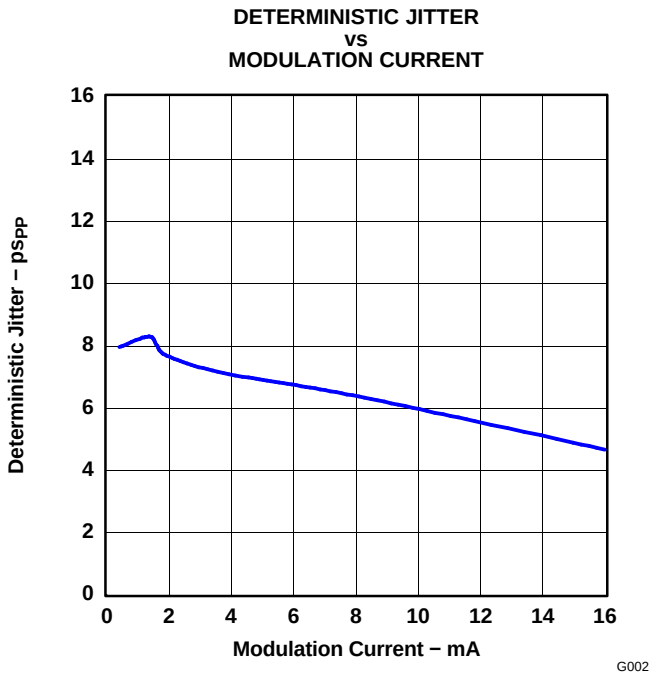



Figure 5.

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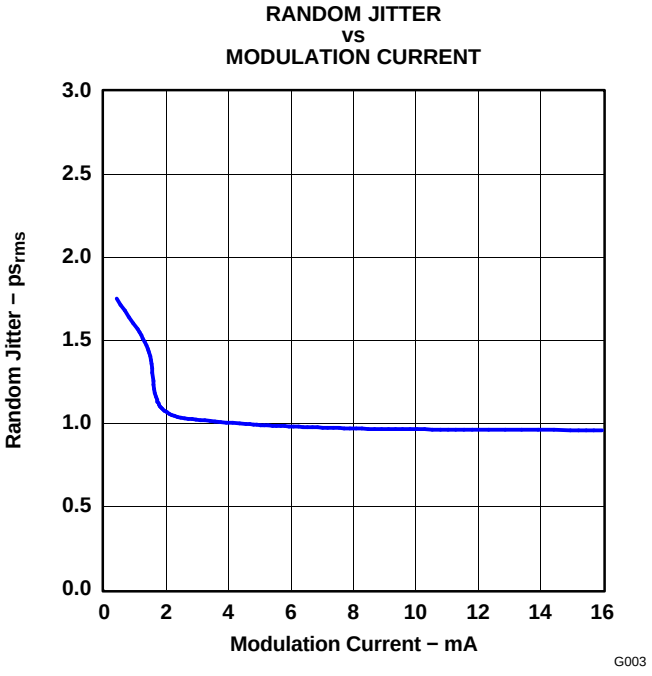



Figure 7.

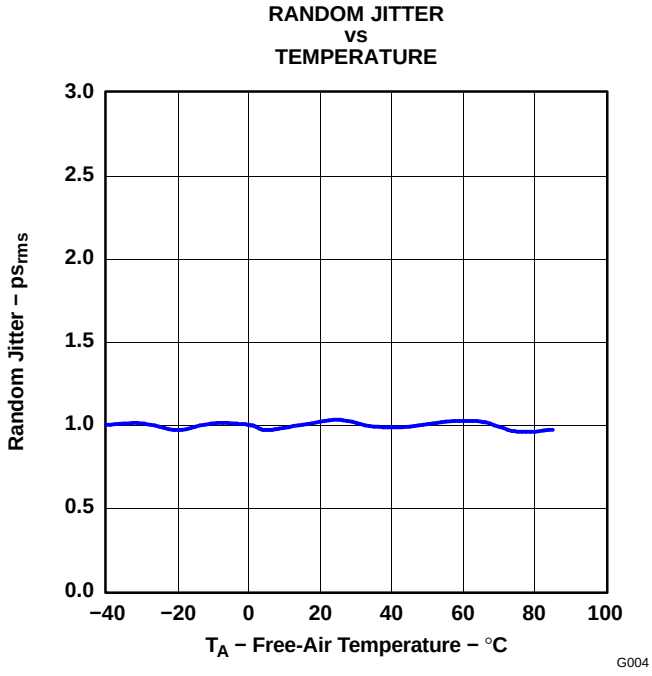



Figure 8.

## TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC}$ = 3.3 V and $T_A$ = 25°C (unless otherwise noted)

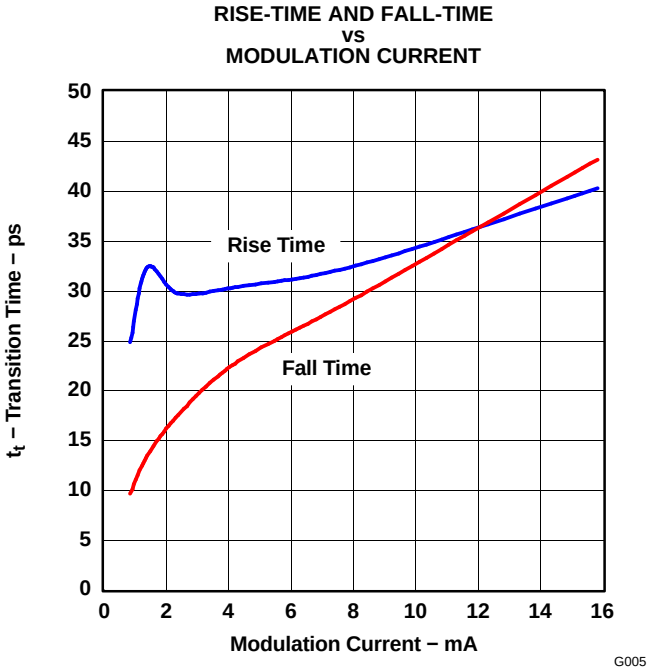



Figure 9.

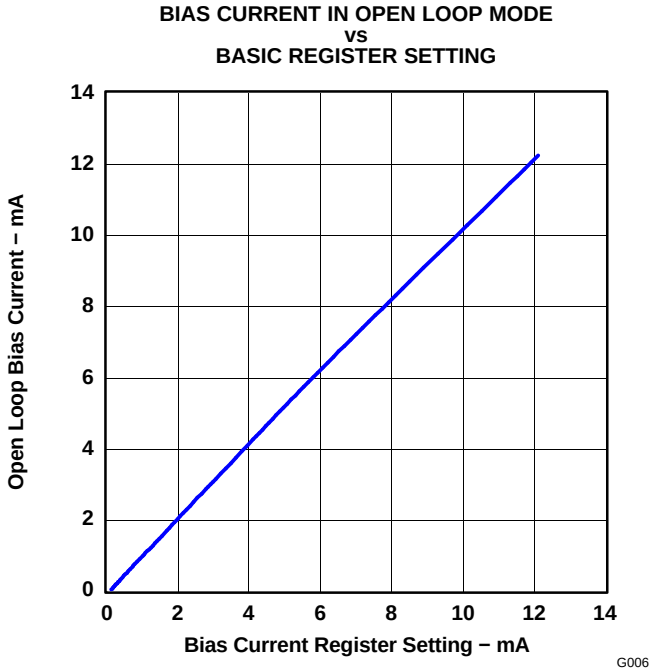



Figure 10.

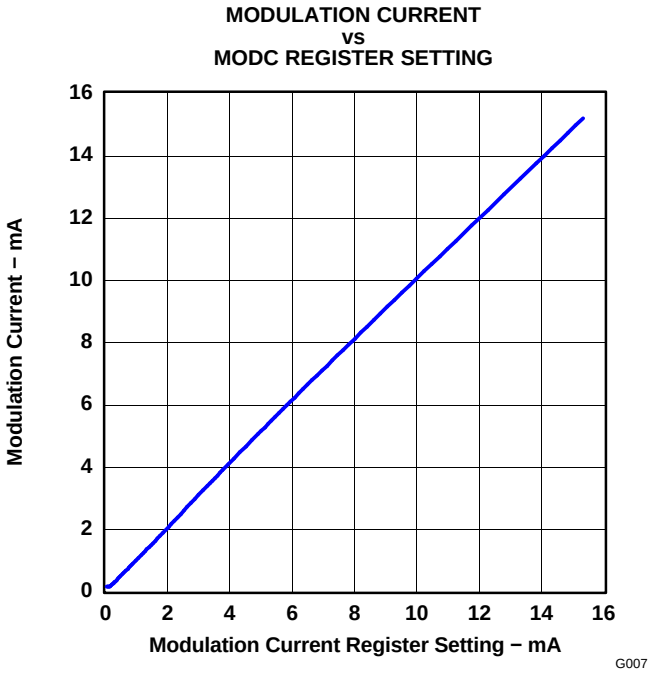



Figure 11.

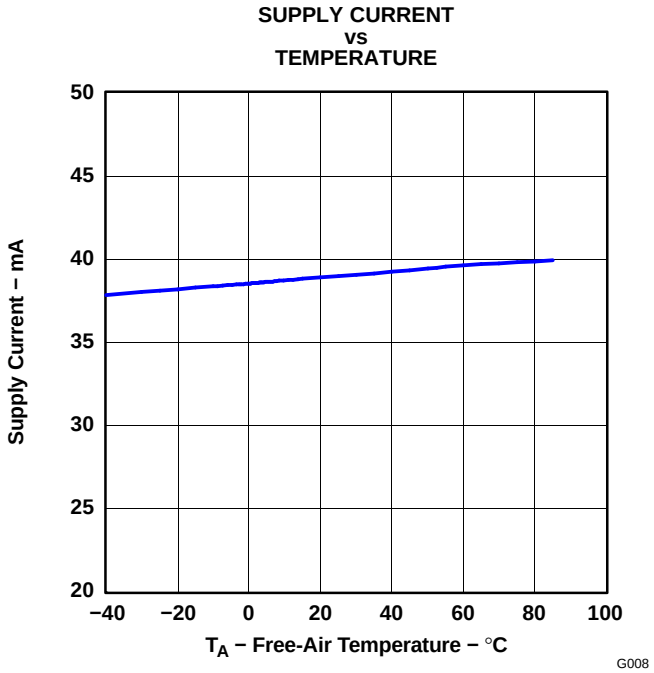



Figure 12.

## TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC}$ = 3.3 V and $T_A$ = 25°C (unless otherwise noted)

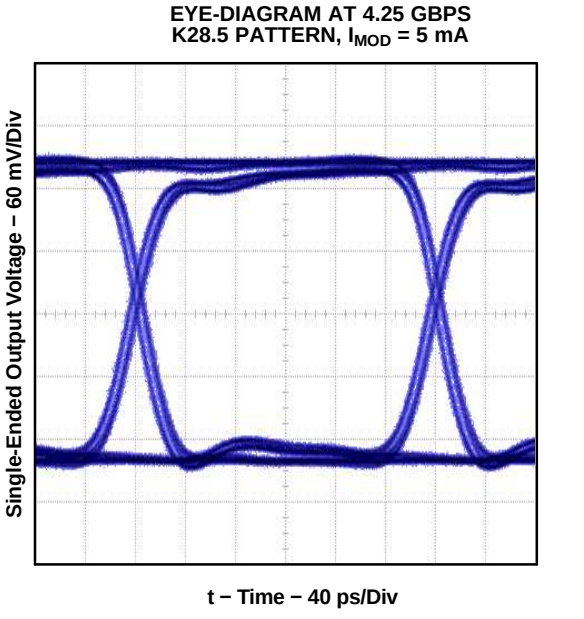



Figure 13.

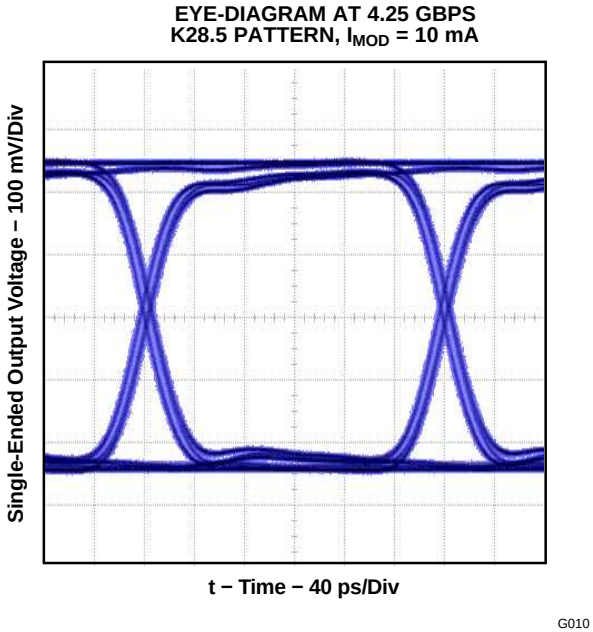



Figure 14.

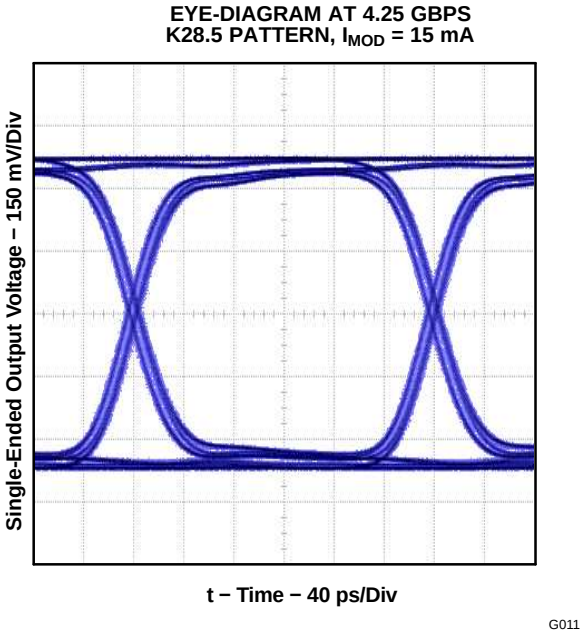



Figure 15.

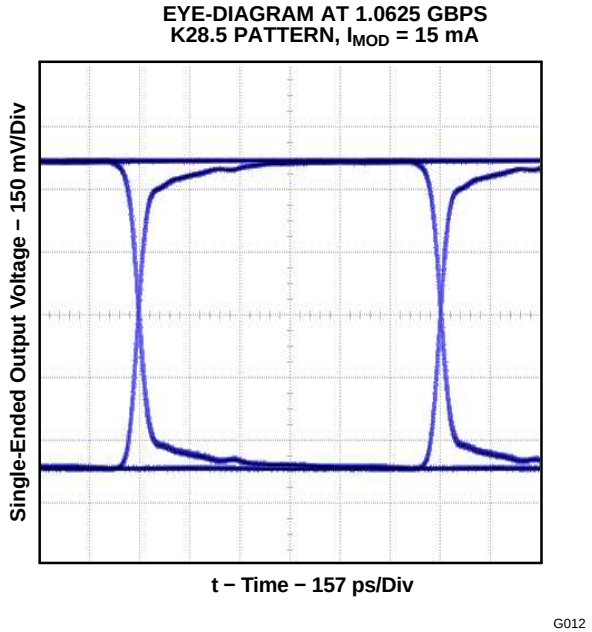



Figure 16.

## APPLICATION INFORMATION

Figure 17 shows a typical application circuit using the ONET4291VA with a common cathode VCSEL connected to ground.

The VCSEL driver is controlled via the 2-wire interface SDA/SCK by a microprocessor.

In a typical application, the FLT, MONB, MONP, and TS outputs are connected to the microcontroller for transceiver management purposes.

The component values in Figure 17 are typical examples and may be varied according to the intended application.

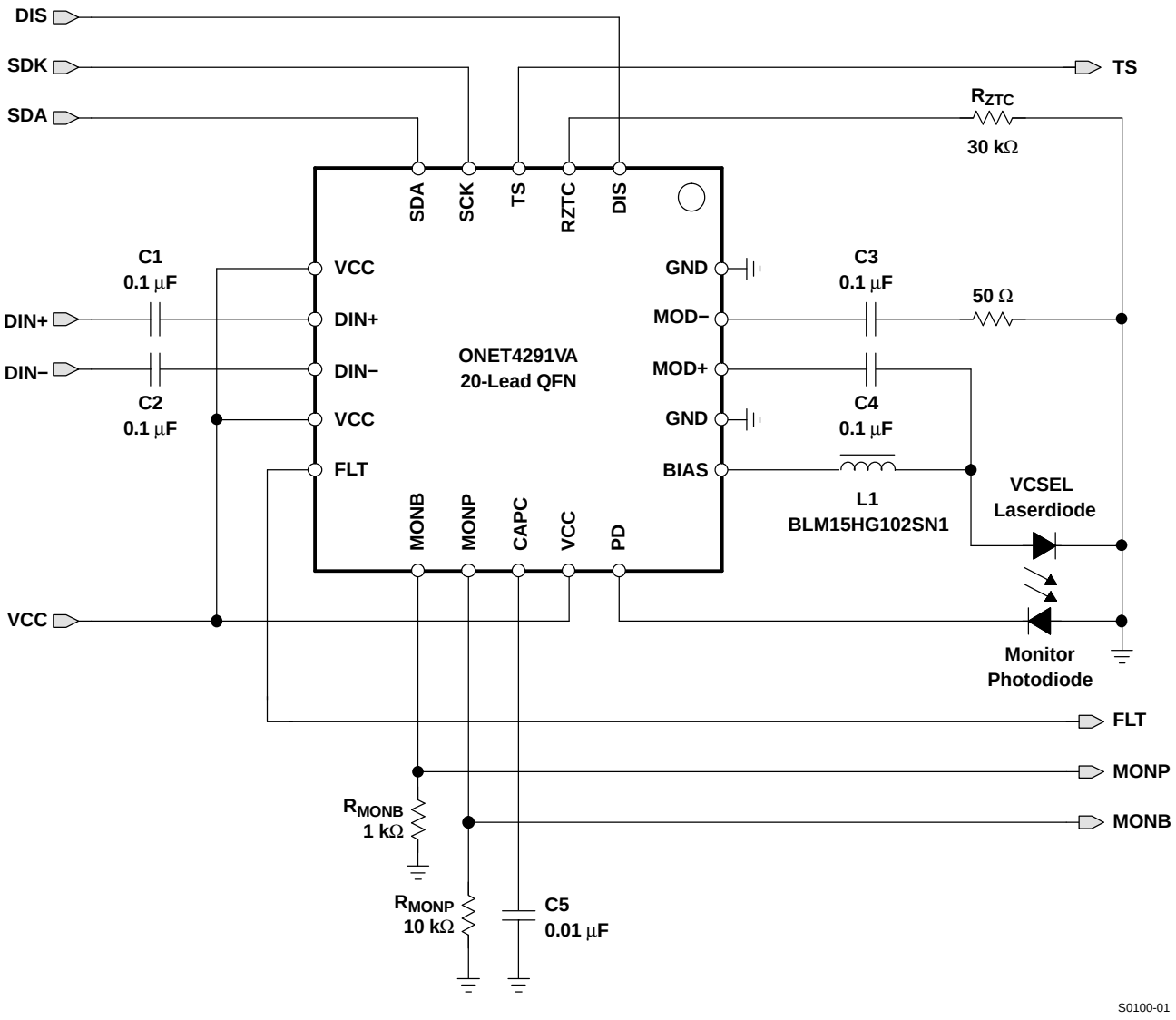



**Figure 17. Basic Application Circuit With a Common Cathode VCSEL**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ONET4291VARGPR | ACTIVE | QFN | RGP | 20 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | ONET 4291V | Samples |
| ONET4291VARGPRG4 | ACTIVE | QFN | RGP | 20 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | ONET 4291V | Samples |
| ONET4291VARGPT | ACTIVE | QFN | RGP | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | ONET 4291V | Samples |
| ONET4291VARGPTG4 | ACTIVE | QFN | RGP | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | ONET 4291V | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

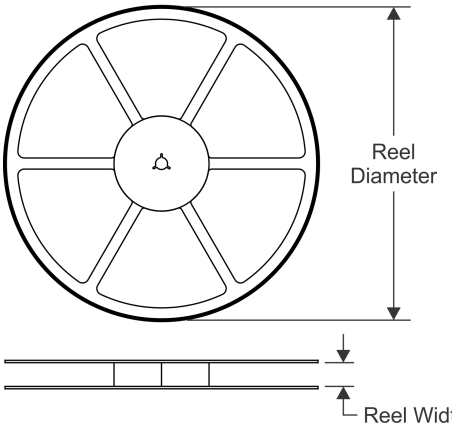
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

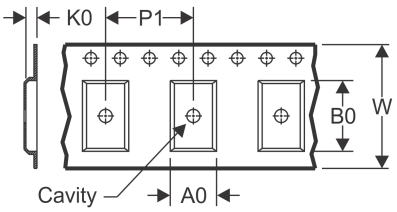
(4) Only one of markings shown within the brackets will appear on the physical device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

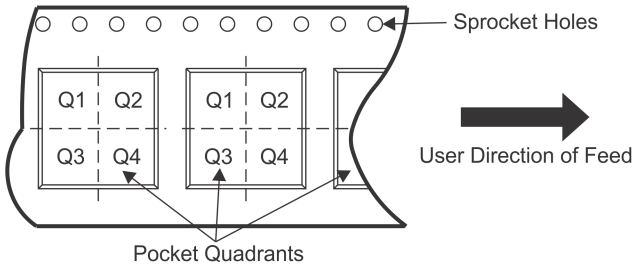



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

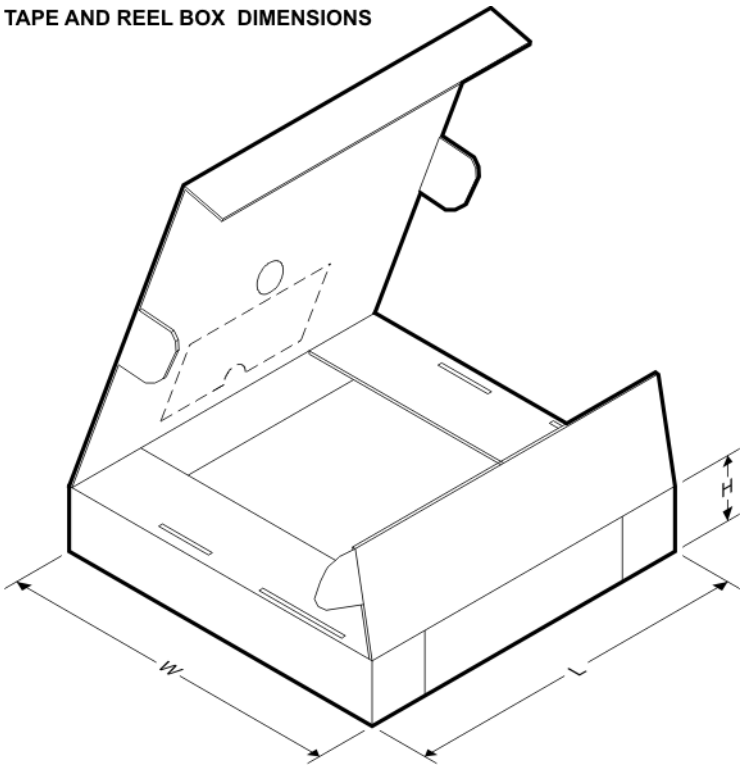
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ONET4291VARGPR | QFN | RGP | 20 | 2500 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| ONET4291VARGPT | QFN | RGP | 20 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

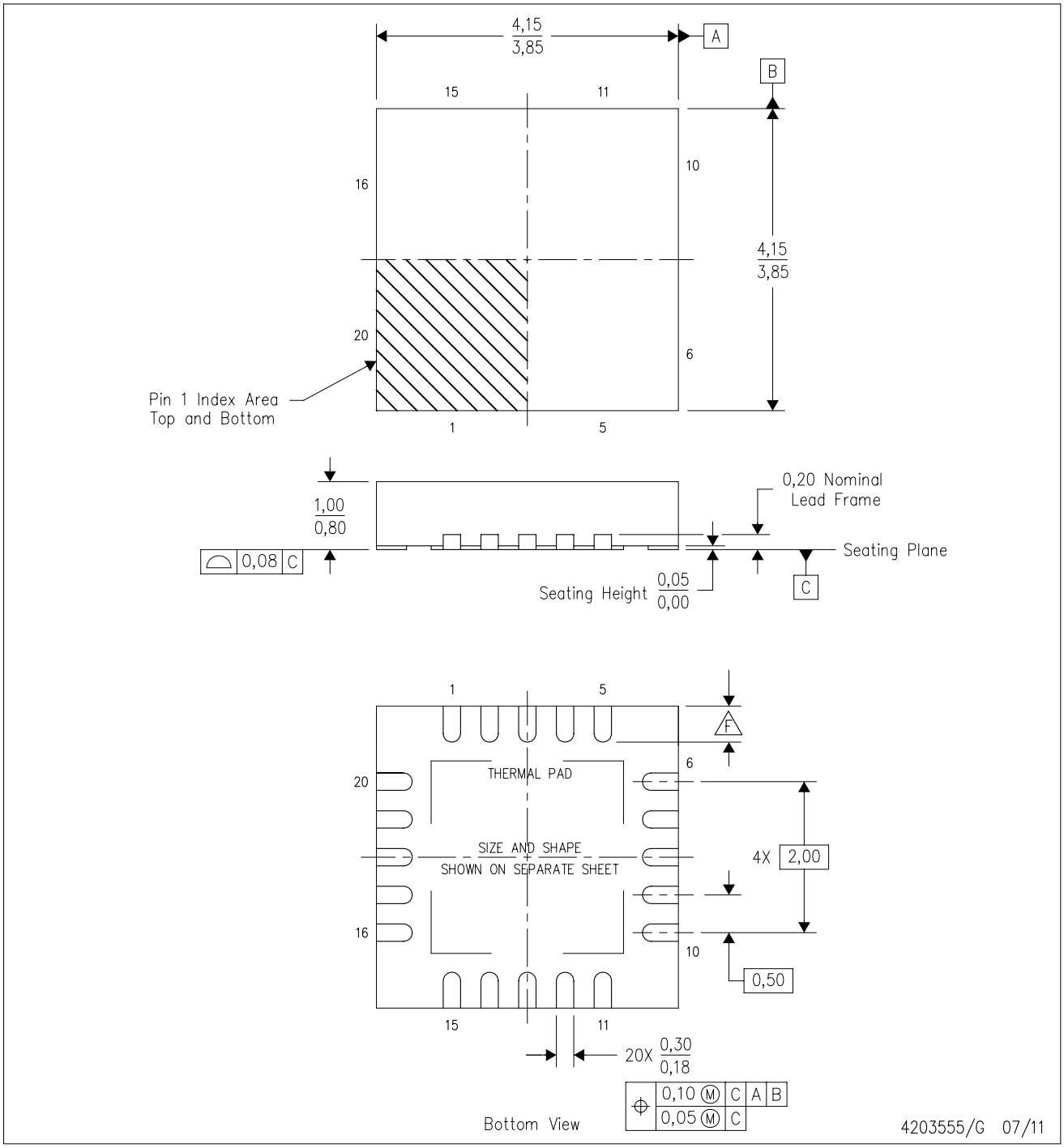
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ONET4291VARGPR | QFN | RGP | 20 | 2500 | 367.0 | 367.0 | 35.0 |
| ONET4291VARGPT | QFN | RGP | 20 | 250 | 210.0 | 185.0 | 35.0 |

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

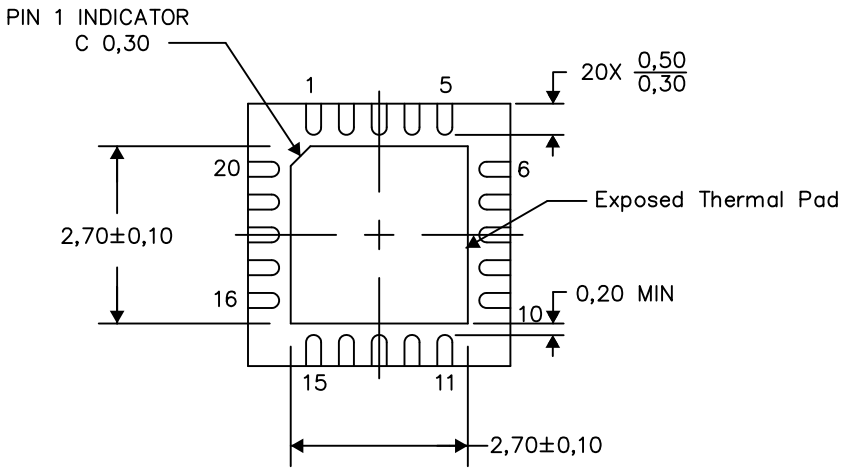
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



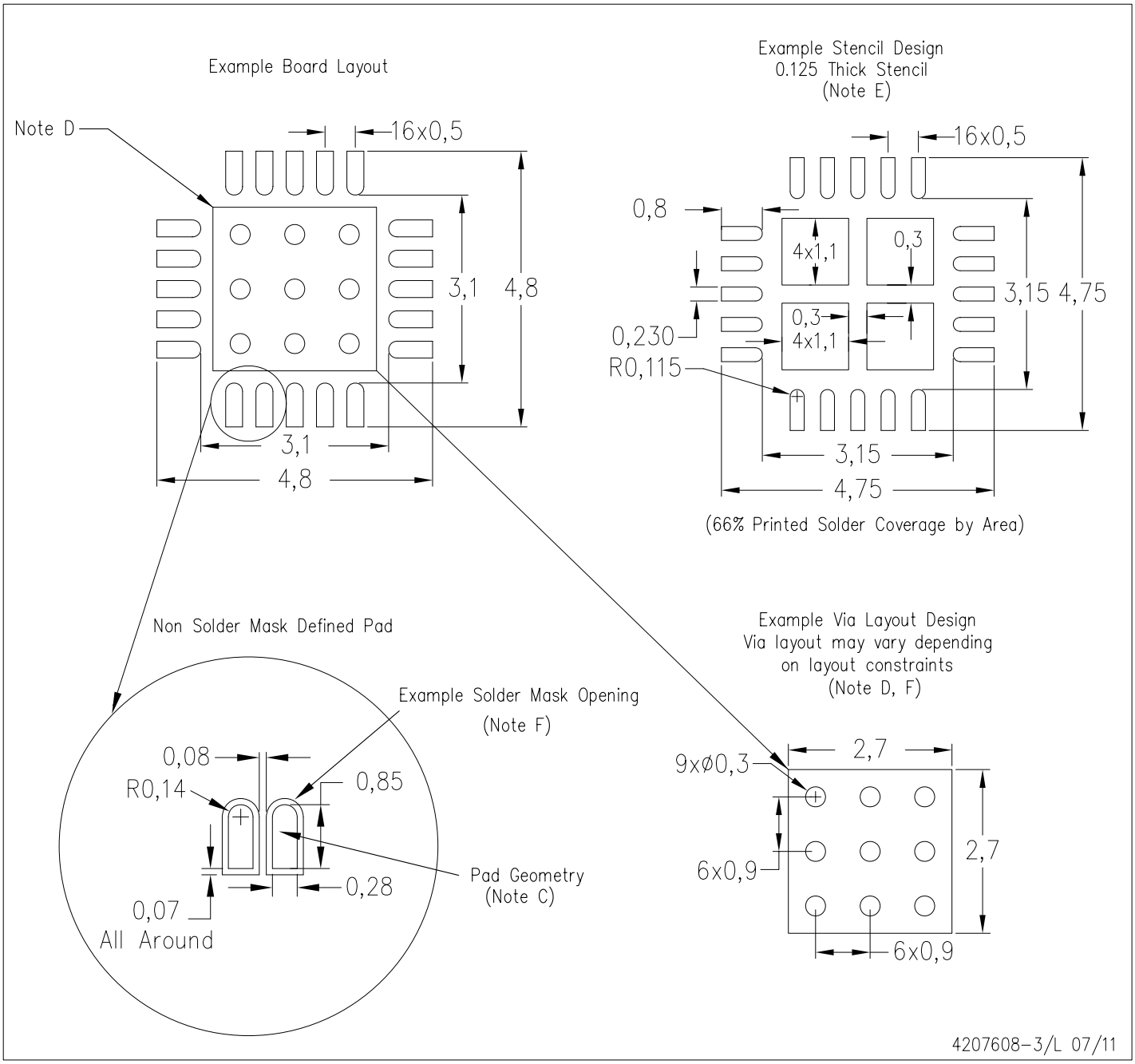

Bottom View

Exposed Thermal Pad Dimensions

4206346–3/Y 12/12

NOTES: A. All linear dimensions are in millimeters

# RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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