

P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)
- 30	0.0056 at V _{GS} = - 10 V	- 50 ^e	45 nC
	0.0070 at V _{GS} = - 6 V	- 50 ^e	
	0.0090 at V _{GS} = - 4.5 V	- 50 ^e	

FEATURES

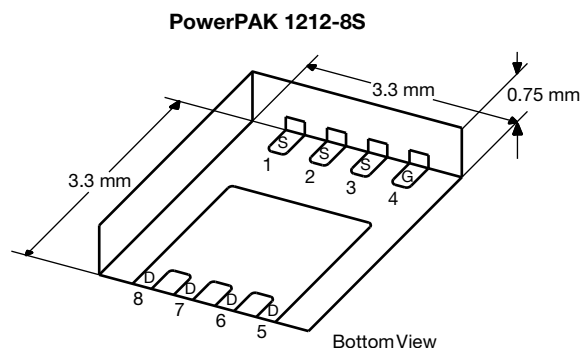
- TrenchFET® Power MOSFET
- Low Thermal Resistance PowerPAK® Package with Small Size and Low 0.75 mm Profile
- 100 % R_g and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



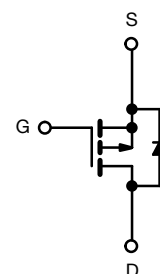
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Notebook Computers and Mobile Computing
 - Adaptor Switch
 - Load Switch
 - DC/DC Converter
 - Power Management



Ordering Information:
SiSS27DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	- 30	V	
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	- 50 ^e	A	
	T _C = 70 °C		- 50 ^e		
	T _A = 25 °C		- 23 ^{a, b}		
	T _A = 70 °C		- 18.5 ^{a, b}		
Pulsed Drain Current (t = 100 μs)		I _{DM}	- 200		
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	- 47.5		
	T _A = 25 °C		- 4 ^{a, b}		
Avalanche Current	L = 0.1 mH	I _{AS}	- 25		
Single-Pulse Avalanche Energy		E _{AS}	31	mJ	
Maximum Power Dissipation	T _C = 25 °C	P _D	57	W	
	T _C = 70 °C		36		
	T _A = 25 °C		4.8 ^{a, b}		
	T _A = 70 °C		3 ^{a, b}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 50 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{c, d}			260		

Notes:

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Package limited.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	21	26	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.7	2.2	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. Maximum under steady state conditions is 63 °C/W.

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 22		mV/ °C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			5.7		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1		- 2.2	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 30 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 30 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 10 V	- 20			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 15 A		0.0046	0.0056	Ω
		V _{GS} = - 6 V, I _D = - 10 A		0.0058	0.0070	
		V _{GS} = - 4.5 V, I _D = - 5 A		0.0073	0.0090	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 15 V, I _D = - 15 A		52		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz		5250		pF
Output Capacitance	C _{oss}			530		
Reverse Transfer Capacitance	C _{rss}			485		
Total Gate Charge	Q _g	V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 20 A		92	140	nC
				45	70	
		V _{DS} = - 15 V, V _{GS} = - 4.5 V, I _D = - 20 A		15		
				16		
Gate-Source Charge	Q _{gs}					
Gate-Drain Charge	Q _{gd}					
Gate Resistance	R _g	f = 1 MHz	0.6	3	6	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 15 V, R _L = 1.5 Ω I _D ≅ - 10 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		60	120	ns
Rise Time	t _r			45	90	
Turn-Off DelayTime	t _{d(off)}			50	100	
Fall Time	t _f			20	40	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 15 V, R _L = 1.5 Ω I _D ≅ - 10 A, V _{GEN} = - 10 V, R _g = 1 Ω		16	30	
Rise Time	t _r			5	10	
Turn-Off DelayTime	t _{d(off)}			65	130	
Fall Time	t _f			10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 50 ^c	A
Pulse Diode Forward Current ^d	I _{SM}				- 200	
Body Diode Voltage	V _{SD}	I _F = - 10 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 10 A, di/dt = 100 A/μs, T _J = 25 °C		30	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			21	40	nC
Reverse Recovery Fall Time	t _a			16		ns
Reverse Recovery Rise Time	t _b			14		

Notes:

a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.

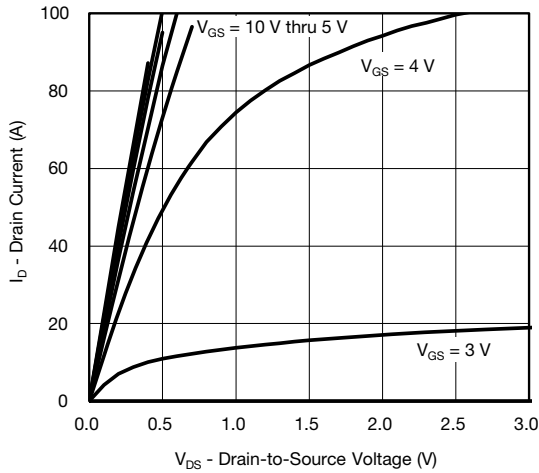
b. Guaranteed by design, not subject to production testing.

c. Package limited.

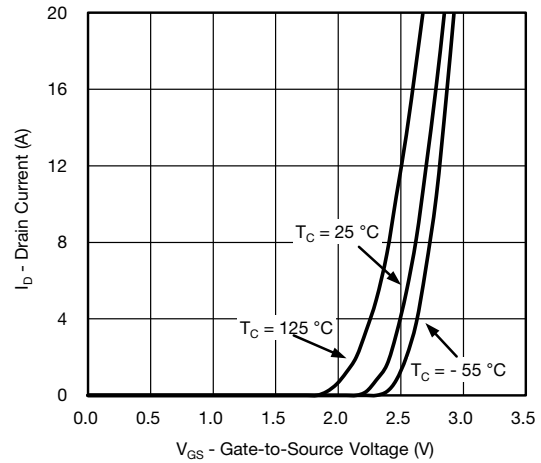
d. $t = 100$ μ s.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

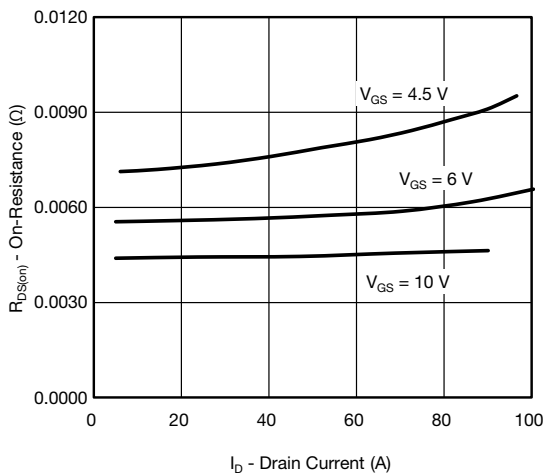
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



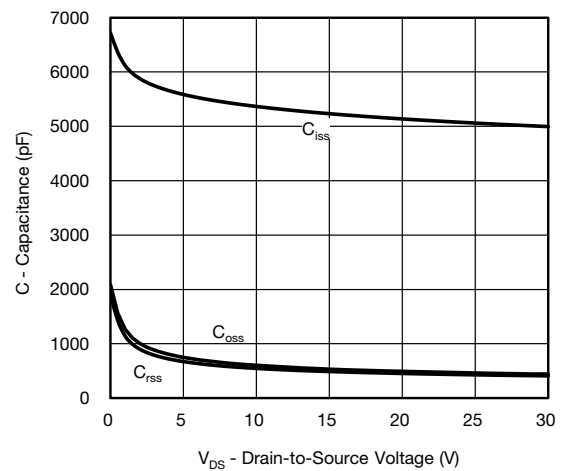
Output Characteristics



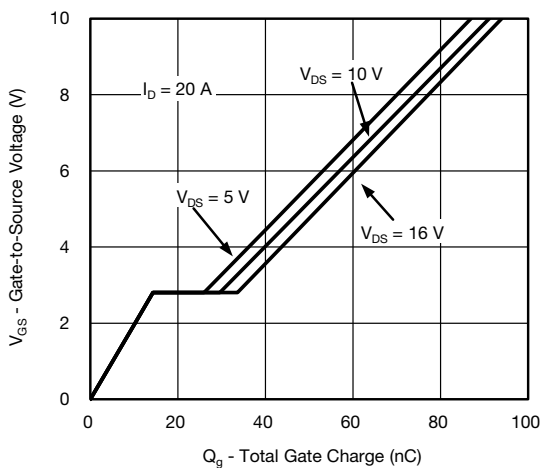
Transfer Characteristics



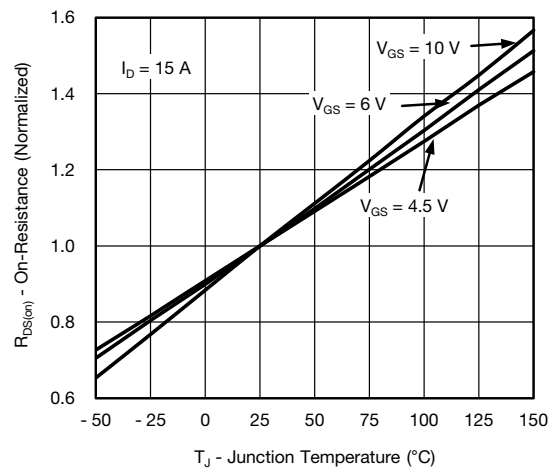
On-Resistance vs. Drain Current and Gate Voltage



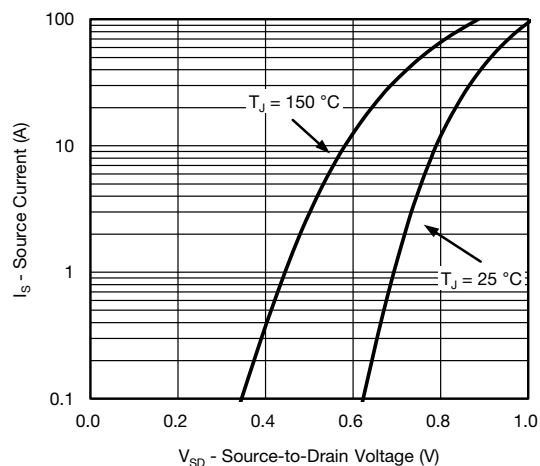
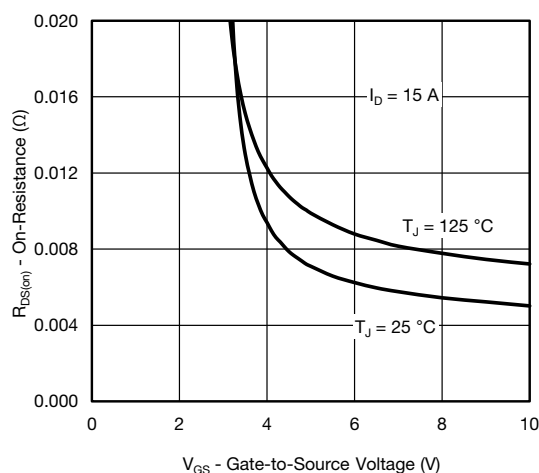
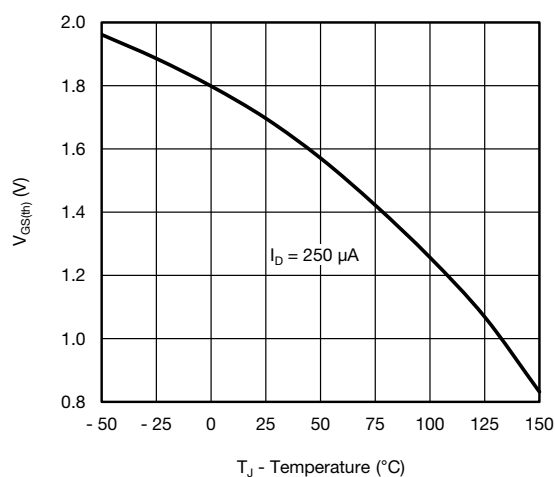
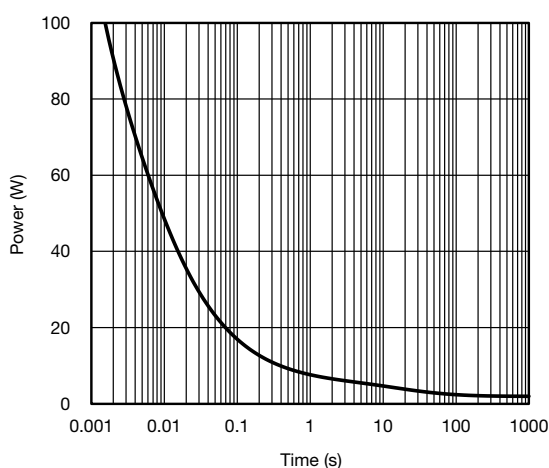
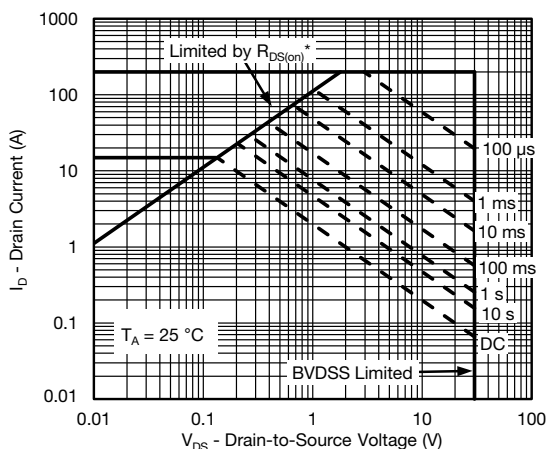
Capacitance

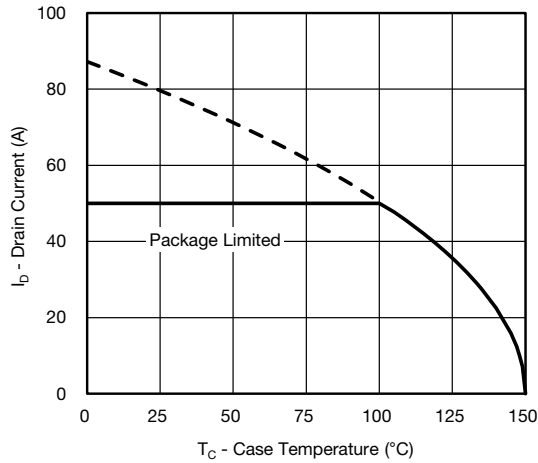
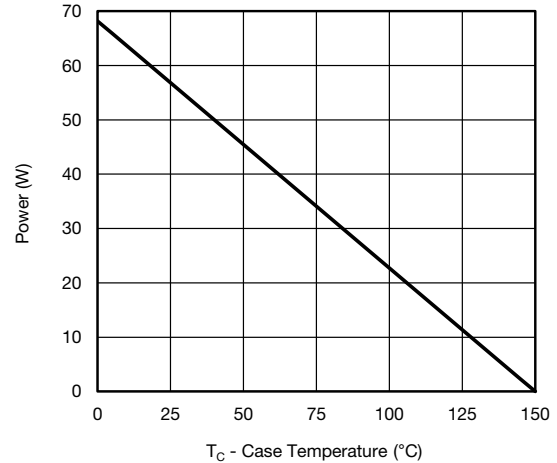


Gate Charge

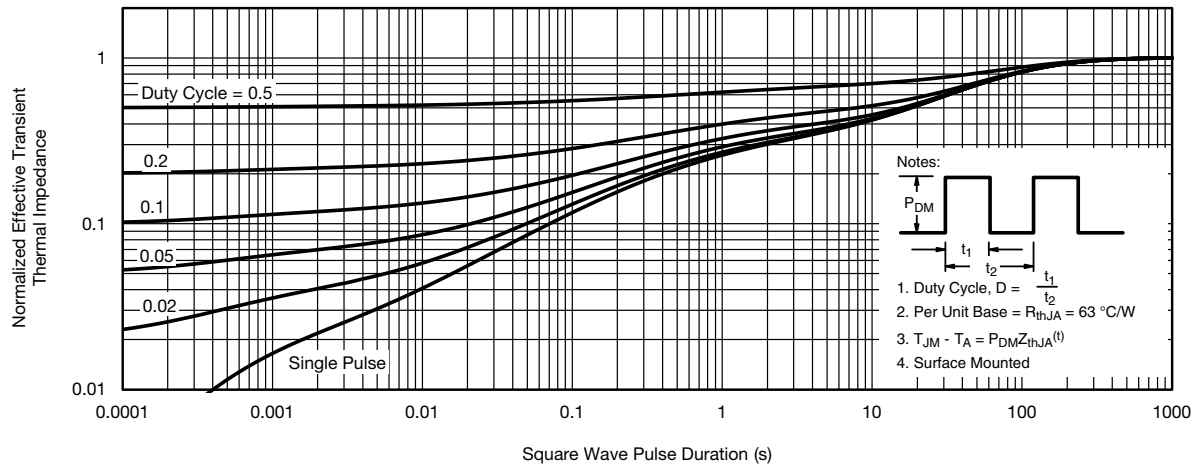


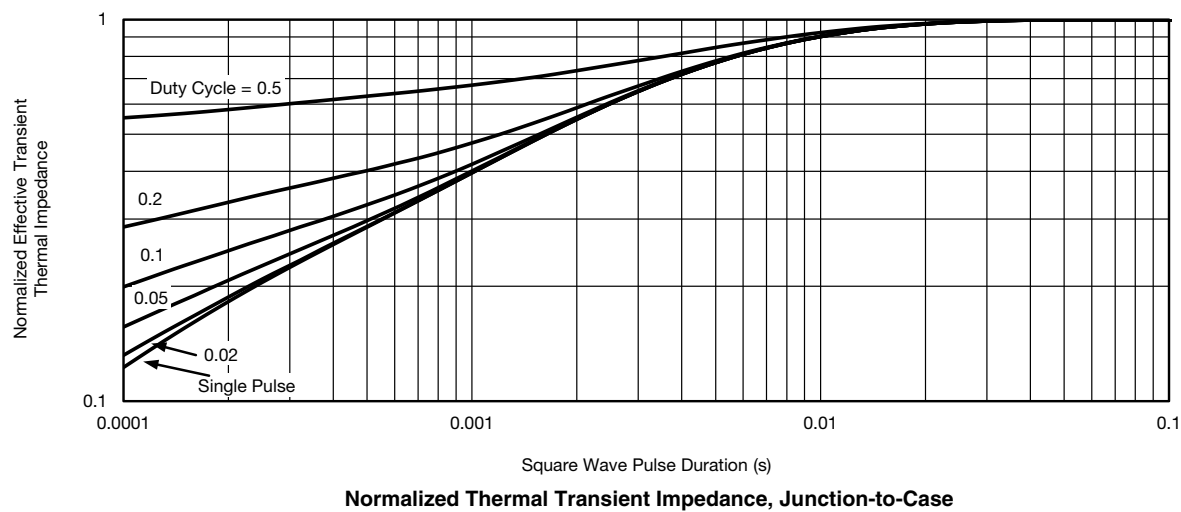
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating*

Power, Junction-to-Case

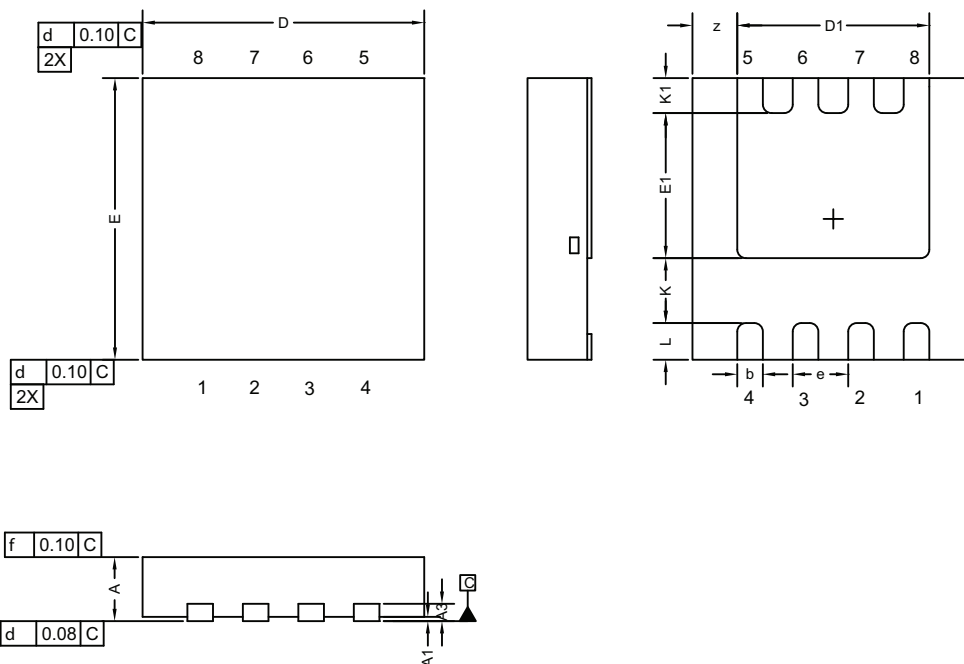
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.


Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

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Case Outline for PowerPAK® 1212-8S

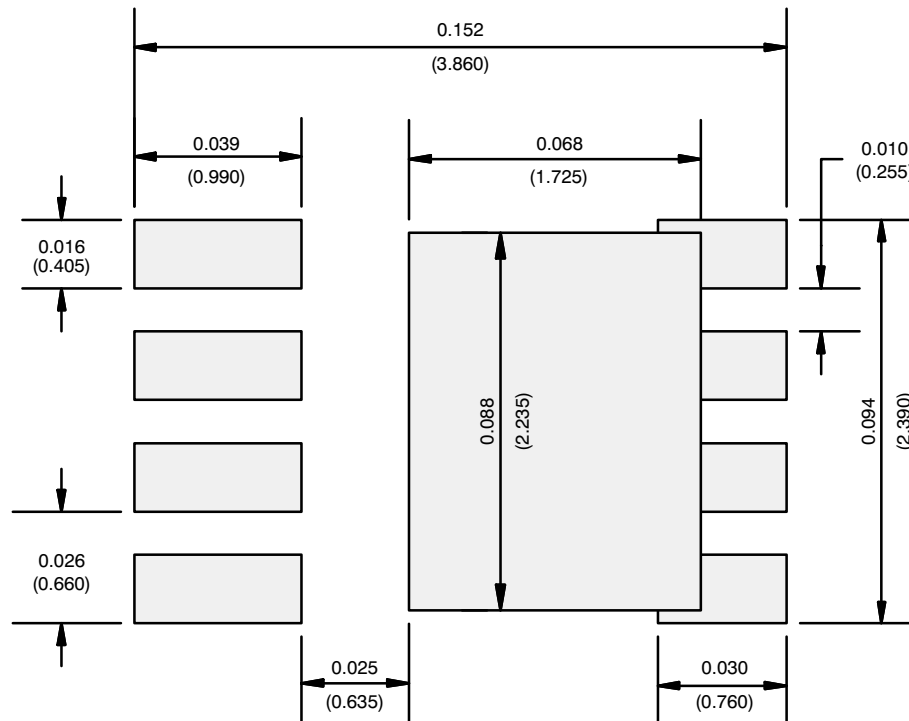


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.67	0.75	0.83	0.027	0.030	0.033
A1	0	-	0.05	0	-	0.002
A3	0.20 REF			0.008 REF		
b	0.30 BSC			0.012 BSC		
D	3.30 BSC			0.130 BSC		
D1	2.15	2.25	2.35	0.084	0.088	0.092
E	3.30 BSC			0.130 BSC		
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 BSC			0.026 BSC		
K	0.76 TYP			0.030 TYP		
K1	0.41 TYP			0.016 TYP		
L	0.43 BSC			0.017 BSC		
z	0.525 TYP			0.021 TYP		
ECN: C12-0200-Rev. A, 12-Mar-12 DWG: 6008						

Note

- Millimeters will govern.

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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