

Output Coupling Capacitor-less Line Amplifier

BD8876FV, BD8878FV

Description

BD8876FV, BD8878FV are output coupling capacitor-less line amplifiers. These IC have a negative voltage generator built-in and generate the negative voltage from the supply voltage. It is possible to drive in a ground reference with both voltage of the supply voltage and the negative voltage. Therefore, these line amplifiers have wide output range, and they can output 2Vrms(5.65V_{P-P}) with the single-supply 5V.

Features

- Possible to output 2Vrms with single-supply 5V
- Output Coupling Capacitor-less
- Variable Gain (+6dB / +9dB Typ.) [BD8876FV]
- Fixed Gain (+6.7dB Typ.) [BD8878FV]
- Integrated Negative Power Supply
- Ground-Referenced Outputs
- Integrated Short-Circuit and Thermal Protection

Applications

Video game console, Projector, Set Top Box, Blu-ray player etc.

Typical Application Circuit

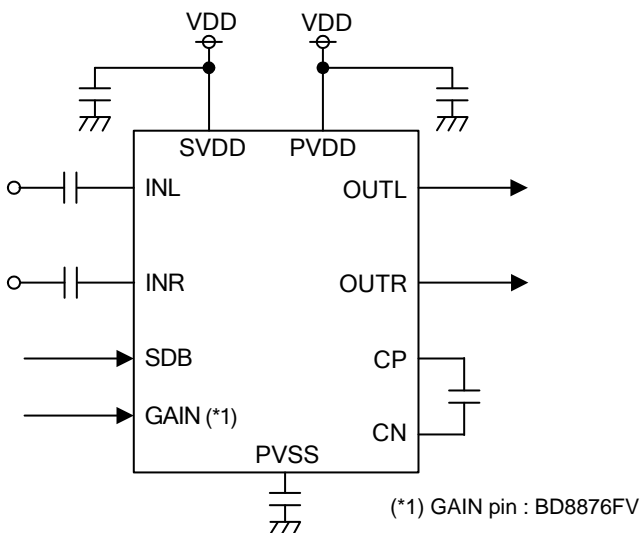


Figure 1. Typical Application Circuit

Key Specifications

- Power Supply voltage: 3V to 5.5V
- THD+N: 0.003% (Typ)
(V_{CC}=5V, R_L=10kΩ, V_o=2Vrms, 20kHz LPF)
- Maximum Output Voltage: 2Vrms (Min)@V_{CC}=5V
- Output Noise: 10μVrms (Typ)
- Circuit Current (Active): 3.2mA (Typ)
- Operating Temperature Range: -40°C to +85°C

Package

SSOP-B14

W(Typ) x D(Typ) x H(Max)
5.00mm x 6.40mm x 1.35mm



	BD8876FV	BD8878FV
Amplifier type	Inverting amplifier	Non-inverting amplifier
Gain	+6.0dB / +9.0dB (Changed by GAIN pin)	+6.7dB
Package	SSOP-B14	

Pin Configurations

(TOP VIEW)

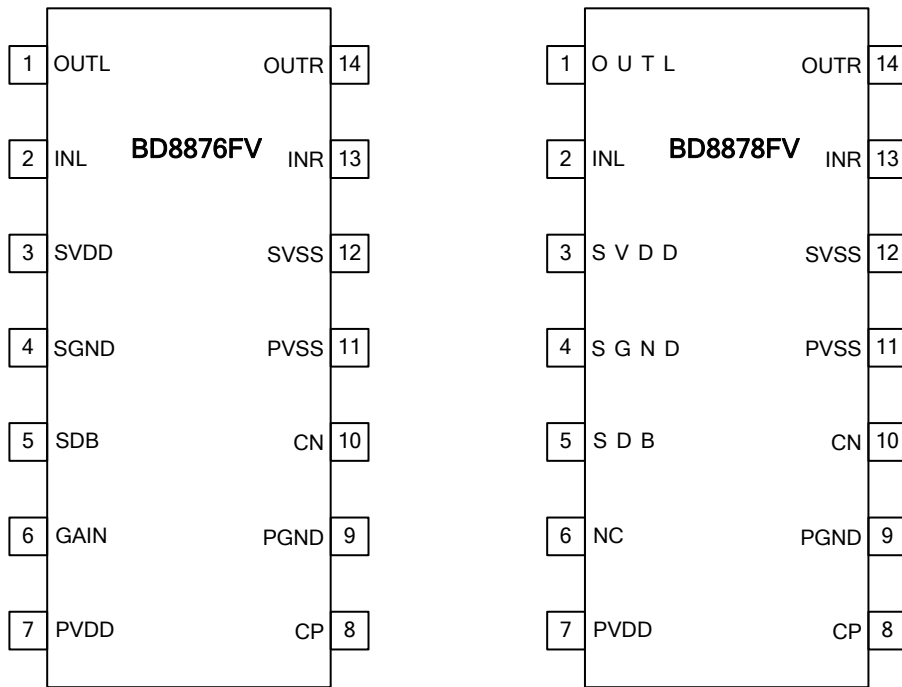
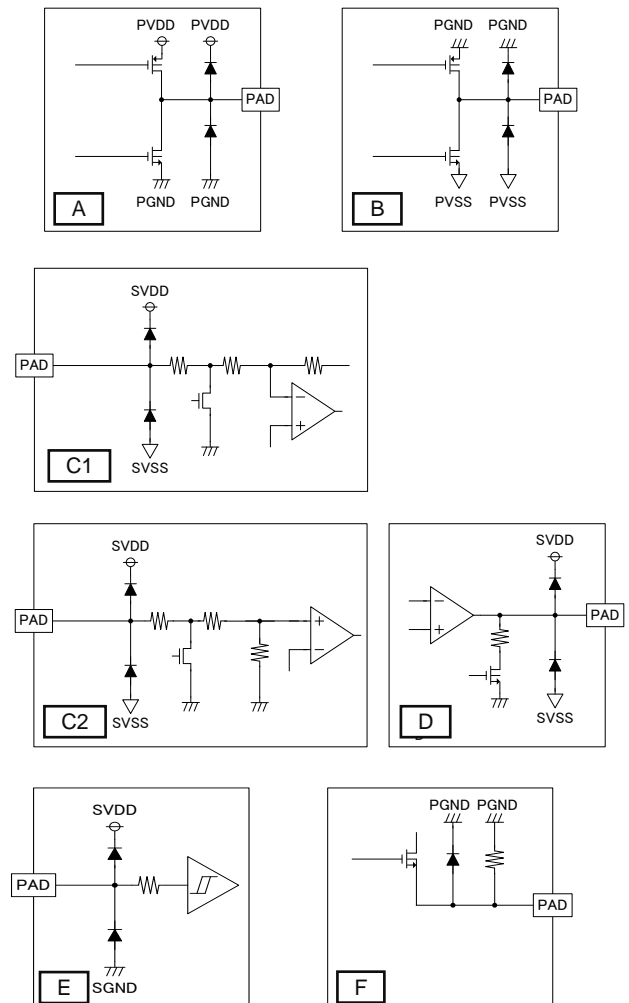


Figure 2. Pin Configurations

Pin Description/Function

PIN No.	Pin name	Function	Equivalence Circuit
1	OUTL	Line amplifier (Lch) output	D
2	INL	Line amplifier (Lch) input	C1 (BD8876FV) C2 (BD8878FV)
3	SVDD	Line amplifier supply voltage	-
4	SGND	Line amplifier ground	-
5	SDB	Shutdown control (H: active, L: shutdown)	E
6	GAIN (BD8876FV) NC (BD8878FV)	Gain control (H: 9.0dB, L: 6.0dB) No Connection	E -
7	PVDD	Charge pump supply voltage	-
8	CP	Flying capacitor positive terminal	A
9	PGND	Charge pump ground	-
10	CN	Flying capacitor negative terminal	B
11	PVSS	Charge pump output voltage	F
12	SVSS	Line amplifier negative supply input	F
13	INR	Line amplifier (Rch) input	C1 (BD8876FV) C2 (BD8878FV)
14	OUTR	Line amplifier (Rch) output	D

Equivalence Circuit



Block Diagrams

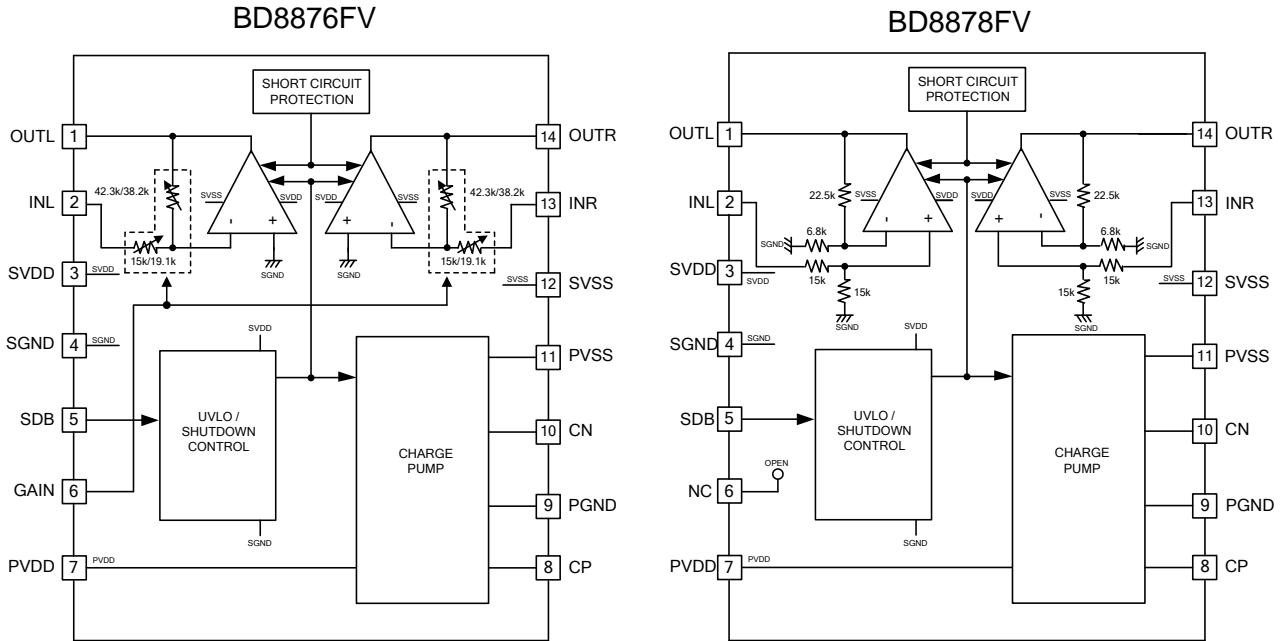


Figure 3. Block Diagrams

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
SVDD-PVDD Voltage	V_{DD}	0	V
SGND-PGND Voltage	V_{GG}	0	V
SVSS-PVSS Voltage	V_{SS}	0	V
SVDD, PVDD-SGND or PGND Voltage	V_{DG}	-0.3~6.0	V
SVSS, PVSS-SGND or PGND Voltage	V_{SG}	-6.0~0.3	V
IN_-SGND Voltage	V_{IN}	(SVSS-0.3)~(SVDD+0.3)	V
OUT_-SGND Voltage	V_{OUT}	(SVSS-0.3)~(SVDD+0.3)	V
CP-PGND Voltage	V_{CP}	(PGND-0.3)~(PVDD+0.3)	V
CN-PGND Voltage	V_{CN}	(PVSS-0.3)~(PGND+0.3)	V
SDB-SGND Voltage	V_{SH}	(SGND-0.3)~(SVDD+0.3)	V
GAIN-SGND Voltage	V_{GA}	(SGND-0.3)~(SVDD+0.3)	V
Input current	I_{IN}	-10~10	mA
Power Dissipation ^(NOTE 1)	P_D	0.87	W
Storage Temperature Range	T_{STG}	-55~+150	°C

(Note 1) Derate by 6.96mW/°C when operating above 25°C when mounted on 70mm x 70mm x 1.6mm, FR4.1-layer glass epoxy board.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Supply Voltage Range	V_{SVDD}, V_{PVDD}	3.0	-	5.5	V
Operating Temperature Range	T_{OPR}	-40	-	+85	°C
Minimum Load Impedance	Z_L	550	-	-	Ω

Electrical Characteristics

(Unless otherwise specified, Ta=25°C, SVDD=PVDD=5V, SGND=PGND=0V, SDB=H, GAIN=L [BD8876FV], C₁=C₂=1μF, R_L=10kΩ, Input coupling capacitor=1μF)

Parameter	Symbol	Limit						Unit	Remarks
		BD8876FV			BD8878FV				
		Min	Typ	Max	Min	Typ	Max		
Circuit current									
Circuit Current (Shutdown)	I _{ST}	-	0.1	2	-	0.1	2	μA	SDB=L
Circuit Current (Active)	I _{DD}	-	3.2	8.2	-	3.2	10.5	mA	SDB=H, No signal, RL=No load
SDB pin/GAIN pin									
H Level Input Voltage	V _{IH}	0.7 x SVDD	-	-	0.7 x SVDD	-	-	V	
L Level Input Voltage	V _{IL}	-	-	0.3 x SVDD	-	-	0.3 x SVDD	V	
Input Leak Current	I _{LEAK}	-	-	±1	-	-	±1	μA	
Line amplifier									
Start up time	t _{SON}	-	470	-	-	470	-	μsec	SDB=L→H
Offset Voltage	V _{IS}	-	±0.5	±5	-	±1	±10	mV	
Maximum Output Voltage	V _{OUT}	2.5	3.5	-	2.05	3.0	-	V _{rms}	f=1kHz, THD+N ≤ 40dB, 20kHz LPF
THD+N	THD+N	-	0.003	0.032	-	0.003	0.032	%	f=1kHz, V _{OUT} =2V _{rms} , 20kHz LPF
Input Impedance	Z _{IN1} ^{*1}	12	19	26	20	30	40	kΩ	*1 GAIN=L (6dB mode) *2 GAIN=H (9dB mode)
	Z _{IN2} ^{*2}	10	15	20					
Gain	A _{V1} ^{*1}	5.0	6.0	7.0	5.7	6.7	7.7	dB	*1 GAIN=L (6dB mode) *2 GAIN=H (9dB mode)
	A _{V2} ^{*2}	8.0	9.0	10.0					
Gain mismatch	ΔA _V	-	1	-	-	1	-	%	
Output Noise	V _N	-	8	-	-	10	-	μV _{rms}	20kHz LPF+A-Weight filter, R _g =0ohm
Slew Rate	SR	-	3.0	-	-	3.0	-	V/μsec	
Maximum Capacitive Load	C _L	-	-	250	-	-	250	pF	
Crosstalk	CT	-	-80	-	-	-65	-	dB	f=1kHz, V _{OUT} =200mV _{P-P} , 1kHz BPF
Power Supply Rejection Ratio	PSRR	-	-65	-	-	-65	-	dB	f=1kHz, V _{ripple} =100mV _{P-P} , 1kHz BPF
Charge-Pump Oscillator Frequency	f _{OSC}	150	300	450	150	300	450	kHz	

(Unless otherwise specified, $T_a=25^{\circ}\text{C}$, $\text{SVDD}=\text{PVDD}=5\text{V}$, $\text{SGND}=\text{PGND}=0\text{V}$, $\text{SDB}=\text{H}$, $\text{GAIN}=\text{L}$ [BD8876FV], $C_1=C_2=1\mu\text{F}$, $R_L=10\text{k}\Omega$, Input coupling capacitor= $1\mu\text{F}$) * SVDD, PVDD shows as "VDD" in the following graphs.

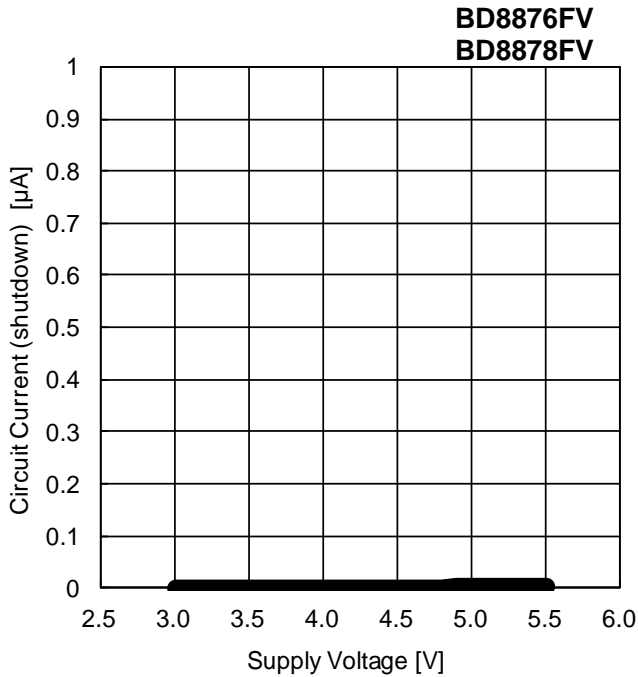


Figure 4.
Circuit Current (Shutdown)
vs. Supply Voltage

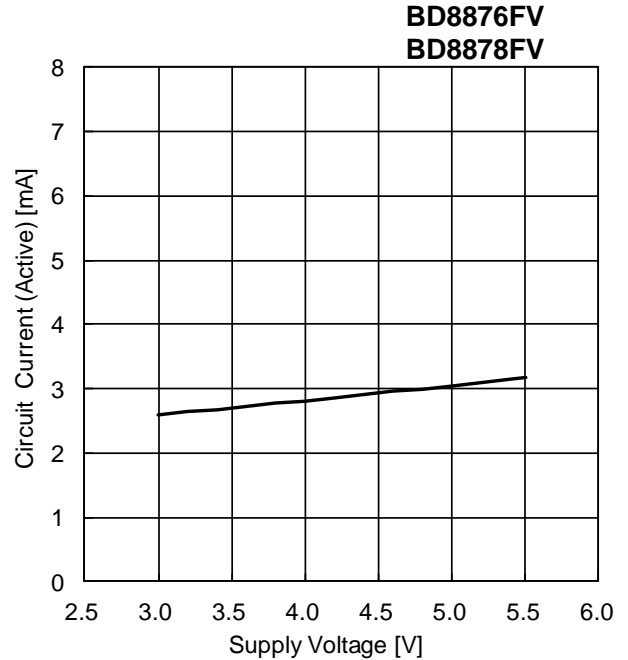


Figure 5.
Circuit Current (Active)
vs. Supply Voltage

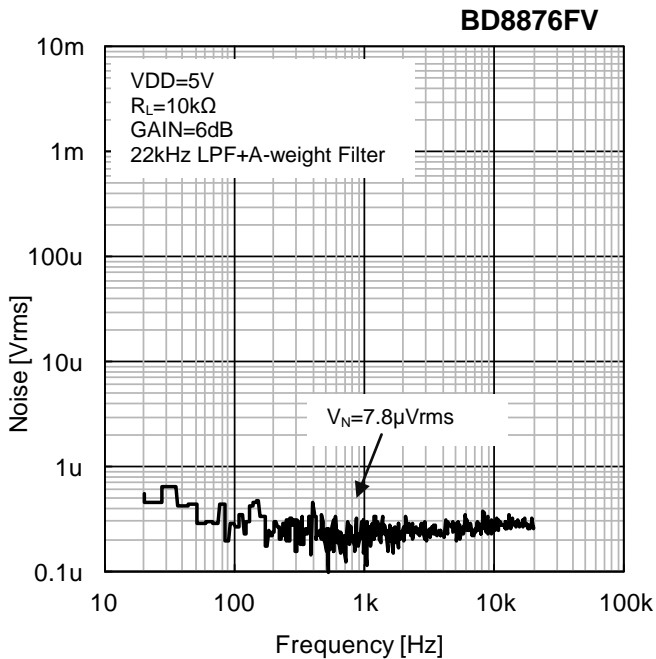


Figure 6.
Noise Level (BD8876FV)

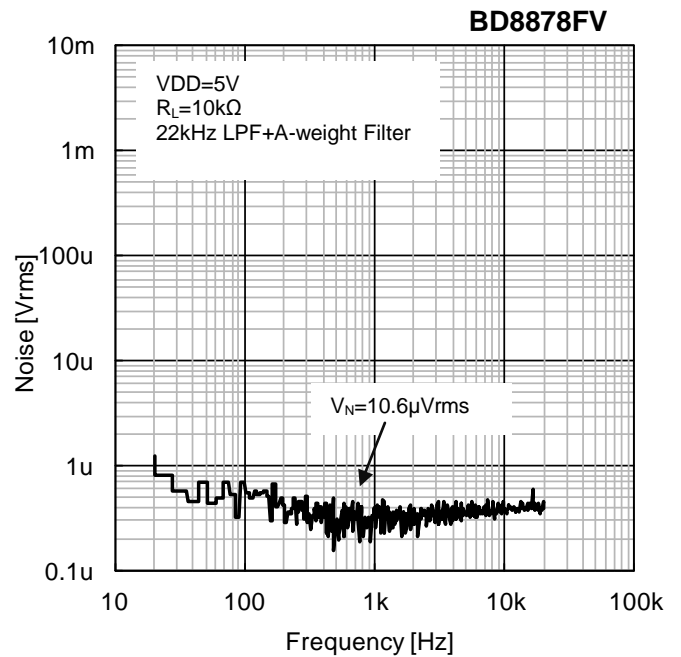


Figure 7.
Noise Level (BD8878FV)

(Unless otherwise specified, $T_a=25^{\circ}\text{C}$, $\text{SVDD}=\text{PVDD}=5\text{V}$, $\text{SGND}=\text{PGND}=0\text{V}$, $\text{SDB}=\text{H}$, $\text{GAIN}=\text{L}$ [BD8876FV], $\text{C}_1=\text{C}_2=1\mu\text{F}$, $\text{R}_\text{L}=10\text{k}\Omega$, Input coupling capacitor= $1\mu\text{F}$) * SVDD, PVDD shows as "VDD" in the following graphs.

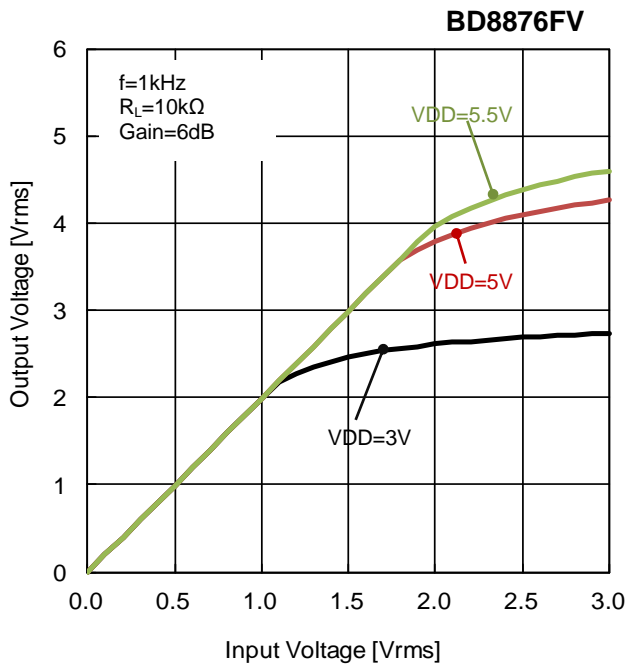


Figure 8.
Output Voltage vs. Input Voltage
(BD8876FV, 6dB)

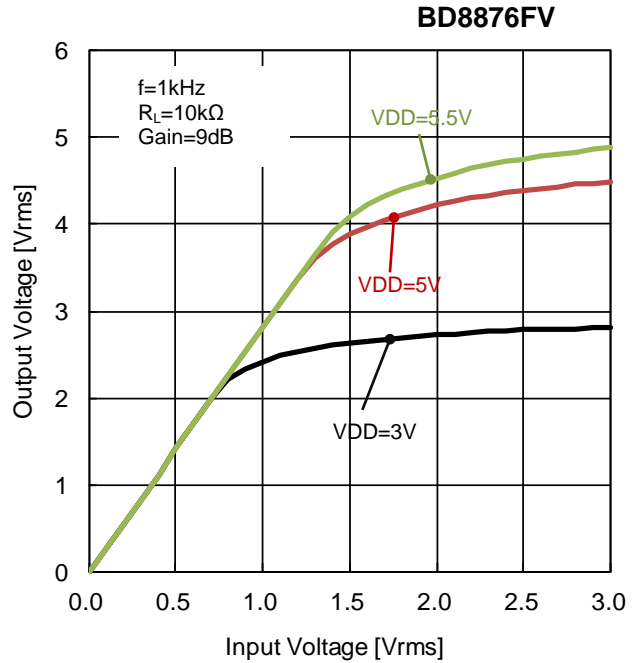


Figure 9.
Output Voltage vs. Input Voltage
(BD8876FV, 9dB)

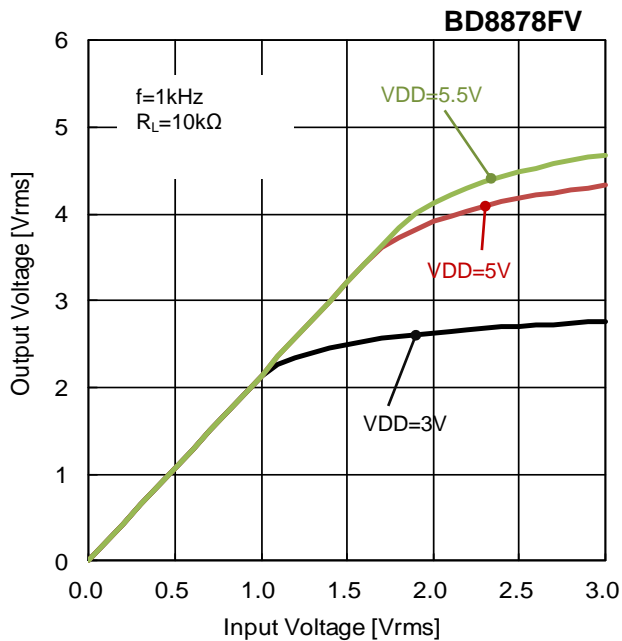


Figure 10.
Output Voltage vs. Input Voltage
(BD8878FV)

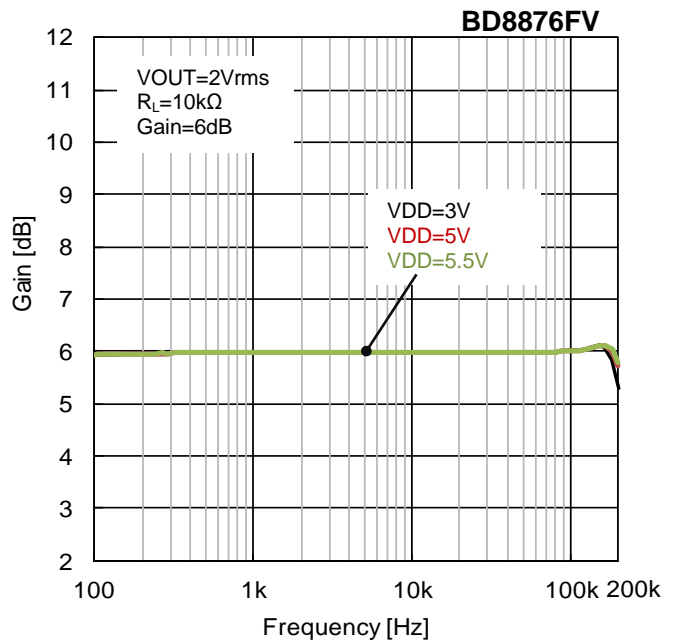


Figure 11.
Gain vs. Frequency
(BD8876FV, 6dB)

(Unless otherwise specified, Ta=25°C, SVDD=PVDD=5V, SGND=PGND=0V, SDB=H, GAIN=L [BD8876FV], C1=C2=1µF, RL=10kΩ, Input coupling capacitor=1µF) * SVDD, PVDD shows as "VDD" in the following graphs.

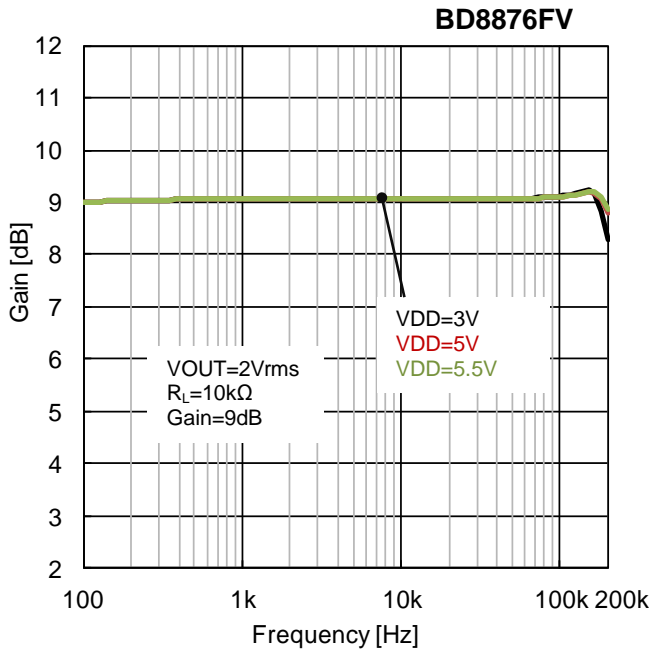


Figure 12.
Gain vs. Frequency
(BD8876FV, 9dB)

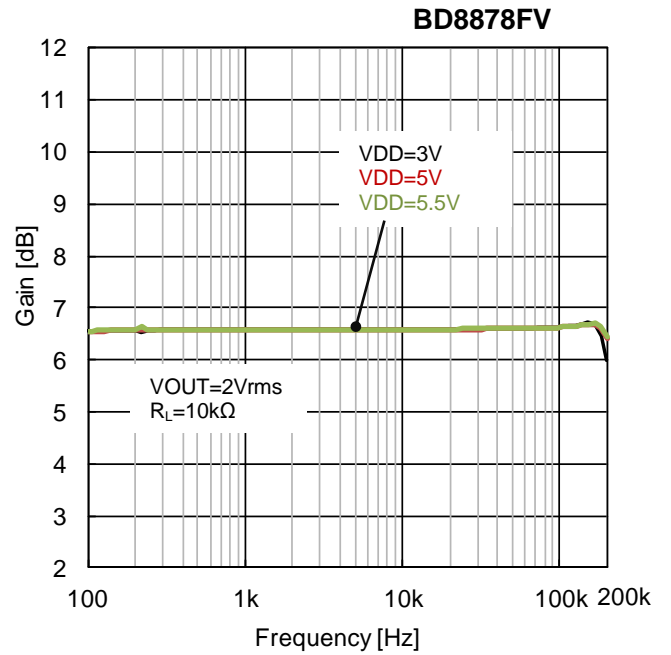


Figure 13.
Gain vs. Frequency
(BD8878FV)

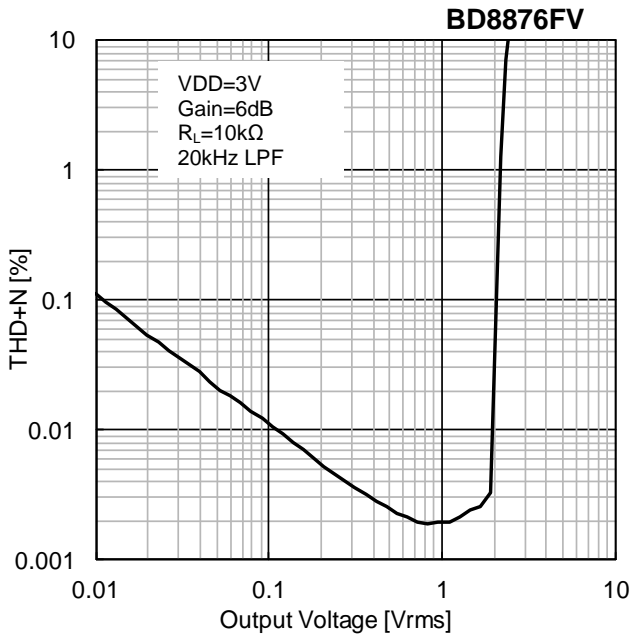


Figure 14.
THD+N vs. Output Voltage
(BD8876FV, 3V)

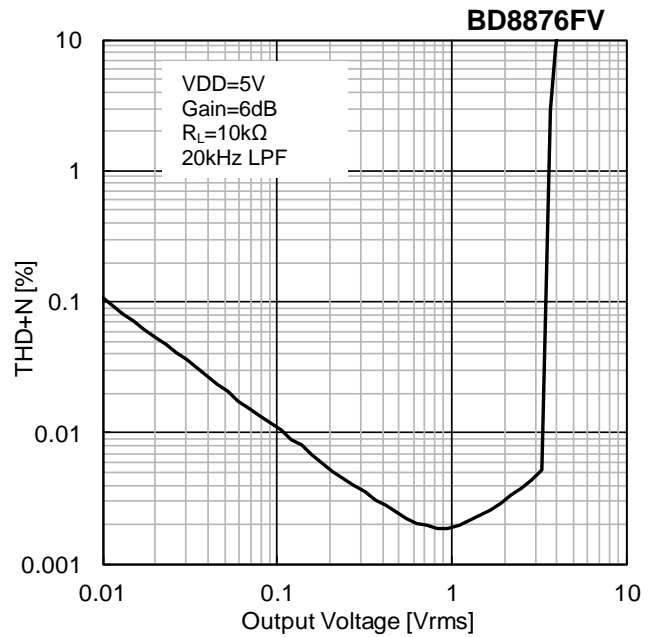


Figure 15.
THD+N vs. Output Voltage
(BD8876FV, 5V)

(Unless otherwise specified, $T_a=25^{\circ}\text{C}$, $\text{SVDD}=\text{PVDD}=5\text{V}$, $\text{SGND}=\text{PGND}=0\text{V}$, $\text{SDB}=\text{H}$, $\text{GAIN}=\text{L}$ [BD8876FV], $C_1=C_2=1\mu\text{F}$, $R_L=10\text{k}\Omega$, Input coupling capacitor= $1\mu\text{F}$) * SVDD, PVDD shows as "VDD" in the following graphs.

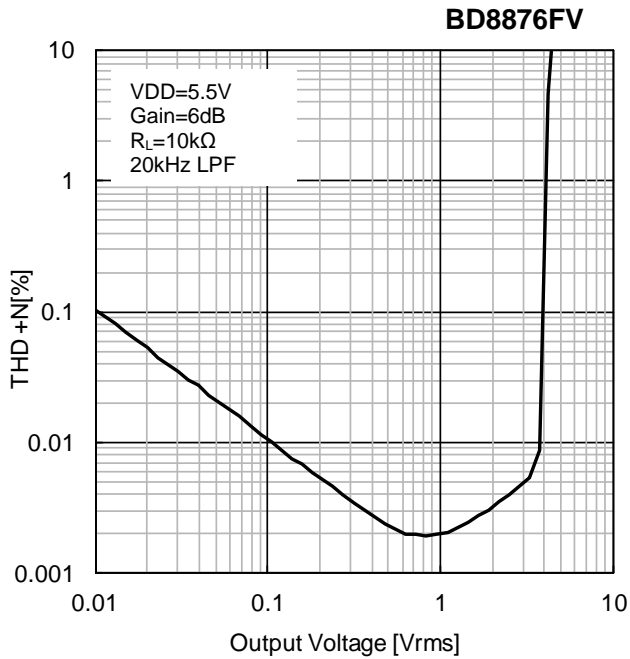


Figure 16.
THD+N vs. Output Voltage
(BD8876FV, 5.5V)

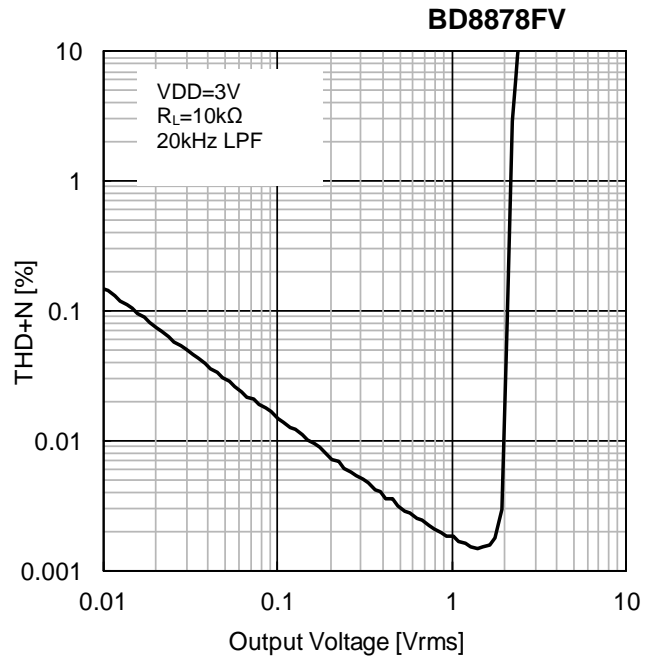


Figure 17.
THD+N vs. Output Voltage
(BD8878FV, 3V)

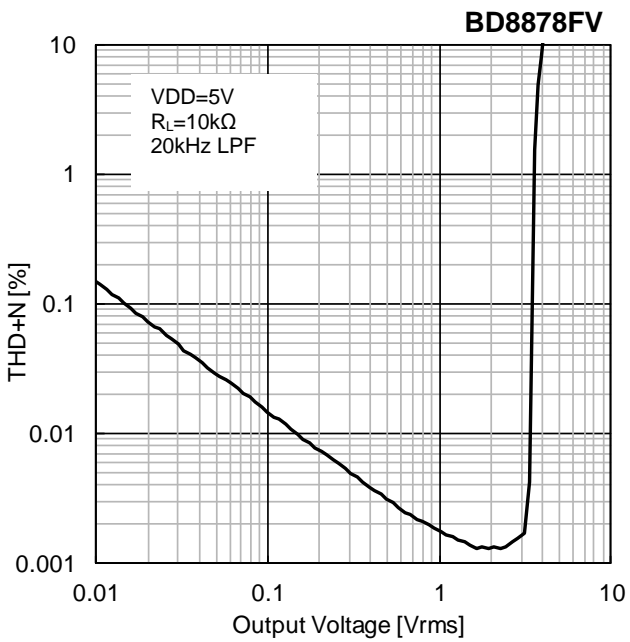


Figure 18.
THD+N vs. Output Voltage
(BD8878FV, 5V)

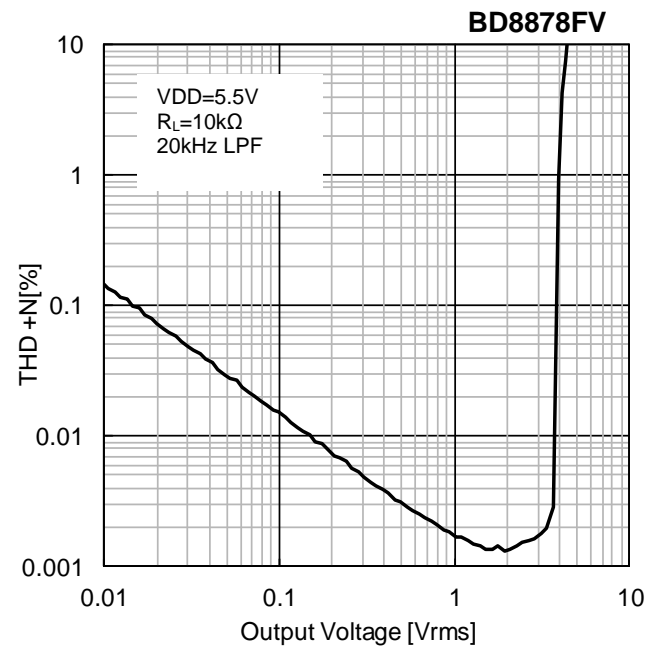


Figure 19.
THD+N vs. Output Voltage
(BD8878FV, 5.5V)

(Unless otherwise specified, Ta=25°C, SVDD=PVDD=5V, SGND=PGND=0V, SDB=H, GAIN=L [BD8876FV], C₁=C₂=1μF, R_L=10kΩ, Input coupling capacitor=1μF) * SVDD, PVDD shows as "VDD" in the following graphs.

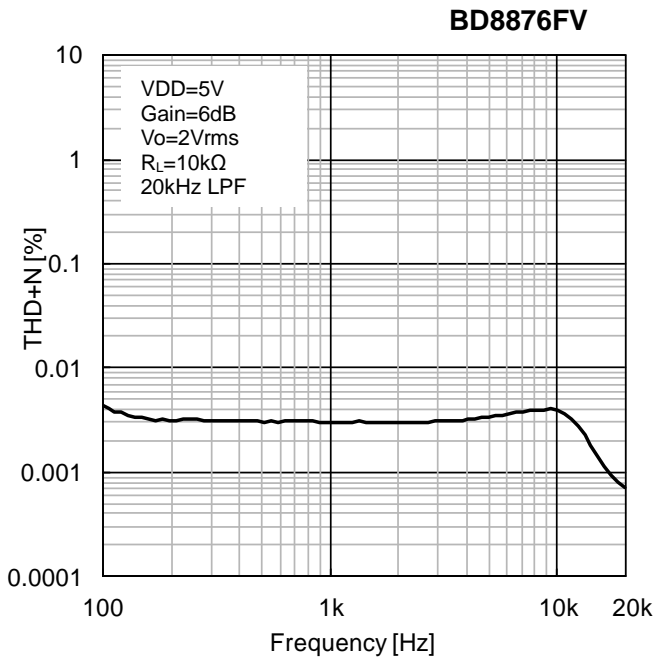


Figure 20.
THD+N vs. Frequency
(BD8876FV)

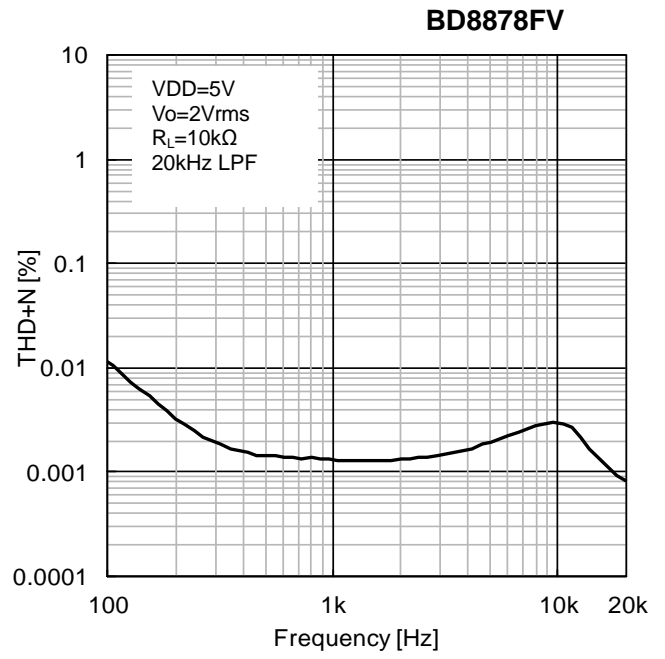


Figure 21.
THD+N vs. Frequency
(BD8878FV)

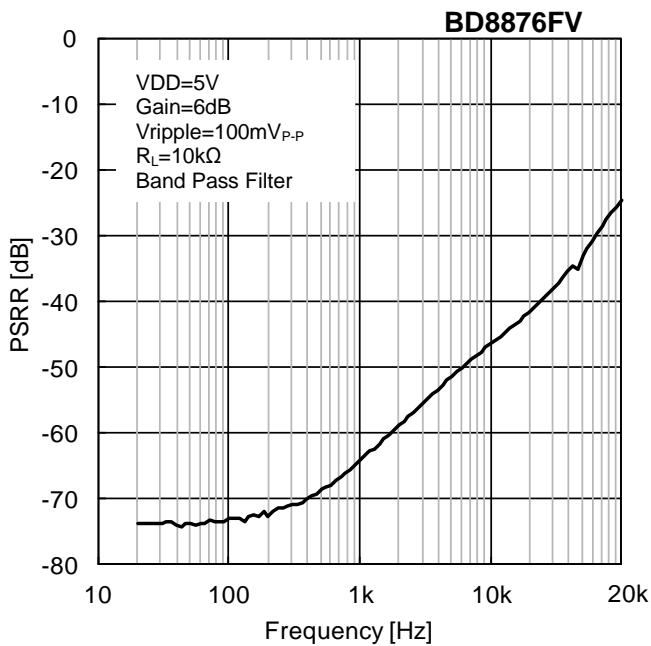


Figure 22.
PSRR vs. Frequency
(BD8876FV)

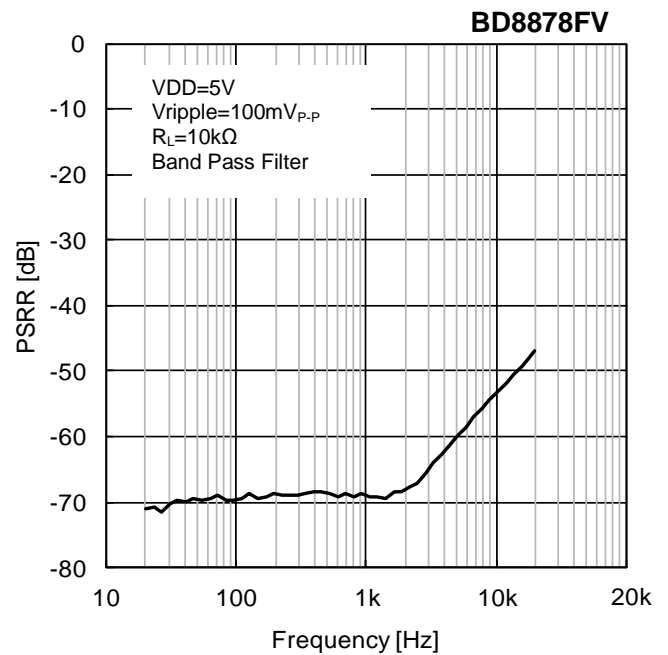


Figure 23.
PSRR vs. Frequency
(BD8878FV)

(Unless otherwise specified, $T_a=25^{\circ}\text{C}$, $\text{SVDD}=\text{PVDD}=5\text{V}$, $\text{SGND}=\text{PGND}=0\text{V}$, $\text{SDB}=\text{H}$, $\text{GAIN}=\text{L}$ [BD8876FV], $C_1=C_2=1\mu\text{F}$, $R_L=10\text{k}\Omega$, Input coupling capacitor= $1\mu\text{F}$) * SVDD, PVDD shows as "VDD" in the following graphs.

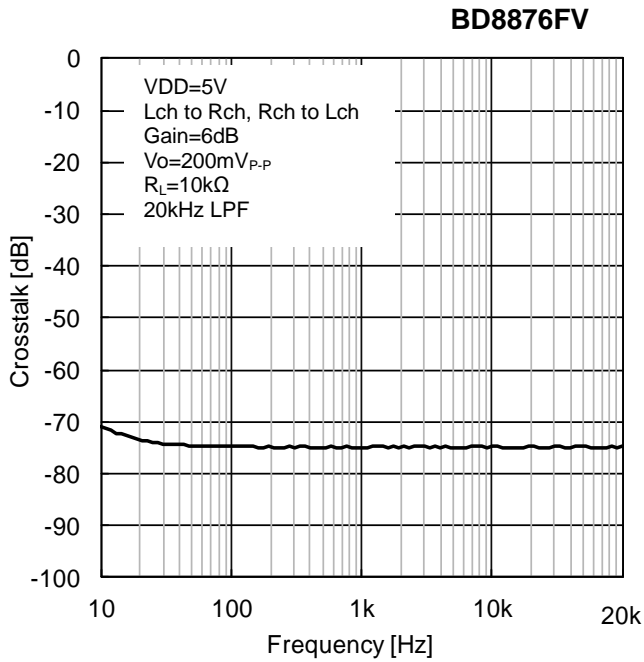


Figure 24.
Crosstalk vs. Frequency
(BD8876FV, 200mV_{p-p})

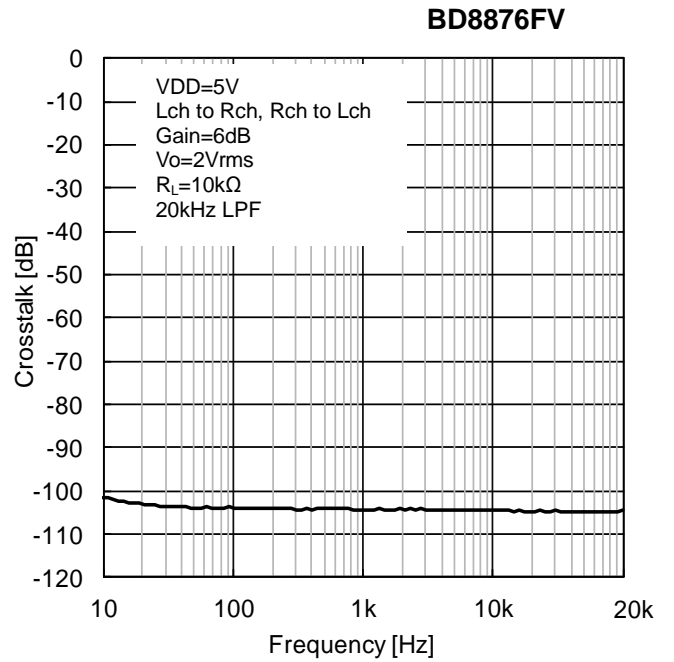


Figure 25.
Crosstalk vs. Frequency
(BD8876FV, 2Vrms)

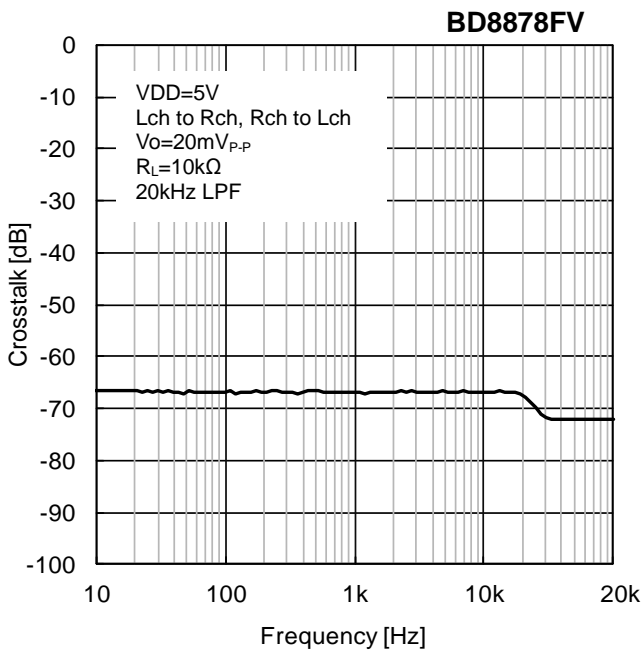


Figure 26.
Crosstalk vs. Frequency
(BD8878FV, 200mV_{p-p})

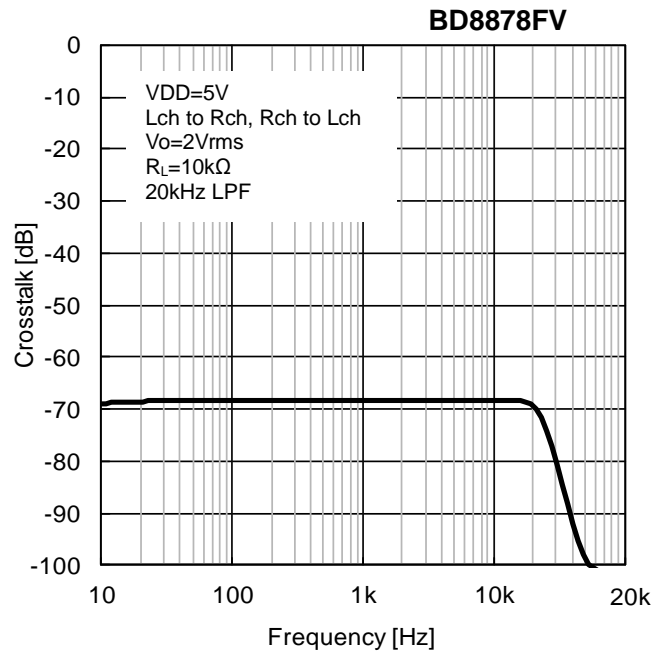


Figure 27.
Crosstalk vs. Frequency
(BD8878FV, 2Vrms)

Application Examples

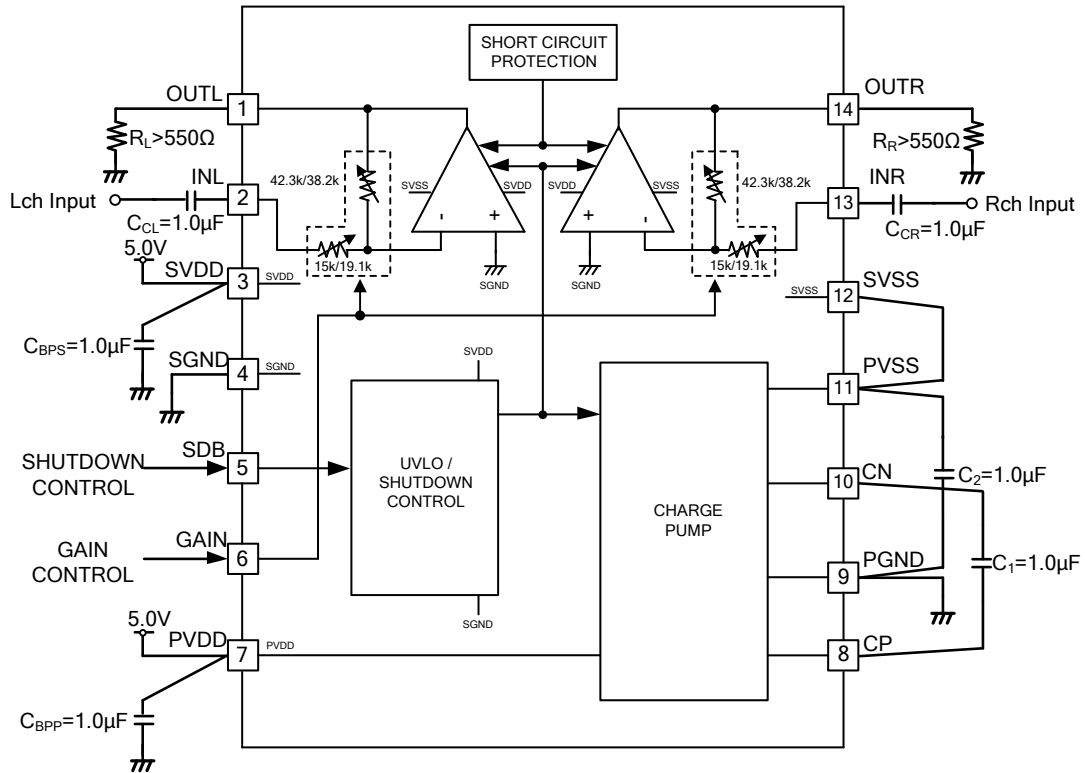


Figure 28. BD8876FV Application circuit example

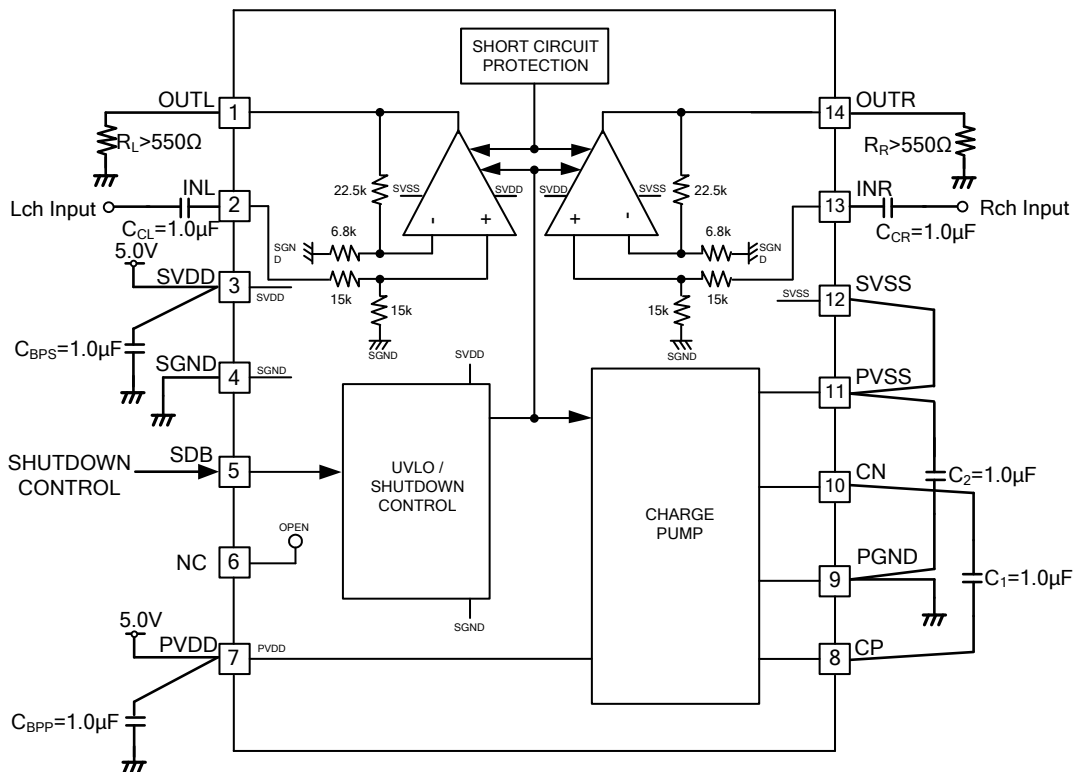


Figure 29. BD8878FV Application circuit example

* PVSS and SVSS are connected each other inside IC. But, please connect PVSS and SVSS outside IC, also.

Timing Chart

< Sequence of start-up / power-down >

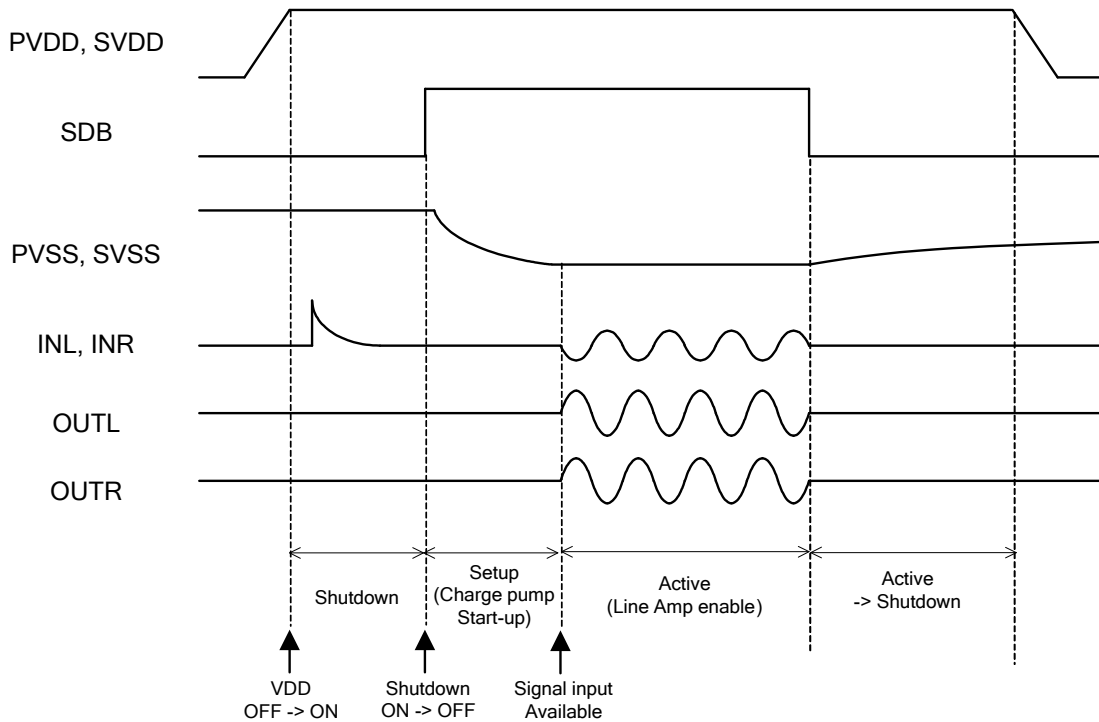


Figure 30. Sequence of start-up / power-down

① The term from “PVDD, SVDD : ON” to “shutdown ON->OFF”

When power supply (PVDD, SVDD) is applied, it is started that charging input coupling capacitors. Therefore, the input terminal voltage “Vin” is changed as following Figure 31. Time constant “τ” of charging input coupling capacitor is decided by input coupling capacitor Cin and Internal input impedance Rin (See formula (1)). Internal impedance Rin in term of shutdown is 7.5kΩ(typ) for making time constant τ shorten. If “SDB” is changed “L” to “H” (shutdown ON -> OFF) during input DC voltage (Vin) is changing, pop noise may occur. It is recommended that shutdown ON -> OFF (“SDB” : L -> H) after 5τ ~ 6τ.

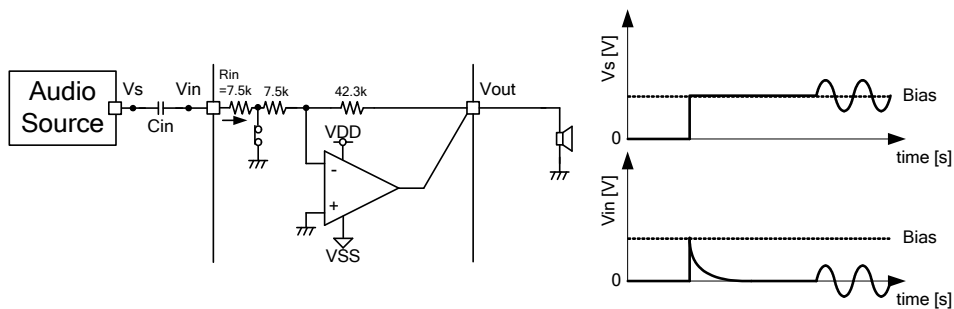


Figure 31. Fluctuation of input terminal voltage when charging input coupling capacitor

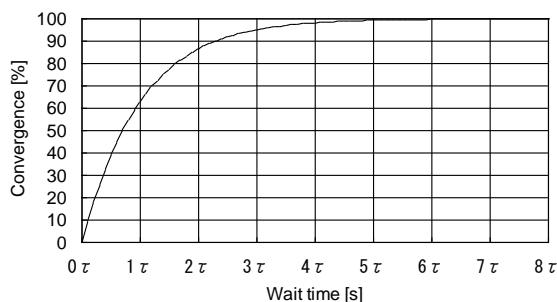


Figure 32. Wait time vs. convergence

$$\tau = R_{in} \times C_{in} \quad (1)$$

(e.g.) in case of $C_{in} = 1.0\mu F$,
 $\tau = R_{in} \times C_{in}$
 $= 7.5k\Omega \times 1.0\mu F$
 $= 7.5 \text{ msec (typ)}$
 $6\tau = 6 \times 7.5\text{msec}$
 $= 45 \text{ msec (typ)}$

② The term from shutdown OFF to line amplifier start-up

When shutdown is ON -> OFF, charge pump starts up. Line amplifier is stopped during "t_{SON} (start-up time of charge pump, 470µsec typ.)" for preventing irregular output. Please input audio signal after "t_{SON}".

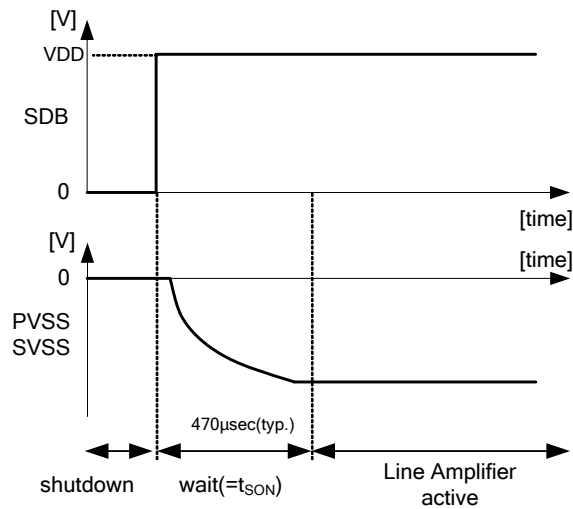


Figure 33. Wait time for Line amplifier from "shutdown ON -> OFF"

Functional Descriptions / Application Information

The composition of conventional line amplifier is shown in Figure 34. Output signal swings in reference to Middle DC bias (e.g. VDD/2). Therefore, Output dynamic range of line amplifier limits until "VDD".

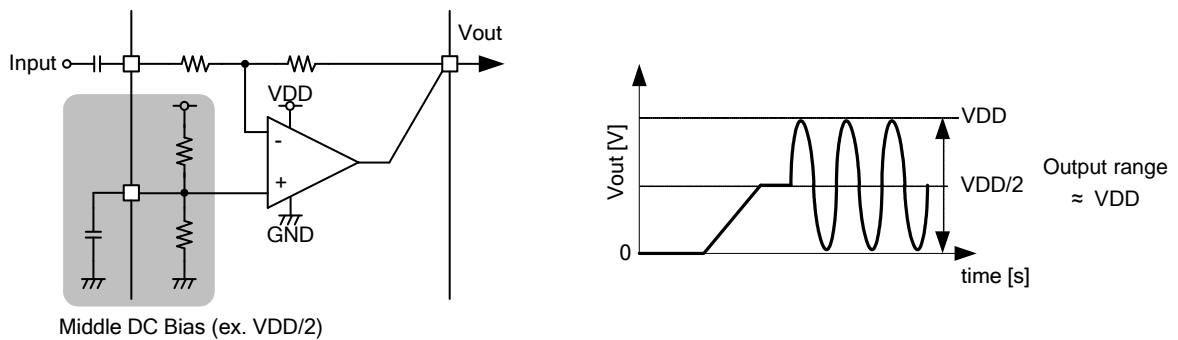


Figure 34. The composition of conventional line amplifier

The composition of BD8876FV/BD8878FV is shown to Figure 35. Output signal swings in reference to ground level. Line amplifier can output between from VSS (-VDD) to VDD. Therefore, Output dynamic range of line amplifier expands "2 x VDD". And, it is possible to drive 2V_{rms} (5.65V_{P-P}) with single supply voltage 5V.

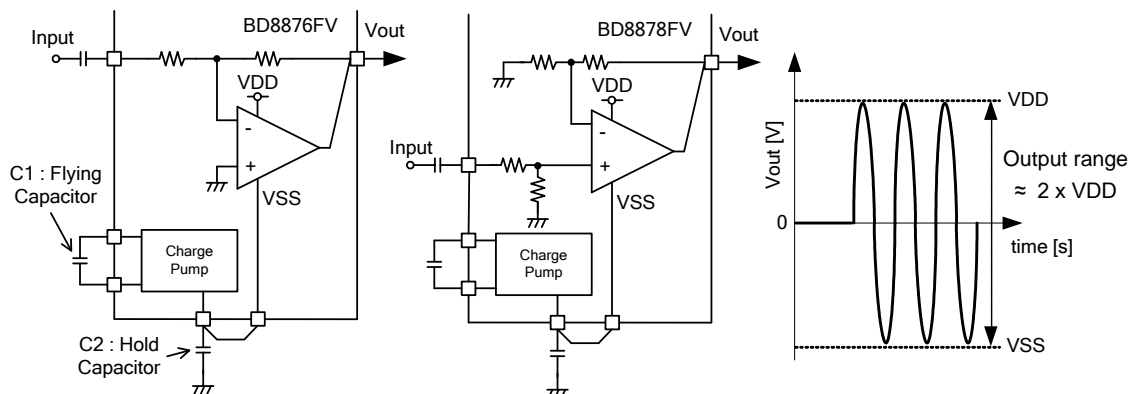


Figure 35. The composition of BD8876FV/BD8878FV

■ CHARGE PUMP

The negative power supply circuit is composed of the regulated charge-pump. This circuit outputs the negative voltage (PVSS) from positive power-supply voltage (PVDD). The negative power supply circuit starts when “SDB=H”, and power is downed when “SDB=L”(See Table 1).

Table 1. Control of the charge pump circuit

SDB	Control
L	Power down
H	Power on

<The flying capacitor and the hold capacitor>

The flying capacitor (Figure 35. C1) and the hold capacitor (Figure 35. C2) have great influences on the characteristic of the charge pump. Please select capacitors that have low ESR characteristic and low voltage coefficient, low temperature coefficient for C1, C2. And, please connect these capacitors as near as possible to IC.

<Over-current Protection>

The charge pump has the over-current protection function. If the terminals of charge pump (CP, CN, PVSS, SVSS) are under the abnormal connecting conditions (e.g. shorting to ground), this function shutdown IC and protect it from the damage.

■Line Amplifier

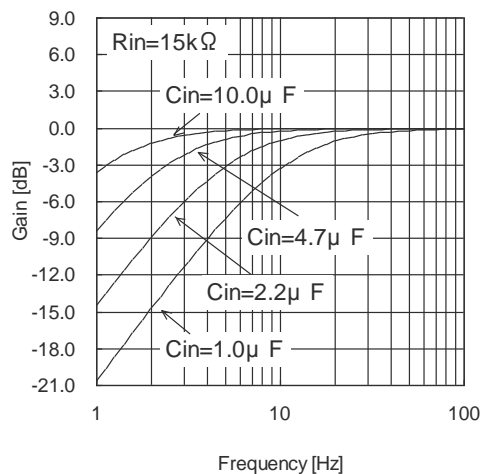
The line amplifier is driven by power-supply voltage (SVDD) and negative voltage (SVSS) based on ground (SGND). Therefore, the amplifier can output 2Vrms for RL=10kohm with the single supply voltage 5V. And BD8876FV can change the gain 6dB and 9dB. The gain of BD8878FV is 6.7dB (fixed). The both of Lch and Rch of the line amplifier are simultaneously controlled by SDB logic (See Table 2). In addition, the over-current protection circuit is built in. The amplifier is shutdown, when the over-current occurs because of the output short-circuit etc., and IC is protected from being destroyed.

Table 2. Control of the Line amplifier circuit

SDB	Lch/Rch amplifier control
L	Power down
H	Power on

<Input coupling capacitor>

Input DC voltage level of BD8876FV/BD8878FV is 0V (SGND). Therefore, input coupling capacitor is needed. Gain is decreased in low frequency because of composing the high-pass filter by input coupling capacitor Cin and internal input impedance Rin of BD8876FV/BD8878FV. Input impedance Rin of BD8876FV is 15kΩ (Typ, Gain=+9dB), and Rin of BD8878FV is 30kΩ (Typ). Cut-off frequency of the high-pass filter is shown to the following formula (2).



$$f_c = \frac{1}{2\pi R_{in} C_{in}} \quad (2)$$

Figure 36. Frequency response by the input coupling capacitor (Reference data: Calculated value)

The degradation of THD happens because of the input coupling capacitor. Therefore, please consider the applied voltage dependence and the temperature characteristic of the capacitor when selecting parts.

■ UVLO / SHUTDOWN CONTROL

BD8876FV/BD8878FV has low voltage protection function (UVLO: Under Voltage Lock Out). UVLO function protects from abnormal operation under lower power supply voltage than the recommended supply voltage range. The detection voltage is 2.8V (Typ). It does not influence the recommended operation voltage (3.0V (Min)). The power control by UVLO works for the whole of IC, and power down the both of the negative power supply charge pump and the line amplifier. If power supply voltage recovers over recommended range (3.0V), all function also recover automatically.

Power Dissipation

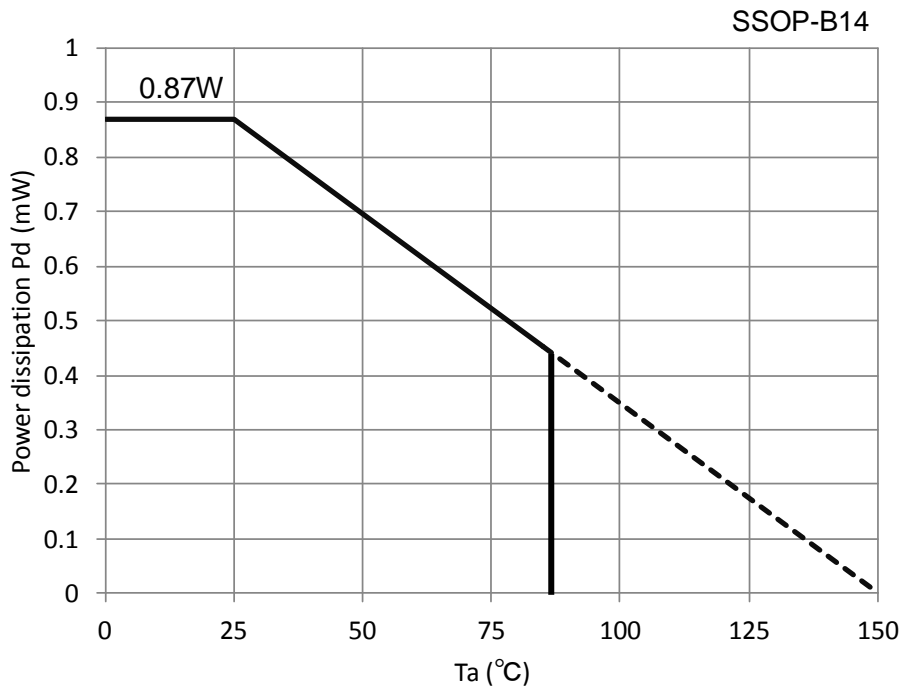


Figure 37. Power Dissipation Curve

Measurement Condition: Mounted on ROHM standard board, glass-epoxy
Board size: 74.2mm×74.2mm×1.6mm (1-layer)
Material: FR4

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Rush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

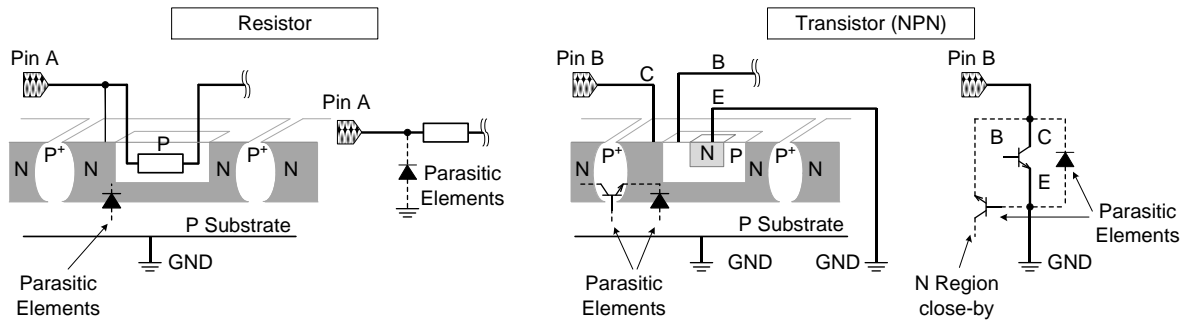


Figure 38. Example of monolithic IC structure

13. Ceramic Capacitor

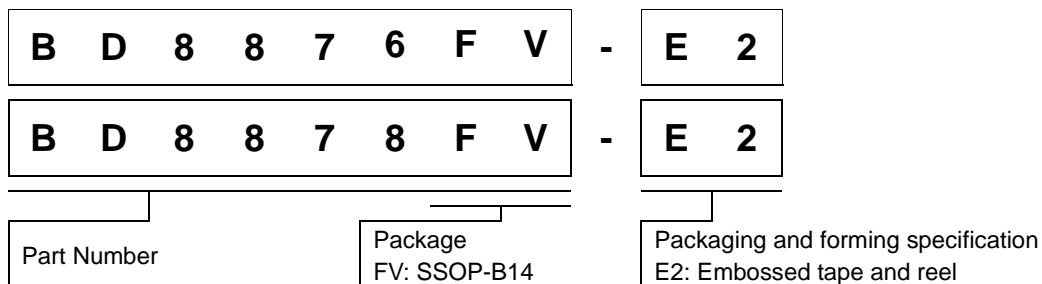
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

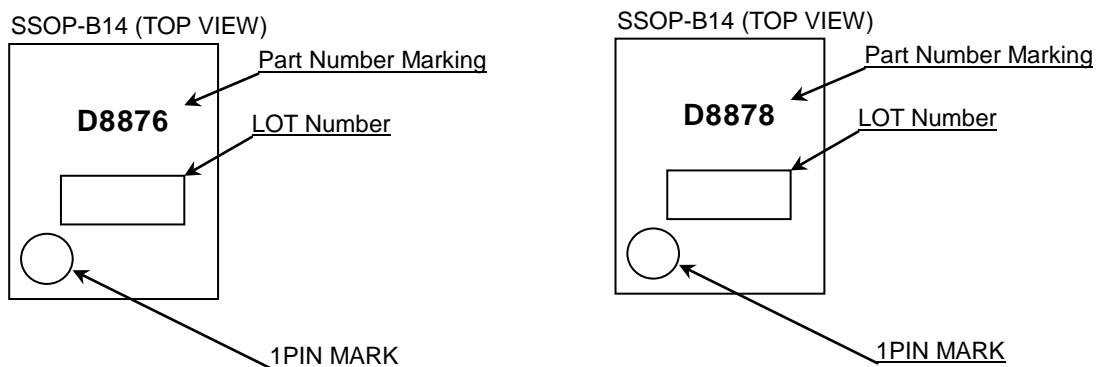
Ordering Information



Line-up

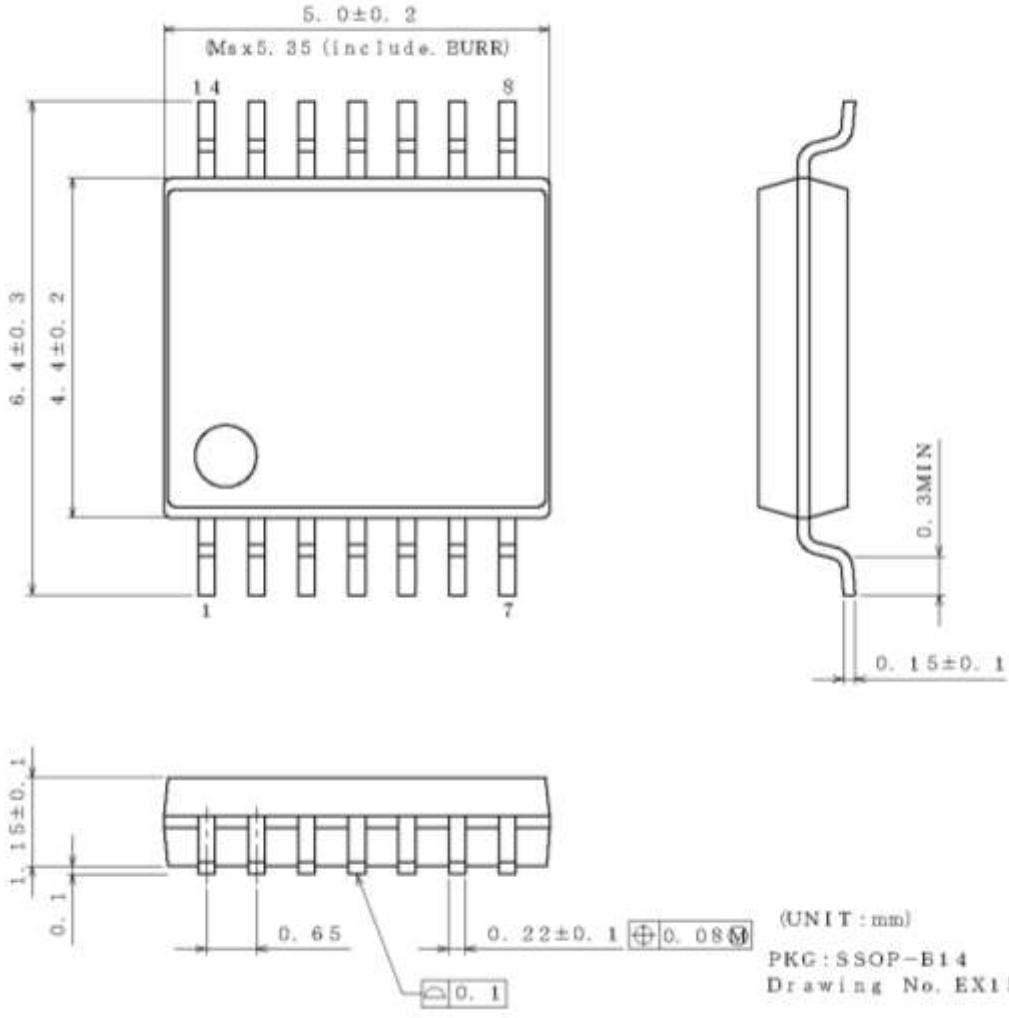
	BD8876FV	BD8878FV
Amplifier type	Inverting amplifier	Non-inverting amplifier
Gain	+6dB / +9dB (Changed by Gain pin)	+6.7dB
Package	SSOP-B14	

Marking Diagram



Physical Dimension, Tape and Reel Information

Package Name	SSOP-B14
--------------	----------



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

Diagram of the carrier tape showing the direction of feed and the location of pin 1. The tape is shown with multiple packages. An arrow labeled "Reel" points to the left, and an arrow labeled "Direction of feed" points to the right. A label "1pin" points to the first pin of a package. A note below the diagram states: "*Order quantity needs to be multiple of the minimum quantity."

Revision History

Date	Revision	Changes
2015/10/30	001	First version

Notice

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- Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

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