

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT186A (TO-220F) "full pack" plastic package intended for use in applications requiring very high inrush current capability, high thermal cycling performance and high junction temperature capability ($T_{j(max)} = 150\text{ °C}$).

2. Features and benefits

- High junction operating temperature capability
- High thermal cycling performance
- High voltage capability
- Isolated package
- Planar passivated for voltage ruggedness and reliability
- Very High current surge capability

3. Applications

- Ignition circuits
- Motor control
- Protection circuits e.g. SMPS inrush current
- Voltage regulation

4. Quick reference data

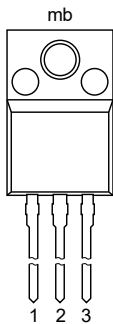

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--------------------------------------|---|-----|-----|------|------|
| V_{RRM} | repetitive peak reverse voltage | | - | - | 800 | V |
| $I_{T(AV)}$ | average on-state current | half sine wave; $T_h \leq 86\text{ °C}$; Fig. 1 | - | - | 10.2 | A |
| $I_{T(RMS)}$ | RMS on-state current | half sine wave; $T_h \leq 86\text{ °C}$; Fig. 2 ; Fig. 3 | - | - | 16 | A |
| I_{TSM} | non-repetitive peak on-state current | half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 210 | A |
| | | half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$ | - | - | 231 | A |
| T_j | junction temperature | | - | - | 150 | °C |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 7 | - | 4.5 | 25 | mA |
| Dynamic characteristics | | | | | | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|-----------------------------------|---|-----|-----|-----|------------------|
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 536 \text{ V}$; $T_j = 150 \text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit | 300 | - | - | V/ μs |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------------------|--|---|
| 1 | K | cathode |  <p style="text-align: center;">TO-220F (SOT186A)</p> |  <p style="text-align: center;">sym037</p> |
| 2 | A | anode | | |
| 3 | G | gate | | |
| mb | n.c. | mounting base; isolated | | |

6. Ordering information

Table 3. Ordering information

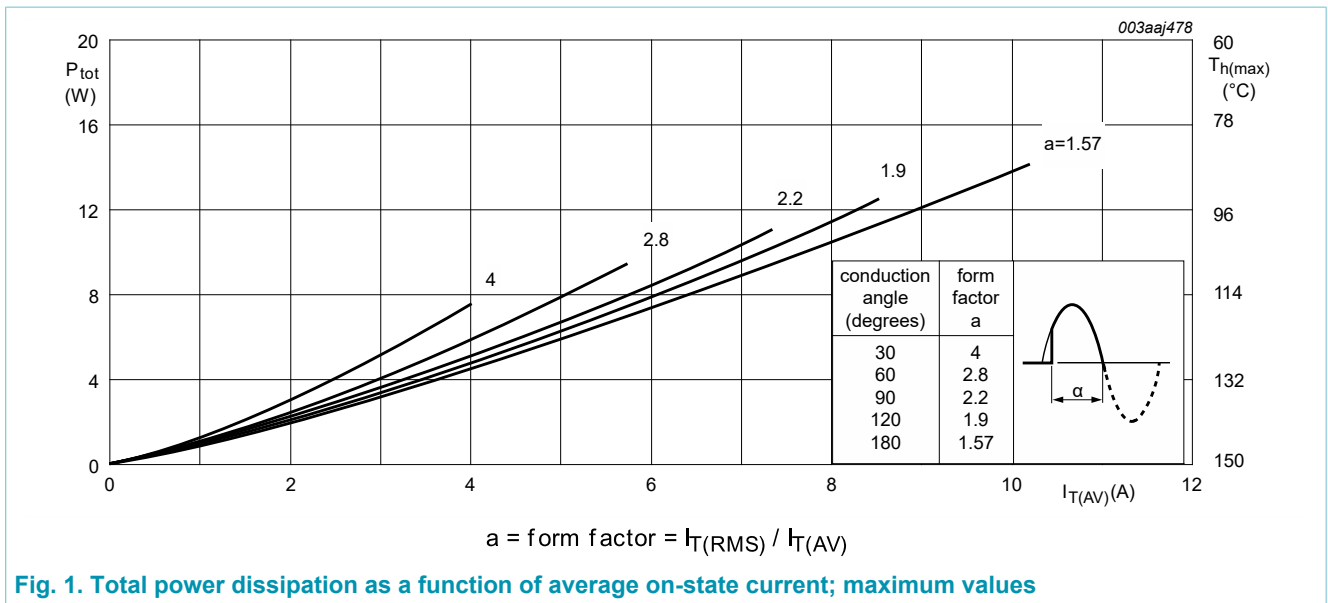
| Type number | Package | | |
|--------------|---------|---|---------|
| | Name | Description | Version |
| TYN16X-800RT | TO-220F | plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" | SOT186A |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--------------------------------------|---|-----|-------|------------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 800 | V |
| V_{RRM} | repetitive peak reverse voltage | | - | 800 | V |
| $I_{T(AV)}$ | average on-state current | half sine wave; $T_h \leq 86\text{ }^\circ\text{C}$; Fig. 1 | - | 10.2 | A |
| $I_{T(RMS)}$ | RMS on-state current | half sine wave; $T_h \leq 86\text{ }^\circ\text{C}$; Fig. 2; Fig. 3 | - | 16 | A |
| I_{TSM} | non-repetitive peak on-state current | half sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 10\text{ ms}$; Fig. 4; Fig. 5 | - | 210 | A |
| | | half sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 8.3\text{ ms}$ | - | 231 | A |
| I^2t | I^2t for fusing | $t_p = 10\text{ ms}$; SIN | - | 220.5 | A^2s |
| dl_T/dt | rate of rise of on-state current | $I_G = 50\text{ mA}$ | - | 50 | $\text{A}/\mu\text{s}$ |
| I_{GM} | peak gate current | | - | 5 | A |
| V_{RGM} | peak reverse gate voltage | | - | 5 | V |
| P_{GM} | peak gate power | | - | 20 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 1 | W |
| T_{stg} | storage temperature | | -40 | 150 | $^\circ\text{C}$ |
| T_j | junction temperature | | - | 150 | $^\circ\text{C}$ |



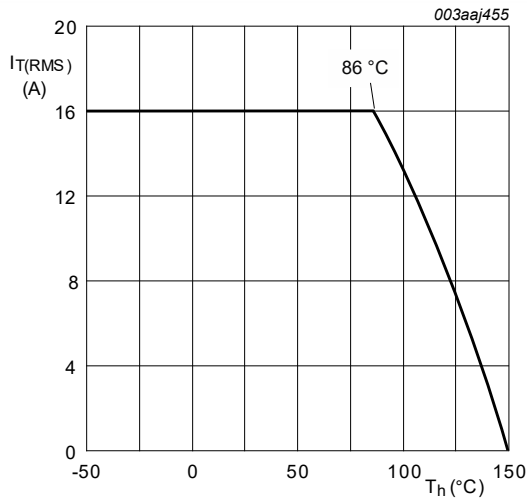


Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values

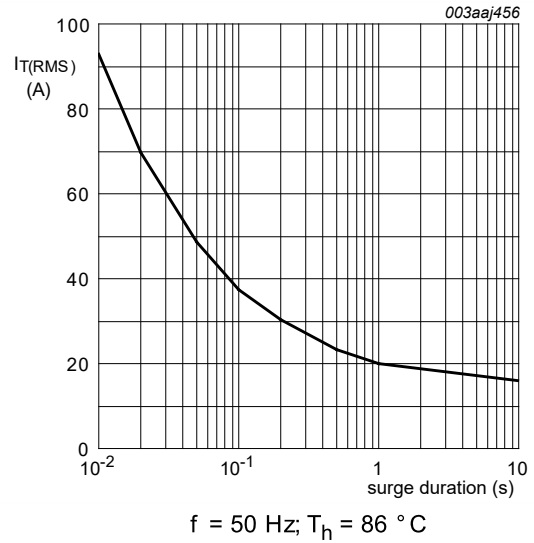


Fig. 3. RMS on-state current as a function of surge duration; maximum values

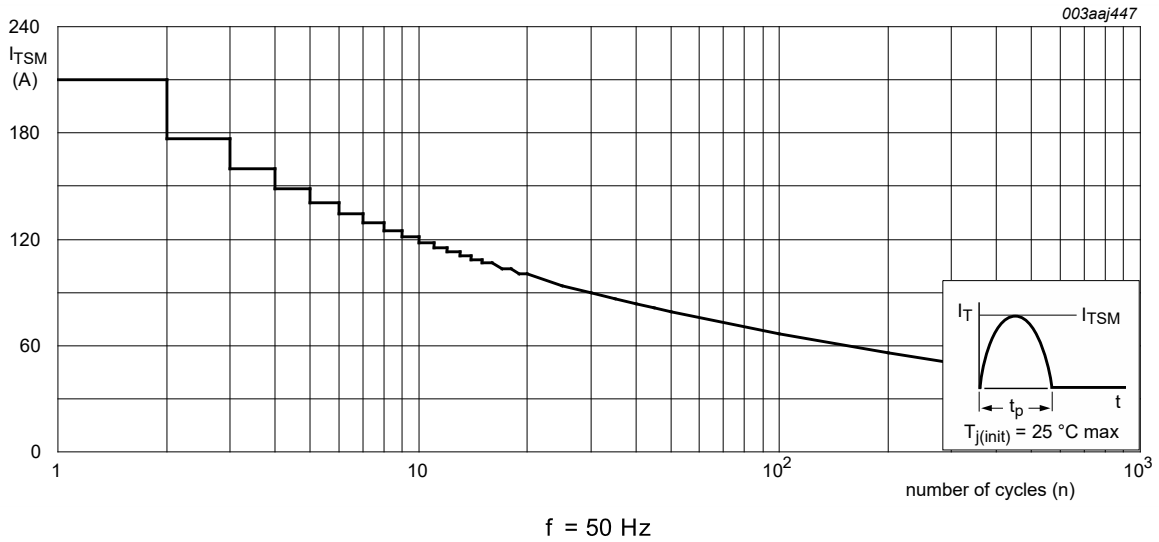
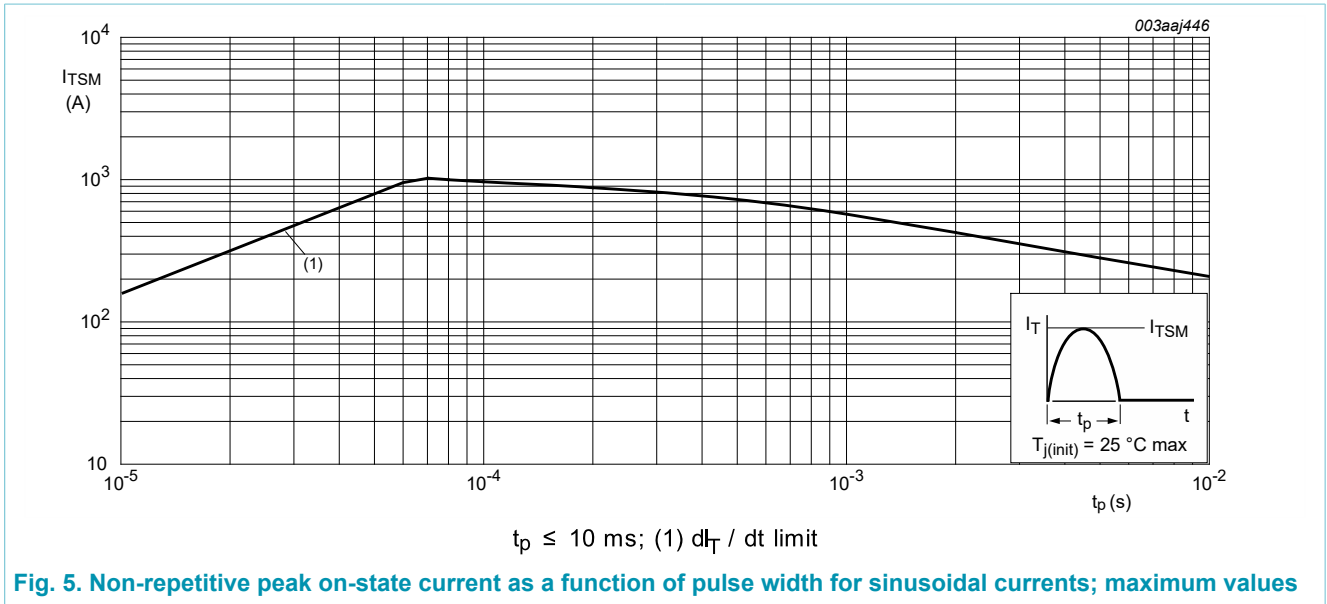


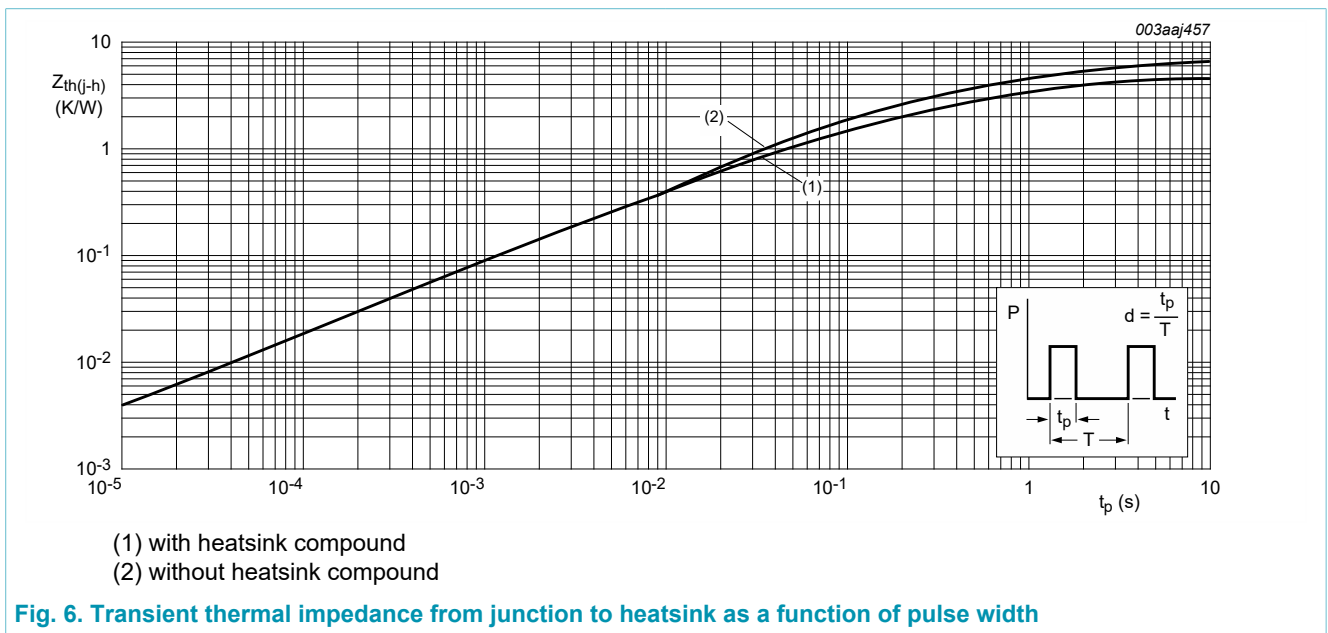
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|--|-----------------------------------|-----|-----|-----|------|
| $R_{th(j-h)}$ | thermal resistance from junction to heatsink | with heatsink compound; Fig. 6 | - | - | 4.5 | K/W |
| | | without heatsink compound; Fig. 6 | - | - | 6.5 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | in free air | - | 55 | - | K/W |



9. Isolation characteristics

Table 6. Isolation characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|-----------------------|--|-----|-----|------|------|
| $V_{isol(RMS)}$ | RMS isolation voltage | from all terminals to external heatsink; sinusoidal waveform; clean and dust free; $50\text{ Hz} \leq f \leq 60\text{ Hz}$; $RH \leq 65\%$; $T_h = 25\text{ }^\circ\text{C}$ | - | - | 2500 | V |
| C_{isol} | isolation capacitance | from anode to external heatsink; $f = 1\text{ MHz}$; $T_h = 25\text{ }^\circ\text{C}$ | - | 10 | - | pF |

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------|--|-----|-----|-----|------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 7 | - | 4.5 | 25 | mA |
| I_L | latching current | $V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 8 | - | 21 | 60 | mA |
| I_H | holding current | $V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 9 | - | 16 | 40 | mA |
| V_T | on-state voltage | $I_T = 32\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 10 | - | 1.2 | 1.5 | V |
| V_{GT} | gate trigger voltage | $V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 11 | - | 0.7 | 1.3 | V |
| | | $V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 150\text{ }^\circ\text{C};$ Fig. 11 | 0.2 | 0.4 | - | V |
| I_D | off-state current | $V_D = 800\text{ V}; T_j = 150\text{ }^\circ\text{C}$ | - | 0.2 | 1 | mA |
| I_R | reverse current | $V_R = 800\text{ V}; T_j = 150\text{ }^\circ\text{C}$ | - | 0.2 | 1 | mA |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 536\text{ V}; T_j = 150\text{ }^\circ\text{C}; (V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit | 300 | - | - | V/ μ s |

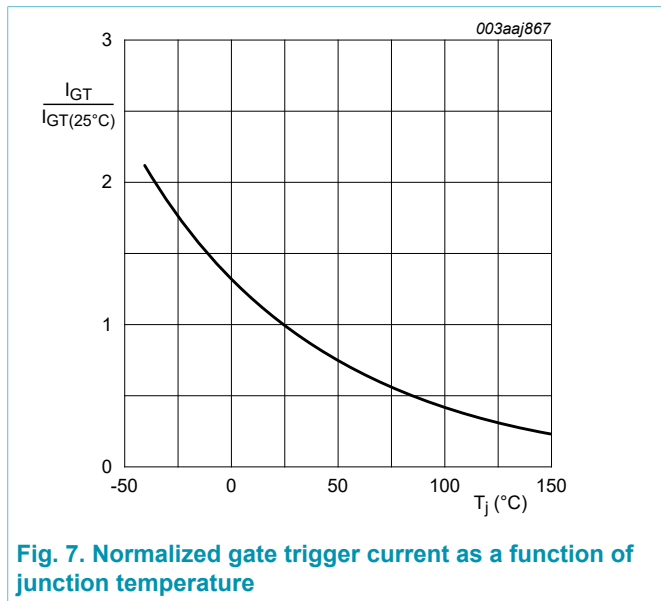


Fig. 7. Normalized gate trigger current as a function of junction temperature

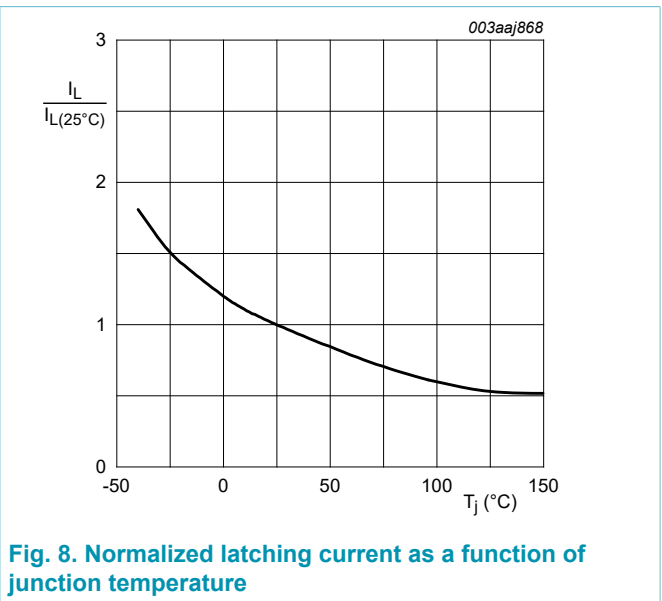


Fig. 8. Normalized latching current as a function of junction temperature

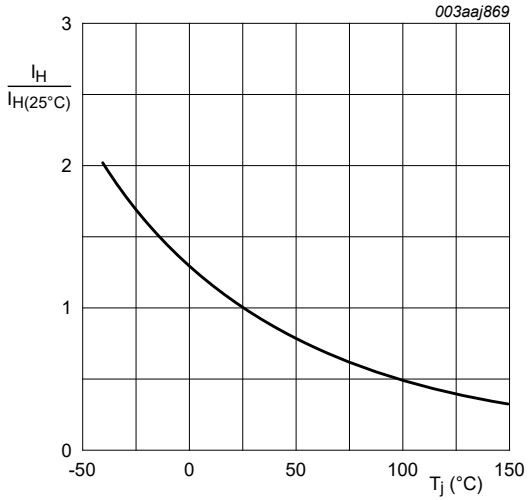
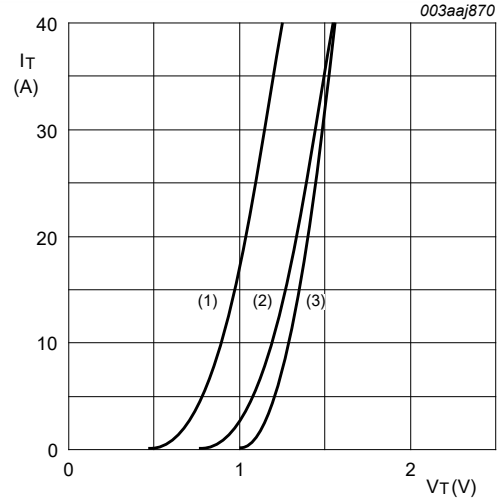


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.0336 \text{ V}; R_s = 0.0141 \Omega$
 (1) $T_j = 150^\circ\text{C}$; typical values
 (2) $T_j = 150^\circ\text{C}$; maximum values
 (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

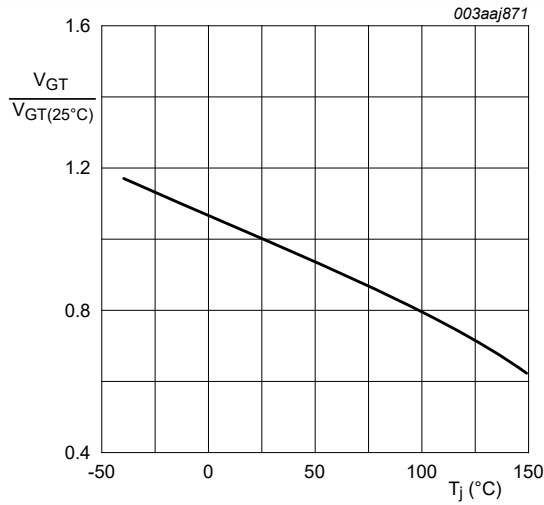


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

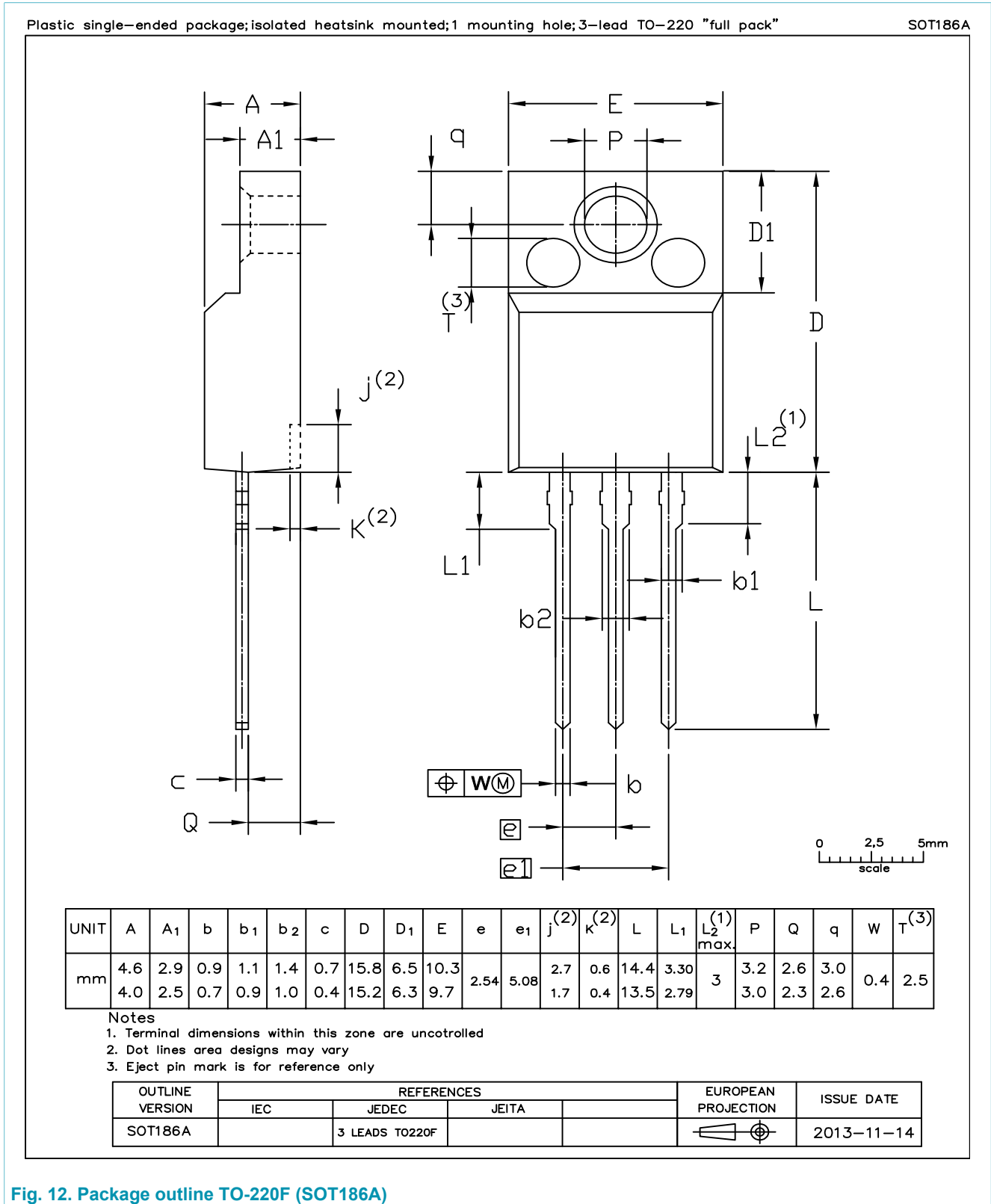


Fig. 12. Package outline TO-220F (SOT186A)

12. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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