

RX111 Group Renesas MCUs

R01DS0190EJ0130

Rev.1.30

May 31, 2016

32 MHz 32-bit RX MCUs, 50 DMIPS, up to 512 Kbytes of flash memory,
USB 2.0 full-speed host/function/OTG, up to 6 comms channels,
12-bit A/D, 8-bit D/A, RTC

Features

■ 32-bit RX CPU core

- 32 MHz maximum operating frequency
Capable of 50 DMIPS when operating at 32 MHz
- Accumulator handles 64-bit results (for a single instruction) from 32-bit × 32-bit operations
- Multiplication and division unit handles 32-bit × 32-bit operations (multiplication instructions take one CPU clock cycle)
- Fast interrupt
- CISC Harvard architecture with five-stage pipeline
- Variable-length instruction format, ultra-compact code
- On-chip debugging circuit

■ Low power consumption functions

- Operation from a single 1.8 to 3.6 V supply
- Three low power consumption modes
- Supply current
High-speed operating mode: 0.11 mA/MHz
Software standby mode: 0.44 μA
- Recovery time from software standby mode: 4.8 μs

■ On-chip flash memory for code, no wait states

- Operation at 32 MHz, read cycle of 31.25 ns
- No wait states for reading at full CPU speed
- 16 to 512 Kbyte capacities
- Programmable at 1.8 V
- For instructions and operands

■ On-chip data flash memory

- 8 Kbytes
1,000,000 Erase/Write cycles (typ.)
- BGO (Background Operation)

■ On-chip SRAM, no wait states

- 8 to 64 Kbyte capacities

■ Data transfer controller (DTC)

- Four transfer modes
- Transfer can be set for each interrupt source.

■ Event link controller (ELC)

- Module operation can be initiated by event signals without going through interrupts.
- Link operation between modules is possible while the CPU is sleeping.

■ Reset and power supply voltage management

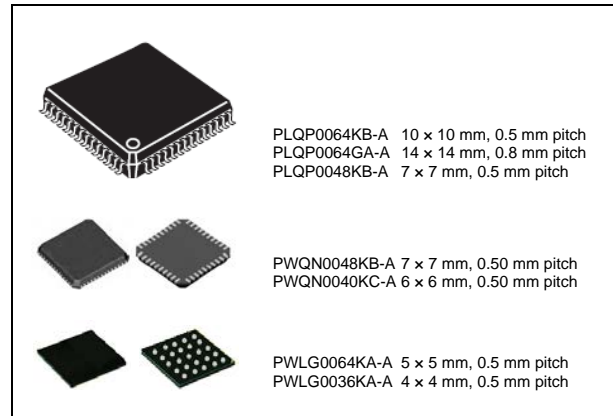
- Six types including Power-On Reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions

- External clock input frequency: Up to 20 MHz
- Main clock oscillator frequency: 1 to 20 MHz
- Sub-clock oscillator frequency: 32.768 kHz
- PLL circuit input: 4 to 8 MHz
- Low-speed on-chip oscillator: 4 MHz
- High-speed on-chip oscillator: 32 MHz±1% (-20 to 85°C)
- IWDT-dedicated on-chip oscillator: 15 kHz
- Generate a dedicated 32.768-kHz clock for the RTC
- On-chip clock frequency accuracy measurement circuit (CAC)

■ Realtime clock (RTC)

- 30-second, leap year, and error adjustment functions
- Calendar count mode or binary count mode selectable
- Capable of initiating exit from software standby mode



■ Independent watchdog timer (IWDT)

- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

■ On-chip functions for IEC 60730 compliance

- Clock frequency accuracy measurement circuit, IWDT, functions to assist in RAM testing, etc.

■ Up to six channels for communication

- USB: USB 2.0 host (32 Kbyte or more ROM)/function/On-The-Go (OTG) (one channel), full-speed = 12 Mbps, low-speed = 1.5 Mbps, isochronous transfer, and BC (Battery Charger) supported
- SCI: Asynchronous mode, clock synchronous mode, smart card interface (up to three channels)
- I²C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (one channel)
- RSPI: Up to 16 Mbps (one channel)

■ Up to 8 extended-function timers

- 16-bit MTU: Input capture/output compare, complementary PWM output, phase counting mode (six channels)
- 16-bit CMT (two channels)

■ 12-bit A/D converter

- Up to 14 channels
- 1.0 μs minimum conversion speed
- Double trigger (data duplication) function for motor control

■ 8-bit D/A converter

- Two channels (for 64 pins only)

■ Temperature sensor

■ General I/O ports

- 5-V tolerant, open drain, input pull-up

■ Multi-function pin controller (MPC)

- Multiple I/O pins can be selected for peripheral functions.

■ Unique ID

- 32-byte ID code for the MCU

■ Operating temperature range

- -40 to +85°C
- -40 to +105°C

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.

Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/3)

| Classification | Module/Function | Description |
|-----------------------|--|---|
| CPU | CPU | <ul style="list-style-type: none"> Maximum operating frequency: 32 MHz 32-bit RX CPU Minimum instruction execution time: One instruction per clock cycle Address space: 4-Gbyte linear Register set <ul style="list-style-type: none"> General purpose: Sixteen 32-bit registers Control: Eight 32-bit registers Accumulator: One 64-bit register Basic instructions: 73 DSP instructions: 9 Addressing modes: 10 Data arrangement <ul style="list-style-type: none"> Instructions: Little endian Data: Selectable as little endian or big endian On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit On-chip divider: 32-bit ÷ 32-bit → 32 bits Barrel shifter: 32 bits |
| Memory | ROM | <ul style="list-style-type: none"> Capacity: 16 K /32 K /64 K /96 K /128 K /256 K /384 K /512 Kbytes 32 MHz, no-wait memory access Programming/erasing method: <ul style="list-style-type: none"> Serial programming (asynchronous serial communication/USB communication), self-programming |
| | RAM | <ul style="list-style-type: none"> Capacity: 8 K /10 K /16 K /32 K /64 Kbytes 32 MHz, no-wait memory access |
| | E2 DataFlash | <ul style="list-style-type: none"> Capacity: 8 Kbytes Number of erase/write cycles: 1,000,000 (typ) |
| MCU operating mode | | Single-chip mode |
| Clock | Clock generation circuit | <ul style="list-style-type: none"> Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator Oscillation stop detection: Available Clock frequency accuracy measurement circuit (CAC) Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) <ul style="list-style-type: none"> The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 32 MHz (at max.) Peripheral modules run in synchronization with the PCLK: 32 MHz (at max.) The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.) The ICLK frequency can only be set to FCLK, PCLKB, or PCLKD multiplied by n (n: 1, 2, 4, 8, 16, 32, 64). |
| Resets | | RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset |
| Voltage detection | Voltage detection circuit (LVDAa) | <ul style="list-style-type: none"> When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 1 is capable of selecting the detection voltage from 10 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels |
| Low power consumption | Low power consumption functions | <ul style="list-style-type: none"> Module stop function Three low power consumption modes <ul style="list-style-type: none"> Sleep mode, deep sleep mode, and software standby mode |
| | Function for lower operating power consumption | <ul style="list-style-type: none"> Operating power control modes <ul style="list-style-type: none"> High-speed operating mode, middle-speed operating mode, and low-speed operating mode |
| Interrupt | Interrupt controller (ICUb) | <ul style="list-style-type: none"> Interrupt vectors: 82 External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) Non-maskable interrupts: 4 (NMI pin, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt) 16 levels specifiable for the order of priority |

Table 1.1 Outline of Specifications (2/3)

| Classification | Module/Function | Description |
|-------------------------|---|--|
| DMA | Data transfer controller (DTCa) | <ul style="list-style-type: none"> Transfer modes: Normal transfer, repeat transfer, and block transfer Activation sources: Interrupts Chain transfer function |
| I/O ports | General I/O ports | 64-pin /48-pin /40-pin /36-pin <ul style="list-style-type: none"> I/O: 46/30/24/20 Input: 2/2/1/1 Pull-up resistors: 38/24/19/16 Open-drain outputs: 34/24/19/16 5-V tolerance: 4/4/4/4 |
| | Event link controller (ELC) | <ul style="list-style-type: none"> Event signals of 35 types can be directly connected to the module Operations of timer modules are selectable at event input Capable of event link operation for port B |
| | Multi-function pin controller (MPC) | Capable of selecting the input/output function from multiple pins |
| Timers | Multi-function timer pulse unit 2 (MTU2a) | <ul style="list-style-type: none"> (16 bits × 6 channels) × 1 unit Time bases for the six 16-bit timer channels can be provided via up to 16 pulse-input/output lines and three pulse-input lines Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. Input capture function 21 output compare/input capture registers Pulse output mode Complementary PWM output mode Reset-synchronized PWM mode Phase counting mode Capable of generating conversion start triggers for the A/D converter |
| | Port output enable 2 (POE2a) | Controls the high-impedance state of the MTU's waveform output pins |
| | Compare match timer (CMT) | <ul style="list-style-type: none"> (16 bits × 2 channels) × 1 unit Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512) |
| | Independent watchdog timer (IWDTa) | <ul style="list-style-type: none"> 14 bits × 1 channel Count clock: Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256 |
| | Realtime clock (RTCA) | <ul style="list-style-type: none"> Clock source: Sub-clock Calendar count mode or binary count mode selectable Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt |
| Communication functions | Serial communications interfaces (SC1e, SC1f) | <ul style="list-style-type: none"> 3 channels (channel 1, 5: SC1e, channel 12: SC1f) Serial communications modes: Asynchronous, clock synchronous, and smart card interface On-chip baud rate generator allows selection of the desired bit rate Choice of LSB first or MSB first transfer Average transfer rate clock can be input from MTU2 timers Simple I²C Simple SPI Master/slave mode supported (SC1f only) Start frame and information frame are included (SC1f only) Start-bit detection in asynchronous mode: Low level or falling edge is selectable |
| | I ² C bus interface (RIIC) | <ul style="list-style-type: none"> 1 channel Communications formats: I²C bus format/SMBus format Master mode or slave mode selectable Supports fast mode |
| | Serial peripheral interface (RSPI) | <ul style="list-style-type: none"> 1 channel Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave Data formats Choice of LSB first or MSB first transfer The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Double buffers for both transmission and reception |

Table 1.1 Outline of Specifications (3/3)

| Classification | Module/Function | Description |
|---|-------------------------------------|--|
| Communication function | USB 2.0 host/function module (USBc) | <ul style="list-style-type: none"> • USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. • Host (32-Kbyte or more ROM)/function module: 1 port • Compliant with USB version 2.0 • Transfer speed: Full-speed (12 Mbps), low-speed (1.5 Mbps) • OTG (On-The-Go) is supported. • Isochronous transfer is supported. • BC (Battery Charger) is supported. |
| 12-bit A/D converter (S12ADb) | | <ul style="list-style-type: none"> • 1 unit (1 unit × 14 channels) • 12-bit resolution • Minimum conversion time: 1.0 μs per channel when the ADCLK is operating at 32 MHz • Operating modes <ul style="list-style-type: none"> Scan mode (single scan mode, continuous scan mode, and group scan mode) • Double trigger mode (duplication of A/D conversion data) • A/D conversion start conditions <ul style="list-style-type: none"> A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC |
| Temperature sensor (TEMPSA) | | <ul style="list-style-type: none"> • 1 channel • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter. |
| D/A converter (DA) | | <ul style="list-style-type: none"> • 2 channels • 8-bit resolution • Output voltage: 0 V to VCC |
| CRC calculator (CRC) | | <ul style="list-style-type: none"> • CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: <ul style="list-style-type: none"> $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB first or MSB first communications is selectable. |
| Data operation circuit (DOC) | | Comparison, addition, and subtraction of 16-bit data |
| Unique ID | | 32-byte ID code for the MCU |
| Power supply voltages/Operating frequencies | | VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 3.6 V: 32 MHz |
| Supply current | | 3.2 mA at 32 MHz (typ.) |
| Operating temperature range | | D version: -40 to +85°C, G version: -40 to +105°C |
| Packages | | 64-pin LQFP (PLQP0064KB-A) 10 × 10 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch 64-pin WFLGA (PWLG0064KA-A) 5 × 5 mm, 0.5 mm pitch 48-pin LQFP (PLQP0048KB-A) 7 × 7 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch 40-pin HWQFN (PWQN0040KC-A) 6 × 6 mm, 0.50 mm pitch 36-pin WFLGA (PWLG0036KA-A) 4 × 4 mm, 0.5 mm pitch |
| On-chip debugging system | | E1 emulator (FINE interface) |

Table 1.2 Comparison of Functions for Different Packages

| Module/Functions | | RX111 Group | | | |
|--|--|--|--|----------------------------|---|
| | | 64 Pins | 48 Pins | 40 Pins | 36 Pins |
| Interrupts | External interrupts | NMI, IRQ0 to IRQ7 | | | |
| DMA | Data transfer controller | Supported | | | |
| Timers | Multi-function timer pulse unit 2 | 6 channels (MTU0 to MTU5) | | | |
| | Port output enable 2 | POE0# to POE3#, POE8# | | POE0#, POE2#, POE3#, POE8# | |
| | Compare match timer | 2 channels x 1 unit | | | |
| | Realtime clock | Supported | | Not supported | |
| | Independent watchdog timer | Supported | | | |
| Communication functions | Serial communications interfaces [simple I ² C, simple SPI] | 2 channels (SCI1, SCI5) | | | |
| | Serial communications interface [simple I ² C, simple SPI] | 1 channel (SCI12) | | | |
| | I ² C bus interface | 1 channel | | | |
| | Serial peripheral interface | 1 channel | 1 channel (SSLA1 and SSLA3 are not supported) | | 1 channel (SSLA1 to SSLA3 are not supported) |
| | USB 2.0 host/function module (USBc) | 1 channel (Host/Function/ OTG) | 1 channel (Host/Function) | | |
| 12-bit A/D converter (including high-precision channels) | | 14 channels (6 channels) | 10 channels (4 channels) | 8 channels (3 channels) | 7 channels (2 channels) |
| D/A converter | | 2 channels | Not supported | | |
| Temperature sensor | | Supported | | | |
| CRC calculator | | Supported | | | |
| Event link controller | | Supported | | | |
| Packages | | 64-pin LQFP 64-pin LQFP 64-pin WFLGA | 48-pin LQFP 48-pin HWQFN | 40-pin HWQFN | 36-pin WFLGA |

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products (1/2)

| Group | Part No. | Orderable Part No. | Package | ROM Capacity | RAM Capacity | E2 DataFlash | Maximum Operating Frequency | Operating Temperature |
|--------------|-----------------|--------------------|--------------|--------------|--------------|--------------|-----------------------------|-----------------------|
| RX111 | R5F51118AGFM | R5F51118AGFM#3A | PLQP0064KB-A | 512 Kbytes | 64 Kbytes | 8 Kbytes | 32 MHz | -40 to +105°C |
| | R5F51118AGFK | R5F51118AGFK#3A | PLQP0064GA-A | | | | | |
| | R5F51118AGFL | R5F51118AGFL#3A | PLQP0048KB-A | | | | | |
| | R5F51118AGNE | R5F51118AGNE#UA | PWQN0048KB-A | | | | | |
| | R5F51117AGFM | R5F51117AGFM#3A | PLQP0064KB-A | 384 Kbytes | | | | |
| | R5F51117AGFK | R5F51117AGFK#3A | PLQP0064GA-A | | | | | |
| | R5F51117AGFL | R5F51117AGFL#3A | PLQP0048KB-A | | | | | |
| | R5F51117AGNE | R5F51117AGNE#UA | PWQN0048KB-A | | | | | |
| | R5F51116AGFM | R5F51116AGFM#3A | PLQP0064KB-A | 256 Kbytes | 32 Kbytes | | | |
| | R5F51116AGFK | R5F51116AGFK#3A | PLQP0064GA-A | | | | | |
| | R5F51116AGFL | R5F51116AGFL#3A | PLQP0048KB-A | | | | | |
| | R5F51116AGNE | R5F51116AGNE#UA | PWQN0048KB-A | | | | | |
| | R5F51115AGFM | R5F51115AGFM#3A | PLQP0064KB-A | 128 Kbytes | 16 Kbytes | | | |
| | R5F51115AGFK | R5F51115AGFK#3A | PLQP0064GA-A | | | | | |
| | R5F51115AGFL | R5F51115AGFL#3A | PLQP0048KB-A | | | | | |
| | R5F51115AGNE | R5F51115AGNE#UA | PWQN0048KB-A | | | | | |
| | R5F51114AGFM | R5F51114AGFM#3A | PLQP0064KB-A | 96 Kbytes | | | | |
| | R5F51114AGFK | R5F51114AGFK#3A | PLQP0064GA-A | | | | | |
| | R5F51114AGFL | R5F51114AGFL#3A | PLQP0048KB-A | | | | | |
| | R5F51114AGNE | R5F51114AGNE#UA | PWQN0048KB-A | | | | | |
| | R5F51113AGFM | R5F51113AGFM#3A | PLQP0064KB-A | 64 Kbytes | 10 Kbytes | | | |
| | R5F51113AGFK | R5F51113AGFK#3A | PLQP0064GA-A | | | | | |
| | R5F51113AGFL | R5F51113AGFL#3A | PLQP0048KB-A | | | | | |
| | R5F51113AGNE | R5F51113AGNE#UA | PWQN0048KB-A | | | | | |
| R5F51113AGNF | R5F51113AGNF#UA | PWQN0040KC-A | | | | | | |
| R5F51111AGFM | R5F51111AGFM#3A | PLQP0064KB-A | 32 Kbytes | | | | | |
| R5F51111AGFK | R5F51111AGFK#3A | PLQP0064GA-A | | | | | | |
| R5F51111AGFL | R5F51111AGFL#3A | PLQP0048KB-A | | | | | | |
| R5F51111AGNE | R5F51111AGNE#UA | PWQN0048KB-A | | | | | | |
| R5F51111AGNF | R5F51111AGNF#UA | PWQN0040KC-A | | | | | | |
| R5F5111JAGFM | R5F5111JAGFM#3A | PLQP0064KB-A | 16 Kbytes | 8 Kbytes | | | | |
| R5F5111JAGFK | R5F5111JAGFK#3A | PLQP0064GA-A | | | | | | |
| R5F5111JAGFL | R5F5111JAGFL#3A | PLQP0048KB-A | | | | | | |
| R5F5111JAGNE | R5F5111JAGNE#UA | PWQN0048KB-A | | | | | | |
| R5F5111JAGNF | R5F5111JAGNF#UA | PWQN0040KC-A | | | | | | |

Table 1.3 List of Products (2/2)

| Group | Part No. | Orderable Part No. | Package | ROM Capacity | RAM Capacity | E2 DataFlash | Maximum Operating Frequency | Operating Temperature |
|--------------|-----------------|--------------------|--------------|--------------|--------------|--------------|-----------------------------|-----------------------|
| RX111 | R5F51118ADFM | R5F51118ADFM#3A | PLQP0064KB-A | 512 Kbytes | 64 Kbytes | 8 Kbytes | 32 MHz | -40 to +85°C |
| | R5F51118ADFK | R5F51118ADFK#3A | PLQP0064GA-A | | | | | |
| | R5F51118ADLF | R5F51118ADLF#UA | PWLG0064KA-A | | | | | |
| | R5F51118ADFL | R5F51118ADFL#3A | PLQP0048KB-A | | | | | |
| | R5F51118ADNE | R5F51118ADNE#UA | PWQN0048KB-A | | | | | |
| | R5F51117ADFM | R5F51117ADFM#3A | PLQP0064KB-A | 384 Kbytes | | | | |
| | R5F51117ADFK | R5F51117ADFK#3A | PLQP0064GA-A | | | | | |
| | R5F51117ADLF | R5F51117ADLF#UA | PWLG0064KA-A | | | | | |
| | R5F51117ADFL | R5F51117ADFL#3A | PLQP0048KB-A | | | | | |
| | R5F51117ADNE | R5F51117ADNE#UA | PWQN0048KB-A | | | | | |
| | R5F51116ADFM | R5F51116ADFM#3A | PLQP0064KB-A | 256 Kbytes | 32 Kbytes | | | |
| | R5F51116ADFK | R5F51116ADFK#3A | PLQP0064GA-A | | | | | |
| | R5F51116ADLF | R5F51116ADLF#UA | PWLG0064KA-A | | | | | |
| | R5F51116ADFL | R5F51116ADFL#3A | PLQP0048KB-A | | | | | |
| | R5F51116ADNE | R5F51116ADNE#UA | PWQN0048KB-A | | | | | |
| | R5F51115ADFM | R5F51115ADFM#3A | PLQP0064KB-A | 128 Kbytes | 16 Kbytes | | | |
| | R5F51115ADFK | R5F51115ADFK#3A | PLQP0064GA-A | | | | | |
| | R5F51115ADLF | R5F51115ADLF#UA | PWLG0064KA-A | | | | | |
| | R5F51115ADFL | R5F51115ADFL#3A | PLQP0048KB-A | | | | | |
| | R5F51115ADNE | R5F51115ADNE#UA | PWQN0048KA-A | | | | | |
| | R5F51114ADFM | R5F51114ADFM#3A | PLQP0064KB-A | 96 Kbytes | | | | |
| | R5F51114ADFK | R5F51114ADFK#3A | PLQP0064GA-A | | | | | |
| | R5F51114ADLF | R5F51114ADLF#UA | PWLG0064KA-A | | | | | |
| | R5F51114ADFL | R5F51114ADFL#3A | PLQP0048KB-A | | | | | |
| | R5F51114ADNE | R5F51114ADNE#UA | PWQN0048KB-A | | | | | |
| | R5F51113ADFM | R5F51113ADFM#3A | PLQP0064KB-A | 64 Kbytes | 10 Kbytes | | | |
| | R5F51113ADFK | R5F51113ADFK#3A | PLQP0064GA-A | | | | | |
| | R5F51113ADLF | R5F51113ADLF#UA | PWLG0064KA-A | | | | | |
| | R5F51113ADFL | R5F51113ADFL#3A | PLQP0048KB-A | | | | | |
| | R5F51113ADNE | R5F51113ADNE#UA | PWQN0048KB-A | | | | | |
| | R5F51113ADLM | R5F51113ADLM#UA | PWLG0036KA-A | | | | | |
| | R5F51113ADNF | R5F51113ADNF#UA | PWQN0040KC-A | | | | | |
| R5F51111ADFM | R5F51111ADFM#3A | PLQP0064KB-A | 32 Kbytes | | | | | |
| R5F51111ADFK | R5F51111ADFK#3A | PLQP0064GA-A | | | | | | |
| R5F51111ADLF | R5F51111ADLF#UA | PWLG0064KA-A | | | | | | |
| R5F51111ADFL | R5F51111ADFL#3A | PLQP0048KB-A | | | | | | |
| R5F51111ADNE | R5F51111ADNE#UA | PWQN0048KB-A | | | | | | |
| R5F51111ADLM | R5F51111ADLM#UA | PWLG0036KA-A | | | | | | |
| R5F51111ADNF | R5F51111ADNF#UA | PWQN0040KC-A | | | | | | |
| R5F5111JADFM | R5F5111JADFM#3A | PLQP0064KB-A | 16 Kbytes | 8 Kbytes | | | | |
| R5F5111JADFK | R5F5111JADFK#3A | PLQP0064GA-A | | | | | | |
| R5F5111JADLF | R5F5111JADLF#UA | PWLG0064KA-A | | | | | | |
| R5F5111JADFL | R5F5111JADFL#3A | PLQP0048KB-A | | | | | | |
| R5F5111JADNE | R5F5111JADNE#UA | PWQN0048KB-A | | | | | | |
| R5F5111JADLM | R5F5111JADLM#UA | PWLG0036KA-A | | | | | | |
| R5F5111JADNF | R5F5111JADNF#UA | PWQN0040KC-A | | | | | | |

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

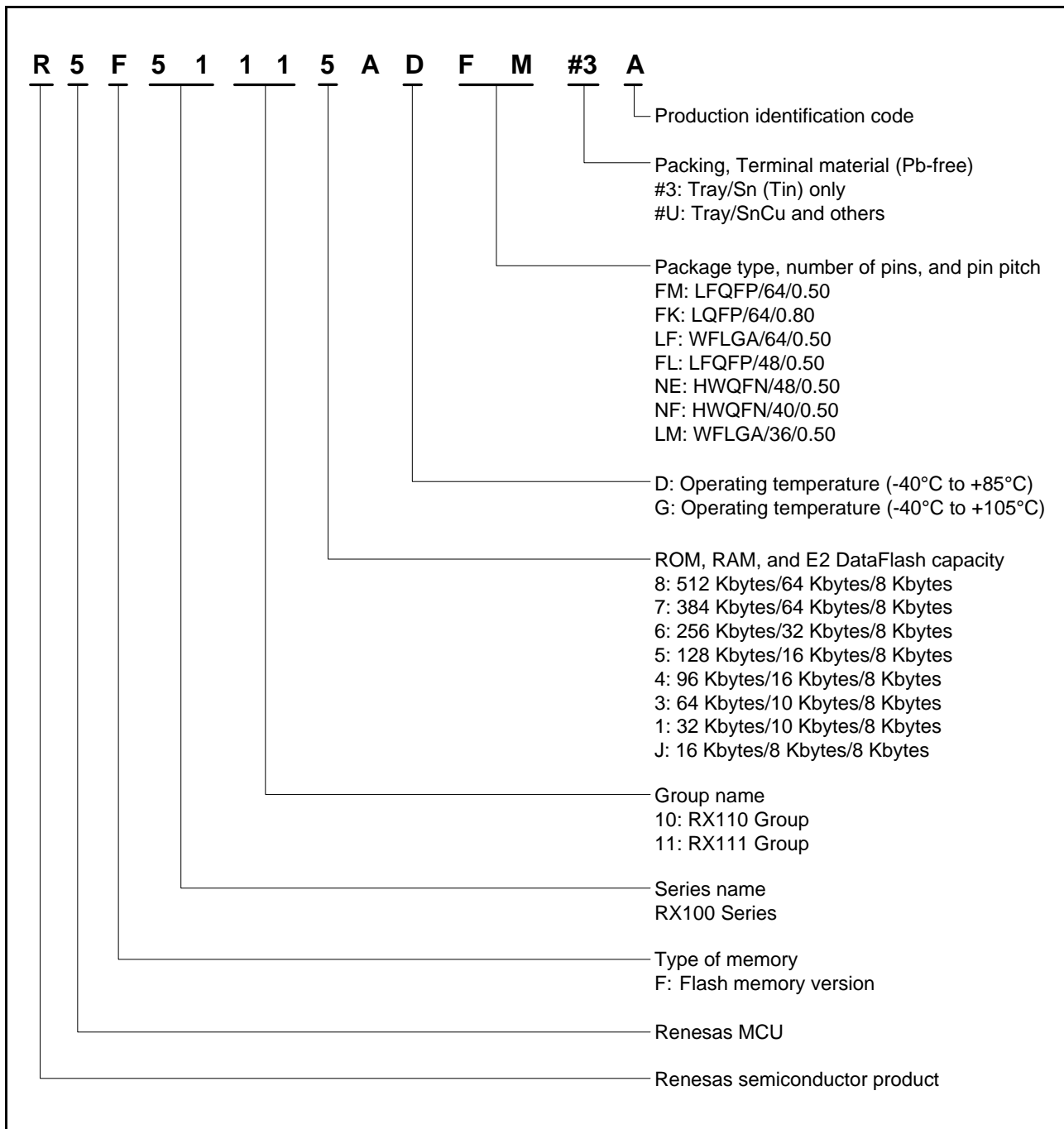


Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type

1.3 Block Diagram

Figure 1.2 shows a block diagram.

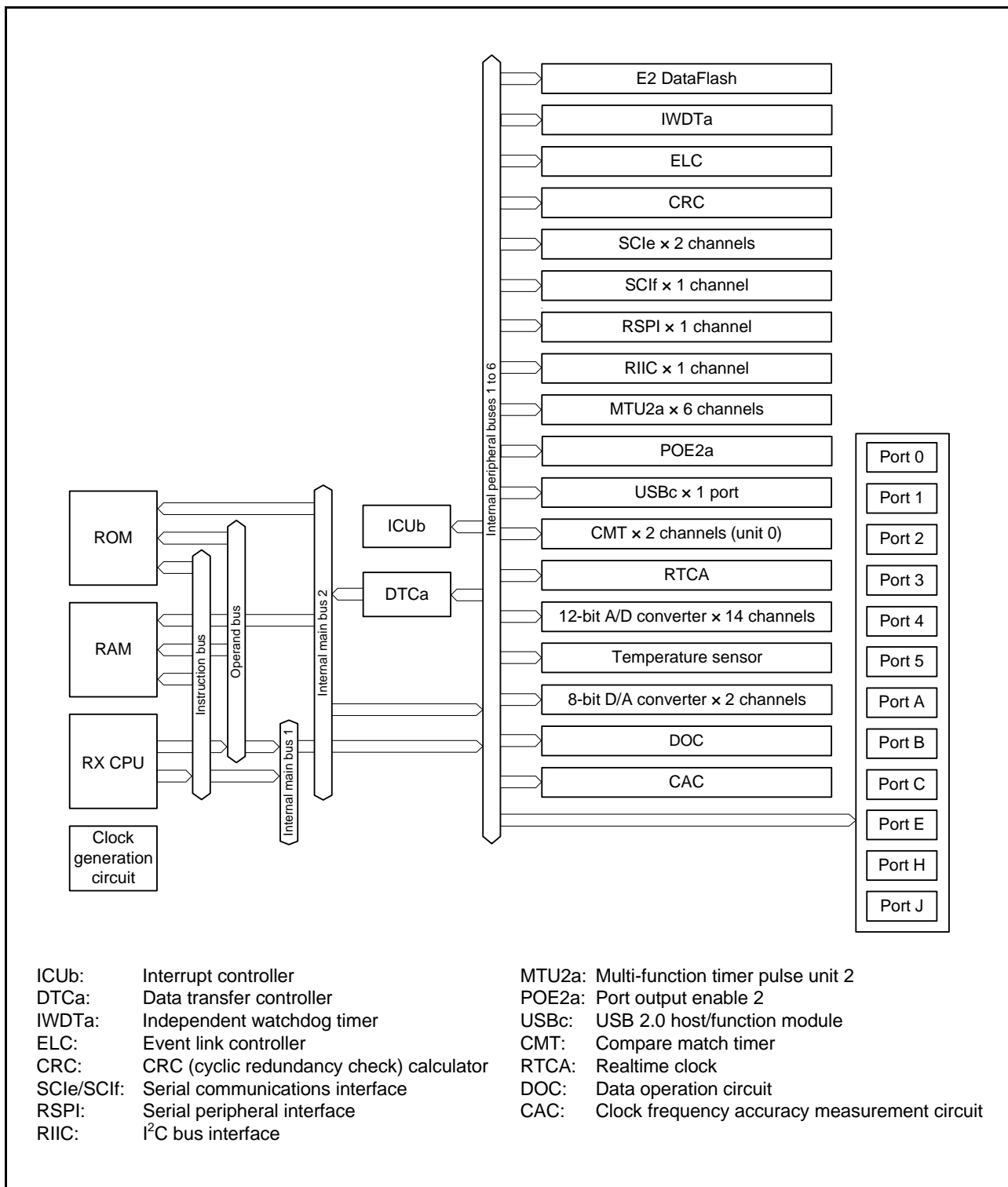


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

| Classifications | Pin Name | I/O | Description |
|-----------------------------------|--------------------------------------|---------------------|--|
| Power supply | VCC | Input | Power supply pin. Connect it to the system power supply. |
| | VCL | — | Connect this pin to the VSS pin via the 4.7 μ F smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| | VCC_USB | Input | Power supply pin for USB. Connect this pin to VCC. |
| | VSS_USB | Input | Ground pin for USB. Connect this pin to VSS. |
| Analog power supply | AVCC0 | Input | Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC when not using the 12-bit A/D converter. |
| | AVSS0 | Input | Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS when not using the 12-bit A/D converter. |
| | VREFH0 | Input | Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC when not using the 12-bit A/D converter. |
| | VREFL0 | Input | Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS when not using the 12-bit A/D converter. |
| Clock | XTAL | Output/ Input *1 | Pins for connecting a crystal. An external clock can be input through the XTAL pin. |
| | EXTAL | Input | |
| | XCIN | Input | Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOU. |
| | XCOU | Output | |
| | CLKOUT | Output | Clock output pin. |
| Operating mode control | MD | Input | Pin for setting the operating mode. The signal levels on this pin must not be changed during operation. |
| | UB# | Input | Pin used for boot mode (USB interface). |
| | UPSEL | Input | Pin used for boot mode (USB interface). |
| System control | RES# | Input | Reset pin. This MCU enters the reset state when this signal goes low. |
| CAC | CACREF | Input | Input pin for the clock frequency accuracy measurement circuit. |
| On-chip emulator | FINED | I/O | FINE interface pin. |
| LVD | CMPA2 | Input | Detection target voltage pin for voltage detection 2 |
| Interrupts | NMI | Input | Non-maskable interrupt request pin. |
| | IRQ0 to IRQ7 | Input | Interrupt request pins. |
| Multi-function timer pulse unit 2 | MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins. |
| | MTIOC1A, MTIOC1B | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins. |
| | MTIOC2A, MTIOC2B | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins. |
| | MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins. |
| | MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D | I/O | The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins. |
| | MTIC5U, MTIC5V, MTIC5W | Input | The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins. |
| | MTCLKA, MTCLKB, MTCLKC, MTCLKD | Input | Input pins for the external clock. |
| Port output enable 2 | POE0# to POE3#, POE8# | Input | Input pins for request signals to place the MTU pins in the high impedance state. |

Table 1.4 Pin Functions (2/3)

| Classifications | Pin Name | I/O | Description | |
|--|--|--------|--|--|
| Realtime clock | RTCOUT | Output | Output pin for the 1-Hz/64-Hz clock. | |
| Serial communications interface (SC1e) | • Asynchronous mode/clock synchronous mode | | | |
| | SCK1, SCK5 | I/O | Input/output pins for the clock. | |
| | RXD1, RXD5 | Input | Input pins for received data. | |
| | TXD1, TXD5 | Output | Output pins for transmitted data. | |
| | CTS1#, CTS5# | Input | Input pins for controlling the start of transmission and reception. | |
| | RTS1#, RTS5# | Output | Output pins for controlling the start of transmission and reception. | |
| Serial communications interface (SC1e) | • Simple I ² C mode | | | |
| | SSCL1, SSCL5 | I/O | Input/output pins for the I ² C clock. | |
| | SSDA1, SSDA5 | I/O | Input/output pins for the I ² C data. | |
| | • Simple SPI mode | | | |
| | SCK1, SCK5 | I/O | Input/output pins for the clock. | |
| | SMISO1, SMISO5 | I/O | Input/output pins for slave transmit data. | |
| | SMOSI1, SMOSI5 | I/O | Input/output pins for master transmit data. | |
| | SS1#, SS5# | Input | Chip-select input pins. | |
| Serial communications interface (SC1f) | • Asynchronous mode/clock synchronous mode | | | |
| | SCK12 | I/O | Input/output pin for the clock. | |
| | RXD12 | Input | Input pin for receiving data. | |
| | TXD12 | Output | Output pin for transmitting data. | |
| | CTS12# | Input | Input pin for controlling the start of transmission and reception. | |
| | RTS12# | Output | Output pin for controlling the start of transmission and reception. | |
| | • Simple I ² C mode | | | |
| | SSCL12 | I/O | Input/output pin for the I ² C clock. | |
| | SSDA12 | I/O | Input/output pin for the I ² C data. | |
| | • Simple SPI mode | | | |
| | SCK12 | I/O | Input/output pin for the clock. | |
| | SMISO12 | I/O | Input/output pin for slave transmit data. | |
| | SMOSI12 | I/O | Input/output pin for master transmit data. | |
| | SS12# | Input | Chip-select input pin. | |
| | • Extended serial mode | | | |
| | RXDX12 | Input | Input pin for data reception by SC1f. | |
| | TXDX12 | Output | Output pin for data transmission by SC1f. | |
| | SIOX12 | I/O | Input/output pin for data reception or transmission by SC1f. | |
| | I ² C bus interface | SCL0 | I/O | Input/output pin for I ² C bus interface clocks. Bus can be directly driven by the N-channel open drain output. |
| | | SDA0 | I/O | Input/output pin for I ² C bus interface data. Bus can be directly driven by the N-channel open drain output. |
| Serial peripheral interface | RSPCKA | I/O | Input/output pin for the RSPI clock. | |
| | MOSIA | I/O | Input/output pin for transmitting data from the RSPI master. | |
| | MISOA | I/O | Input/output pin for transmitting data from the RSPI slave. | |
| | SSLA0 | I/O | Input/output pin to select the slave for the RSPI. | |
| | SSLA1 to SSLA3 | Output | Output pins to select the slave for the RSPI. | |

Table 1.4 Pin Functions (3/3)

| Classifications | Pin Name | I/O | Description |
|----------------------------------|--|--------|---|
| USB 2.0 host/ function module | USB0_DP | I/O | D+ I/O pin of the USB on-chip transceiver. |
| | USB0_DM | I/O | D- I/O pin of the USB on-chip transceiver. |
| | USB0_VBUS | Input | USB cable connection monitor pin. |
| | USB0_EXICEN | Output | Low-power control signal for the OTG chip. |
| | USB0_VBUSEN | Output | VBUS (5 V) supply enable signal for the OTG chip. |
| | USB0_OVRCURA, USB0_OVRCURB | Input | External overcurrent detection pins. |
| | USB0_ID | Input | Mini-AB connector ID input pin during operation in OTG mode. |
| 12-bit A/D converter | AN000 to AN004, AN006, AN008 to AN015 | Input | Input pins for the analog signals to be processed by the A/D converter. |
| | ADTRG0# | Input | Input pin for the external trigger signals that start the A/D conversion. |
| D/A converter | DA0, DA1 | Output | Output pins for the analog signals to be processed by the D/A converter. |
| I/O ports | P03, P05 | I/O | 2-bit input/output pins. |
| | P14 to P17 | I/O | 4-bit input/output pins. |
| | P26, P27 | I/O | 2-bit input/output pins. |
| | P30 to P32, P35 | I/O | 4-bit input/output pins (P35 input pin). |
| | P40 to P44, P46 | I/O | 6-bit input/output pins. |
| | P54, P55 | I/O | 2-bit input/output pins. |
| | PA0, PA1, PA3, PA4, PA6 | I/O | 5-bit input/output pins. |
| | PB0, PB1, PB3, PB5 to PB7 | I/O | 6-bit input/output pins. |
| | PC0 to PC7 | I/O | 8-bit input/output pins. |
| | PE0 to PE7 | I/O | 8-bit input/output pins. |
| | PH7 | Input | 1-bit input pin. |
| | PJ6, PJ7 | I/O | 2-bit input/output pins. |

Note 1. For external clock input.

1.5 Pin Assignments

Figure 1.3 to Figure 1.7 show the pin assignments. Table 1.5 to Table 1.9 show the lists of pins and pin functions.

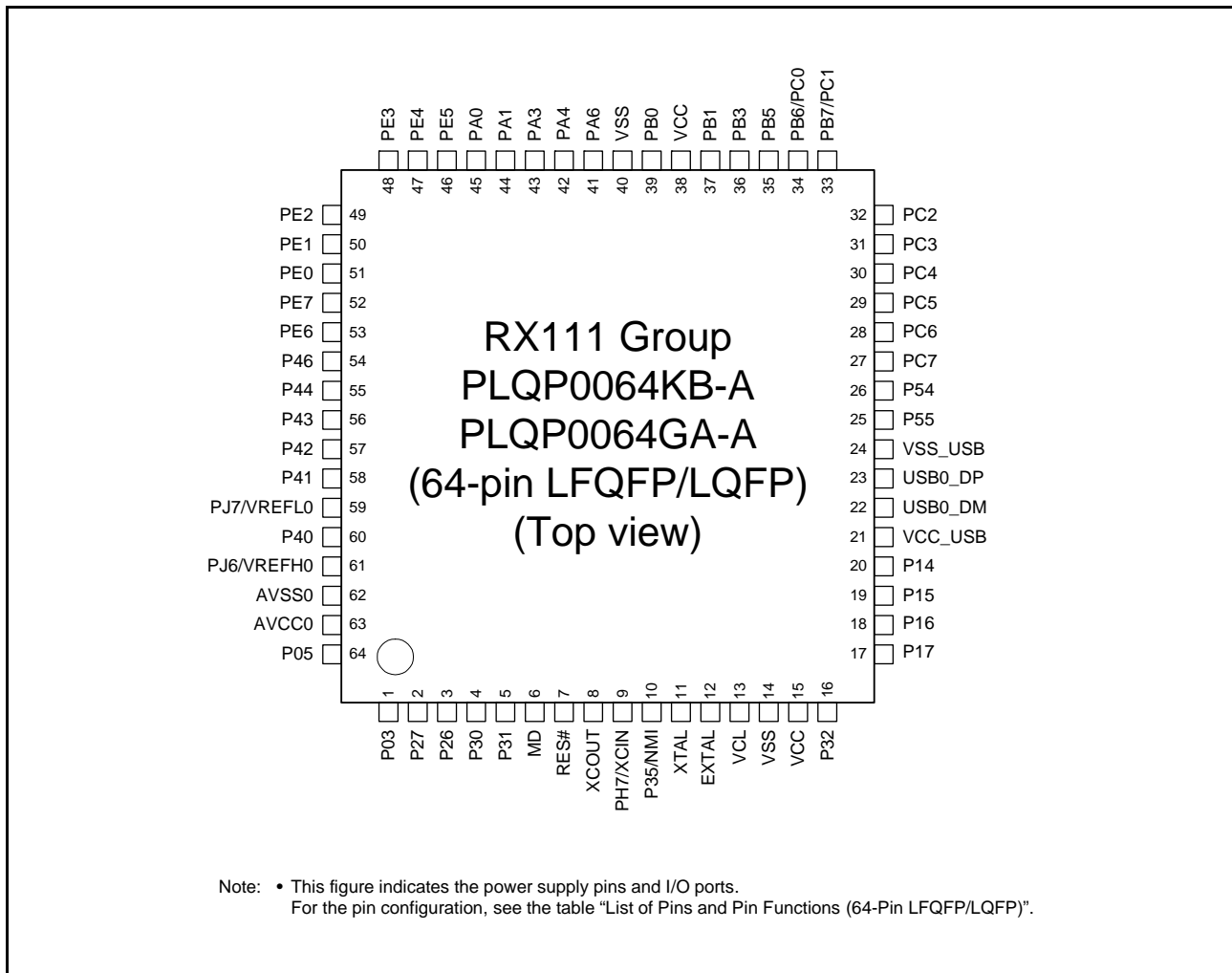


Figure 1.3 Pin Assignments of the 64-Pin LQFP/LQFP

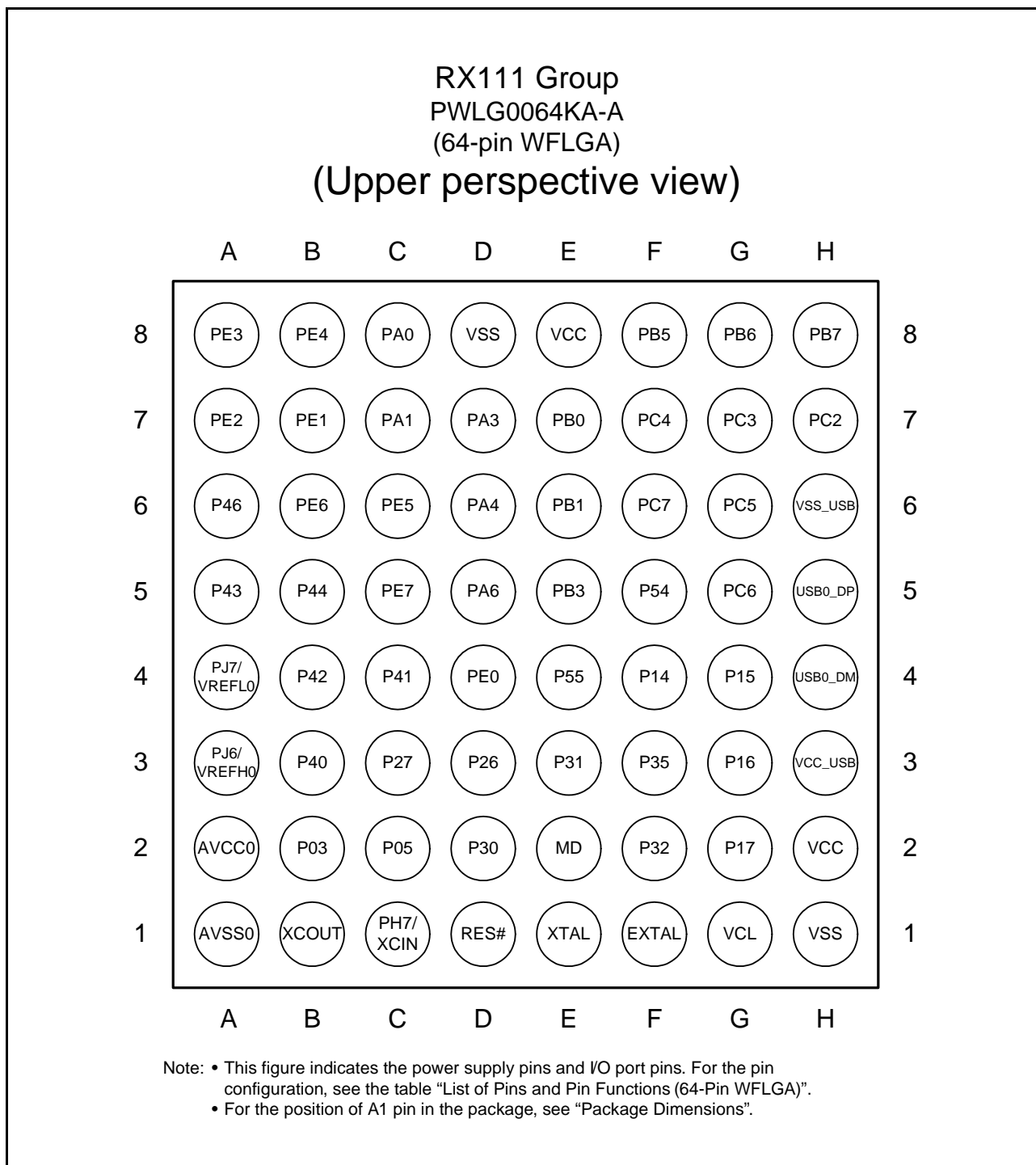


Figure 1.4 Pin Assignments of the 64-Pin WFLGA

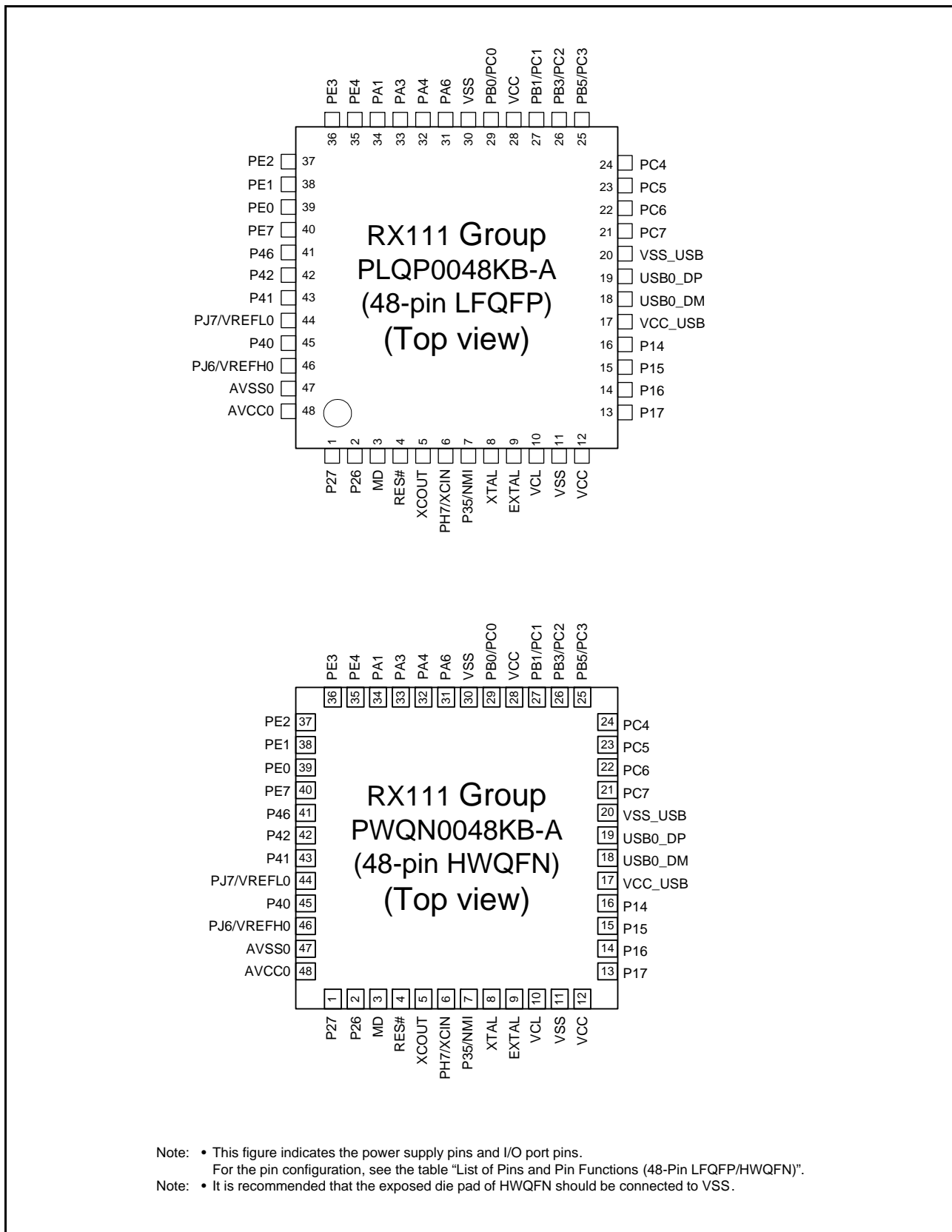


Figure 1.5 Pin Assignments of the 48-Pin LQFP/HWQFN

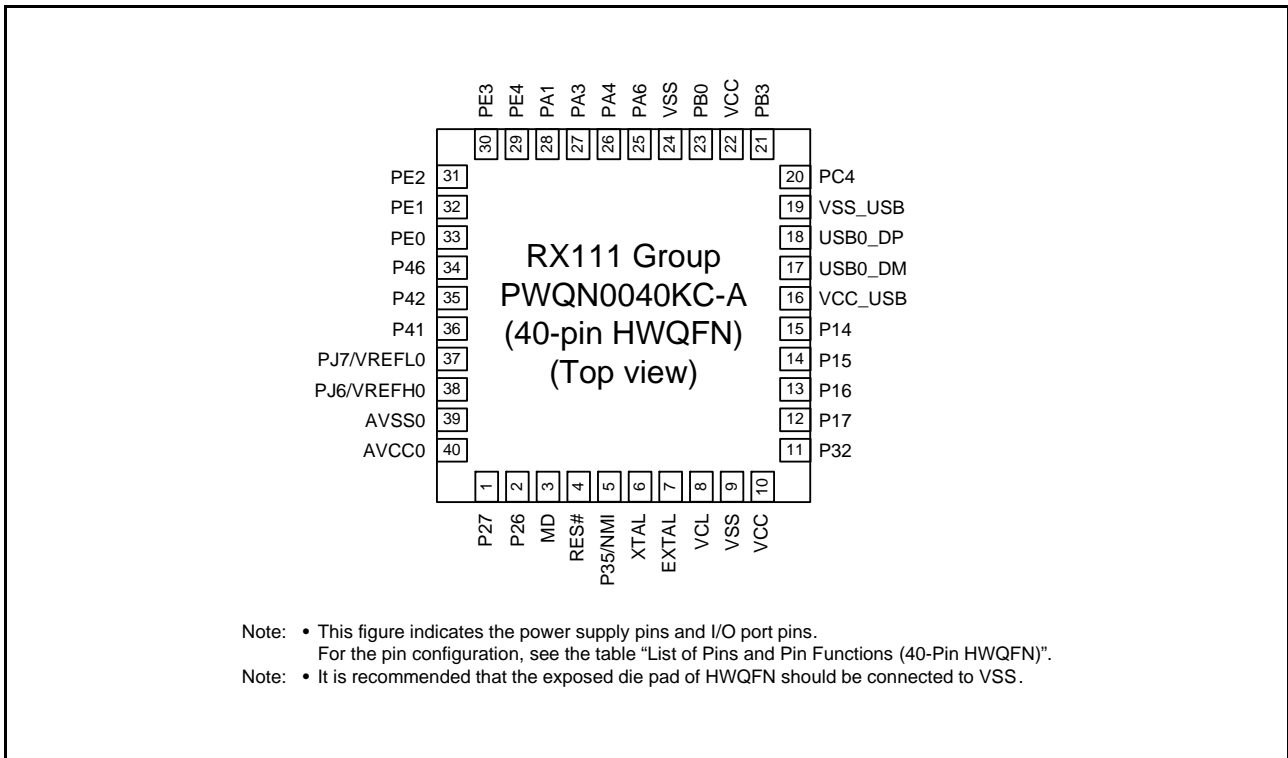


Figure 1.6 Pin Assignments of the 40-Pin HWQFN



Figure 1.7 Pin Assignments of the 36-Pin WFLGA

Table 1.5 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (1/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, POE, RTC) | Communication (SCle, SCIf, RSPI, RIIC, USB) | Others |
|---------|-------------------------------------|----------|-----------------------------------|---|-------------------------------|
| 1 | | P03 | | | DA0 |
| 2 | | P27 | MTIOC2B | SCK1/SCK12 | IRQ3/CMPA2/ CACREF/ADTRG0# |
| 3 | | P26 | MTIOC2A | TXD1/SMOS1/SSDA1/USB0_VBUSEN | |
| 4 | | P30 | MTIOC4B/POE8# | RXD1/SMISO1/SSCL1 | IRQ0 |
| 5 | | P31 | MTIOC4D | CTS1#/RTS1#/SS1# | IRQ1 |
| 6 | MD | | | | FINED |
| 7 | RES# | | | | |
| 8 | XCOUT | | | | |
| 9 | XCIN | PH7 | | | |
| 10 | UPSEL | P35 | | | NMI |
| 11 | XTAL | | | | |
| 12 | EXTAL | | | | |
| 13 | VCL | | | | |
| 14 | VSS | | | | |
| 15 | VCC | | | | |
| 16 | | P32 | MTIOC0C/RTCOUT | | IRQ2 |
| 17 | | P17 | MTIOC0C/MTIOC3A/ MTIOC3B/POE8# | SCK1/MISOA/SDA0/RXD12/RXD12/ SMISO12/SSCL12 | IRQ7 |
| 18 | | P16 | MTIOC3C/MTIOC3D/ RTCOUT | TXD1/SMOS1/SSDA1/MOSIA/SCL0/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB | IRQ6/ADTRG0# |
| 19 | | P15 | MTIOC0B/MTCLKB | RXD1/SMISO1/SSCL1/RSPCKA | IRQ5/CLKOUT |
| 20 | UB# | P14 | MTIOC0A/MTIOC3A/ MTCLKA | CTS1#/RTS1#/SS1#/SSLA0/TXD12/ TXD12/SIOX12/SMOS112/SSDA12/ USB0_OVRCURA | IRQ4 |
| 21 | VCC_USB | | | | |
| 22 | | | | USB0_DM | |
| 23 | | | | USB0_DP | |
| 24 | VSS_USB | | | | |
| 25 | | P55 | MTIOC4D | | |
| 26 | | P54 | MTIOC4B | | |
| 27 | | PC7 | MTIOC3A/MTCLKB | TXD1/SMOS1/SSDA1/MISOA/ USB0_OVRCURB | CACREF |
| 28 | | PC6 | MTIOC3C/MTCLKA | RXD1/SMISO1/SSCL1/MOSIA/ USB0_EXICEN | |
| 29 | | PC5 | MTIOC3B/MTCLKD | SCK1/RSPCKA/USB0_ID | |
| 30 | | PC4 | MTIOC3D/MTCLKC/POE0# | SCK5/SSLA0/USB0_VBUS*/ USB0_VBUSEN | IRQ2/CLKOUT |
| 31 | | PC3 | MTIOC4D | TXD5/SMOS5/SSDA5 | |
| 32 | | PC2 | MTIOC4B | RXD5/SMISO5/SSCL5/SSLA3 | |
| 33 | | PB7/PC1 | MTIOC3B | | |
| 34 | | PB6/PC0 | MTIOC3D | | |
| 35 | | PB5 | MTIOC2A/MTIOC1B/POE1# | | |
| 36 | | PB3 | MTIOC0A/MTIOC3B/ MTIOC4A/POE3# | USB0_OVRCURA | |
| 37 | | PB1 | MTIOC0C/MTIOC4C | | IRQ4 |
| 38 | VCC | | | | |
| 39 | | PB0 | MTIC5W/MTIOC0C/ RTCOUT | SCL0/RSPCKA | IRQ2/ADTRG0# |
| 40 | VSS | | | | |
| 41 | | PA6 | MTIC5V/MTCLKB/MTIOC2A/ POE2# | CTS5#/RTS5#/SS5#/SDA0/MOSIA | IRQ3 |

Table 1.5 List of Pins and Pin Functions (64-Pin LQFP/LQFP) (2/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, POE, RTC) | Communication (SCle, SCIf, RSPI, RIIC, USB) | Others |
|---------|-------------------------------------|----------|-------------------------------|---|------------|
| 42 | | PA4 | MTIC5U/MTCLKA/MTIOC2B | TXD5/SMOSI5/SSDA5/SSLA0 | IRQ5 |
| 43 | | PA3 | MTIOC0D/MTCLKD/MTIOC1B/POE0# | RXD5/SMISO5/SSCL5/MISOA | IRQ6 |
| 44 | | PA1 | MTIOC0B/MTCLKC/RTCOUT | SCK5/SSLA2 | |
| 45 | | PA0 | MTIOC4A | SSLA1 | CACREF |
| 46 | | PE5 | MTIOC4C/MTIOC2B | | IRQ5/AN013 |
| 47 | | PE4 | MTIOC4D/MTIOC1A/MTIOC3A | MOSIA | IRQ4/AN012 |
| 48 | | PE3 | MTIOC0A/MTIOC1B/MTIOC4B/POE8# | CTS12#/RTS12#/SS12#/RSPCKA | IRQ3/AN011 |
| 49 | | PE2 | MTIOC4A | RXD12/RXDX12/SMISO12/SSCL12 | IRQ7/AN010 |
| 50 | | PE1 | MTIOC4C | TXD12/TXDX12/SIOX12/SMOSI12/SSDA12 | IRQ1/AN009 |
| 51 | | PE0 | MTIOC2A/POE3# | SCK12 | IRQ0/AN008 |
| 52 | | PE7 | | | IRQ7/AN015 |
| 53 | | PE6 | | | IRQ6/AN014 |
| 54 | | P46*2 | | | AN006 |
| 55 | | P44*2 | | | AN004 |
| 56 | | P43*2 | | | AN003 |
| 57 | | P42*2 | | | AN002 |
| 58 | | P41*2 | | | AN001 |
| 59 | VREFL0 | PJ7*2 | | | |
| 60 | | P40*2 | | | AN000 |
| 61 | VREFH0 | PJ6*2 | | | |
| 62 | AVSS0 | | | | |
| 63 | AVCC0 | | | | |
| 64 | | P05 | | | DA1 |

Note 1. Not 5 V tolerant.

Note 2. The power source of the I/O buffer for these pins is AVCC0.

Table 1.6 List of Pins and Pin Functions (64-Pin WFLGA) (1/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, POE, RTC) | Communication (SCIE, SCIf, RSPI, RIIC, USB) | Others |
|---------|-------------------------------------|----------|-----------------------------------|---|-------------------------------|
| A1 | AVSS0 | | | | |
| A2 | AVCC0 | | | | |
| A3 | VREFH0 | PJ6*2 | | | |
| A4 | VREFL0 | PJ7*2 | | | |
| A5 | | P43*2 | | | AN003 |
| A6 | | P46*2 | | | AN006 |
| A7 | | PE2 | MTIOC4A | RXD12/RXDX12/SMISO12/SSCL12 | IRQ7/AN010 |
| A8 | | PE3 | MTIOC0A/MTIOC1B/ MTIOC4B/POE8# | CTS12#/RTS12#/SS12#/RSPCKA | IRQ3/AN011 |
| B1 | XCOUT | | | | |
| B2 | | P03 | | | DA0 |
| B3 | | P40*2 | | | AN000 |
| B4 | | P42*2 | | | AN002 |
| B5 | | P44*2 | | | AN004 |
| B6 | | PE6 | | | IRQ6/AN014 |
| B7 | | PE1 | MTIOC4C | TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12 | IRQ1/AN009 |
| B8 | | PE4 | MTIOC1A/MTIOC3A/ MTIOC4D | MOSIA | IRQ4/AN012 |
| C1 | XCIN | PH7 | | | |
| C2 | | P05 | | | DA1 |
| C3 | | P27 | MTIOC2B | SCK1/SCK12 | IRQ3/CMPA2/CACREF/ ADTRG0# |
| C4 | | P41*2 | | | AN001 |
| C5 | | PE7 | | | IRQ7/AN015 |
| C6 | | PE5 | MTIOC2B/MTIOC4C | | IRQ5/AN013 |
| C7 | | PA1 | MTIOC0B/MTCLKC/ RTCOUT | SCK5/SSLA2 | |
| C8 | | PA0 | MTIOC4A | SSLA1 | CACREF |
| D1 | RES# | | | | |
| D2 | | P30 | MTIOC4B/POE8# | RXD1/SMISO1/SSCL1 | IRQ0 |
| D3 | | P26 | MTIOC2A | TXD1/SMOSI1/SSDA1/ USB0_VBUSEN | |
| D4 | | PE0 | MTIOC2A/POE3# | SCK12 | IRQ0/AN008 |
| D5 | | PA6 | MTIC5V/MTIOC2A/MTCLKB/ POE2# | CTS5#/RTS5#/SS5#/SDA0/MOSIA | IRQ3 |
| D6 | | PA4 | MTIC5U/MTIOC2B/MTCLKA | TXD5/SMOSI5/SSDA5/SSLA0 | IRQ5 |
| D7 | | PA3 | MTIOC0D/MTCLKD/ MTIOC1B/POE0# | RXD5/SMISO5/SSCL5/MISOA | IRQ6 |
| D8 | VSS | | | | |
| E1 | XTAL | | | | |
| E2 | MD | | | | FINED |
| E3 | | P31 | MTIOC4D | CTS1#/RTS1#/SS1# | IRQ1 |
| E4 | | P55 | MTIOC4D | | |
| E5 | | PB3 | MTIOC0A/MTIOC3B/ MTIOC4A/POE3# | USB0_OVRCURA | |
| E6 | | PB1 | MTIOC0C/MTIOC4C | | IRQ4 |
| E7 | | PB0 | MTIC5W/MTIOC0C/ RTCOUT | SCL0/RSPCKA | IRQ2/ADTRG0# |
| E8 | VCC | | | | |
| F1 | EXTAL | | | | |

Table 1.6 List of Pins and Pin Functions (64-Pin WFLGA) (2/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, POE, RTC) | Communication (SCIE, SCIF, RSPI, RIIC, USB) | Others |
|---------|-------------------------------------|----------|-------------------------------|---|--------------|
| F2 | | P32 | MTIOC0C/RTCCOUT | | IRQ2 |
| F3 | UPSEL | P35 | | | NMI |
| F4 | UB# | P14 | MTIOC0A/MTIOC3A/MTCLKA | CTS1#/RTS1#/SS1#/TXD12/TXD12/SIOX12/SMOSI12/SSDA12/SSLA0/USB0_OVRCURA | IRQ4 |
| F5 | | P54 | MTIOC4B | | |
| F6 | | PC7 | MTIOC3A/MTCLKB | TXD1/SMOSI1/SSDA1/MISOA/USB0_OVRCURB | CACREF |
| F7 | | PC4 | MTCLKC/MTIOC3D/POE0# | SCK5/SSLA0/USB0_VBUSEN/USB0_VBUS*1 | IRQ2/CLKOUT |
| F8 | | PB5 | MTIOC1B/MTIOC2A/POE1# | | |
| G1 | VCL | | | | |
| G2 | | P17 | MTIOC0C/MTIOC3A/MTIOC3B/POE8# | SCK1/MISOA/SDA0/RXD12/RDX12/SMISO12/SSCL12 | IRQ7 |
| G3 | | P16 | MTIOC3C/MTIOC3D/RTCCOUT | TXD1/SMOSI1/SSDA1/SCL0/MOSIA/USB0_VBUSEN/USB0_OVRCURB/USB0_VBUS | IRQ6/ADTRG0# |
| G4 | | P15 | MTIOC0B/MTCLKB | RXD1/SMISO1/SSCL1/RSPCKA | IRQ5/CLKOUT |
| G5 | | PC6 | MTIOC3C/MTCLKA | RXD1/SMISO1/SSCL1/MOSIA/USB0_EXICEN | |
| G6 | | PC5 | MTIOC3B/MTCLKD | SCK1/RSPCKA/USB0_ID | |
| G7 | | PC3 | MTIOC4D | TXD5/SMOSI5/SSDA5 | |
| G8 | | PB6/PC0 | MTIOC3D | | |
| H1 | VSS | | | | |
| H2 | VCC | | | | |
| H3 | VCC_USB | | | | |
| H4 | | | | USB0_DM | |
| H5 | | | | USB0_DP | |
| H6 | VSS_USB | | | | |
| H7 | | PC2 | MTIOC4B | RXD5/SMISO5/SSCL5/SSLA3 | |
| H8 | | PB7/PC1 | MTIOC3B | | |

Note 1. Not 5 V tolerant.

Note 2. The power source of the I/O buffer for these pins is AVCC0.

Table 1.7 List of Pins and Pin Functions (48-Pin LQFP/HWQFN) (1/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, POE, RTC) | Communication (SCle, SCIf, RSPI, RIIC, USB) | Others |
|---------|-------------------------------------|----------|-----------------------------------|--|-------------------------------|
| 1 | | P27 | MTIOC2B | SCK1/SCK12 | IRQ3/CMPA2/ CACREF/ADTRG0# |
| 2 | | P26 | MTIOC2A | TXD1/SMOSI1/SSDA1/USB0_VBUSEN | |
| 3 | MD | | | | FINED |
| 4 | RES# | | | | |
| 5 | XCOUT | | | | |
| 6 | XCIN | PH7 | | | |
| 7 | UPSEL | P35 | | | NMI |
| 8 | XTAL | | | | |
| 9 | EXTAL | | | | |
| 10 | VCL | | | | |
| 11 | VSS | | | | |
| 12 | VCC | | | | |
| 13 | | P17 | MTIOC0C/MTIOC3A/ MTIOC3B/POE8# | SCK1/MISOA/SDA0/RXD12/RDX12/ SMISO12/SSCL12 | IRQ7 |
| 14 | | P16 | MTIOC3C/MTIOC3D/ RTCOUT | TXD1/SMOSI1/SSDA1/MOSIA/SCL0/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB | IRQ6/ADTRG0# |
| 15 | | P15 | MTIOC0B/MTCLKB | RXD1/SMISO1/SSCL1/RSPCKA | IRQ5/CLKOUT |
| 16 | UB# | P14 | MTIOC0A/MTIOC3A/ MTCLKA | CTS1#/RTS1#/SS1#/SSLA0/TXD12/ TXDX12/SIOX12/SMOSI12/SSDA12/ USB0_OVRCURA | IRQ4 |
| 17 | VCC_USB | | | | |
| 18 | | | | USB0_DM | |
| 19 | | | | USB0_DP | |
| 20 | VSS_USB | | | | |
| 21 | | PC7 | MTIOC3A/MTCLKB | TXD1/SMOSI1/SSDA1/MISOA/ USB0_OVRCURB | CACREF |
| 22 | | PC6 | MTIOC3C/MTCLKA | RXD1/SMISO1/SSCL1/MOSIA/ USB0_EXICEN | |
| 23 | | PC5 | MTIOC3B/MTCLKD | SCK1/RSPCKA/USB0_ID | |
| 24 | | PC4 | MTIOC3D/MTCLKC/POE0# | SCK5/SSLA0/USB0_VBUS*1/ USB0_VBUSEN | IRQ2/CLKOUT |
| 25 | | PB5/PC3 | MTIOC2A/MTIOC1B/POE1# | | |
| 26 | | PB3/PC2 | MTIOC0A/MTIOC3B/ MTIOC4A/POE3# | USB0_OVRCURA | |
| 27 | | PB1/PC1 | MTIOC0C/MTIOC4C | | IRQ4 |
| 28 | VCC | | | | |
| 29 | | PB0/PC0 | MTIC5W/MTIOC0C/ RTCOUT | SCL0/RSPCKA | IRQ2/ADTRG0# |
| 30 | VSS | | | | |
| 31 | | PA6 | MTIC5V/MTCLKB/MTIOC2A/ POE2# | CTS5#/RTS5#/SS5#/SDA0/MOSIA | IRQ3 |
| 32 | | PA4 | MTIC5U/MTCLKA/MTIOC2B | TXD5/SMOSI5/SSDA5/SSLA0 | IRQ5 |
| 33 | | PA3 | MTIOC0D/MTCLKD/ MTIOC1B/POE0# | RXD5/SMISO5/SSCL5/MISOA | IRQ6 |
| 34 | | PA1 | MTIOC0B/MTCLKC/ RTCOUT | SCK5/SSLA2 | |
| 35 | | PE4 | MTIOC4D/MTIOC1A/ MTIOC3A | MOSIA | IRQ4/AN012 |
| 36 | | PE3 | MTIOC0A/MTIOC1B/ MTIOC4B/POE8# | CTS12#/RTS12#/SS12#/RSPCKA | IRQ3/AN011 |
| 37 | | PE2 | MTIOC4A | RXD12/RDX12/SMISO12/SSCL12 | IRQ7/AN010 |
| 38 | | PE1 | MTIOC4C | TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12 | IRQ1/AN009 |

Table 1.7 List of Pins and Pin Functions (48-Pin LQFP/HWQFN) (2/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, POE, RTC) | Communication (SCle, SCIf, RSPI, RIIC, USB) | Others |
|---------|-------------------------------------|----------|------------------------|---|------------|
| 39 | | PE0 | MTIOC2A/POE3# | SCK12 | IRQ0/AN008 |
| 40 | | PE7 | | | IRQ7/AN015 |
| 41 | | P46*2 | | | AN006 |
| 42 | | P42*2 | | | AN002 |
| 43 | | P41*2 | | | AN001 |
| 44 | VREFL0 | PJ7*2 | | | |
| 45 | | P40*2 | | | AN000 |
| 46 | VREFH0 | PJ6*2 | | | |
| 47 | AVSS0 | | | | |
| 48 | AVCC0 | | | | |

Note 1. Not 5 V tolerant.

Note 2. The power source of the I/O buffer for these pins is AVCC0.

Table 1.8 List of Pins and Pin Functions (40-Pin HWQFN) (1/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, POE, RTC) | Communication (SCIE, SCIf, RSPI, RIIC, USB) | Others |
|---------|-------------------------------------|----------|-------------------------------|---|---------------------------|
| 1 | | P27 | MTIOC2B | SCK1/SCK12 | IRQ3/CMPA2/CACREF/ADTRG0# |
| 2 | | P26 | MTIOC2A | TXD1/SMOSI1/SSDA1/USB0_VBUSEN | |
| 3 | MD | | | | FINED |
| 4 | RES# | | | | |
| 5 | UPSEL | P35 | | | NMI |
| 6 | XTAL | | | | |
| 7 | EXTAL | | | | |
| 8 | VCL | | | | |
| 9 | VSS | | | | |
| 10 | VCC | | | | |
| 11 | | P32 | MTIOC0C | | IRQ2 |
| 12 | | P17 | MTIOC0C/MTIOC3A/MTIOC3B/POE8# | SCK1/MISOA/SDA0/RXD12/RDX12/SMISO12/SSCL12 | IRQ7 |
| 13 | | P16 | MTIOC3C/MTIOC3D | TXD1/SMOSI1/SSDA1/SCL0/MOSIA/USB0_VBUSEN/USB0_OVRCURB/USB0_VBUS | IRQ6/ADTRG0# |
| 14 | | P15 | MTIOC0B/MTCLKB | RXD1/SMISO1/SSCL1/RSPCKA | IRQ5/CLKOUT |
| 15 | UB# | P14 | MTIOC0A/MTIOC3A/MTCLKA | CTS1#/RTS1#/SS1#/SSLA0/TXD12/TXD12/SIOX12/SMOSI12/SSDA12/USB0_OVRCURA | IRQ4 |
| 16 | VCC_USB | | | | |
| 17 | | | | USB0_DM | |
| 18 | | | | USB0_DP | |
| 19 | VSS_USB | | | | |
| 20 | | PC4 | MTIOC3D/MTCLKC/POE0# | SCK5/SSLA0/USB0_VBUS*/USB0_VBUSEN | IRQ2/CLKOUT |
| 21 | | PB3 | MTIOC0A/MTIOC3B/MTIOC4A/POE3# | USB0_OVRCURA | |
| 22 | VCC | | | | |
| 23 | | PB0 | MTIOC0C/MTIC5W | SCL0/RSPCKA | IRQ2/ADTRG0# |
| 24 | VSS | | | | |
| 25 | | PA6 | MTIOC2A/MTIC5V/MTCLKB/POE2# | CTS5#/RTS5#/SS5#/SDA0/MOSIA | IRQ3 |
| 26 | | PA4 | MTIOC2B/MTIC5U/MTCLKA | TXD5/SMOSI5/SSDA5/SSLA0 | IRQ5 |
| 27 | | PA3 | MTIOC0D/MTIOC1B/MTCLKD/POE0# | RXD5/SMISO5/SSCL5/MISOA | IRQ6 |
| 28 | | PA1 | MTIOC0B/MTCLKC | SCK5/SSLA2 | |
| 29 | | PE4 | MTIOC1A/MTIOC3A/MTIOC4D | MOSIA | IRQ4/AN012 |
| 30 | | PE3 | MTIOC0A/MTIOC1B/MTIOC4B/POE8# | CTS12#/RTS12#/SS12#/RSPCKA | IRQ3/AN011 |
| 31 | | PE2 | MTIOC4A | RXD12/RDX12/SMISO12/SSCL12 | IRQ7/AN010 |
| 32 | | PE1 | MTIOC4C | TXD12/TXD12/SIOX12/SMOSI12/SSDA12 | IRQ1/AN009 |
| 33 | | PE0 | MTIOC2A/POE3# | SCK12 | IRQ0/AN008 |
| 34 | | P46*2 | | | AN006 |
| 35 | | P42*2 | | | AN002 |
| 36 | | P41*2 | | | AN001 |
| 37 | VREFL0 | PJ7*2 | | | |
| 38 | VREFH0 | PJ6*2 | | | |
| 39 | AVSS0 | | | | |

Table 1.8 List of Pins and Pin Functions (40-Pin HWQFN) (2/2)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, POE, RTC) | Communication (SCIE, SCIF, RSPI, RIIC, USB) | Others |
|---------|-------------------------------------|----------|------------------------|---|--------|
| 40 | AVCC0 | | | | |

Note 1. Not 5 V tolerant.

Note 2. The power source of the I/O buffer for these pins is AVCC0.

Table 1.9 List of Pins and Pin Functions (36-Pin WFLGA)

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, POE, RTC) | Communication (SCIE, SCIf, RSPI, RIIC, USB) | Others |
|---------|-------------------------------------|----------|-------------------------------|---|---------------------------|
| A1 | AVSS0 | | | | |
| A2 | AVCC0 | | | | |
| A3 | VREFH0 | PJ6*2 | | | |
| A4 | | P42*2 | | | AN002 |
| A5 | | P41*2 | | | AN001 |
| A6 | | PE2 | MTIOC4A | RXD12/RXD12/SMISO12/SSCL12 | IRQ7/AN010 |
| B1 | RES# | | | | |
| B2 | | P27 | MTIOC2B | SCK1/SCK12 | IRQ3/CMPA2/CACREF/ADTRG0# |
| B3 | VREFL0 | PJ7*2 | | | |
| B4 | | PE0 | MTIOC2A/POE3# | SCK12 | IRQ0/AN008 |
| B5 | | PE1 | MTIOC4C | TXD12/TXD12/SIOX12/SMOSI12/SSDA12 | IRQ1/AN009 |
| B6 | | PA3 | MTIOC0D/MTCLKD/MTIOC1B/POE0# | RXD5/SMISO5/SSCL5/MISOA | IRQ6 |
| C1 | XTAL | | | | |
| C2 | MD | | | | FINED |
| C3 | | PE3 | MTIOC0A/MTIOC1B/MTIOC4B/POE8# | CTS12#/RTS12#/SS12#/RSPCKA | IRQ3/AN011 |
| C4 | | PE4 | MTIOC1A/MTIOC3A/MTIOC4D | MOSIA | IRQ4/AN012 |
| C5 | | PA4 | MTIOC2B/MTIC5U/MTCLKA | TXD5/SMOSI5/SSDA5/SSLA0 | IRQ5 |
| C6 | VSS | | | | |
| D1 | EXTAL | | | | |
| D2 | UPSEL | P35 | | | NMI |
| D3 | UB# | P14 | MTIOC0A/MTIOC3A/MTCLKA | CTS1#/RTS1#/SS1#/SSLA0/TXD12/TXD12/SIOX12/SMOSI12/SSDA12/USB0_OVRCURA | IRQ4 |
| D4 | | PA6 | MTIC5V/MTCLKB/MTIOC2A/POE2# | CTS5#/RTS5#/SS5#/SDA0/MOSIA | IRQ3 |
| D5 | | PB3 | MTIOC0A/MTIOC3B/MTIOC4A/POE3# | USB0_OVRCURA | |
| D6 | | PB0 | MTIOC0C/MTIC5W | SCL0/RSPCKA | IRQ2/ADTRG0# |
| E1 | VCL | | | | |
| E2 | | P17 | MTIOC0C/MTIOC3A/MTIOC3B/POE8# | SCK1/MISOA/SDA0/RXD12/RXD12/SMISO12/SSCL12 | IRQ7 |
| E3 | | P16 | MTIOC3C/MTIOC3D | TXD1/SMOSI1/SSDA1/SCL0/MOSIA/USB0_VBUSEN/USB0_OVRCURB/USB0_VBUS | IRQ6/ADTRG0# |
| E4 | | P15 | MTIOC0B/MTCLKB | RXD1/SMISO1/SSCL1/RSPCKA | IRQ5/CLKOUT |
| E5 | | PC4 | MTIOC3D/MTCLKC/POE0# | SCK5/SSLA0/USB0_VBUSEN/USB0_VBUS*1 | IRQ2/CLKOUT |
| E6 | VCC | | | | |
| F1 | VSS | | | | |
| F2 | VCC | | | | |
| F3 | VCC_USB | | | | |
| F4 | | | | USB0_DM | |
| F5 | | | | USB0_DP | |
| F6 | VSS_USB | | | | |

Note 1. Not 5 V tolerant.

Note 2. The power source of the I/O buffer for these pins is AVCC0.

2. CPU

Figure 2.1 shows the register set of the CPU.

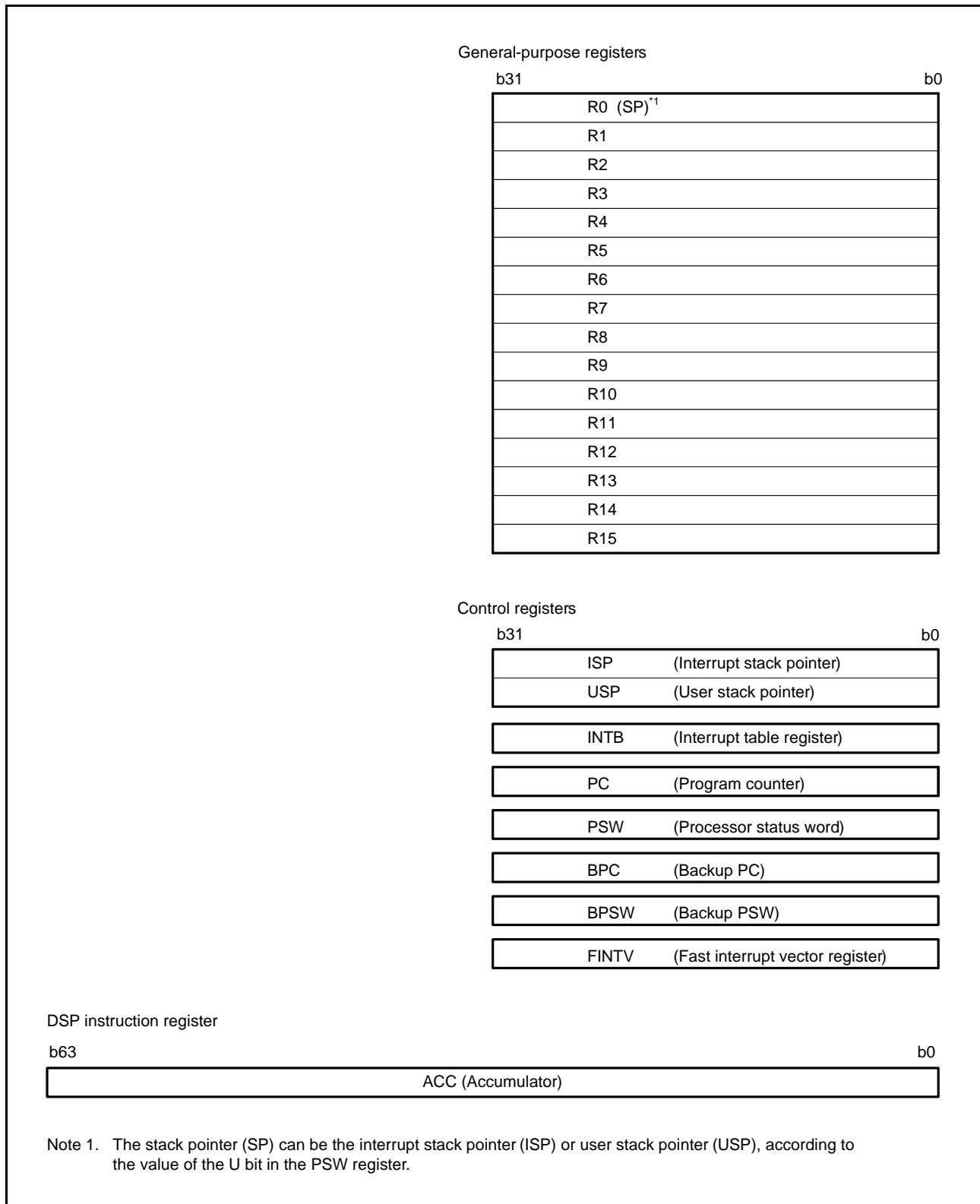


Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has 16 general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of 4, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory map.

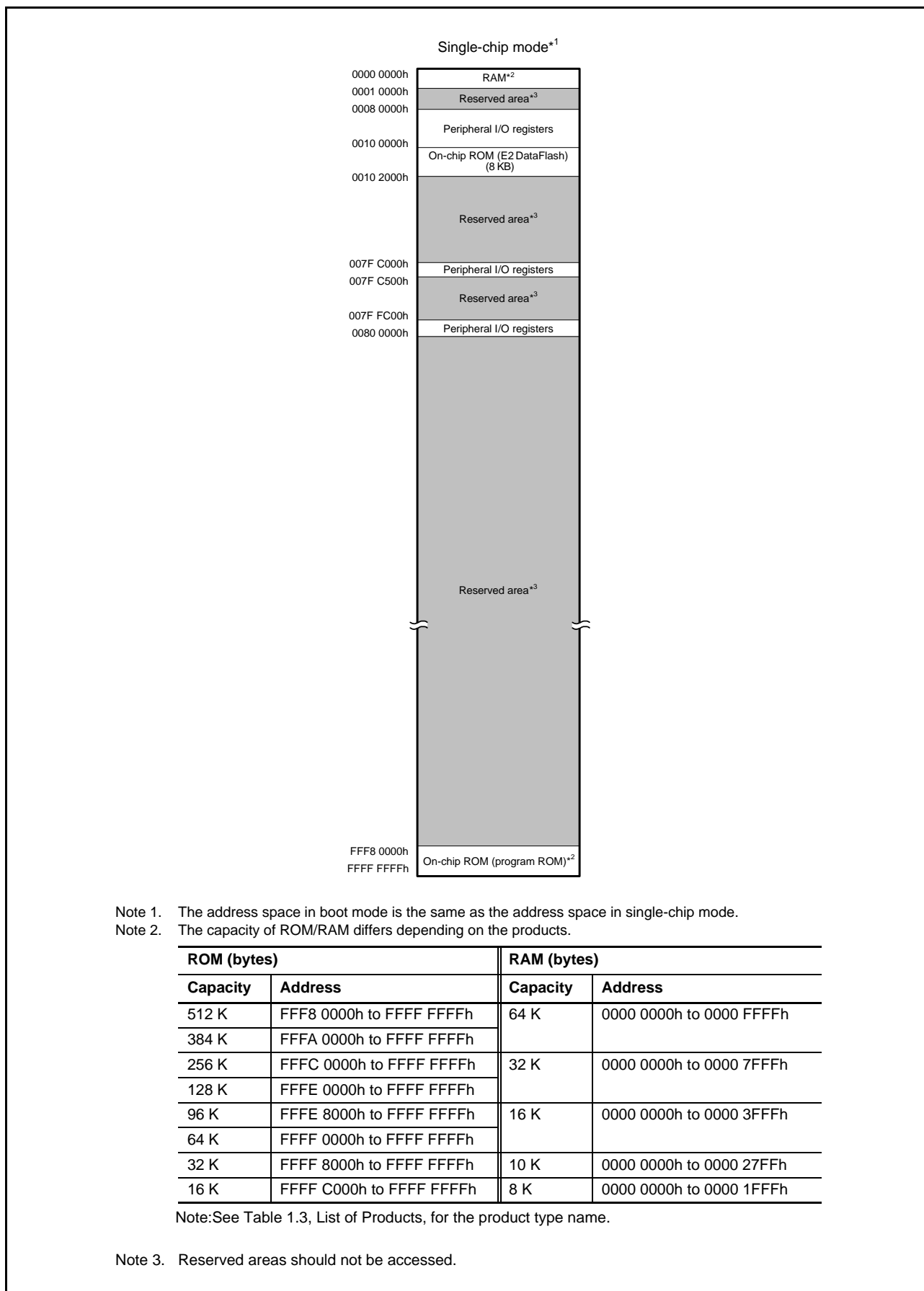


Figure 3.1 Memory Map

4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to I/O registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

While writing to an I/O register, the CPU starts executing subsequent instructions before the I/O register write access is completed. This may cause the subsequent instructions to be executed before the write value is reflected in the operation. The examples below show how subsequent instructions must be executed after a write access to an I/O register is completed.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) set to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value in the I/O register and write it to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

Example of instructions

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

When executing an instruction after writing to multiple registers, only read the last I/O register written to and execute the instruction using that value; it is not necessary to execute the instruction using the values written to all the registers.

(3) Number of cycles necessary for accessing I/O registers

See Table 4.1 for details on the number of clock cycles necessary for accessing I/O registers.

The number of access cycles to I/O registers is obtained by following equation.*1

$$\begin{aligned} \text{Number of access cycles to I/O registers} = & \text{Number of bus cycles for internal main bus 1} + \\ & \text{Number of divided clock synchronization cycles} + \\ & \text{Number of bus cycles for internal peripheral buses 1 to 6} \end{aligned}$$

The number of bus cycles of internal peripheral buses 1 to 6 differs according to the register to be accessed.

When peripheral functions connected to internal peripheral buses 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.

The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DTC).

(4) Notes on sleep mode and mode transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| 0008 0000h | SYSTEM | Mode Monitor Register | MDMONR | 16 | 16 | 3 ICLK |
| 0008 0008h | SYSTEM | System Control Register 1 | SYSCR1 | 16 | 16 | 3 ICLK |
| 0008 000Ch | SYSTEM | Standby Control Register | SBYCR | 16 | 16 | 3 ICLK |
| 0008 0010h | SYSTEM | Module Stop Control Register A | MSTPCRA | 32 | 32 | 3 ICLK |
| 0008 0014h | SYSTEM | Module Stop Control Register B | MSTPCRB | 32 | 32 | 3 ICLK |
| 0008 0018h | SYSTEM | Module Stop Control Register C | MSTPCRC | 32 | 32 | 3 ICLK |
| 0008 0020h | SYSTEM | System Clock Control Register | SCKCR | 32 | 32 | 3 ICLK |
| 0008 0026h | SYSTEM | System Clock Control Register 3 | SCKCR3 | 16 | 16 | 3 ICLK |
| 0008 0028h | SYSTEM | PLL Control Register | PLLCR | 16 | 16 | 3 ICLK |
| 0008 002Ah | SYSTEM | PLL Control Register 2 | PLLCR2 | 8 | 8 | 3 ICLK |
| 0008 0032h | SYSTEM | Main Clock Oscillator Control Register | MOSCCR | 8 | 8 | 3 ICLK |
| 0008 0033h | SYSTEM | Sub-Clock Oscillator Control Register | SOSCCR | 8 | 8 | 3 ICLK |
| 0008 0034h | SYSTEM | Low-Speed On-Chip Oscillator Control Register | LOCOCR | 8 | 8 | 3 ICLK |
| 0008 0035h | SYSTEM | IWDT-Dedicated On-Chip Oscillator Control Register | ILOCOCR | 8 | 8 | 3 ICLK |
| 0008 0036h | SYSTEM | High-Speed On-Chip Oscillator Control Register | HOCOCR | 8 | 8 | 3 ICLK |
| 0008 003Ch | SYSTEM | Oscillation Stabilization Flag Register | OSCOVFSR | 8 | 8 | 3 ICLK |
| 0008 003Eh | SYSTEM | CLKOUT Output Control Register | CKOCR | 16 | 16 | 3 ICLK |
| 0008 0040h | SYSTEM | Oscillation Stop Detection Control Register | OSTDCR | 8 | 8 | 3 ICLK |
| 0008 0041h | SYSTEM | Oscillation Stop Detection Status Register | OSTDSR | 8 | 8 | 3 ICLK |
| 0008 00A0h | SYSTEM | Operating Power Control Register | OPCCR | 8 | 8 | 3 ICLK |
| 0008 00A1h | SYSTEM | Sleep Mode Return Clock Source Switching Register | RSTCKCR | 8 | 8 | 3 ICLK |
| 0008 00A2h | SYSTEM | Main Clock Oscillator Wait Control Register | MOSCWTCR | 8 | 8 | 3 ICLK |
| 0008 00A5h | SYSTEM | High-Speed On-Chip Oscillator Wait Control Register | HOCOWTCR | 8 | 8 | 3 ICLK |
| 0008 00AAh | SYSTEM | Sub Operating Power Control Register | SOPCCR | 8 | 8 | 3 ICLK |
| 0008 00C0h | SYSTEM | Reset Status Register 2 | RSTSR2 | 8 | 8 | 3 ICLK |
| 0008 00C2h | SYSTEM | Software Reset Register | SWRR | 16 | 16 | 3 ICLK |
| 0008 00E0h | SYSTEM | Voltage Monitoring 1 Circuit Control Register 1 | LVD1CR1 | 8 | 8 | 3 ICLK |
| 0008 00E1h | SYSTEM | Voltage Monitoring 1 Circuit Status Register | LVD1SR | 8 | 8 | 3 ICLK |
| 0008 00E2h | SYSTEM | Voltage Monitoring 2 Circuit Control Register 1 | LVD2CR1 | 8 | 8 | 3 ICLK |
| 0008 00E3h | SYSTEM | Voltage Monitoring 2 Circuit Status Register | LVD2SR | 8 | 8 | 3 ICLK |
| 0008 03FEh | SYSTEM | Protect Register | PRCR | 16 | 16 | 3 ICLK |
| 0008 1300h | BSC | Bus Error Status Clear Register | BERCLR | 8 | 8 | 2 ICLK |
| 0008 1304h | BSC | Bus Error Monitoring Enable Register | BEREN | 8 | 8 | 2 ICLK |
| 0008 1308h | BSC | Bus Error Status Register 1 | BERSR1 | 8 | 8 | 2 ICLK |
| 0008 130Ah | BSC | Bus Error Status Register 2 | BERSR2 | 16 | 16 | 2 ICLK |
| 0008 1310h | BSC | Bus Priority Control Register | BUSPRI | 16 | 16 | 2 ICLK |
| 0008 2400h | DTC | DTC Control Register | DTCCR | 8 | 8 | 2 ICLK |
| 0008 2404h | DTC | DTC Vector Base Register | DTCVBR | 32 | 32 | 2 ICLK |
| 0008 2408h | DTC | DTC Address Mode Register | DTCADMOD | 8 | 8 | 2 ICLK |
| 0008 240Ch | DTC | DTC Module Start Register | DTCST | 8 | 8 | 2 ICLK |
| 0008 240Eh | DTC | DTC Status Register | DTCSTS | 16 | 16 | 2 ICLK |
| 0008 7010h | ICU | Interrupt Request Register 016 | IR016 | 8 | 8 | 2 ICLK |
| 0008 701Bh | ICU | Interrupt Request Register 027 | IR027 | 8 | 8 | 2 ICLK |
| 0008 701Ch | ICU | Interrupt Request Register 028 | IR028 | 8 | 8 | 2 ICLK |
| 0008 701Dh | ICU | Interrupt Request Register 029 | IR029 | 8 | 8 | 2 ICLK |
| 0008 7020h | ICU | Interrupt Request Register 032 | IR032 | 8 | 8 | 2 ICLK |
| 0008 7021h | ICU | Interrupt Request Register 033 | IR033 | 8 | 8 | 2 ICLK |
| 0008 7022h | ICU | Interrupt Request Register 034 | IR034 | 8 | 8 | 2 ICLK |
| 0008 7024h | ICU | Interrupt Request Register 036 | IR036 | 8 | 8 | 2 ICLK |
| 0008 7025h | ICU | Interrupt Request Register 037 | IR037 | 8 | 8 | 2 ICLK |

Table 4.1 List of I/O Registers (Address Order) (2/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|--------------------------------|-----------------|----------------|-------------|-------------------------|
| 0008 7026h | ICU | Interrupt Request Register 038 | IR038 | 8 | 8 | 2 ICLK |
| 0008 702Ch | ICU | Interrupt Request Register 044 | IR044 | 8 | 8 | 2 ICLK |
| 0008 702Dh | ICU | Interrupt Request Register 045 | IR045 | 8 | 8 | 2 ICLK |
| 0008 702Eh | ICU | Interrupt Request Register 046 | IR046 | 8 | 8 | 2 ICLK |
| 0008 702Fh | ICU | Interrupt Request Register 047 | IR047 | 8 | 8 | 2 ICLK |
| 0008 7039h | ICU | Interrupt Request Register 057 | IR057 | 8 | 8 | 2 ICLK |
| 0008 703Fh | ICU | Interrupt Request Register 063 | IR063 | 8 | 8 | 2 ICLK |
| 0008 7040h | ICU | Interrupt Request Register 064 | IR064 | 8 | 8 | 2 ICLK |
| 0008 7041h | ICU | Interrupt Request Register 065 | IR065 | 8 | 8 | 2 ICLK |
| 0008 7042h | ICU | Interrupt Request Register 066 | IR066 | 8 | 8 | 2 ICLK |
| 0008 7043h | ICU | Interrupt Request Register 067 | IR067 | 8 | 8 | 2 ICLK |
| 0008 7044h | ICU | Interrupt Request Register 068 | IR068 | 8 | 8 | 2 ICLK |
| 0008 7045h | ICU | Interrupt Request Register 069 | IR069 | 8 | 8 | 2 ICLK |
| 0008 7046h | ICU | Interrupt Request Register 070 | IR070 | 8 | 8 | 2 ICLK |
| 0008 7047h | ICU | Interrupt Request Register 071 | IR071 | 8 | 8 | 2 ICLK |
| 0008 7058h | ICU | Interrupt Request Register 088 | IR088 | 8 | 8 | 2 ICLK |
| 0008 7059h | ICU | Interrupt Request Register 089 | IR089 | 8 | 8 | 2 ICLK |
| 0008 705Ah | ICU | Interrupt Request Register 090 | IR090 | 8 | 8 | 2 ICLK |
| 0008 705Ch | ICU | Interrupt Request Register 092 | IR092 | 8 | 8 | 2 ICLK |
| 0008 705Dh | ICU | Interrupt Request Register 093 | IR093 | 8 | 8 | 2 ICLK |
| 0008 7066h | ICU | Interrupt Request Register 102 | IR102 | 8 | 8 | 2 ICLK |
| 0008 7067h | ICU | Interrupt Request Register 103 | IR103 | 8 | 8 | 2 ICLK |
| 0008 706Ah | ICU | Interrupt Request Register 106 | IR106 | 8 | 8 | 2 ICLK |
| 0008 7072h | ICU | Interrupt Request Register 114 | IR114 | 8 | 8 | 2 ICLK |
| 0008 7073h | ICU | Interrupt Request Register 115 | IR115 | 8 | 8 | 2 ICLK |
| 0008 7074h | ICU | Interrupt Request Register 116 | IR116 | 8 | 8 | 2 ICLK |
| 0008 7075h | ICU | Interrupt Request Register 117 | IR117 | 8 | 8 | 2 ICLK |
| 0008 7076h | ICU | Interrupt Request Register 118 | IR118 | 8 | 8 | 2 ICLK |
| 0008 7077h | ICU | Interrupt Request Register 119 | IR119 | 8 | 8 | 2 ICLK |
| 0008 7078h | ICU | Interrupt Request Register 120 | IR120 | 8 | 8 | 2 ICLK |
| 0008 7079h | ICU | Interrupt Request Register 121 | IR121 | 8 | 8 | 2 ICLK |
| 0008 707Ah | ICU | Interrupt Request Register 122 | IR122 | 8 | 8 | 2 ICLK |
| 0008 707Bh | ICU | Interrupt Request Register 123 | IR123 | 8 | 8 | 2 ICLK |
| 0008 707Ch | ICU | Interrupt Request Register 124 | IR124 | 8 | 8 | 2 ICLK |
| 0008 707Dh | ICU | Interrupt Request Register 125 | IR125 | 8 | 8 | 2 ICLK |
| 0008 707Eh | ICU | Interrupt Request Register 126 | IR126 | 8 | 8 | 2 ICLK |
| 0008 707Fh | ICU | Interrupt Request Register 127 | IR127 | 8 | 8 | 2 ICLK |
| 0008 7080h | ICU | Interrupt Request Register 128 | IR128 | 8 | 8 | 2 ICLK |
| 0008 7081h | ICU | Interrupt Request Register 129 | IR129 | 8 | 8 | 2 ICLK |
| 0008 7082h | ICU | Interrupt Request Register 130 | IR130 | 8 | 8 | 2 ICLK |
| 0008 7083h | ICU | Interrupt Request Register 131 | IR131 | 8 | 8 | 2 ICLK |
| 0008 7084h | ICU | Interrupt Request Register 132 | IR132 | 8 | 8 | 2 ICLK |
| 0008 7085h | ICU | Interrupt Request Register 133 | IR133 | 8 | 8 | 2 ICLK |
| 0008 7086h | ICU | Interrupt Request Register 134 | IR134 | 8 | 8 | 2 ICLK |
| 0008 7087h | ICU | Interrupt Request Register 135 | IR135 | 8 | 8 | 2 ICLK |
| 0008 7088h | ICU | Interrupt Request Register 136 | IR136 | 8 | 8 | 2 ICLK |
| 0008 7089h | ICU | Interrupt Request Register 137 | IR137 | 8 | 8 | 2 ICLK |
| 0008 708Ah | ICU | Interrupt Request Register 138 | IR138 | 8 | 8 | 2 ICLK |
| 0008 708Bh | ICU | Interrupt Request Register 139 | IR139 | 8 | 8 | 2 ICLK |
| 0008 708Ch | ICU | Interrupt Request Register 140 | IR140 | 8 | 8 | 2 ICLK |
| 0008 708Dh | ICU | Interrupt Request Register 141 | IR141 | 8 | 8 | 2 ICLK |
| 0008 70AAh | ICU | Interrupt Request Register 170 | IR170 | 8 | 8 | 2 ICLK |

Table 4.1 List of I/O Registers (Address Order) (3/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|------------------------------------|-----------------|----------------|-------------|-------------------------|
| 0008 70ABh | ICU | Interrupt Request Register 171 | IR171 | 8 | 8 | 2 ICLK |
| 0008 70DAh | ICU | Interrupt Request Register 218 | IR218 | 8 | 8 | 2 ICLK |
| 0008 70DBh | ICU | Interrupt Request Register 219 | IR219 | 8 | 8 | 2 ICLK |
| 0008 70DCh | ICU | Interrupt Request Register 220 | IR220 | 8 | 8 | 2 ICLK |
| 0008 70DDh | ICU | Interrupt Request Register 221 | IR221 | 8 | 8 | 2 ICLK |
| 0008 70DEh | ICU | Interrupt Request Register 222 | IR222 | 8 | 8 | 2 ICLK |
| 0008 70DFh | ICU | Interrupt Request Register 223 | IR223 | 8 | 8 | 2 ICLK |
| 0008 70E0h | ICU | Interrupt Request Register 224 | IR224 | 8 | 8 | 2 ICLK |
| 0008 70E1h | ICU | Interrupt Request Register 225 | IR225 | 8 | 8 | 2 ICLK |
| 0008 70EEh | ICU | Interrupt Request Register 238 | IR238 | 8 | 8 | 2 ICLK |
| 0008 70EFh | ICU | Interrupt Request Register 239 | IR239 | 8 | 8 | 2 ICLK |
| 0008 70F0h | ICU | Interrupt Request Register 240 | IR240 | 8 | 8 | 2 ICLK |
| 0008 70F1h | ICU | Interrupt Request Register 241 | IR241 | 8 | 8 | 2 ICLK |
| 0008 70F2h | ICU | Interrupt Request Register 242 | IR242 | 8 | 8 | 2 ICLK |
| 0008 70F3h | ICU | Interrupt Request Register 243 | IR243 | 8 | 8 | 2 ICLK |
| 0008 70F4h | ICU | Interrupt Request Register 244 | IR244 | 8 | 8 | 2 ICLK |
| 0008 70F5h | ICU | Interrupt Request Register 245 | IR245 | 8 | 8 | 2 ICLK |
| 0008 70F6h | ICU | Interrupt Request Register 246 | IR246 | 8 | 8 | 2 ICLK |
| 0008 70F7h | ICU | Interrupt Request Register 247 | IR247 | 8 | 8 | 2 ICLK |
| 0008 70F8h | ICU | Interrupt Request Register 248 | IR248 | 8 | 8 | 2 ICLK |
| 0008 70F9h | ICU | Interrupt Request Register 249 | IR249 | 8 | 8 | 2 ICLK |
| 0008 711Bh | ICU | DTC Activation Enable Register 027 | DTCER027 | 8 | 8 | 2 ICLK |
| 0008 711Ch | ICU | DTC Activation Enable Register 028 | DTCER028 | 8 | 8 | 2 ICLK |
| 0008 711Dh | ICU | DTC Activation Enable Register 029 | DTCER029 | 8 | 8 | 2 ICLK |
| 0008 7124h | ICU | DTC Activation Enable Register 036 | DTCER036 | 8 | 8 | 2 ICLK |
| 0008 7125h | ICU | DTC Activation Enable Register 037 | DTCER037 | 8 | 8 | 2 ICLK |
| 0008 712Dh | ICU | DTC Activation Enable Register 045 | DTCER045 | 8 | 8 | 2 ICLK |
| 0008 712Eh | ICU | DTC Activation Enable Register 046 | DTCER046 | 8 | 8 | 2 ICLK |
| 0008 7140h | ICU | DTC Activation Enable Register 064 | DTCER064 | 8 | 8 | 2 ICLK |
| 0008 7141h | ICU | DTC Activation Enable Register 065 | DTCER065 | 8 | 8 | 2 ICLK |
| 0008 7142h | ICU | DTC Activation Enable Register 066 | DTCER066 | 8 | 8 | 2 ICLK |
| 0008 7143h | ICU | DTC Activation Enable Register 067 | DTCER067 | 8 | 8 | 2 ICLK |
| 0008 7144h | ICU | DTC Activation Enable Register 068 | DTCER068 | 8 | 8 | 2 ICLK |
| 0008 7145h | ICU | DTC Activation Enable Register 069 | DTCER069 | 8 | 8 | 2 ICLK |
| 0008 7146h | ICU | DTC Activation Enable Register 070 | DTCER070 | 8 | 8 | 2 ICLK |
| 0008 7147h | ICU | DTC Activation Enable Register 071 | DTCER071 | 8 | 8 | 2 ICLK |
| 0008 7166h | ICU | DTC Activation Enable Register 102 | DTCER102 | 8 | 8 | 2 ICLK |
| 0008 7167h | ICU | DTC Activation Enable Register 103 | DTCER103 | 8 | 8 | 2 ICLK |
| 0008 716Ah | ICU | DTC Activation Enable Register 106 | DTCER106 | 8 | 8 | 2 ICLK |
| 0008 7172h | ICU | DTC Activation Enable Register 114 | DTCER114 | 8 | 8 | 2 ICLK |
| 0008 7173h | ICU | DTC Activation Enable Register 115 | DTCER115 | 8 | 8 | 2 ICLK |
| 0008 7174h | ICU | DTC Activation Enable Register 116 | DTCER116 | 8 | 8 | 2 ICLK |
| 0008 7175h | ICU | DTC Activation Enable Register 117 | DTCER117 | 8 | 8 | 2 ICLK |
| 0008 7179h | ICU | DTC Activation Enable Register 121 | DTCER121 | 8 | 8 | 2 ICLK |
| 0008 717Ah | ICU | DTC Activation Enable Register 122 | DTCER122 | 8 | 8 | 2 ICLK |
| 0008 717Dh | ICU | DTC Activation Enable Register 125 | DTCER125 | 8 | 8 | 2 ICLK |
| 0008 717Eh | ICU | DTC Activation Enable Register 126 | DTCER126 | 8 | 8 | 2 ICLK |
| 0008 7181h | ICU | DTC Activation Enable Register 129 | DTCER129 | 8 | 8 | 2 ICLK |
| 0008 7182h | ICU | DTC Activation Enable Register 130 | DTCER130 | 8 | 8 | 2 ICLK |
| 0008 7183h | ICU | DTC Activation Enable Register 131 | DTCER131 | 8 | 8 | 2 ICLK |
| 0008 7184h | ICU | DTC Activation Enable Register 132 | DTCER132 | 8 | 8 | 2 ICLK |
| 0008 7186h | ICU | DTC Activation Enable Register 134 | DTCER134 | 8 | 8 | 2 ICLK |

Table 4.1 List of I/O Registers (Address Order) (4/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|
| 0008 7187h | ICU | DTC Activation Enable Register 135 | DTCER135 | 8 | 8 | 2 ICLK |
| 0008 7188h | ICU | DTC Activation Enable Register 136 | DTCER136 | 8 | 8 | 2 ICLK |
| 0008 7189h | ICU | DTC Activation Enable Register 137 | DTCER137 | 8 | 8 | 2 ICLK |
| 0008 718Ah | ICU | DTC Activation Enable Register 138 | DTCER138 | 8 | 8 | 2 ICLK |
| 0008 718Bh | ICU | DTC Activation Enable Register 139 | DTCER139 | 8 | 8 | 2 ICLK |
| 0008 718Ch | ICU | DTC Activation Enable Register 140 | DTCER140 | 8 | 8 | 2 ICLK |
| 0008 718Dh | ICU | DTC Activation Enable Register 141 | DTCER141 | 8 | 8 | 2 ICLK |
| 0008 71DBh | ICU | DTC Activation Enable Register 219 | DTCER219 | 8 | 8 | 2 ICLK |
| 0008 71DCh | ICU | DTC Activation Enable Register 220 | DTCER220 | 8 | 8 | 2 ICLK |
| 0008 71DFh | ICU | DTC Activation Enable Register 223 | DTCER223 | 8 | 8 | 2 ICLK |
| 0008 71E0h | ICU | DTC Activation Enable Register 224 | DTCER224 | 8 | 8 | 2 ICLK |
| 0008 71EFh | ICU | DTC Activation Enable Register 239 | DTCER239 | 8 | 8 | 2 ICLK |
| 0008 71F0h | ICU | DTC Activation Enable Register 240 | DTCER240 | 8 | 8 | 2 ICLK |
| 0008 71F7h | ICU | DTC Activation Enable Register 247 | DTCER247 | 8 | 8 | 2 ICLK |
| 0008 71F8h | ICU | DTC Activation Enable Register 248 | DTCER248 | 8 | 8 | 2 ICLK |
| 0008 7202h | ICU | Interrupt Request Enable Register 02 | IER02 | 8 | 8 | 2 ICLK |
| 0008 7203h | ICU | Interrupt Request Enable Register 03 | IER03 | 8 | 8 | 2 ICLK |
| 0008 7204h | ICU | Interrupt Request Enable Register 04 | IER04 | 8 | 8 | 2 ICLK |
| 0008 7205h | ICU | Interrupt Request Enable Register 05 | IER05 | 8 | 8 | 2 ICLK |
| 0008 7207h | ICU | Interrupt Request Enable Register 07 | IER07 | 8 | 8 | 2 ICLK |
| 0008 7208h | ICU | Interrupt Request Enable Register 08 | IER08 | 8 | 8 | 2 ICLK |
| 0008 720Bh | ICU | Interrupt Request Enable Register 0B | IER0B | 8 | 8 | 2 ICLK |
| 0008 720Ch | ICU | Interrupt Request Enable Register 0C | IER0C | 8 | 8 | 2 ICLK |
| 0008 720Dh | ICU | Interrupt Request Enable Register 0D | IER0D | 8 | 8 | 2 ICLK |
| 0008 720Eh | ICU | Interrupt Request Enable Register 0E | IER0E | 8 | 8 | 2 ICLK |
| 0008 720Fh | ICU | Interrupt Request Enable Register 0F | IER0F | 8 | 8 | 2 ICLK |
| 0008 7210h | ICU | Interrupt Request Enable Register 10 | IER10 | 8 | 8 | 2 ICLK |
| 0008 7211h | ICU | Interrupt Request Enable Register 11 | IER11 | 8 | 8 | 2 ICLK |
| 0008 7215h | ICU | Interrupt Request Enable Register 15 | IER15 | 8 | 8 | 2 ICLK |
| 0008 721Bh | ICU | Interrupt Request Enable Register 1B | IER1B | 8 | 8 | 2 ICLK |
| 0008 721Ch | ICU | Interrupt Request Enable Register 1C | IER1C | 8 | 8 | 2 ICLK |
| 0008 721Dh | ICU | Interrupt Request Enable Register 1D | IER1D | 8 | 8 | 2 ICLK |
| 0008 721Eh | ICU | Interrupt Request Enable Register 1E | IER1E | 8 | 8 | 2 ICLK |
| 0008 721Fh | ICU | Interrupt Request Enable Register 1F | IER1F | 8 | 8 | 2 ICLK |
| 0008 72E0h | ICU | Software Interrupt Activation Register | SWINTR | 8 | 8 | 2 ICLK |
| 0008 72F0h | ICU | Fast Interrupt Set Register | FIR | 16 | 16 | 2 ICLK |
| 0008 7300h | ICU | Interrupt Source Priority Register 000 | IPR000 | 8 | 8 | 2 ICLK |
| 0008 7303h | ICU | Interrupt Source Priority Register 003 | IPR003 | 8 | 8 | 2 ICLK |
| 0008 7304h | ICU | Interrupt Source Priority Register 004 | IPR004 | 8 | 8 | 2 ICLK |
| 0008 7305h | ICU | Interrupt Source Priority Register 005 | IPR005 | 8 | 8 | 2 ICLK |
| 0008 7320h | ICU | Interrupt Source Priority Register 032 | IPR032 | 8 | 8 | 2 ICLK |
| 0008 7321h | ICU | Interrupt Source Priority Register 033 | IPR033 | 8 | 8 | 2 ICLK |
| 0008 7322h | ICU | Interrupt Source Priority Register 034 | IPR034 | 8 | 8 | 2 ICLK |
| 0008 7324h | ICU | Interrupt Source Priority Register 036 | IPR036 | 8 | 8 | 2 ICLK |
| 0008 7325h | ICU | Interrupt Source Priority Register 037 | IPR037 | 8 | 8 | 2 ICLK |
| 0008 7326h | ICU | Interrupt Source Priority Register 038 | IPR038 | 8 | 8 | 2 ICLK |
| 0008 732Ch | ICU | Interrupt Source Priority Register 044 | IPR044 | 8 | 8 | 2 ICLK |
| 0008 7339h | ICU | Interrupt Source Priority Register 057 | IPR057 | 8 | 8 | 2 ICLK |
| 0008 733Fh | ICU | Interrupt Source Priority Register 063 | IPR063 | 8 | 8 | 2 ICLK |
| 0008 7340h | ICU | Interrupt Source Priority Register 064 | IPR064 | 8 | 8 | 2 ICLK |
| 0008 7341h | ICU | Interrupt Source Priority Register 065 | IPR065 | 8 | 8 | 2 ICLK |
| 0008 7342h | ICU | Interrupt Source Priority Register 066 | IPR066 | 8 | 8 | 2 ICLK |

Table 4.1 List of I/O Registers (Address Order) (5/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|
| 0008 7343h | ICU | Interrupt Source Priority Register 067 | IPR067 | 8 | 8 | 2 ICLK |
| 0008 7344h | ICU | Interrupt Source Priority Register 068 | IPR068 | 8 | 8 | 2 ICLK |
| 0008 7345h | ICU | Interrupt Source Priority Register 069 | IPR069 | 8 | 8 | 2 ICLK |
| 0008 7346h | ICU | Interrupt Source Priority Register 070 | IPR070 | 8 | 8 | 2 ICLK |
| 0008 7347h | ICU | Interrupt Source Priority Register 071 | IPR071 | 8 | 8 | 2 ICLK |
| 0008 7358h | ICU | Interrupt Source Priority Register 088 | IPR088 | 8 | 8 | 2 ICLK |
| 0008 7359h | ICU | Interrupt Source Priority Register 089 | IPR089 | 8 | 8 | 2 ICLK |
| 0008 735Ah | ICU | Interrupt Source Priority Register 090 | IPR090 | 8 | 8 | 2 ICLK |
| 0008 735Ch | ICU | Interrupt Source Priority Register 092 | IPR092 | 8 | 8 | 2 ICLK |
| 0008 735Dh | ICU | Interrupt Source Priority Register 093 | IPR093 | 8 | 8 | 2 ICLK |
| 0008 7366h | ICU | Interrupt Source Priority Register 102 | IPR102 | 8 | 8 | 2 ICLK |
| 0008 7367h | ICU | Interrupt Source Priority Register 103 | IPR103 | 8 | 8 | 2 ICLK |
| 0008 736Ah | ICU | Interrupt Source Priority Register 106 | IPR106 | 8 | 8 | 2 ICLK |
| 0008 7372h | ICU | Interrupt Source Priority Register 114 | IPR114 | 8 | 8 | 2 ICLK |
| 0008 7376h | ICU | Interrupt Source Priority Register 118 | IPR118 | 8 | 8 | 2 ICLK |
| 0008 7379h | ICU | Interrupt Source Priority Register 121 | IPR121 | 8 | 8 | 2 ICLK |
| 0008 737Bh | ICU | Interrupt Source Priority Register 123 | IPR123 | 8 | 8 | 2 ICLK |
| 0008 737Dh | ICU | Interrupt Source Priority Register 125 | IPR125 | 8 | 8 | 2 ICLK |
| 0008 737Fh | ICU | Interrupt Source Priority Register 127 | IPR127 | 8 | 8 | 2 ICLK |
| 0008 7381h | ICU | Interrupt Source Priority Register 129 | IPR129 | 8 | 8 | 2 ICLK |
| 0008 7385h | ICU | Interrupt Source Priority Register 133 | IPR133 | 8 | 8 | 2 ICLK |
| 0008 7386h | ICU | Interrupt Source Priority Register 134 | IPR134 | 8 | 8 | 2 ICLK |
| 0008 738Ah | ICU | Interrupt Source Priority Register 138 | IPR138 | 8 | 8 | 2 ICLK |
| 0008 738Bh | ICU | Interrupt Source Priority Register 139 | IPR139 | 8 | 8 | 2 ICLK |
| 0008 73AAh | ICU | Interrupt Source Priority Register 170 | IPR170 | 8 | 8 | 2 ICLK |
| 0008 73ABh | ICU | Interrupt Source Priority Register 171 | IPR171 | 8 | 8 | 2 ICLK |
| 0008 73DAh | ICU | Interrupt Source Priority Register 218 | IPR218 | 8 | 8 | 2 ICLK |
| 0008 73DEh | ICU | Interrupt Source Priority Register 222 | IPR222 | 8 | 8 | 2 ICLK |
| 0008 73EEh | ICU | Interrupt Source Priority Register 238 | IPR238 | 8 | 8 | 2 ICLK |
| 0008 73F2h | ICU | Interrupt Source Priority Register 242 | IPR242 | 8 | 8 | 2 ICLK |
| 0008 73F3h | ICU | Interrupt Source Priority Register 243 | IPR243 | 8 | 8 | 2 ICLK |
| 0008 73F4h | ICU | Interrupt Source Priority Register 244 | IPR244 | 8 | 8 | 2 ICLK |
| 0008 73F5h | ICU | Interrupt Source Priority Register 245 | IPR245 | 8 | 8 | 2 ICLK |
| 0008 73F6h | ICU | Interrupt Source Priority Register 246 | IPR246 | 8 | 8 | 2 ICLK |
| 0008 73F7h | ICU | Interrupt Source Priority Register 247 | IPR247 | 8 | 8 | 2 ICLK |
| 0008 73F8h | ICU | Interrupt Source Priority Register 248 | IPR248 | 8 | 8 | 2 ICLK |
| 0008 73F9h | ICU | Interrupt Source Priority Register 249 | IPR249 | 8 | 8 | 2 ICLK |
| 0008 7500h | ICU | IRQ Control Register 0 | IRQCR0 | 8 | 8 | 2 ICLK |
| 0008 7501h | ICU | IRQ Control Register 1 | IRQCR1 | 8 | 8 | 2 ICLK |
| 0008 7502h | ICU | IRQ Control Register 2 | IRQCR2 | 8 | 8 | 2 ICLK |
| 0008 7503h | ICU | IRQ Control Register 3 | IRQCR3 | 8 | 8 | 2 ICLK |
| 0008 7504h | ICU | IRQ Control Register 4 | IRQCR4 | 8 | 8 | 2 ICLK |
| 0008 7505h | ICU | IRQ Control Register 5 | IRQCR5 | 8 | 8 | 2 ICLK |
| 0008 7506h | ICU | IRQ Control Register 6 | IRQCR6 | 8 | 8 | 2 ICLK |
| 0008 7507h | ICU | IRQ Control Register 7 | IRQCR7 | 8 | 8 | 2 ICLK |
| 0008 7510h | ICU | IRQ Pin Digital Filter Enable Register 0 | IRQFLTE0 | 8 | 8 | 2 ICLK |
| 0008 7514h | ICU | IRQ Pin Digital Filter Setting Register 0 | IRQFLTC0 | 16 | 16 | 2 ICLK |
| 0008 7580h | ICU | Non-Maskable Interrupt Status Register | NMISR | 8 | 8 | 2 ICLK |
| 0008 7581h | ICU | Non-Maskable Interrupt Enable Register | NMIER | 8 | 8 | 2 ICLK |
| 0008 7582h | ICU | Non-Maskable Interrupt Status Clear Register | NMICLR | 8 | 8 | 2 ICLK |
| 0008 7583h | ICU | NMI Pin Interrupt Control Register | NMICR | 8 | 8 | 2 ICLK |
| 0008 7590h | ICU | NMI Pin Digital Filter Enable Register | NMIFLTE | 8 | 8 | 2 ICLK |

Table 4.1 List of I/O Registers (Address Order) (6/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| 0008 7594h | ICU | NMI Pin Digital Filter Setting Register | NMIFLTC | 8 | 8 | 2 ICLK |
| 0008 8000h | CMT | Compare Match Timer Start Register 0 | CMSTR0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 8002h | CMT0 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8004h | CMT0 | Compare Match Timer Counter | CMCNT | 16 | 16 | 2 or 3 PCLKB |
| 0008 8006h | CMT0 | Compare Match Timer Constant Register | CMCOR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8008h | CMT1 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2 or 3 PCLKB |
| 0008 800Ah | CMT1 | Compare Match Timer Counter | CMCNT | 16 | 16 | 2 or 3 PCLKB |
| 0008 800Ch | CMT1 | Compare Match Timer Constant Register | CMCOR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8030h | IWDT | IWDT Refresh Register | IWDTRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8032h | IWDT | IWDT Control Register | IWDTCR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8034h | IWDT | IWDT Status Register | IWDTSR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8036h | IWDT | IWDT Reset Control Register | IWDTRCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8038h | IWDT | IWDT Count Stop Control Register | IWDTCSTPR | 8 | 8 | 2 or 3 PCLKB |
| 0008 80C0h | DA | D/A Data Register 0 | DADR0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 80C2h | DA | D/A Data Register 1 | DADR1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 80C4h | DA | D/A Control Register | DACR | 8 | 8 | 2 or 3 PCLKB |
| 0008 80C5h | DA | DADRM Format Select Register | DADPR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8280h | CRC | CRC Control Register | CRCCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8281h | CRC | CRC Data Input Register | CRCDIR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8282h | CRC | CRC Data Output Register | CRCDOR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8300h | RIIC0 | I ² C Bus Control Register 1 | ICCR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8301h | RIIC0 | I ² C Bus Control Register 2 | ICCR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8302h | RIIC0 | I ² C Bus Mode Register 1 | ICMR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8303h | RIIC0 | I ² C Bus Mode Register 2 | ICMR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8304h | RIIC0 | I ² C Bus Mode Register 3 | ICMR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8305h | RIIC0 | I ² C Bus Function Enable Register | ICFER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8306h | RIIC0 | I ² C Bus Status Enable Register | ICSER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8307h | RIIC0 | I ² C Bus Interrupt Enable Register | ICIER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8308h | RIIC0 | I ² C Bus Status Register 1 | ICSR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8309h | RIIC0 | I ² C Bus Status Register 2 | ICSR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Ah | RIIC0 | Slave Address Register L0 | SARL0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Ah | RIIC0 | Timeout Internal Counter L | TMOCNTL | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Bh | RIIC0 | Slave Address Register U0 | SARU0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Bh | RIIC0 | Timeout Internal Counter U | TMOCNTU | 8 | 8 *1 | 2 or 3 PCLKB |
| 0008 830Ch | RIIC0 | Slave Address Register L1 | SARL1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Dh | RIIC0 | Slave Address Register U1 | SARU1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Eh | RIIC0 | Slave Address Register L2 | SARL2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 830Fh | RIIC0 | Slave Address Register U2 | SARU2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8310h | RIIC0 | I ² C Bus Bit Rate Low-Level Register | ICBRL | 8 | 8 | 2 or 3 PCLKB |
| 0008 8311h | RIIC0 | I ² C Bus Bit Rate High-Level Register | ICBRH | 8 | 8 | 2 or 3 PCLKB |
| 0008 8312h | RIIC0 | I ² C Bus Transmit Data Register | ICDRT | 8 | 8 | 2 or 3 PCLKB |
| 0008 8313h | RIIC0 | I ² C Bus Receive Data Register | ICDRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8380h | RSPI0 | RSPI Control Register | SPCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8381h | RSPI0 | RSPI Slave Select Polarity Register | SSLP | 8 | 8 | 2 or 3 PCLKB |
| 0008 8382h | RSPI0 | RSPI Pin Control Register | SPPCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8383h | RSPI0 | RSPI Status Register | SPSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8384h | RSPI0 | RSPI Data Register | SPDR | 32 | 16, 32 | 2 or 3 PCLKB/2ICLK |
| 0008 8388h | RSPI0 | RSPI Sequence Control Register | SPSCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8389h | RSPI0 | RSPI Sequence Status Register | SPSSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Ah | RSPI0 | RSPI Bit Rate Register | SPBR | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Bh | RSPI0 | RSPI Data Control Register | SPDCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Ch | RSPI0 | RSPI Clock Delay Register | SPCKD | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (7/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| 0008 838Dh | RSPI0 | RSPI Slave Select Negation Delay Register | SSLND | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Eh | RSPI0 | RSPI Next-Access Delay Register | SPND | 8 | 8 | 2 or 3 PCLKB |
| 0008 838Fh | RSPI0 | RSPI Control Register 2 | SPCR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8390h | RSPI0 | RSPI Command Register 0 | SPCMD0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 8392h | RSPI0 | RSPI Command Register 1 | SPCMD1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 8394h | RSPI0 | RSPI Command Register 2 | SPCMD2 | 16 | 16 | 2 or 3 PCLKB |
| 0008 8396h | RSPI0 | RSPI Command Register 3 | SPCMD3 | 16 | 16 | 2 or 3 PCLKB |
| 0008 8398h | RSPI0 | RSPI Command Register 4 | SPCMD4 | 16 | 16 | 2 or 3 PCLKB |
| 0008 839Ah | RSPI0 | RSPI Command Register 5 | SPCMD5 | 16 | 16 | 2 or 3 PCLKB |
| 0008 839Ch | RSPI0 | RSPI Command Register 6 | SPCMD6 | 16 | 16 | 2 or 3 PCLKB |
| 0008 839Eh | RSPI0 | RSPI Command Register 7 | SPCMD7 | 16 | 16 | 2 or 3 PCLKB |
| 0008 8600h | MTU3 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8601h | MTU4 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8602h | MTU3 | Timer Mode Register | TMDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8603h | MTU4 | Timer Mode Register | TMDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8604h | MTU3 | Timer I/O Control Register H | TIORH | 8 | 8 | 2 or 3 PCLKB |
| 0008 8605h | MTU3 | Timer I/O Control Register L | TIORL | 8 | 8 | 2 or 3 PCLKB |
| 0008 8606h | MTU4 | Timer I/O Control Register H | TIORH | 8 | 8 | 2 or 3 PCLKB |
| 0008 8607h | MTU4 | Timer I/O Control Register L | TIORL | 8 | 8 | 2 or 3 PCLKB |
| 0008 8608h | MTU3 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8609h | MTU4 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2 or 3 PCLKB |
| 0008 860Ah | MTU | Timer Output Master Enable Register | TOER | 8 | 8 | 2 or 3 PCLKB |
| 0008 860Dh | MTU | Timer Gate Control Register | TGCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 860Eh | MTU | Timer Output Control Register 1 | TOCR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 860Fh | MTU | Timer Output Control Register 2 | TOCR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8610h | MTU3 | Timer Counter | TCNT | 16 | 16 | 2 or 3 PCLKB |
| 0008 8612h | MTU4 | Timer Counter | TCNT | 16 | 16 | 2 or 3 PCLKB |
| 0008 8614h | MTU | Timer Cycle Data Register | TCDR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8616h | MTU | Timer Dead Time Data Register | TDDR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8618h | MTU3 | Timer General Register A | TGRA | 16 | 16 | 2 or 3 PCLKB |
| 0008 861Ah | MTU3 | Timer General Register B | TGRB | 16 | 16 | 2 or 3 PCLKB |
| 0008 861Ch | MTU4 | Timer General Register A | TGRA | 16 | 16 | 2 or 3 PCLKB |
| 0008 861Eh | MTU4 | Timer General Register B | TGRB | 16 | 16 | 2 or 3 PCLKB |
| 0008 8620h | MTU | Timer Subcounter | TCNTS | 16 | 16 | 2 or 3 PCLKB |
| 0008 8622h | MTU | Timer Cycle Buffer Register | TCBR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8624h | MTU3 | Timer General Register C | TGRC | 16 | 16 | 2 or 3 PCLKB |
| 0008 8626h | MTU3 | Timer General Register D | TGRD | 16 | 16 | 2 or 3 PCLKB |
| 0008 8628h | MTU4 | Timer General Register C | TGRC | 16 | 16 | 2 or 3 PCLKB |
| 0008 862Ah | MTU4 | Timer General Register D | TGRD | 16 | 16 | 2 or 3 PCLKB |
| 0008 862Ch | MTU3 | Timer Status Register | TSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 862Dh | MTU4 | Timer Status Register | TSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8630h | MTU | Timer Interrupt Skipping Set Register | TITCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8631h | MTU | Timer Interrupt Skipping Counter | TITCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 8632h | MTU | Timer Buffer Transfer Set Register | TBTERR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8634h | MTU | Timer Dead Time Enable Register | TDER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8636h | MTU | Timer Output Level Buffer Register | TOLBR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8638h | MTU3 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 2 or 3 PCLKB |
| 0008 8639h | MTU4 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 2 or 3 PCLKB |
| 0008 8640h | MTU4 | Timer A/D Converter Start Request Control Register | TADCR | 16 | 16 | 2 or 3 PCLKB |
| 0008 8644h | MTU4 | Timer A/D Converter Start Request Cycle Set Register A | TADCORA | 16 | 16 | 2 or 3 PCLKB |
| 0008 8646h | MTU4 | Timer A/D Converter Start Request Cycle Set Register B | TADCORB | 16 | 16 | 2 or 3 PCLKB |
| 0008 8648h | MTU4 | Timer A/D Converter Start Request Cycle Set Buffer Register A | TADCOBRA | 16 | 16 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (8/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| 0008 864Ah | MTU4 | Timer A/D Converter Start Request Cycle Set Buffer Register B | TADCOBRB | 16 | 16 | 2 or 3 PCLKB |
| 0008 8660h | MTU | Timer Waveform Control Register | TWCR | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 8680h | MTU | Timer Start Register | TSTR | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 8681h | MTU | Timer Synchronous Register | TSYR | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 8684h | MTU | Timer Read/Write Enable Register | TRWER | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 8690h | MTU0 | Noise Filter Control Register | NFCR | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 8691h | MTU1 | Noise Filter Control Register | NFCR | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 8692h | MTU2 | Noise Filter Control Register | NFCR | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 8693h | MTU3 | Noise Filter Control Register | NFCR | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 8694h | MTU4 | Noise Filter Control Register | NFCR | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 8695h | MTU5 | Noise Filter Control Register | NFCR | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 8700h | MTU0 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8701h | MTU0 | Timer Mode Register | TMDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8702h | MTU0 | Timer I/O Register H | TIORH | 8 | 8 | 2 or 3 PCLKB |
| 0008 8703h | MTU0 | Timer I/O Control Register L | TIORL | 8 | 8 | 2 or 3 PCLKB |
| 0008 8704h | MTU0 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8705h | MTU0 | Timer Status Register | TSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8706h | MTU0 | Timer Counter | TCNT | 16 | 16 | 2 or 3 PCLKB |
| 0008 8708h | MTU0 | Timer General Register A | TGRA | 16 | 16 | 2 or 3 PCLKB |
| 0008 870Ah | MTU0 | Timer General Register B | TGRB | 16 | 16 | 2 or 3 PCLKB |
| 0008 870Ch | MTU0 | Timer General Register C | TGRC | 16 | 16 | 2 or 3 PCLKB |
| 0008 870Eh | MTU0 | Timer General Register D | TGRD | 16 | 16 | 2 or 3 PCLKB |
| 0008 8720h | MTU0 | Timer General Register E | TGRE | 16 | 16 | 2 or 3 PCLKB |
| 0008 8722h | MTU0 | Timer General Register F | TGRF | 16 | 16 | 2 or 3 PCLKB |
| 0008 8724h | MTU0 | Timer Interrupt Enable Register 2 | TIER2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 8726h | MTU0 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 2 or 3 PCLKB |
| 0008 8780h | MTU1 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8781h | MTU1 | Timer Mode Register | TMDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8782h | MTU1 | Timer I/O Control Register | TIOR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8784h | MTU1 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8785h | MTU1 | Timer Status Register | TSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8786h | MTU1 | Timer Counter | TCNT | 16 | 16 | 2 or 3 PCLKB |
| 0008 8788h | MTU1 | Timer General Register A | TGRA | 16 | 16 | 2 or 3 PCLKB |
| 0008 878Ah | MTU1 | Timer General Register B | TGRB | 16 | 16 | 2 or 3 PCLKB |
| 0008 8790h | MTU1 | Timer Input Capture Control Register | TICCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8800h | MTU2 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8801h | MTU2 | Timer Mode Register | TMDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8802h | MTU2 | Timer I/O Control Register | TIOR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8804h | MTU2 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2 or 3 PCLKB |
| 0008 8805h | MTU2 | Timer Status Register | TSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8806h | MTU2 | Timer Counter | TCNT | 16 | 16 | 2 or 3 PCLKB |
| 0008 8808h | MTU2 | Timer General Register A | TGRA | 16 | 16 | 2 or 3 PCLKB |
| 0008 880Ah | MTU2 | Timer General Register B | TGRB | 16 | 16 | 2 or 3 PCLKB |
| 0008 8880h | MTU5 | Timer Counter U | TCNTU | 16 | 16 | 2 or 3 PCLKB |
| 0008 8882h | MTU5 | Timer General Register U | TGRU | 16 | 16 | 2 or 3 PCLKB |
| 0008 8884h | MTU5 | Timer Control Register U | TCRU | 8 | 8 | 2 or 3 PCLKB |
| 0008 8886h | MTU5 | Timer I/O Control Register U | TIORU | 8 | 8 | 2 or 3 PCLKB |
| 0008 8890h | MTU5 | Timer Counter V | TCNTV | 16 | 16 | 2 or 3 PCLKB |
| 0008 8892h | MTU5 | Timer General Register V | TGRV | 16 | 16 | 2 or 3 PCLKB |
| 0008 8894h | MTU5 | Timer Control Register V | TCRV | 8 | 8 | 2 or 3 PCLKB |
| 0008 8896h | MTU5 | Timer I/O Control Register V | TIORV | 8 | 8 | 2 or 3 PCLKB |
| 0008 88A0h | MTU5 | Timer Counter W | TCNTW | 16 | 16 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (9/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|
| 0008 88A2h | MTU5 | Timer General Register W | TGRW | 16 | 16 | 2 or 3 PCLKB |
| 0008 88A4h | MTU5 | Timer Control Register W | TCRW | 8 | 8 | 2 or 3 PCLKB |
| 0008 88A6h | MTU5 | Timer I/O Control Register W | TIORW | 8 | 8 | 2 or 3 PCLKB |
| 0008 88B2h | MTU5 | Timer Interrupt Enable Register | TIER | 8 | 8 | 2 or 3 PCLKB |
| 0008 88B4h | MTU5 | Timer Start Register | TSTR | 8 | 8 | 2 or 3 PCLKB |
| 0008 88B6h | MTU5 | Timer Compare Match Clear Register | TCNTCMPCLR | 8 | 8 | 2 or 3 PCLKB |
| 0008 8900h | POE | Input Level Control/Status Register 1 | ICSR1 | 16 | 8, 16 | 2 or 3 PCLKB |
| 0008 8902h | POE | Output Level Control/Status Register 1 | OCSR1 | 16 | 8, 16 | 2 or 3 PCLKB |
| 0008 8908h | POE | Input Level Control/Status Register 2 | ICSR2 | 16 | 8, 16 | 2 or 3 PCLKB |
| 0008 890Ah | POE | Software Port Output Enable Register | SPOER | 8 | 8 | 2 or 3 PCLKB |
| 0008 890Bh | POE | Port Output Enable Control Register 1 | POECR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 890Ch | POE | Port Output Enable Control Register 2 | POECR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 890Eh | POE | Input Level Control/Status Register 3 | ICSR3 | 16 | 8, 16 | 2 or 3 PCLKB |
| 0008 9000h | S12AD | A/D Control Register | ADCSR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9004h | S12AD | A/D Channel Select Register A | ADANSA | 16 | 16 | 2 or 3 PCLKB |
| 0008 9008h | S12AD | A/D-Converted Value Addition Mode Select Register | ADADS | 16 | 16 | 2 or 3 PCLKB |
| 0008 900Ch | S12AD | A/D-Converted Value Addition Count Select Register | ADADC | 8 | 8 | 2 or 3 PCLKB |
| 0008 900Eh | S12AD | A/D Control Extended Register | ADCER | 16 | 16 | 2 or 3 PCLKB |
| 0008 9010h | S12AD | A/D Start Trigger Select Register | ADSTRGR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9012h | S12AD | A/D Converted Extended Input Control Register | ADEXICR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9014h | S12AD | A/D Channel Select Register B | ADANSB | 16 | 16 | 2 or 3 PCLKB |
| 0008 9018h | S12AD | A/D Data Duplication Register | ADDBLDR | 16 | 16 | 2 or 3 PCLKB |
| 0008 901Ah | S12AD | A/D Temperature Sensor Data Register | ADTSRDR | 16 | 16 | 2 or 3 PCLKB |
| 0008 901Ch | S12AD | A/D Internal Reference Voltage Data Register | ADOCDR | 16 | 16 | 2 or 3 PCLKB |
| 0008 9020h | S12AD | A/D Data Register 0 | ADDR0 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9022h | S12AD | A/D Data Register 1 | ADDR1 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9024h | S12AD | A/D Data Register 2 | ADDR2 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9026h | S12AD | A/D Data Register 3 | ADDR3 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9028h | S12AD | A/D Data Register 4 | ADDR4 | 16 | 16 | 2 or 3 PCLKB |
| 0008 902Ch | S12AD | A/D Data Register 6 | ADDR6 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9030h | S12AD | A/D Data Register 8 | ADDR8 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9032h | S12AD | A/D Data Register 9 | ADDR9 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9034h | S12AD | A/D Data Register 10 | ADDR10 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9036h | S12AD | A/D Data Register 11 | ADDR11 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9038h | S12AD | A/D Data Register 12 | ADDR12 | 16 | 16 | 2 or 3 PCLKB |
| 0008 903Ah | S12AD | A/D Data Register 13 | ADDR13 | 16 | 16 | 2 or 3 PCLKB |
| 0008 903Ch | S12AD | A/D Data Register 14 | ADDR14 | 16 | 16 | 2 or 3 PCLKB |
| 0008 903Eh | S12AD | A/D Data Register 15 | ADDR15 | 16 | 16 | 2 or 3 PCLKB |
| 0008 9060h | S12AD | A/D Sampling State Register 0 | ADSSTR0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 9061h | S12AD | A/D Sampling State Register L | ADSSTRL | 8 | 8 | 2 or 3 PCLKB |
| 0008 9070h | S12AD | A/D Sampling State Register T | ADSSTRT | 8 | 8 | 2 or 3 PCLKB |
| 0008 9071h | S12AD | A/D Sampling State Register O | ADSSTRO | 8 | 8 | 2 or 3 PCLKB |
| 0008 9073h | S12AD | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 9074h | S12AD | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 9075h | S12AD | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 9076h | S12AD | A/D Sampling State Register 4 | ADSSTR4 | 8 | 8 | 2 or 3 PCLKB |
| 0008 9078h | S12AD | A/D Sampling State Register 6 | ADSSTR6 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A020h | SCI1 | Serial Mode Register | SMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A021h | SCI1 | Bit Rate Register | BRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A022h | SCI1 | Serial Control Register | SCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A023h | SCI1 | Transmit Data Register | TDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A024h | SCI1 | Serial Status Register | SSR | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (10/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|
| 0008 A025h | SCI1 | Receive Data Register | RDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A026h | SCI1 | Smart Card Mode Register | SCMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A027h | SCI1 | Serial Extended Mode Register | SEMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A028h | SCI1 | Noise Filter Setting Register | SNFR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A029h | SCI1 | I ² C Mode Register 1 | SIMR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Ah | SCI1 | I ² C Mode Register 2 | SIMR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Bh | SCI1 | I ² C Mode Register 3 | SIMR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Ch | SCI1 | I ² C Status Register | SISR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A02Dh | SCI1 | SPI Mode Register | SPMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A0h | SCI5 | Serial Mode Register | SMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A1h | SCI5 | Bit Rate Register | BRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A2h | SCI5 | Serial Control Register | SCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A3h | SCI5 | Transmit Data Register | TDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A4h | SCI5 | Serial Status Register | SSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A5h | SCI5 | Receive Data Register | RDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A6h | SCI5 | Smart Card Mode Register | SCMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A7h | SCI5 | Serial Extended Mode Register | SEMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A8h | SCI5 | Noise Filter Setting Register | SNFR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0A9h | SCI5 | I ² C Mode Register 1 | SIMR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0AAh | SCI5 | I ² C Mode Register 2 | SIMR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0ABh | SCI5 | I ² C Mode Register 3 | SIMR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0ACh | SCI5 | I ² C Status Register | SISR | 8 | 8 | 2 or 3 PCLKB |
| 0008 A0ADh | SCI5 | SPI Mode Register | SPMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B000h | CAC | CAC Control Register 0 | CACR0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B001h | CAC | CAC Control Register 1 | CACR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B002h | CAC | CAC Control Register 2 | CACR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B003h | CAC | CAC Interrupt Request Enable Register | CAICR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B004h | CAC | CAC Status Register | CASTR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B006h | CAC | CAC Upper-Limit Value Setting Register | CAULVR | 16 | 16 | 2 or 3 PCLKB |
| 0008 B008h | CAC | CAC Lower-Limit Value Setting Register | CALLVR | 16 | 16 | 2 or 3 PCLKB |
| 0008 B00Ah | CAC | CAC Counter Buffer Register | CACNTBR | 16 | 16 | 2 or 3 PCLKB |
| 0008 B080h | DOC | DOC Control Register | DOCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B082h | DOC | DOC Data Input Register | DODIR | 16 | 16 | 2 or 3 PCLKB |
| 0008 B084h | DOC | DOC Data Setting Register | DODSR | 16 | 16 | 2 or 3 PCLKB |
| 0008 B100h | ELC | Event Link Control Register | ELCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B102h | ELC | Event Link Setting Register 1 | ELSR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B103h | ELC | Event Link Setting Register 2 | ELSR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B104h | ELC | Event Link Setting Register 3 | ELSR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B105h | ELC | Event Link Setting Register 4 | ELSR4 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B108h | ELC | Event Link Setting Register 7 | ELSR7 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B110h | ELC | Event Link Setting Register 15 | ELSR15 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B111h | ELC | Event Link Setting Register 16 | ELSR16 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B113h | ELC | Event Link Setting Register 18 | ELSR18 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B115h | ELC | Event Link Setting Register 20 | ELSR20 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B117h | ELC | Event Link Setting Register 22 | ELSR22 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B119h | ELC | Event Link Setting Register 24 | ELSR24 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B11Ah | ELC | Event Link Setting Register 25 | ELSR25 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B11Fh | ELC | Event Link Option Setting Register A | ELOPA | 8 | 8 | 2 or 3 PCLKB |
| 0008 B120h | ELC | Event Link Option Setting Register B | ELOPB | 8 | 8 | 2 or 3 PCLKB |
| 0008 B121h | ELC | Event Link Option Setting Register C | ELOPC | 8 | 8 | 2 or 3 PCLKB |
| 0008 B123h | ELC | Port Group Setting Register 1 | PGR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B125h | ELC | Port Group Control Register 1 | PGC1 | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (11/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| 0008 B127h | ELC | Port Buffer Register 1 | PDBF1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B129h | ELC | Event Link Port Setting Register 0 | PEL0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B12Ah | ELC | Event Link Port Setting Register 1 | PEL1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B12Dh | ELC | Event Link Software Event Generation Register | ELSEGR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B300h | SCI12 | Serial Mode Register | SMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B301h | SCI12 | Bit Rate Register | BRR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B302h | SCI12 | Serial Control Register | SCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B303h | SCI12 | Transmit Data Register | TDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B304h | SCI12 | Serial Status Register | SSR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B305h | SCI12 | Receive Data Register | RDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B306h | SCI12 | Smart Card Mode Register | SCMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B307h | SCI12 | Serial Extended Mode Register | SEMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B308h | SCI12 | Noise Filter Setting Register | SNFR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B309h | SCI12 | I ² C Mode Register 1 | SIMR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B30Ah | SCI12 | I ² C Mode Register 2 | SIMR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B30Bh | SCI12 | I ² C Mode Register 3 | SIMR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B30Ch | SCI12 | I ² C Status Register | SISR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B30Dh | SCI12 | SPI Mode Register | SPMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B320h | SCI12 | Extended Serial Mode Enable Register | ESMER | 8 | 8 | 2 or 3 PCLKB |
| 0008 B321h | SCI12 | Control Register 0 | CR0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B322h | SCI12 | Control Register 1 | CR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B323h | SCI12 | Control Register 2 | CR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B324h | SCI12 | Control Register 3 | CR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 B325h | SCI12 | Port Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B326h | SCI12 | Interrupt Control Register | ICR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B327h | SCI12 | Status Register | STR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B328h | SCI12 | Status Clear Register | STCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B329h | SCI12 | Control Field 0 Data Register | CF0DR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B32Ah | SCI12 | Control Field 0 Compare Enable Register | CF0CR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B32Bh | SCI12 | Control Field 0 Receive Data Register | CF0RR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B32Ch | SCI12 | Primary Control Field 1 Data Register | PCF1DR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B32Dh | SCI12 | Secondary Control Field 1 Data Register | SCF1DR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B32Eh | SCI12 | Control Field 1 Compare Enable Register | CF1CR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B32Fh | SCI12 | Control Field 1 Receive Data Register | CF1RR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B330h | SCI12 | Timer Control Register | TCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B331h | SCI12 | Timer Mode Register | TMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 B332h | SCI12 | Timer Prescaler Register | TPRE | 8 | 8 | 2 or 3 PCLKB |
| 0008 B333h | SCI12 | Timer Count Register | TCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 C000h | PORT0 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C001h | PORT1 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C002h | PORT2 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C003h | PORT3 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C004h | PORT4 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C005h | PORT5 | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C00Ah | PORTA | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C00Bh | PORTB | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C00Ch | PORTC | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C00Eh | PORTE | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C012h | PORTJ | Port Direction Register | PDR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C020h | PORT0 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C021h | PORT1 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C022h | PORT2 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (12/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|---------------------------|-----------------|----------------|-------------|---|
| 0008 C023h | PORT3 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C024h | PORT4 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C025h | PORT5 | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C02Ah | PORTA | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C02Bh | PORTB | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C02Ch | PORTC | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C02Eh | PORTE | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C032h | PORTJ | Port Output Data Register | PODR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C040h | PORT0 | Port Input Data Register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing |
| 0008 C041h | PORT1 | Port Input Data Register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing |
| 0008 C042h | PORT2 | Port Input Data Register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing |
| 0008 C043h | PORT3 | Port Input Data Register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing |
| 0008 C044h | PORT4 | Port Input Data Register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing |
| 0008 C045h | PORT5 | Port Input Data Register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing |
| 0008 C04Ah | PORTA | Port Input Data Register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing |
| 0008 C04Bh | PORTB | Port Input Data Register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing |
| 0008 C04Ch | PORTC | Port Input Data Register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing |
| 0008 C04Eh | PORTE | Port Input Data Register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing |
| 0008 C051h | PORTH | Port Input Data Register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing |
| 0008 C052h | PORTJ | Port Input Data Register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing |
| 0008 C060h | PORT0 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C061h | PORT1 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C062h | PORT2 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C063h | PORT3 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C064h | PORT4 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C065h | PORT5 | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C06Ah | PORTA | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C06Bh | PORTB | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C06Ch | PORTC | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C06Eh | PORTE | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C071h | PORTH | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C072h | PORTJ | Port Mode Register | PMR | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (13/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|
| 0008 C083h | PORT1 | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C085h | PORT2 | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C086h | PORT3 | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C094h | PORTA | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C095h | PORTA | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C096h | PORTB | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C097h | PORTB | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C098h | PORTC | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C099h | PORTC | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C09Ch | PORTE | Open Drain Control Register 0 | ODR0 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C09Dh | PORTE | Open Drain Control Register 1 | ODR1 | 8 | 8, 16 | 2 or 3 PCLKB |
| 0008 C0C0h | PORT0 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C1h | PORT1 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C2h | PORT2 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C3h | PORT3 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0C5h | PORT5 | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0CAh | PORTA | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0CBh | PORTB | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0CCh | PORTC | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C0CEh | PORTE | Pull-Up Control Register | PCR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C11Fh | MPC | Write-Protect Register | PWPR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C120h | PORT | Port Switching Register B | PSRB | 8 | 8 | 2 or 3 PCLKB |
| 0008 C121h | PORT | Port Switching Register A | PSRA | 8 | 8 | 2 or 3 PCLKB |
| 0008 C143h | MPC | P03 Pin Function Control Register | P03PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C145h | MPC | P05 Pin Function Control Register | P05PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C14Ch | MPC | P14 Pin Function Control Register | P14PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C14Dh | MPC | P15 Pin Function Control Register | P15PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C14Eh | MPC | P16 Pin Function Control Register | P16PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C14Fh | MPC | P17 Pin Function Control Register | P17PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C156h | MPC | P26 Pin Function Control Register | P26PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C157h | MPC | P27 Pin Function Control Register | P27PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C158h | MPC | P30 Pin Function Control Register | P30PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C159h | MPC | P31 Pin Function Control Register | P31PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C15Ah | MPC | P32 Pin Function Control Register | P32PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C160h | MPC | P40 Pin Function Control Register | P40PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C161h | MPC | P41 Pin Function Control Register | P41PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C162h | MPC | P42 Pin Function Control Register | P42PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C163h | MPC | P43 Pin Function Control Register | P43PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C164h | MPC | P44 Pin Function Control Register | P44PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C166h | MPC | P46 Pin Function Control Register | P46PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C16Ch | MPC | P54 Pin Function Control Register | P54PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C16Dh | MPC | P55 Pin Function Control Register | P55PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C190h | MPC | PA0 Pin Function Control Register | PA0PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C191h | MPC | PA1 Pin Function Control Register | PA1PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C193h | MPC | PA3 Pin Function Control Register | PA3PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C194h | MPC | PA4 Pin Function Control Register | PA4PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C196h | MPC | PA6 Pin Function Control Register | PA6PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C198h | MPC | PB0 Pin Function Control Register | PB0PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C199h | MPC | PB1 Pin Function Control Register | PB1PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Bh | MPC | PB3 Pin Function Control Register | PB3PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Dh | MPC | PB5 Pin Function Control Register | PB5PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C19Eh | MPC | PB6 Pin Function Control Register | PB6PFS | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (14/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| 0008 C19Fh | MPC | PB7 Pin Function Control Register | PB7PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A2h | MPC | PC2 Pin Function Control Register | PC2PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A3h | MPC | PC3 Pin Function Control Register | PC3PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A4h | MPC | PC4 Pin Function Control Register | PC4PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A5h | MPC | PC5 Pin Function Control Register | PC5PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A6h | MPC | PC6 Pin Function Control Register | PC6PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1A7h | MPC | PC7 Pin Function Control Register | PC7PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B0h | MPC | PE0 Pin Function Control Register | PE0PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B1h | MPC | PE1 Pin Function Control Register | PE1PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B2h | MPC | PE2 Pin Function Control Register | PE2PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B3h | MPC | PE3 Pin Function Control Register | PE3PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B4h | MPC | PE4 Pin Function Control Register | PE4PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B5h | MPC | PE5 Pin Function Control Register | PE5PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B6h | MPC | PE6 Pin Function Control Register | PE6PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1B7h | MPC | PE7 Pin Function Control Register | PE7PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1D6h | MPC | PJ6 Pin Function Control Register | PJ6PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C1D7h | MPC | PJ7 Pin Function Control Register | PJ7PFS | 8 | 8 | 2 or 3 PCLKB |
| 0008 C290h | SYSTEM | Reset Status Register 0 | RSTSR0 | 8 | 8 | 4 or 5 PCLKB |
| 0008 C291h | SYSTEM | Reset Status Register 1 | RSTSR1 | 8 | 8 | 4 or 5 PCLKB |
| 0008 C293h | SYSTEM | Main Clock Oscillator Forced Oscillation Control Register | MOFCR | 8 | 8 | 4 or 5 PCLKB |
| 0008 C297h | SYSTEM | Voltage Monitoring Circuit Control Register | LVCMPCR | 8 | 8 | 4 or 5 PCLKB |
| 0008 C298h | SYSTEM | Voltage Detection Level Select Register | LVDLVLR | 8 | 8 | 4 or 5 PCLKB |
| 0008 C29Ah | SYSTEM | Voltage Monitoring 1 Circuit Control Register 0 | LVD1CR0 | 8 | 8 | 4 or 5 PCLKB |
| 0008 C29Bh | SYSTEM | Voltage Monitoring 2 Circuit Control Register 0 | LVD2CR0 | 8 | 8 | 4 or 5 PCLKB |
| 0008 C400h | RTC | 64-Hz Counter | R64CNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 C402h | RTC | Second Counter | RSECCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 C402h | RTC | Binary Counter 0 | BCNT0 | 8 | 8 | 2 or 3 PCLKB |
| 0008 C404h | RTC | Minute Counter | RMINCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 C404h | RTC | Binary Counter 1 | BCNT1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 C406h | RTC | Hour Counter | RHRCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 C406h | RTC | Binary Counter 2 | BCNT2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 C408h | RTC | Day-Of-Week Counter | RWKCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 C408h | RTC | Binary Counter 3 | BCNT3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 C40Ah | RTC | Date Counter | RDAYCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 C40Ch | RTC | Month Counter | RMONCNT | 8 | 8 | 2 or 3 PCLKB |
| 0008 C40Eh | RTC | Year Counter | RYRCNT | 16 | 16 | 2 or 3 PCLKB |
| 0008 C410h | RTC | Second Alarm Register | RSECAR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C410h | RTC | Binary Counter 0 Alarm Register | BCNT0AR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C412h | RTC | Minute Alarm Register | RMINAR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C412h | RTC | Binary Counter 1 Alarm Register | BCNT1AR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C414h | RTC | Hour Alarm Register | RHRAR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C414h | RTC | Binary Counter 2 Alarm Register | BCNT2AR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C416h | RTC | Day-of-Week Alarm Register | RWKAR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C416h | RTC | Binary Counter 3 Alarm Register | BCNT3AR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C418h | RTC | Date Alarm Register | RDAYAR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C418h | RTC | Binary Counter 0 Alarm Enable Register | BCNT0AER | 8 | 8 | 2 or 3 PCLKB |
| 0008 C41Ah | RTC | Month Alarm Register | RMONAR | 8 | 8 | 2 or 3 PCLKB |
| 0008 C41Ah | RTC | Binary Counter 1 Alarm Enable Register | BCNT1AER | 8 | 8 | 2 or 3 PCLKB |
| 0008 C41Ch | RTC | Year Alarm Register | RYRAR | 16 | 16 | 2 or 3 PCLKB |
| 0008 C41Ch | RTC | Binary Counter 2 Alarm Enable Register | BCNT2AER | 16 | 16 | 2 or 3 PCLKB |
| 0008 C41Eh | RTC | Year Alarm Enable Register | RYRAREN | 8 | 8 | 2 or 3 PCLKB |
| 0008 C41Eh | RTC | Binary Counter 3 Alarm Enable Register | BCNT3AER | 8 | 8 | 2 or 3 PCLKB |

Table 4.1 List of I/O Registers (Address Order) (15/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|
| 0008 C422h | RTC | RTC Control Register 1 | RCR1 | 8 | 8 | 2 or 3 PCLKB |
| 0008 C424h | RTC | RTC Control Register 2 | RCR2 | 8 | 8 | 2 or 3 PCLKB |
| 0008 C426h | RTC | RTC Control Register 3 | RCR3 | 8 | 8 | 2 or 3 PCLKB |
| 0008 C42Eh | RTC | Time Error Adjustment Register | RADJ | 8 | 8 | 2 or 3 PCLKB |
| 000A 0000h | USB0 | System Configuration Control Register | SYSCFG | 16 | 16 | 3 or 4 PCLKB |
| 000A 0004h | USB0 | System Configuration Status Register 0 | SYSSTS0 | 16 | 16 | 9 PCLK or more |
| 000A 0008h | USB0 | Device State Control Register 0 | DVSTCTR0 | 16 | 16 | 9 PCLK or more |
| 000A 0014h | USB0 | CFIFO Port Register | CFIFO | 16 | 16 | 3 or 4 PCLKB |
| 000A 0018h | USB0 | D0FIFO Port Register | D0FIFO | 16 | 16 | 3 or 4 PCLKB |
| 000A 001Ch | USB0 | D1FIFO Port Register | D1FIFO | 16 | 16 | 3 or 4 PCLKB |
| 000A 0020h | USB0 | CFIFO Port Select Register | CFIFOSEL | 16 | 16 | 3 or 4 PCLKB |
| 000A 0028h | USB0 | D0FIFO Port Select Register | D0FIFOSEL | 16 | 16 | 3 or 4 PCLKB |
| 000A 002Ch | USB0 | D1FIFO Port Select Register | D1FIFOSEL | 16 | 16 | 3 or 4 PCLKB |
| 000A 0022h | USB0 | CFIFO Port Control Register | CFIFOCTR | 16 | 16 | 3 or 4 PCLKB |
| 000A 002Ah | USB0 | D0FIFO Port Control Register | D0FIFOCTR | 16 | 16 | 3 or 4 PCLKB |
| 000A 002Eh | USB0 | D1FIFO Port Control Register | D1FIFOCTR | 16 | 16 | 3 or 4 PCLKB |
| 000A 0030h | USB0 | Interrupt Enable Register 0 | INTENB0 | 16 | 16 | 9 PCLKB or more |
| 000A 0032h | USB0 | Interrupt Enable Register 1 | INTENB1 | 16 | 16 | 9 PCLKB or more |
| 000A 0036h | USB0 | BRDY Interrupt Enable Register | BRDYENB | 16 | 16 | 9 PCLKB or more |
| 000A 0038h | USB0 | NRDY Interrupt Enable Register | NRDYENB | 16 | 16 | 9 PCLKB or more |
| 000A 003Ah | USB0 | BEMP Interrupt Enable Register | BEMPENB | 16 | 16 | 9 PCLKB or more |
| 000A 003Ch | USB0 | SOF Output Configuration Register | SOFCFG | 16 | 16 | 9 PCLKB or more |
| 000A 0040h | USB0 | Interrupt Status Register 0 | INTSTS0 | 16 | 16 | 9 PCLKB or more |
| 000A 0042h | USB0 | Interrupt Status Register 1 | INTSTS1 | 16 | 16 | 9 PCLKB or more |
| 000A 0046h | USB0 | BRDY Interrupt Status Register | BRDYSTS | 16 | 16 | 9 PCLKB or more |
| 000A 0048h | USB0 | NRDY Interrupt Status Register | NRDYSTS | 16 | 16 | 9 PCLKB or more |
| 000A 004Ah | USB0 | BEMP Interrupt Status Register | BEMPSTS | 16 | 16 | 9 PCLKB or more |
| 000A 004Ch | USB0 | Frame Number Register | FRMNUM | 16 | 16 | 9 PCLKB or more |
| 000A 0054h | USB0 | USB Request Type Register | USBREQ | 16 | 16 | 9 PCLKB or more |
| 000A 0056h | USB0 | USB Request Value Register | USBVAL | 16 | 16 | 9 PCLKB or more |
| 000A 0058h | USB0 | USB Request Index Register | USBINDX | 16 | 16 | 9 PCLKB or more |
| 000A 005Ah | USB0 | USB Request Length Register | USBLENG | 16 | 16 | 9 PCLKB or more |
| 000A 005Ch | USB0 | DCP Configuration Register | DCPCFG | 16 | 16 | 9 PCLKB or more |
| 000A 005Eh | USB0 | DCP Maximum Packet Size Register | DCPMAXP | 16 | 16 | 9 PCLKB or more |
| 000A 0060h | USB0 | DCP Control Register | DCPCTR | 16 | 16 | 9 PCLKB or more |
| 000A 0064h | USB0 | Pipe Window Select Register | PIPESEL | 16 | 16 | 9 PCLKB or more |
| 000A 0068h | USB0 | Pipe Configuration Register | PIPECFG | 16 | 16 | 9 PCLKB or more |
| 000A 006Ch | USB0 | Pipe Maximum Packet Size Register | PIPEMAXP | 16 | 16 | 9 PCLKB or more |
| 000A 006Eh | USB0 | Pipe Cycle Control Register | PIPEPERI | 16 | 16 | 9 PCLKB or more |
| 000A 0070h | USB0 | PIPE1 Control Register | PIPE1CTR | 16 | 16 | 9 PCLKB or more |
| 000A 0072h | USB0 | PIPE2 Control Register | PIPE2CTR | 16 | 16 | 9 PCLKB or more |
| 000A 0074h | USB0 | PIPE3 Control Register | PIPE3CTR | 16 | 16 | 9 PCLKB or more |
| 000A 0076h | USB0 | PIPE4 Control Register | PIPE4CTR | 16 | 16 | 9 PCLKB or more |
| 000A 0078h | USB0 | PIPE5 Control Register | PIPE5CTR | 16 | 16 | 9 PCLKB or more |
| 000A 007Ah | USB0 | PIPE6 Control Register | PIPE6CTR | 16 | 16 | 9 PCLKB or more |
| 000A 007Ch | USB0 | PIPE7 Control Register | PIPE7CTR | 16 | 16 | 9 PCLKB or more |
| 000A 007Eh | USB0 | PIPE8 Control Register | PIPE8CTR | 16 | 16 | 9 PCLKB or more |
| 000A 0080h | USB0 | PIPE9 Control Register | PIPE9CTR | 16 | 16 | 9 PCLKB or more |
| 000A 0090h | USB0 | PIPE1 Transaction Counter Enable Register | PIPE1TRE | 16 | 16 | 9 PCLKB or more |
| 000A 0092h | USB0 | PIPE1 Transaction Counter Register | PIPE1TRN | 16 | 16 | 9 PCLKB or more |
| 000A 0094h | USB0 | PIPE2 Transaction Counter Enable Register | PIPE2TRE | 16 | 16 | 9 PCLKB or more |
| 000A 0096h | USB0 | PIPE2 Transaction Counter Register | PIPE2TRN | 16 | 16 | 9 PCLKB or more |

Table 4.1 List of I/O Registers (Address Order) (16/16)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|
| 000A 0098h | USB0 | PIPE3 Transaction Counter Enable Register | PIPE3TRE | 16 | 16 | 9 PCLKB or more |
| 000A 009Ah | USB0 | PIPE3 Transaction Counter Register | PIPE3TRN | 16 | 16 | 9 PCLKB or more |
| 000A 009Ch | USB0 | PIPE4 Transaction Counter Enable Register | PIPE4TRE | 16 | 16 | 9 PCLKB or more |
| 000A 009Eh | USB0 | PIPE4 Transaction Counter Register | PIPE4TRN | 16 | 16 | 9 PCLKB or more |
| 000A 00A0h | USB0 | PIPE5 Transaction Counter Enable Register | PIPE5TRE | 16 | 16 | 9 PCLKB or more |
| 000A 00A2h | USB0 | PIPE5 Transaction Counter Register | PIPE5TRN | 16 | 16 | 9 PCLKB or more |
| 000A 00B0h | USB0 | BC Control Register 0 | USBBCCTRL0 | 16 | 16 | 9 PCLKB or more |
| 000A 00CCh | USB0 | USB Module Control Register | USBMC | 16 | 16 | 9 PCLKB or more |
| 000A 00D0h | USB0 | Device Address 0 Configuration Register | DEVADD0 | 16 | 16 | 9 PCLKB or more |
| 000A 00D2h | USB0 | Device Address 1 Configuration Register | DEVADD1 | 16 | 16 | 9 PCLKB or more |
| 000A 00D4h | USB0 | Device Address 2 Configuration Register | DEVADD2 | 16 | 16 | 9 PCLKB or more |
| 000A 00D6h | USB0 | Device Address 3 Configuration Register | DEVADD3 | 16 | 16 | 9 PCLKB or more |
| 000A 00D8h | USB0 | Device Address 4 Configuration Register | DEVADD4 | 16 | 16 | 9 PCLKB or more |
| 000A 00DAh | USB0 | Device Address 5 Configuration Register | DEVADD5 | 16 | 16 | 9 PCLKB or more |
| 007F C090h | FLASH | E2 DataFlash Control Register | DFCTL | 8 | 8 | 2 or 3 FCLK |
| 007F C0ACh | TEMPS | Temperature Sensor Calibration Data Register | TSCDRL | 8 | 8 | 1 or 2 PCLKB |
| 007F C0ADh | TEMPS | Temperature Sensor Calibration Data Register | TSCDRH | 8 | 8 | 1 or 2 PCLKB |
| 007F C0B0h | FLASH | Flash Start-Up Setting Monitor Register | FSCMR | 16 | 16 | 2 or 3 FCLK |
| 007F C0B2h | FLASH | Flash Access Window Start Address Monitor | FAWSMR | 16 | 16 | 2 or 3 FCLK |
| 007F C0B4h | FLASH | Flash Access Window End Address Monitor Register | FAWEMR | 16 | 16 | 2 or 3 FCLK |
| 007F C0B6h | FLASH | Flash Initial Setting Register | FISR | 8 | 8 | 2 or 3 FCLK |
| 007F C0B7h | FLASH | Flash Extra Area Control Register | FEXCR | 8 | 8 | 2 or 3 FCLK |
| 007F C0B8h | FLASH | Flash Error Address Monitor Register L | FEAML | 16 | 16 | 2 or 3 FCLK |
| 007F C0BAh | FLASH | Flash Error Address Monitor Register H | FEAMH | 8 | 8 | 2 or 3 FCLK |
| 007F C0C0h | FLASH | Protection Unlock Register | FPR | 8 | 8 | 2 or 3 FCLK |
| 007F C0C1h | FLASH | Protection Unlock Status Register | FPSR | 8 | 8 | 2 or 3 FCLK |
| 007F C0C2h | FLASH | Flash Read Buffer Register L | FRBL | 16 | 16 | 2 or 3 FCLK |
| 007F C0C4h | FLASH | Flash Read Buffer Register H | FRBH | 16 | 16 | 2 or 3 FCLK |
| 007F FF80h | FLASH | Flash P/E Mode Control Register | FPMCR | 8 | 8 | 2 or 3 FCLK |
| 007F FF81h | FLASH | Flash Area Select Register | FASR | 8 | 8 | 2 or 3 FCLK |
| 007F FF82h | FLASH | Flash Processing Start Address Register L | FSARL | 16 | 16 | 2 or 3 FCLK |
| 007F FF84h | FLASH | Flash Processing Start Address Register H | FSARH | 8 | 8 | 2 or 3 FCLK |
| 007F FF85h | FLASH | Flash Control Register | FCR | 8 | 8 | 2 or 3 FCLK |
| 007F FF86h | FLASH | Flash Processing End Address Register L | FEARL | 16 | 16 | 2 or 3 FCLK |
| 007F FF88h | FLASH | Flash Processing End Address Register H | FEARH | 8 | 8 | 2 or 3 FCLK |
| 007F FF89h | FLASH | Flash Reset Register | FRESETR | 8 | 8 | 2 or 3 FCLK |
| 007F FF8Ah | FLASH | Flash Status Register 0 | FSTATR0 | 8 | 8 | 2 or 3 FCLK |
| 007F FF8Bh | FLASH | Flash Status Register 1 | FSTATR1 | 8 | 8 | 2 or 3 FCLK |
| 007F FF8Ch | FLASH | Flash Write Buffer Register L | FWBL | 16 | 16 | 2 or 3 FCLK |
| 007F FF8Eh | FLASH | Flash Write Buffer Register H | FWBH | 16 | 16 | 2 or 3 FCLK |
| 007F FFB2h | FLASH | Flash P/E Mode Entry Register | FENTRYR | 16 | 16 | 2 or 3 FCLK |

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCNTL register. Table 27.6 lists register allocation for 16-bit access in the User's Manual: Hardware.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = VSS_USB = 0 V

| Item | | Symbol | Value | Unit |
|--------------------------------|--|------------------|--|------|
| Power supply voltage | | VCC, VCC_USB | -0.3 to +4.6 | V |
| Input voltage | Ports for 5 V tolerant*1 | V _{in} | -0.3 to +6.5 | V |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | V _{in} | -0.3 to AVCC0 +0.3 | V |
| | Ports other than above | V _{in} | -0.3 to VCC +0.3 | V |
| Reference power supply voltage | | VREFH0 | -0.3 to AVCC0 +0.3 | V |
| Analog power supply voltage | | AVCC0 | -0.3 to +4.6 | V |
| Analog input voltage | | V _{AN} | -0.3 to AVCC0 + 0.3 (when AN000 to AN004 and AN006 used) -0.3 to VCC + 0.3 (when AN008 to AN015 used) | V |
| Operating temperature*2 | | T _{opr} | -40 to +85 -40 to +105 | °C |
| Storage temperature | | T _{stg} | -55 to +125 | °C |

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, and between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 μF as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin via a 4.7 μF capacitor. The capacitor must be placed close to the pin, refer to section 5.12.1, Connecting VCL Capacitor and Bypass Capacitors.

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered. The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

If input voltage (within the specified range from -0.3 to + 6.5V) is applied to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports P16, P17, PA6, and PB0 are 5 V tolerant.

Note 2. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to 1.2 List of Products.

Table 5.2 Operating Conditions

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|------------------------------|-------------|-------------------|------|------|-------|------|
| Power supply voltages | VCC*1 | When USB not used | 1.8 | — | 3.6 | V |
| | | When USB used | 3.0 | — | 3.6 | V |
| | VSS | | — | 0 | — | V |
| USB power supply voltages | VCC_USB | | — | VCC | — | V |
| | VSS_USB | | — | 0 | — | V |
| Analog power supply voltages | AVCC0*1, *2 | | 1.8 | — | 3.6 | V |
| | AVSS0 | | — | 0 | — | V |
| | VREFH0 | | 1.8 | — | AVCC0 | V |
| | VREFL0 | | — | 0 | — | V |

Note 1. When powering on AVCC0 and VCC, power them on at the same time or VCC first.

Note 2. For details, refer to section 30.7.10, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)Conditions: $2.7\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $2.7\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|--------------|---------------------------|------|---------------------------|------|-----------------|
| Schmitt trigger input voltage | RIIC input pin (except for SMBus, 5 V tolerant) | V_{IH} | $\text{VCC} \times 0.7$ | — | 5.8 | V | |
| | Ports P16, P17, port PA6, port PB0 (5 V tolerant) | | $\text{VCC} \times 0.8$ | — | 5.8 | | |
| | Ports P03, P05, ports P14, P15, ports P26, P27, ports P30 to P32, P35, ports P54, P55, ports PA0, PA1, PA3, PA4, ports PB1, PB3, PB5 to PB7, ports PC2 to PC7, ports PE0 to PE7, port PH7, RES# | | $\text{VCC} \times 0.8$ | — | $\text{VCC} + 0.3$ | | |
| | RIIC input pin (except for SMBus) | V_{IL} | -0.3 | — | $\text{VCC} \times 0.3$ | | |
| | Other than RIIC input pin | | -0.3 | — | $\text{VCC} \times 0.2$ | | |
| | RIIC input pin (except for SMBus) | ΔV_T | $\text{VCC} \times 0.05$ | — | — | | |
| | Other than RIIC input pin | | $\text{VCC} \times 0.1$ | — | — | | |
| Input voltage (except for Schmitt trigger input pins) | MD | V_{IH} | $\text{VCC} \times 0.9$ | — | $\text{VCC} + 0.3$ | V | |
| | XTAL (external clock input) | | $\text{VCC} \times 0.8$ | — | $\text{VCC} + 0.3$ | | |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | $\text{AVCC0} \times 0.7$ | — | $\text{AVCC0} + 0.3$ | | |
| | RIIC input pin (SMBus) | | 2.1 | — | $\text{VCC} + 0.3$ | | |
| | MD | V_{IL} | -0.3 | — | $\text{VCC} \times 0.1$ | | |
| | XTAL (external clock input) | | -0.3 | — | $\text{VCC} \times 0.2$ | | |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | -0.3 | — | $\text{AVCC0} \times 0.3$ | | |
| | RIIC input pin (SMBus) | | -0.3 | — | 0.8 | | |

Table 5.4 DC Characteristics (2)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} < 2.7\text{ V}$, $1.8\text{ V} \leq AV_{SS0} < 2.7\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|--------------|-----------------------|------|-----------------------|-----------------|
| Schmitt trigger input voltage | Ports P16, P17, port PA6, port PB0 (5 V tolerant) | V_{IH} | $V_{CC} \times 0.8$ | — | 5.8 | V |
| | Ports P03, P05, ports P14, P15, ports P26, P27, ports P30 to P32, P35, ports P54, P55, ports PA0, PA1, PA3, PA4, ports PB1, PB3, PB5 to PB7, ports PC2 to PC7, ports PE0 to PE7, port PH7, RES# | | $V_{CC} \times 0.8$ | — | $V_{CC} + 0.3$ | |
| | All pins | | -0.3 | — | $V_{CC} \times 0.2$ | |
| | All pins | ΔV_T | $V_{CC} \times 0.01$ | — | — | |
| Input voltage (except for Schmitt trigger input pins) | MD | V_{IH} | $V_{CC} \times 0.9$ | — | $V_{CC} + 0.3$ | V |
| | XTAL (external clock input) | | $V_{CC} \times 0.8$ | — | $V_{CC} + 0.3$ | |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | $AV_{CC0} \times 0.7$ | — | $AV_{CC0} + 0.3$ | |
| | MD | V_{IL} | -0.3 | — | $V_{CC} \times 0.1$ | |
| | XTAL (external clock input) | | -0.3 | — | $V_{CC} \times 0.2$ | |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | -0.3 | — | $AV_{CC0} \times 0.3$ | |

Table 5.5 DC Characteristics (3)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{SS0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|--|-------------|------|------|------|---|
| Input leakage current | RES#, MD, port P35, port PH7 | $ I_{in} $ | — | — | 1.0 | μA , $V_{in} = 0\text{ V}$, VCC |
| Three-state leakage current (off-state) | Ports for 5 V tolerant | $ I_{TSI} $ | — | — | 1.0 | μA , $V_{in} = 0\text{ V}$, 5.8 V |
| | Pins other than above | | — | — | 1.0 | μA , $V_{in} = 0\text{ V}$, VCC |
| Input capacitance | All input pins (except for port P16, port P35, USB0_DM, USB0_DP) | C_{in} | — | — | 15 | pF , $V_{in} = 0\text{ mV}$, Frequency: 1 MHz, $T_a = 25^\circ\text{C}$ |
| | Port P16, port P35, USB0_DM, USB0_DP | | — | — | 30 | |

Table 5.6 DC Characteristics (4)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{SS0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|------------------------|---|-------|------|------|------|--|
| Input pull-up resistor | All ports (except for port P35, port PH7) | R_U | 10 | 20 | 100 | $\text{k}\Omega$, $V_{in} = 0\text{ V}$ |

[128-Kbyte or less flash memory]

Table 5.7 DC Characteristics (5) (1/2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVSS0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = -40 to +105°C

| Item | | | | Symbol | Typ *4 | Max | Unit | Test Conditions | |
|---------------------------------------|---------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|-----------------|---------------|------|--------------------|---|
| Supply current*1 | High-speed operating mode | Normal operating mode | No peripheral operation*2 | ICLK = 32 MHz | I _{CC} | 3.2 | — | mA | |
| | | | | ICLK = 16 MHz | | 2.2 | — | | |
| | | | | ICLK = 8 MHz | | 1.7 | — | | |
| | | | All peripheral operation: Normal*3 | ICLK = 32 MHz | | 10.6 | — | | |
| | | | | ICLK = 16 MHz | | 6.1 | — | | |
| | | | | ICLK = 8 MHz | | 3.7 | — | | |
| | | All peripheral operation: Max.*3 | ICLK = 32 MHz | — | 24 | | | | |
| | | | Sleep mode | No peripheral operation*2 | ICLK = 32 MHz | 1.8 | — | | |
| | | | | | ICLK = 16 MHz | 1.4 | — | | |
| | | ICLK = 8 MHz | | | 1.1 | — | | | |
| | | All peripheral operation: Normal*3 | ICLK = 32 MHz | 6.4 | — | | | | |
| | | | ICLK = 16 MHz | 3.7 | — | | | | |
| | ICLK = 8 MHz | | 2.4 | — | | | | | |
| | Deep sleep mode | No peripheral operation*2 | ICLK = 32 MHz | 1.2 | — | | | | |
| | | | ICLK = 16 MHz | 1.0 | — | | | | |
| | | | ICLK = 8 MHz | 0.90 | — | | | | |
| | | All peripheral operation: Normal*3 | ICLK = 32 MHz | 4.6 | — | | | | |
| | | | ICLK = 16 MHz | 2.8 | — | | | | |
| | | | ICLK = 8 MHz | 1.8 | — | | | | |
| | Increase during flash rewrite*5 | | | | | 2.5 | — | | |
| | Middle-speed operating modes | Normal operating mode | No peripheral operation*6 | ICLK = 12 MHz | I _{CC} | 2.0 | — | mA | |
| | | | | ICLK = 8 MHz | | 1.3 | — | | |
| | | | | ICLK = 1 MHz | | 0.75 | — | | |
| | | | | All peripheral operation: Normal*7 | | ICLK = 12 MHz | 4.9 | | — |
| ICLK = 8 MHz | | | | | | 3.5 | — | | |
| ICLK = 1 MHz | | | | | | 1.2 | — | | |
| All peripheral operation: Max.*7 | | | ICLK = 12 MHz | — | | 11 | | | |
| | | | Sleep mode | No peripheral operation*6 | | ICLK = 12 MHz | 1.4 | | — |
| | | | | | | ICLK = 8 MHz | 0.85 | | — |
| ICLK = 1 MHz | | | | | | 0.65 | — | | |
| All peripheral operation: Normal*7 | | | ICLK = 12 MHz | 3.2 | | — | | | |
| | | | ICLK = 8 MHz | 2.2 | | — | | | |
| | | ICLK = 1 MHz | 1.0 | — | | | | | |
| Deep sleep mode | | No peripheral operation*6 | ICLK = 12 MHz | 1.2 | — | | | | |
| | | | ICLK = 8 MHz | 0.70 | — | | | | |
| | | | ICLK = 1 MHz | 0.60 | — | | | | |
| | | All peripheral operation: Normal*7 | ICLK = 12 MHz | 2.5 | — | | | | |
| | | | ICLK = 8 MHz | 1.8 | — | | | | |
| | | | ICLK = 1 MHz | 0.90 | — | | | | |
| Increase during flash rewrite*5 | | | | | 2.5 | — | | | |

Table 5.7 DC Characteristics (5) (2/2)Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | | | Symbol | Typ *4 | Max | Unit | Test Conditions |
|---------------------|-----------------------------|-----------------------------|--|-------------------|-----------------|------|------|--------------------|
| Supply current*1 | Low-speed operating mode | Normal operating mode | No peripheral operation*8 | ICLK = 32.768 kHz | I _{CC} | 4.0 | — | μA |
| | | | All peripheral operation: Normal*9, *10 | ICLK = 32.768 kHz | | 11.5 | — | |
| | | | All peripheral operation: Max.*9, *10 | ICLK = 32.768 kHz | | — | 40 | |
| | | Sleep mode | No peripheral operation*8 | ICLK = 32.768 kHz | | 2.2 | — | |
| | | | All peripheral operation: Normal*9 | ICLK = 32.768 kHz | | 7.1 | — | |
| | | Deep sleep mode | No peripheral operation*8 | ICLK = 32.768 kHz | | 1.8 | — | |
| | | | All peripheral operation: Normal*9 | ICLK = 32.768 kHz | | 5.3 | — | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to the same frequency as ICLK.

Note 4. Values when $VCC = 3.3\text{ V}$.

Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.

Note 6. Clock supply to the peripheral functions is stopped. The clock source is PLL when ICLK = 12 MHz, and HOCO otherwise. FCLK and PCLK are set to divided by 64.

Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK = 12 MHz, and HOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.

Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.

Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.

Note 10. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to "transition to the module stop state is made".

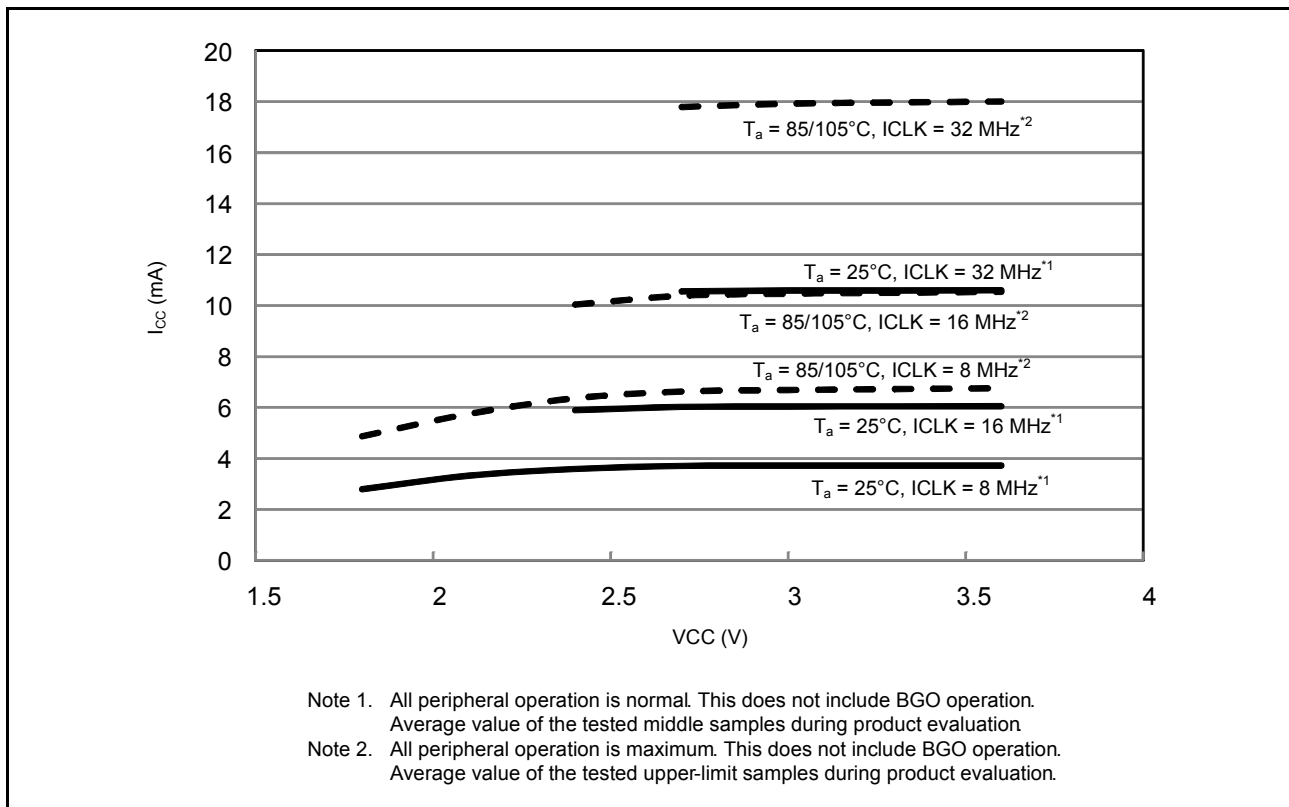


Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)

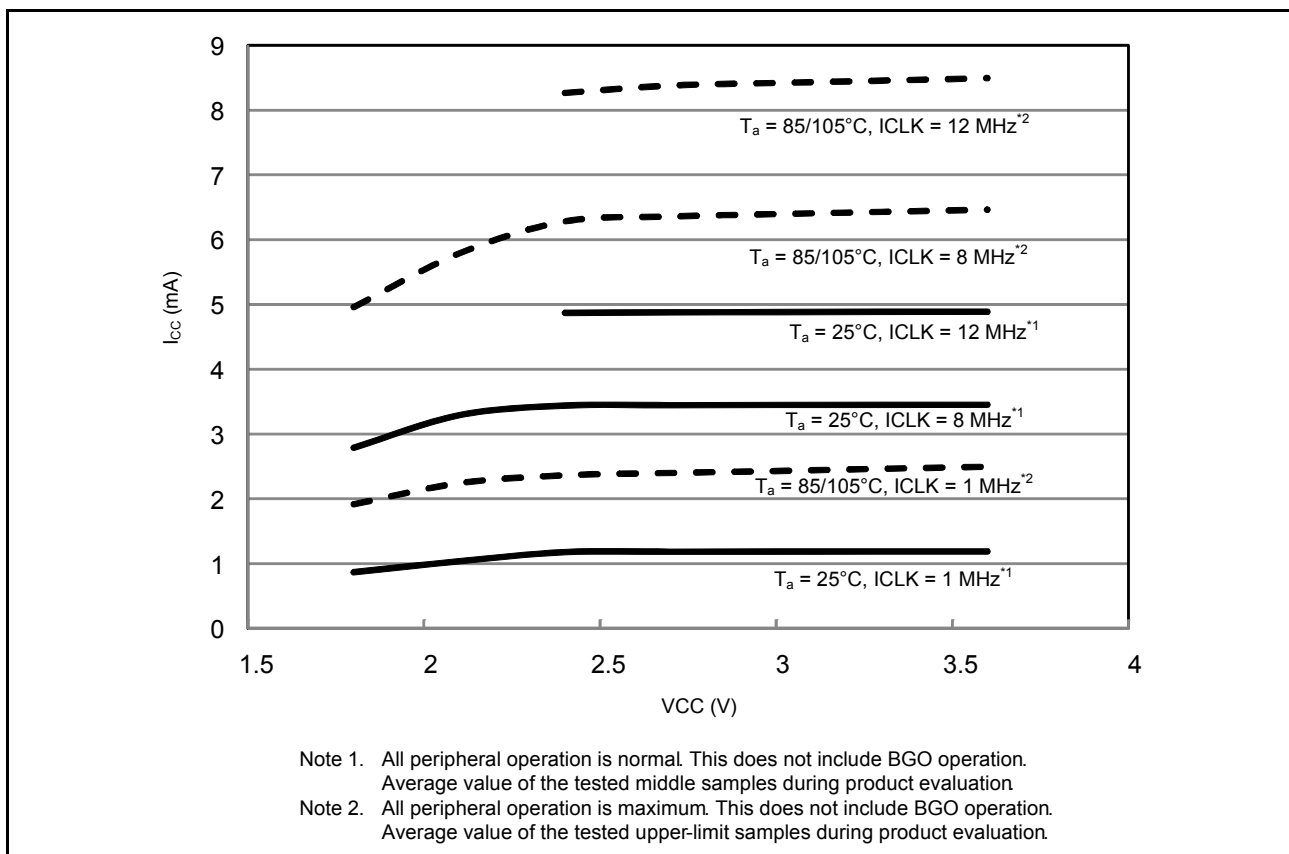


Figure 5.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)

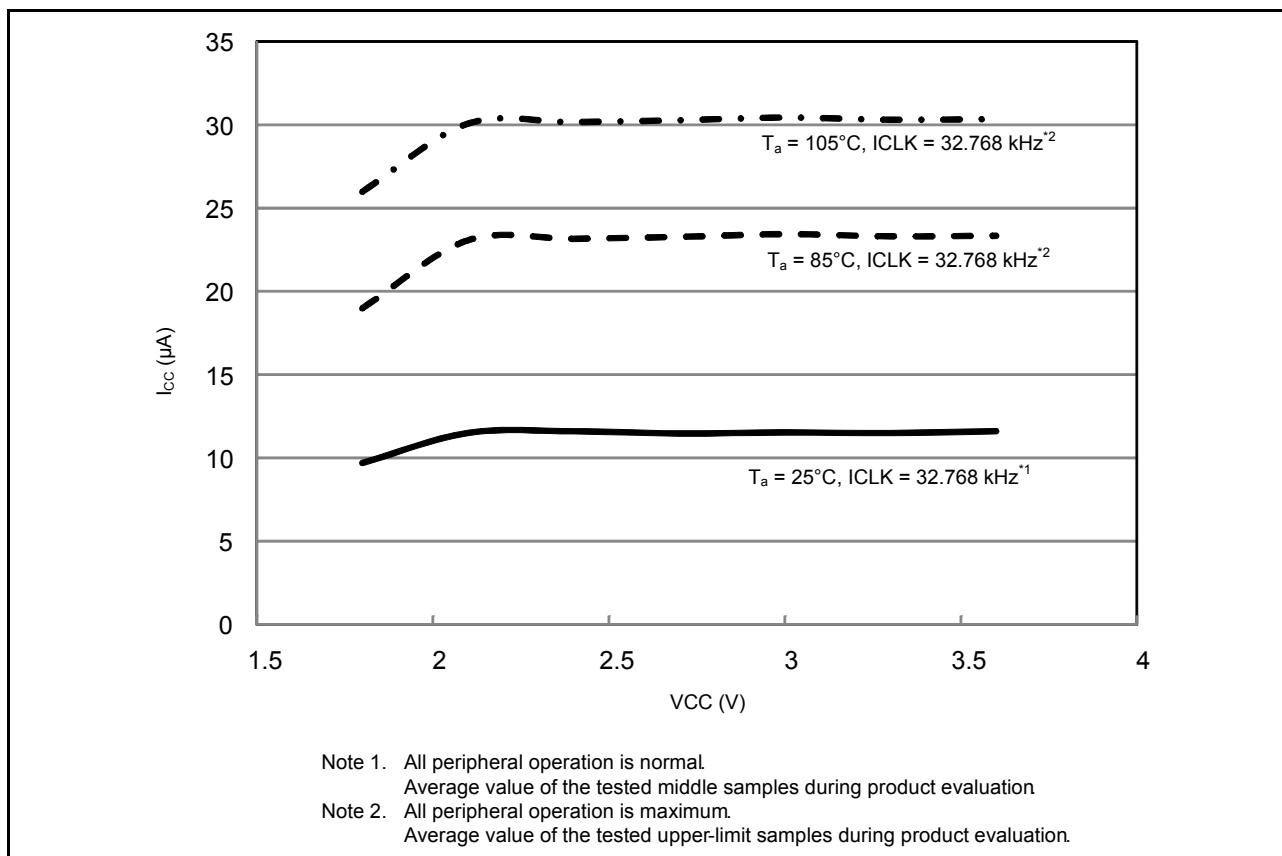


Figure 5.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

[256-Kbyte or more flash memory]

Table 5.8 DC Characteristics (6) (1/2)Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | | | | Symbol | Typ *4 | Max | Unit | Test Conditions | |
|---------------------------------------|------------------------------------|---------------------------------------|---------------------------------------|------------------------------|-----------------|---------------|-----|------|--------------------|---|
| Supply current*1 | High-speed operating mode | Normal operating mode | No peripheral operation*2 | ICLK = 32 MHz | I _{CC} | 3.6 | — | mA | | |
| | | | | ICLK = 16 MHz | | 2.4 | — | | | |
| | | | | ICLK = 8 MHz | | 1.8 | — | | | |
| | | | All peripheral operation: Normal*3 | ICLK = 32 MHz | | 13.4 | — | | | |
| | | | | ICLK = 16 MHz | | 7.5 | — | | | |
| | | | | ICLK = 8 MHz | | 4.5 | — | | | |
| | | All peripheral operation: Max.*3 | ICLK = 32 MHz | — | | 27 | | | | |
| | | | Sleep mode | No peripheral operation*2 | | ICLK = 32 MHz | 1.9 | | | — |
| | | | | | | ICLK = 16 MHz | 1.5 | | | — |
| | | ICLK = 8 MHz | | | | 1.3 | — | | | |
| | | All peripheral operation: Normal*3 | ICLK = 32 MHz | 7.6 | | — | | | | |
| | | | ICLK = 16 MHz | 4.4 | | — | | | | |
| | ICLK = 8 MHz | | 2.8 | — | | | | | | |
| | Deep sleep mode | No peripheral operation*2 | ICLK = 32 MHz | 1.1 | — | | | | | |
| | | | ICLK = 16 MHz | 1.0 | — | | | | | |
| | | | ICLK = 8 MHz | 0.9 | — | | | | | |
| | | All peripheral operation: Normal*3 | ICLK = 32 MHz | 5.8 | — | | | | | |
| | | | ICLK = 16 MHz | 3.4 | — | | | | | |
| | | | ICLK = 8 MHz | 2.1 | — | | | | | |
| | Increase during flash rewrite*5 | | | | | 2.5 | — | | | |
| | Middle-speed operating modes | Normal operating mode | No peripheral operation*6 | ICLK = 12 MHz | I _{CC} | 2.1 | — | mA | | |
| | | | | ICLK = 8 MHz | | 1.4 | — | | | |
| | | | | ICLK = 1 MHz | | 0.8 | — | | | |
| | | | All peripheral operation: Normal*7 | ICLK = 12 MHz | | 5.9 | — | | | |
| ICLK = 8 MHz | | | | 4.2 | | — | | | | |
| ICLK = 1 MHz | | | | 1.3 | | — | | | | |
| All peripheral operation: Max.*7 | | | ICLK = 12 MHz | — | | 12.2 | | | | |
| | | | Sleep mode | No peripheral operation*6 | | ICLK = 12 MHz | 1.4 | | — | |
| | | | | | | ICLK = 8 MHz | 0.9 | | — | |
| ICLK = 1 MHz | | | | | | 0.7 | — | | | |
| All peripheral operation: Normal*7 | | | ICLK = 12 MHz | 3.6 | | — | | | | |
| | | | ICLK = 8 MHz | 2.5 | | — | | | | |
| | | ICLK = 1 MHz | 1.1 | — | | | | | | |
| Deep sleep mode | | No peripheral operation*6 | ICLK = 12 MHz | 1.1 | — | | | | | |
| | | | ICLK = 8 MHz | 0.6 | — | | | | | |
| | | | ICLK = 1 MHz | 0.6 | — | | | | | |
| | | All peripheral operation: Normal*7 | ICLK = 12 MHz | 2.9 | — | | | | | |
| | | | ICLK = 8 MHz | 2.0 | — | | | | | |
| | | | ICLK = 1 MHz | 0.9 | — | | | | | |
| Increase during flash rewrite*5 | | | | | 2.5 | — | | | | |

Table 5.8 DC Characteristics (6) (2/2)Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | | | | Symbol | Typ *4 | Max | Unit | Test Conditions |
|---------------------|--------------------------------|-----------------------------|--|-------------------|-----------------|-----------|-----|------|--------------------|
| Supply current*1 | Low-speed operating mode | Normal operating mode | No peripheral operation*8 | ICLK = 32.768 kHz | I _{CC} | 4.3 | — | μA | |
| | | | All peripheral operation: Normal*9, *10 | ICLK = 32.768 kHz | | 14.7 | — | | |
| | | | All peripheral operation: Max.*9, *10 | ICLK = 32.768kHz | | — | 60 | | |
| | | Sleep mode | No peripheral operation*8 | ICLK = 32.768 kHz | | 2.2 | — | | |
| | | | All peripheral operation: Normal*9 | ICLK = 32.768 kHz | | 8.3 | — | | |
| | | Deep sleep mode | No peripheral operation*8 | ICLK = 32.768 kHz | | 1.7 | — | | |
| | | | All peripheral operation: Normal*9 | ICLK = 32.768 kHz | | 6.7 | — | | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to the same frequency as ICLK.

Note 4. Values when $VCC = 3.3\text{ V}$.

Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.

Note 6. Clock supply to the peripheral functions is stopped. The clock source is PLL when ICLK = 12 MHz, and HOCO otherwise. FCLK and PCLK are set to divided by 64.

Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK = 12 MHz, and HOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.

Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.

Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.

Note 10. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to "transition to the module stop state is made".



Figure 5.4 Voltage Dependency in High-Speed Operating Mode (Reference Data)



Figure 5.5 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)



Figure 5.6 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

[128-Kbyte or less flash memory]

Table 5.9 DC Characteristics (7)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Symbol | Typ.*3 | Max. | Unit | Test Conditions | |
|------------------|-------------------------------|----------|---------------------------|------|-------|-----------------|--|
| Supply current*1 | Software standby mode*2 | I_{CC} | $T_a = 25^\circ\text{C}$ | 0.35 | 0.53 | μA | RCR3.RTCDV[2:0] = 010b RCR3.RTCDV[2:0] = 100b |
| | | | $T_a = 55^\circ\text{C}$ | 0.58 | 1.45 | | |
| | | | $T_a = 85^\circ\text{C}$ | 1.60 | 7.30 | | |
| | | | $T_a = 105^\circ\text{C}$ | 3.30 | 16.50 | | |
| | Increment for RTC operation*4 | | 0.31 | — | | | |
| | Increment for IWDT operation | | 1.09 | — | | | |
| | | | 0.37 | — | | | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. The IWDT and LVD are stopped.

Note 3. $VCC = 3.3\text{ V}$.

Note 4. Includes the oscillation circuit.



Figure 5.7 Voltage Dependency in Software Standby Mode (Reference Data)



Figure 5.8 Temperature Dependency in Software Standby Mode (Reference Data)

[256-Kbyte or more flash memory]

Table 5.10 DC Characteristics (8)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Symbol | Typ.*3 | Max. | Unit | Test Conditions | |
|------------------|-------------------------------|----------|---------------------------|------|------|-----------------|--|
| Supply current*1 | Software standby mode*2 | I_{CC} | $T_a = 25^\circ\text{C}$ | 0.44 | 0.98 | μA | RCR3.RTCDV[2:0] = 010b RCR3.RTCDV[2:0] = 100b |
| | | | $T_a = 55^\circ\text{C}$ | 0.80 | 3.47 | | |
| | | | $T_a = 85^\circ\text{C}$ | 2.7 | 12.0 | | |
| | | | $T_a = 105^\circ\text{C}$ | 6.17 | 42.7 | | |
| | Increment for RTC operation*4 | 0.31 | — | | | | |
| | Increment for IWDG operation | 1.09 | — | | | | |
| | | | 0.37 | — | | | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. The IWDG and LVD are stopped.

Note 3. $VCC = 3.3\text{ V}$.

Note 4. Includes the oscillation circuit.

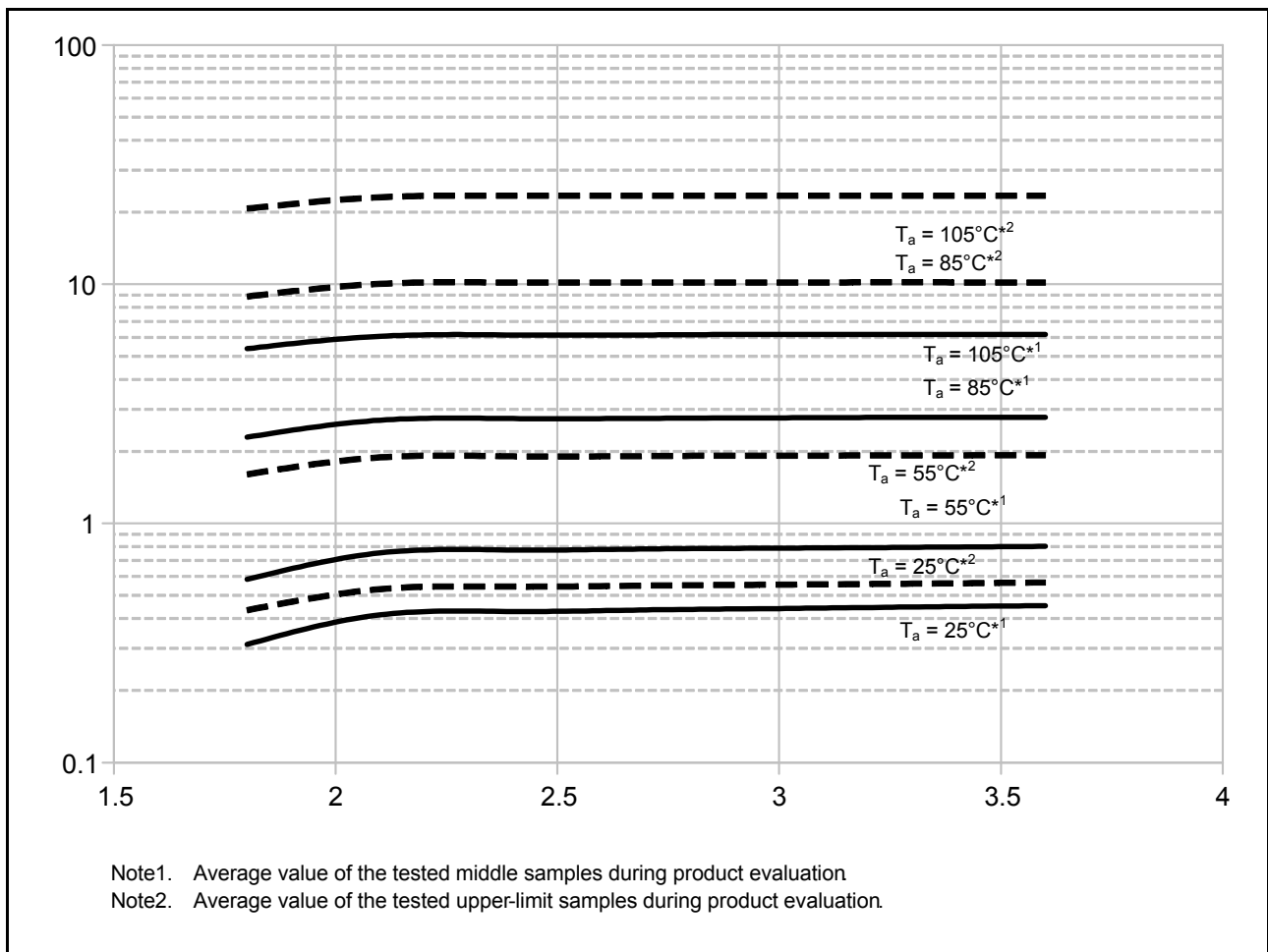


Figure 5.9 Voltage Dependency in Software Standby Mode (Reference Data)

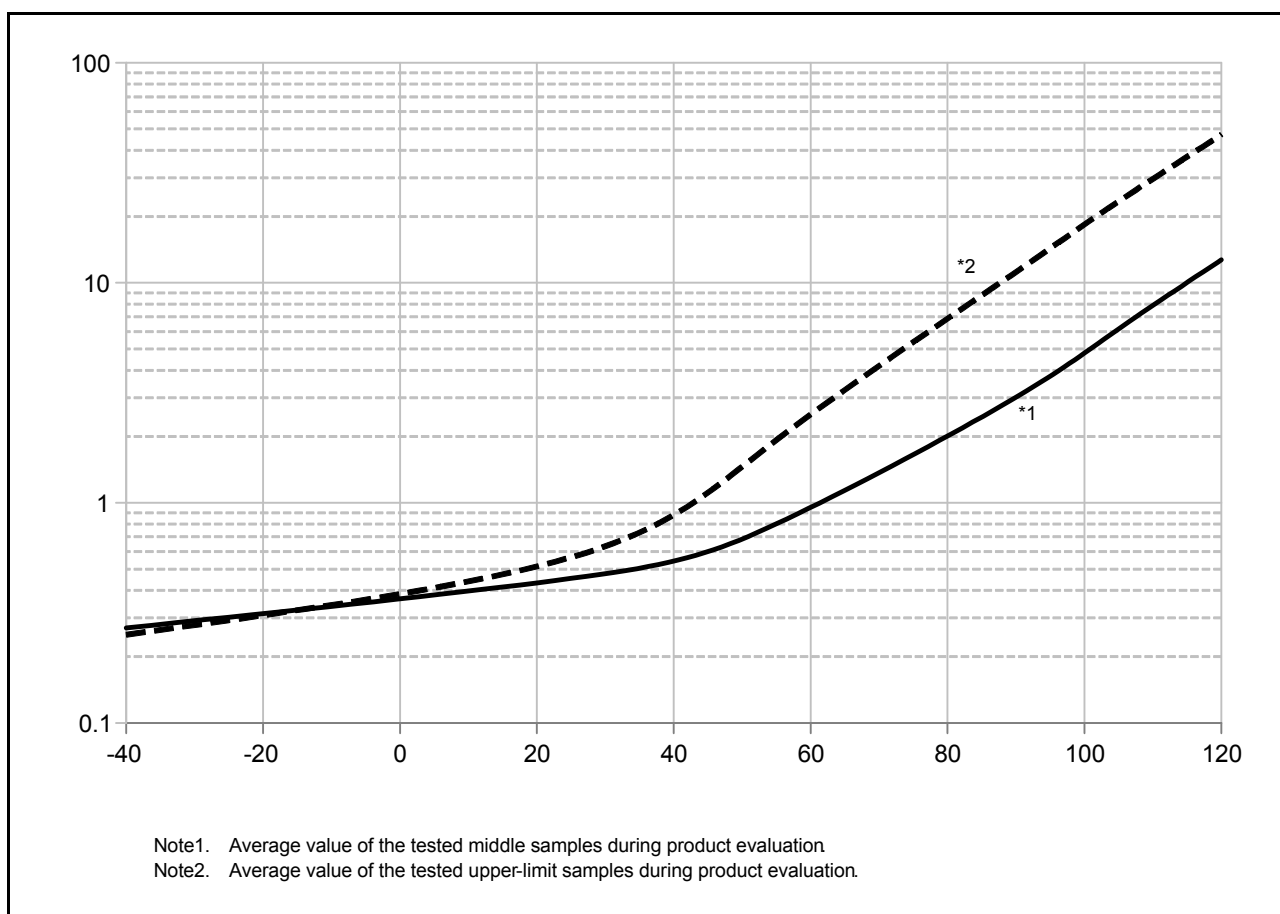


Figure 5.10 Temperature Dependency in Software Standby Mode (Reference Data)

Table 5.11 DC Characteristics (9)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVCC0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$

| Item | Symbol | Typ. | Max. | Unit | Test Conditions |
|---------------------------------------|--------|------|------|------|---|
| Permissible total consumption power*1 | Pd | — | 300 | mW | D version ($T_a = -40\text{ to }85^\circ\text{C}$) |
| | | — | 105 | | G version ($T_a = -40\text{ to }105^\circ\text{C}$)*2 |

Note 1. Total power dissipated by the entire chip (including output currents).

Note 2. Please contact Renesas Electronics sales office for derating under $T_a = +85^\circ\text{C}$ to 105°C . Derating is the systematic reduction of load for the sake of improved reliability.

Table 5.12 DC Characteristics (10)Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Symbol | Min. | Typ.*7 | Max. | Unit | Test Conditions |
|--------------------------------|---|---------------|------|-----------------------------------|------|---------------|-----------------|
| Analog power supply current | During A/D conversion (at high-speed conversion) | I_{AVCC} | — | 0.7 | 1.2 | mA | |
| | Waiting for A/D (all units) | | — | — | 0.3 | μA | |
| | During D/A conversion (per channel)*5 | | — | — | 1.5 | mA | |
| Reference power supply current | During A/D conversion (at high-speed conversion) | I_{REFH0} | — | 25 | 52 | μA | |
| | Waiting for A/D conversion (all units) | | — | — | 60 | nA | |
| Temperature sensor*6 | | I_{TEMP} | — | 75 | — | μA | |
| LDV1, 2 | Per channel | I_{LVD} | — | 0.15 | — | μA | |
| USB operating current | During USB communication operation under the following settings and conditions <ul style="list-style-type: none"> Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) \times 1, bulk IN transfer (64 bytes) \times 1 Connect peripheral devices via a 1-meter USB cable from the USB port. | I_{USBH} *2 | — | 4.3 (VCC) 0.9 (VCC_USB) *4 | — | mA | |
| | During USB communication operation under the following settings and conditions <ul style="list-style-type: none"> Function controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) \times 1, bulk IN transfer (64 bytes) \times 1 Connect the host device via a 1-meter USB cable from the USB port. | I_{USBF} *2 | — | 3.6 (VCC) 1.1 (VCC_USB) *4 | — | mA | |
| | During suspended state under the following setting and conditions <ul style="list-style-type: none"> Function controller operation is set to full-speed mode (pull up the USB0_DP pin) Software standby mode Connect the host device via a 1-meter USB cable from the USB port. | I_{SUSP} *3 | — | 0.35 (VCC) 170 (VCC_USB) *4 | — | μA | |

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.

Note 2. Current consumed only by the USB module.

Note 3. Includes the current supplied from the pull-up resistor of the USB0_DP pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.

Note 4. When $VCC = VCC_USB = 3.3\text{ V}$.

Note 5. The value of the current flowing to VCC.

Note 6. Current consumed by the power supply (VCC).

Note 7. When $VCC = AVCC0 = VCC_USB = 3.3\text{ V}$.**Table 5.13 DC Characteristics (11)**Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---------------------|-----------|------|------|------|------|-----------------|
| RAM standby voltage | V_{RAM} | 1.8 | — | — | V | |

Table 5.14 DC Characteristics (12)

Conditions: $0\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|------------------------------|---|--------|------|------|------|------|-----------------|
| Power-on VCC rising gradient | At normal startup*1 | SrVCC | 0.02 | — | 20 | ms/V | |
| | During fast startup time*2 | | 0.02 | — | 2 | | |
| | Voltage monitoring 1 reset enabled at startup*3, *4 | | 0.02 | — | — | | |

Note: When powering on AVCC0 and VCC, power them on at the same time or VCC first.

Note 1. When OFS1.(STUPLVD1REN, FASTSTUP) = 11b.

Note 2. When OFS1.(STUPLVD1REN, FASTSTUP) = 10b.

Note 3. When OFS1.STUPLVD1REN = 0.

Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

Table 5.15 DC Characteristics (13)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

The ripple voltage must meet the allowable ripple frequency $f_{r(\text{VCC})}$ within the range between the VCC upper limit (3.6 V) and lower limit (1.8 V).

When VCC change exceeds $\text{VCC} \pm 10\%$, the allowable voltage change rising/falling gradient $dt/d\text{VCC}$ must be met.

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--|---------------------|------|------|------|------|--|
| Allowable ripple frequency | $f_{r(\text{VCC})}$ | — | — | 10 | kHz | Figure 5.11 $V_{r(\text{VCC})} \leq \text{VCC} \times 0.2$ |
| | | — | — | 1 | MHz | Figure 5.11 $V_{r(\text{VCC})} \leq \text{VCC} \times 0.08$ |
| | | — | — | 10 | MHz | Figure 5.11 $V_{r(\text{VCC})} \leq \text{VCC} \times 0.06$ |
| Allowable voltage change rising/falling gradient | $dt/d\text{VCC}$ | 1.0 | — | — | ms/V | When VCC change exceeds $\text{VCC} \pm 10\%$ |



Figure 5.11 Ripple Waveform

Table 5.16 DC Characteristics (14)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|------------------|------|------|------|---------------|-----------------|
| Permissible error of VCL pin external capacitance | C_{VCL} | 1.4 | 4.7 | 7.0 | μF | |

Note: • The recommended capacitance is 4.7 μF . Variations in connected capacitors should be within the above range.

Table 5.17 Permissible Output Currents (1)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $T_a = -40\text{ to }+85^\circ\text{C}$ (D version)

| Item | | Symbol | Max. | Unit |
|--|--|-----------------|------|------|
| Permissible output low current (average value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | I_{OL} | 0.4 | mA |
| | Ports other than above | | 8.0 | |
| Permissible output low current (maximum value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | | 0.4 | |
| | Ports other than above | | 8.0 | |
| Permissible output low current | Total of ports P40 to P44, P46, ports PJ6, PJ7 | ΣI_{OL} | 2.4 | |
| | Total of ports P03, P05, ports P26, P27, ports P30, P31 | | 30 | |
| | Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7 | | 30 | |
| | Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7 | | 30 | |
| | Total of all output pins | | 60 | |
| Permissible output high current (average value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | I_{OH} | -0.1 | |
| | Ports other than above | | -4.0 | |
| Permissible output high current (maximum value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | | -0.1 | |
| | Ports other than above | | -4.0 | |
| Permissible output high current | Total of ports P40 to P44, P46, ports PJ6, PJ7 | ΣI_{OH} | -0.6 | |
| | Total of ports P03, P05, ports P26, P27, ports P30, P31 | | -10 | |
| | Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7 | | -15 | |
| | Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7 | | -15 | |
| | Total of all output pins | | -40 | |

Note: Do not exceed the permissible total supply current.

Table 5.18 Permissible Output Currents (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$ (G version)

| | Item | Symbol | Max. | Unit |
|--|--|-----------------|------|------|
| Permissible output low current (average value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | I_{OL} | 0.4 | mA |
| | Ports other than above | | 8.0 | |
| Permissible output low current (maximum value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | | 0.4 | |
| | Ports other than above | | 8.0 | |
| Permissible output low current | Total of ports P40 to P44, P46, ports PJ6, PJ7 | ΣI_{OL} | 1.6 | |
| | Total of ports P03, P05, ports P26, P27, ports P30, P31 | | 20 | |
| | Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7 | | 20 | |
| | Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7 | | 20 | |
| | Total of all output pins | | 40 | |
| Permissible output high current (average value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | I_{OH} | -0.1 | |
| | Ports other than above | | -4.0 | |
| Permissible output high current (maximum value per pin) | Ports P40 to P44, P46, ports PJ6, PJ7 | | -0.1 | |
| | Ports other than above | | -4.0 | |
| Permissible output high current | Total of ports P40 to P44, P46, ports PJ6, PJ7 | ΣI_{OH} | -0.6 | |
| | Total of ports P03, P05, ports P26, P27, ports P30, P31 | | -10 | |
| | Total of ports P14 to P17, port P32, ports P54, P55, ports PB0, PB1, PB3, PB5 to PB7, ports PC2 to PC7 | | -15 | |
| | Total of ports PA0, PA1, PA3, PA4, PA6, ports PE0 to PE7 | | -15 | |
| | Total of all output pins | | -40 | |

Note: Do not exceed the permissible total supply current.

Table 5.19 Output Voltage (1)Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $2.7\text{ V} \leq AV_{SS0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Symbol | Min. | Max. | Unit | Test Conditions | |
|---------------------------|---|----------|------------------|------|------|---------------------------|--------------------------|
| Low-level output voltage | All output ports (except for RIIC, ports P40 to P44, P46, ports PJ6, PJ7) | V_{OL} | — | 0.6 | V | $I_{OL} = 3.0\text{ mA}$ | |
| | | | — | 0.4 | | $I_{OL} = 1.5\text{ mA}$ | |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | — | 0.4 | | $I_{OL} = 0.4\text{ mA}$ | |
| | RIIC pins | | Standard mode | — | | 0.4 | $I_{OL} = 3.0\text{ mA}$ |
| | | | Fast mode | — | | 0.6 | $I_{OL} = 6.0\text{ mA}$ |
| High-level output voltage | All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7) | V_{OH} | $V_{CC} - 0.5$ | — | V | $I_{OH} = -2.0\text{ mA}$ | |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | $AV_{CC0} - 0.5$ | — | | $I_{OH} = -0.1\text{ mA}$ | |

Table 5.20 Output Voltage (2)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 2.7\text{ V}$, $1.8\text{ V} \leq AV_{SS0} \leq 2.7\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---------------------------|---|----------|------------------|------|------|---------------------------|
| Low-level output voltage | All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7) | V_{OL} | — | 0.6 | V | $I_{OL} = 1.5\text{ mA}$ |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | — | 0.4 | | $I_{OL} = 0.4\text{ mA}$ |
| High-level output voltage | All output ports (except for ports P40 to P44, P46, ports PJ6, PJ7) | V_{OH} | $V_{CC} - 0.5$ | — | V | $I_{OH} = -1.0\text{ mA}$ |
| | Ports P40 to P44, P46, ports PJ6, PJ7 | | $AV_{CC0} - 0.5$ | — | | $I_{OH} = -0.1\text{ mA}$ |

5.2.1 Standard I/O Pin Output Characteristics (1)

Figure 5.12 to Figure 5.15 show the characteristics of general ports (except for the RIIC output pin, ports P40 to P44, P46, ports PJ6, PJ7)



Figure 5.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics of General Ports (Except for the RIIC Output Pin, Ports P40 to P44, P46, Ports PJ6, PJ7) at $T_a = 25^\circ\text{C}$ (Reference Data)



Figure 5.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of General Ports (Except for the RIIC Output Pin, Ports P40 to P44, P46, Ports PJ6, PJ7) at $V_{CC} = 1.8\text{V}$ (Reference Data)

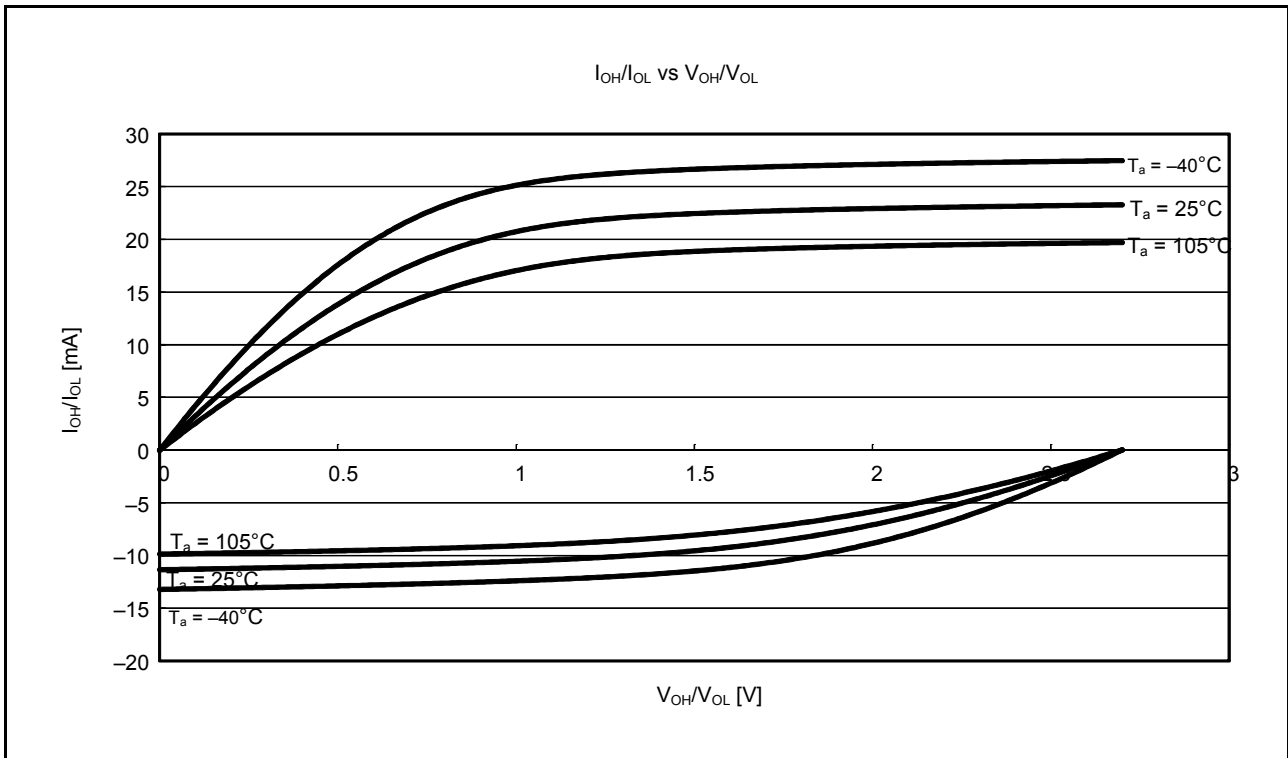


Figure 5.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of General Ports (Except for the RIIC Output Pin, Ports P40 to P44, P46, Ports PJ6, PJ7) at $V_{CC} = 2.7$ V (Reference Data)



Figure 5.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of General Ports (Except for the RIIC Output Pin, Ports P40 to P44, P46, Ports PJ6, PJ7) at $V_{CC} = 3.3$ V (Reference Data)

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.16 to Figure 5.18 show the characteristics of the RIIC output pin.

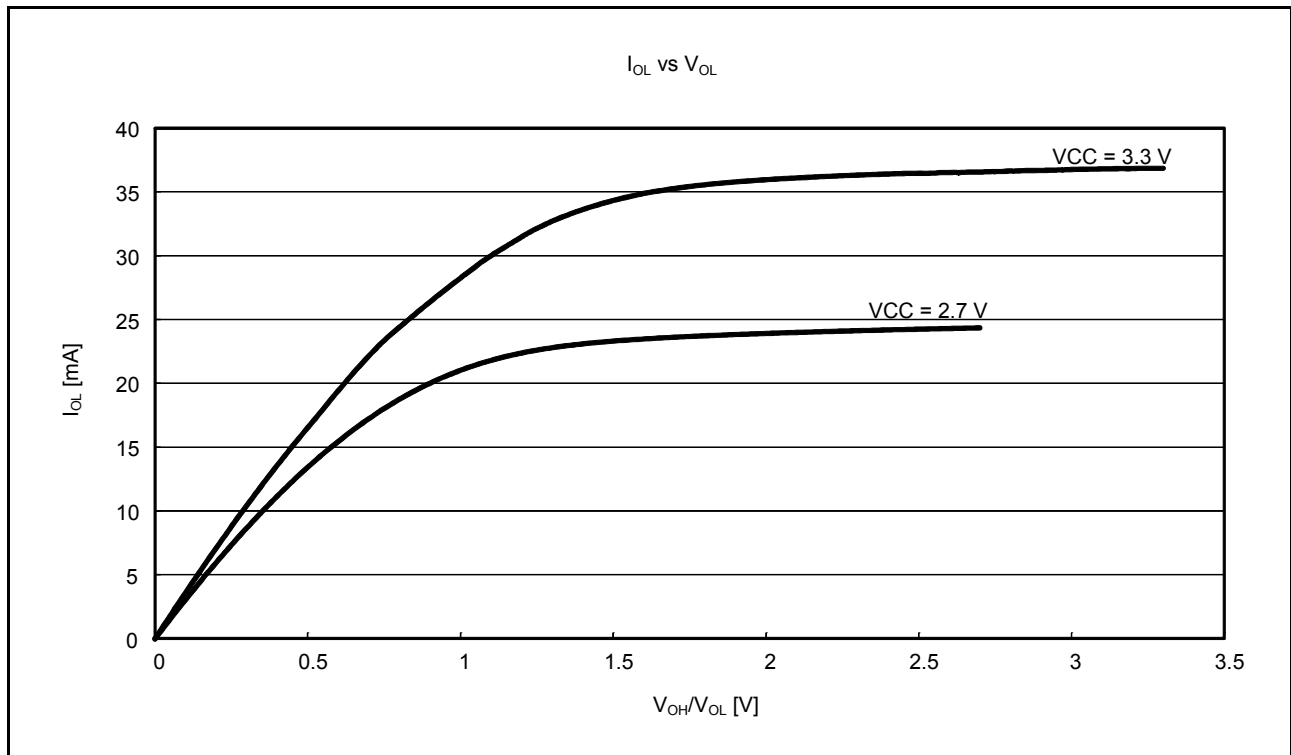


Figure 5.16 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at $T_a = 25^\circ\text{C}$ (Reference Data)

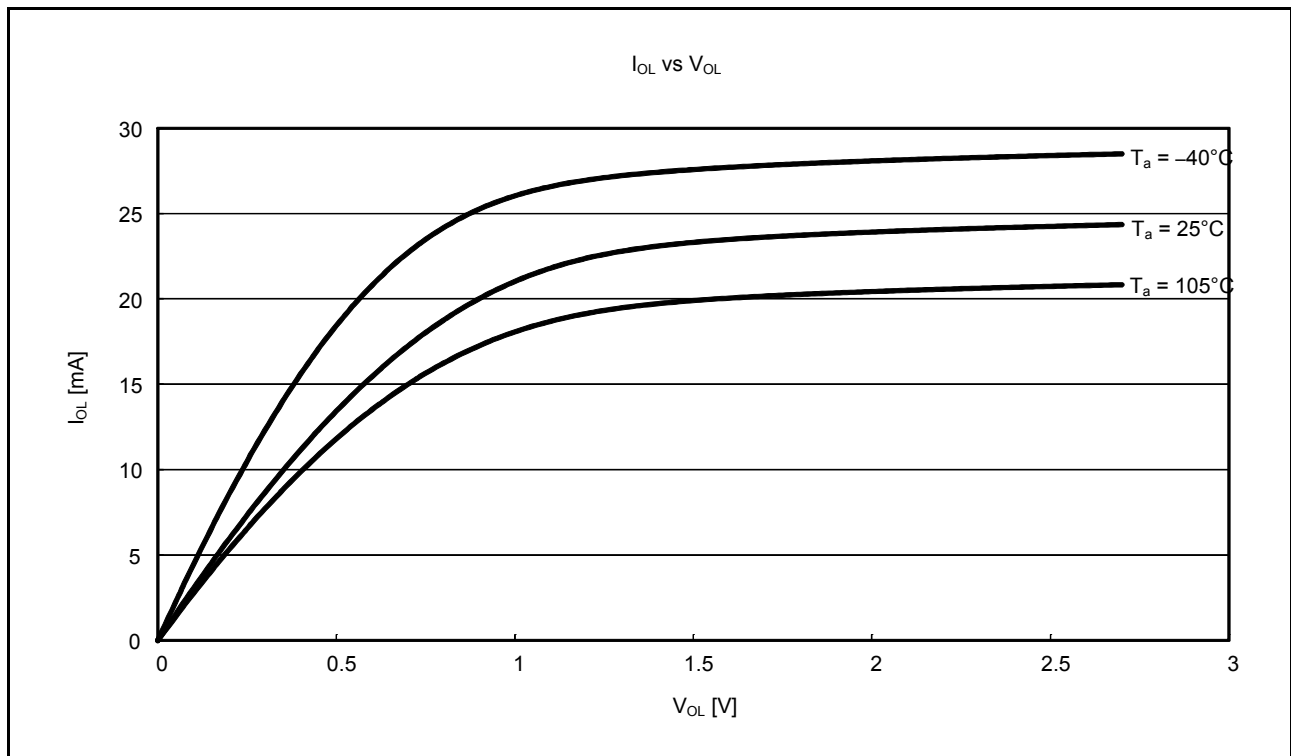


Figure 5.17 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at $V_{CC} = 2.7\text{ V}$ (Reference Data)

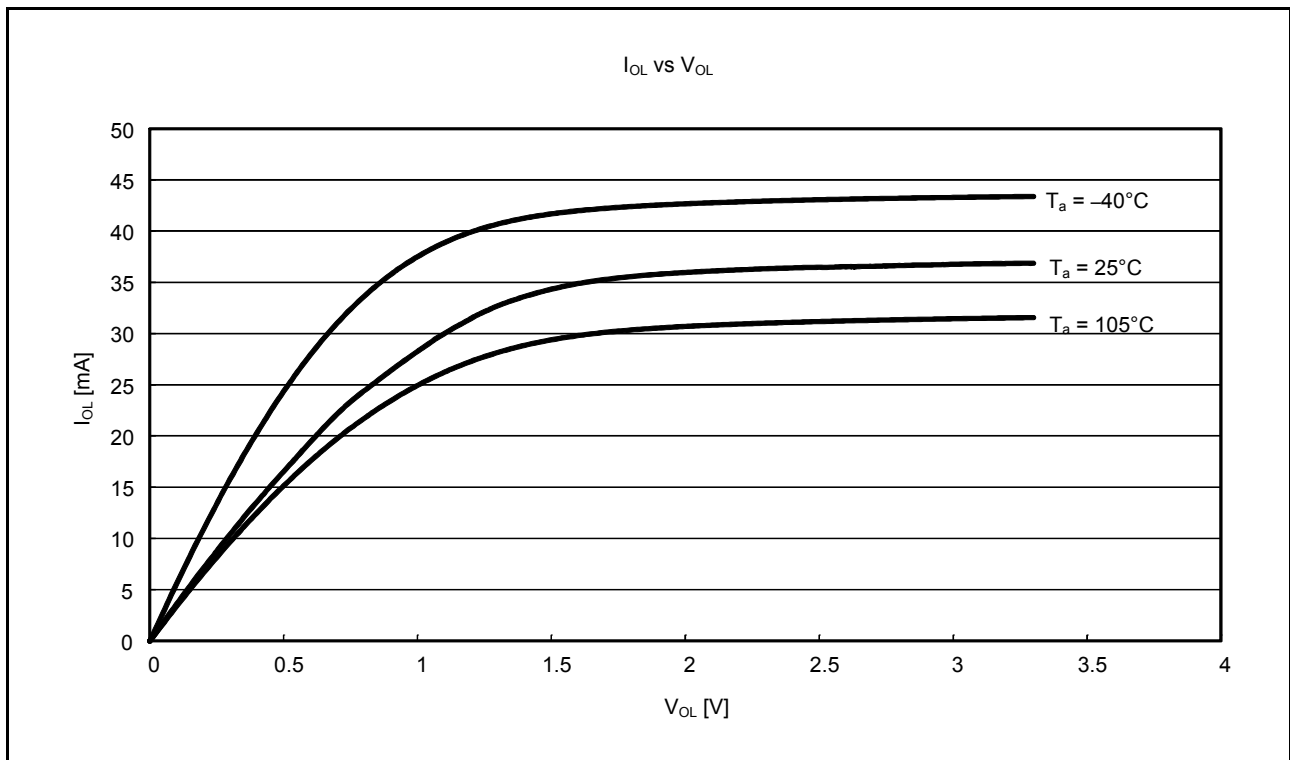


Figure 5.18 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

5.2.3 Standard I/O Pin Output Characteristics (3)

Figure 5.19 to Figure 5.22 show the characteristics of ports P40 to P44, P46, ports PJ6, PJ7.



Figure 5.19 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics of Ports P40 to P44, P46, Ports PJ6, PJ7 at $T_a = 25^\circ\text{C}$ (Reference Data)

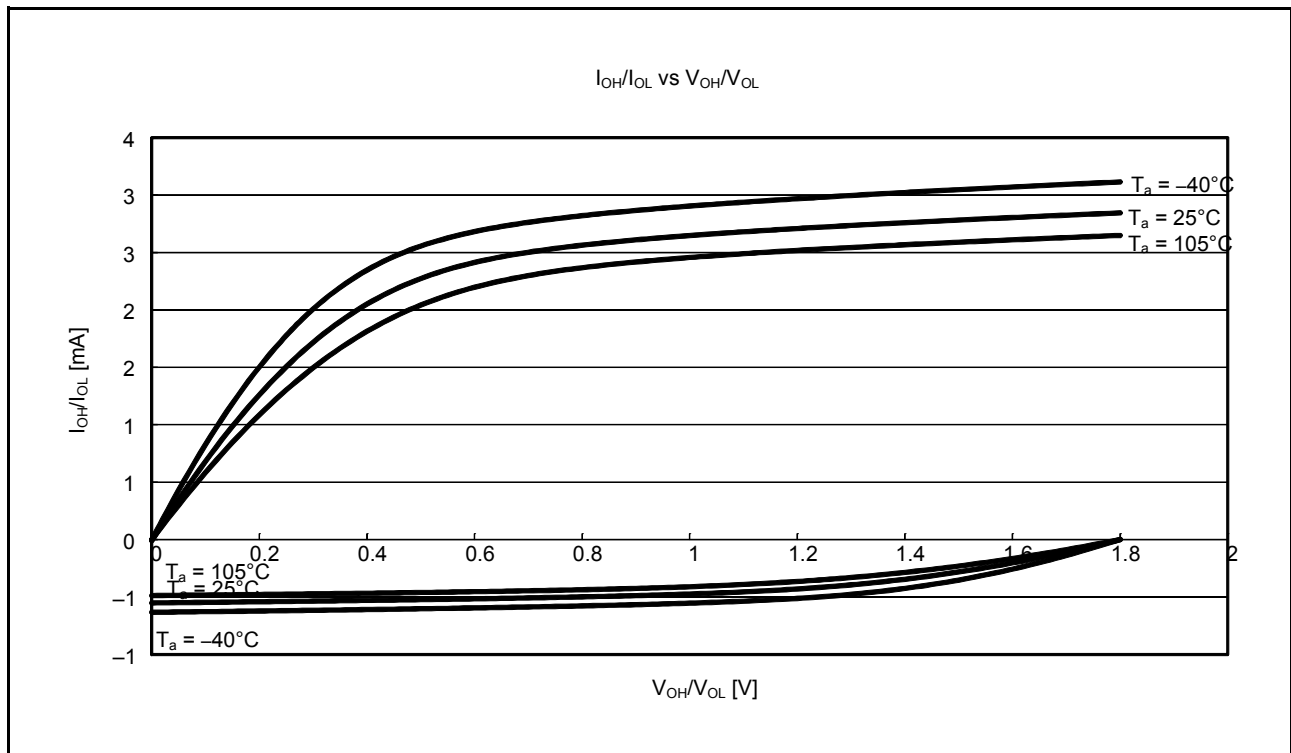


Figure 5.20 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Ports P40 to P44, P46, Ports PJ6, PJ7 at $V_{CC} = 1.8\text{ V}$ (Reference Data)

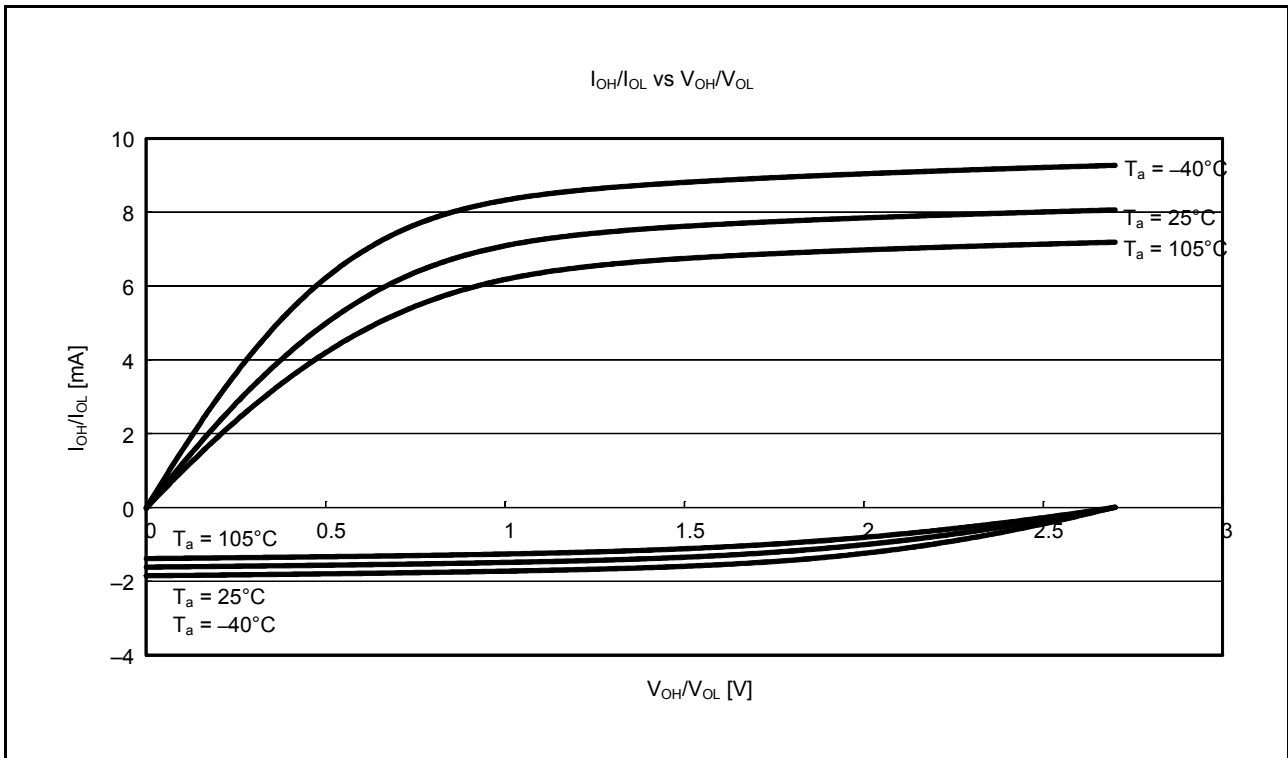


Figure 5.21 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Ports P40 to P44, P46, Ports PJ6, PJ7 at $V_{CC} = 2.7$ V (Reference Data)



Figure 5.22 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Ports P40 to P44, P46, Ports PJ6, PJ7 at $V_{CC} = 3.3$ V (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.21 Operation Frequency Value (High-Speed Operating Mode)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

| Item | | Symbol | VCC | | | | Unit |
|-----------------------------|-----------------------------------|------------------|--------------|--------------|--------------|-------------------|------|
| | | | 1.8 to 2.4 V | 2.4 to 2.7 V | 2.7 to 3.6 V | When USB in Use*4 | |
| Maximum operating frequency | System clock (ICLK) | f_{max} | 8 | 16 | 32 | 24 | MHz |
| | FlashIF clock (FCLK)*1, *2 | | 8 | 16 | 32 | 24 | |
| | Peripheral module clock (PCLKB) | | 8 | 16 | 32 | 24 | |
| | Peripheral module clock (PCLKD)*3 | | 8 | 16 | 32 | 24 | |
| | USB clock (UCLK) | f_{usb} | — | — | — | 48 | |

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK should be $\pm 3.5\%$. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.

Note 4. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.

Table 5.22 Operation Frequency Value (Middle-Speed Operating Mode)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

| Item | | Symbol | VCC | | | | Unit |
|-----------------------------|-----------------------------------|------------------|--------------|--------------|--------------|-------------------|------|
| | | | 1.8 to 2.4 V | 2.4 to 2.7 V | 2.7 to 3.6 V | When USB in Use*4 | |
| Maximum operating frequency | System clock (ICLK) | f_{max} | 8 | 12 | 12 | 12 | MHz |
| | FlashIF clock (FCLK)*1, *2 | | 8 | 12 | 12 | 12 | |
| | Peripheral module clock (PCLKB) | | 8 | 12 | 12 | 12 | |
| | Peripheral module clock (PCLKD)*3 | | 8 | 12 | 12 | 12 | |
| | USB clock (UCLK) | f_{usb} | — | — | — | 48 | |

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK should be $\pm 3.5\%$.

Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the A/D converter is in use.

Note 4. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.

Table 5.23 Operation Frequency Value (Low-Speed Operating Mode)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

| Item | | Symbol | VCC | | | Unit |
|-----------------------------|-----------------------------------|------------------|--------------|--------------|--------------|------|
| | | | 1.8 to 2.4 V | 2.4 to 2.7 V | 2.7 to 3.6 V | |
| Maximum operating frequency | System clock (ICLK) | f_{max} | 32.768 | | | kHz |
| | FlashIF clock (FCLK)*1 | | 32.768 | | | |
| | Peripheral module clock (PCLKB) | | 32.768 | | | |
| | Peripheral module clock (PCLKD)*2 | | 32.768 | | | |

Note 1. Programming and erasing the flash memory is impossible.

Note 2. The A/D converter cannot be used.

Table 5.24 Clock TimingConditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|----------------------|--------------------------------|--------|-------|---------------|---|-----|
| XTAL external clock input cycle time | t_{Xcyc} | 50 | — | — | ns | Figure 5.23 | |
| XTAL external clock input high pulse width | t_{XH} | 20 | — | — | ns | | |
| XTAL external clock input low pulse width | t_{XL} | 20 | — | — | ns | | |
| XTAL external clock rising time | t_{Xr} | — | — | 5 | ns | | |
| XTAL external clock falling time | t_{Xf} | — | — | 5 | ns | | |
| XTAL external clock input wait time*1 | t_{EXWT} | 0.5 | — | — | μs | Figure 5.25 | |
| Main clock oscillator oscillation frequency | f_{MAIN} | $2.4 \leq \text{VCC} \leq 3.6$ | 1 | — | 20 | | MHz |
| | | $1.8 \leq \text{VCC} < 2.4$ | 1 | — | 8 | | |
| Main clock oscillation stabilization time (crystal)*2 | t_{MAINOSC} | — | 3 | — | ms | Figure 5.25 | |
| Main clock oscillation stabilization time (ceramic resonator)*2 | t_{MAINOSC} | — | 50 | — | μs | | |
| LOCO clock oscillation frequency | f_{LOCO} | 3.44 | 4.0 | 4.56 | MHz | Figure 5.26 | |
| LOCO clock oscillation stabilization time | t_{LOCO} | — | — | 0.5 | μs | | |
| IWDT-dedicated clock oscillation frequency | f_{ILOCO} | 12.75 | 15 | 17.25 | kHz | Figure 5.24 | |
| IWDT-dedicated clock oscillation stabilization time | t_{ILOCO} | — | — | 50 | μs | | |
| HOCO clock oscillation frequency | f_{HOCO} | 31.52 | 32 | 32.48 | MHz | $T_a = -40\text{ to }85^\circ\text{C}$ | |
| | | 31.68 | 32 | 32.32 | | $T_a = -20\text{ to }85^\circ\text{C}$ | |
| | | 31.36 | 32 | 32.64 | | $T_a = -40\text{ to }105^\circ\text{C}$ | |
| HOCO clock oscillation stabilization time | t_{HOCO2} | — | — | 56 | μs | Figure 5.28 | |
| PLL input frequency*3 | f_{PLLIN} | 4 | — | 8 | MHz | Figure 5.29 | |
| PLL circuit oscillation frequency*3 | f_{PLL} | 32 | — | 48 | MHz | | |
| PLL clock oscillation stabilization time | t_{PLL} | — | — | 50 | μs | Figure 5.29 | |
| PLL free-running oscillation frequency | f_{PLLFR} | — | 8 | — | MHz | Figure 5.30 | |
| Sub-clock oscillator oscillation frequency*5 | f_{SUB} | — | 32.768 | — | kHz | | |
| Sub-clock oscillation stabilization time*4 | t_{SUBOSC} | — | 0.5 | — | s | Figure 5.30 | |

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8-MHz oscillator is used.

When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the oscillator-manufacturer-recommended value.

After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that it has become 1, and then start using the main clock.

Note 3. The VCC range that the PLL can be used is 2.4 to 3.6 V.

Note 4. After changing the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

Reference value when a 32.768-kHz resonator is used.

Note 5. Only 32.768 kHz can be used.



Figure 5.23 XTAL External Clock Input Timing



Figure 5.24 IWDT-Dedicated Clock Oscillation Start Timing



Figure 5.25 Main Clock Oscillation Start Timing



Figure 5.26 LOCO Clock Oscillation Start Timing



Figure 5.27 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)



Figure 5.28 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOEN.HCSTP Bit)



Figure 5.29 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)



Figure 5.30 Sub-Clock Oscillation Start Timing

5.3.2 Reset Timing

Table 5.25 Reset Timing

Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|----------------------------|-------------|------|------|------------------|-----------------|-------------|
| RES# pulse width | At power-on | t_{RESWP} | 3 | — | — | ms | Figure 5.31 |
| | Other than above | t_{RESW} | 30 | — | — | μs | Figure 5.32 |
| Wait time after RES# cancellation (at power-on) | At normal startup*1 | t_{RESWT} | — | 8.5 | — | ms | Figure 5.31 |
| | During fast startup time*2 | t_{RESWT} | — | 560 | — | μs | |
| Wait time after RES# cancellation (during powered-on state) | t_{RESWT} | — | 114 | — | μs | Figure 5.32 | |
| Independent watchdog timer reset period | t_{RESWIW} | — | 1 | — | IWDT clock cycle | Figure 5.33 | |
| Software reset period | t_{RESWSW} | — | 1 | — | ICLK cycle | | |
| Wait time after independent watchdog timer reset cancellation*3 | t_{RESW2} | — | 300 | — | μs | | |
| Wait time after software reset cancellation | t_{RESW2} | — | 168 | — | μs | | |

Note 1. When OFS1.(STUPLVD1REN, FASTSTUP) = 11b.

Note 2. When OFS1.(STUPLVD1REN, FASTSTUP) \neq 11b.

Note 3. When IWDTCR.CKS[3:0] = 0000b.

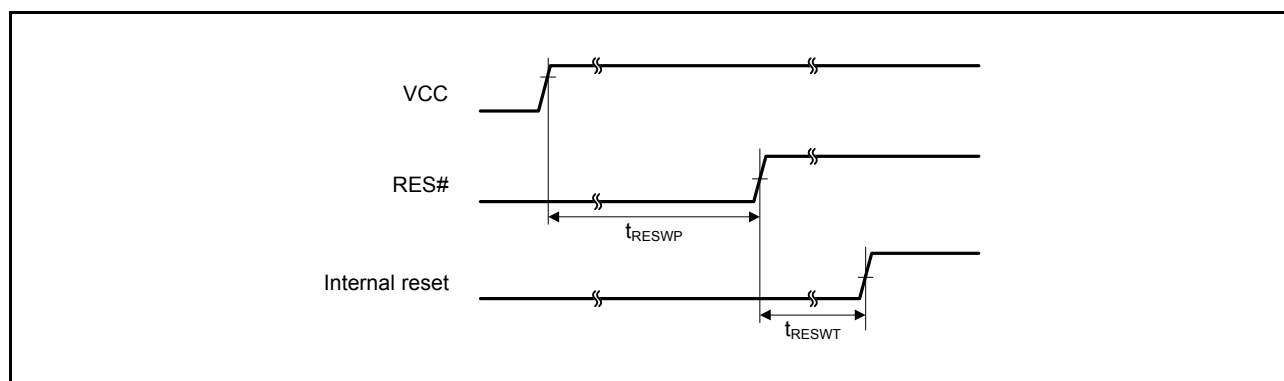


Figure 5.31 Reset Input Timing at Power-On

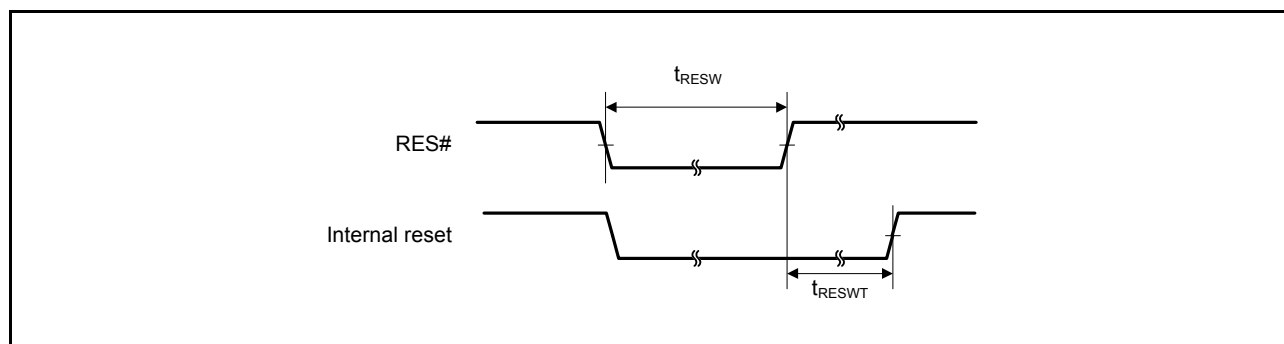


Figure 5.32 Reset Input Timing (1)

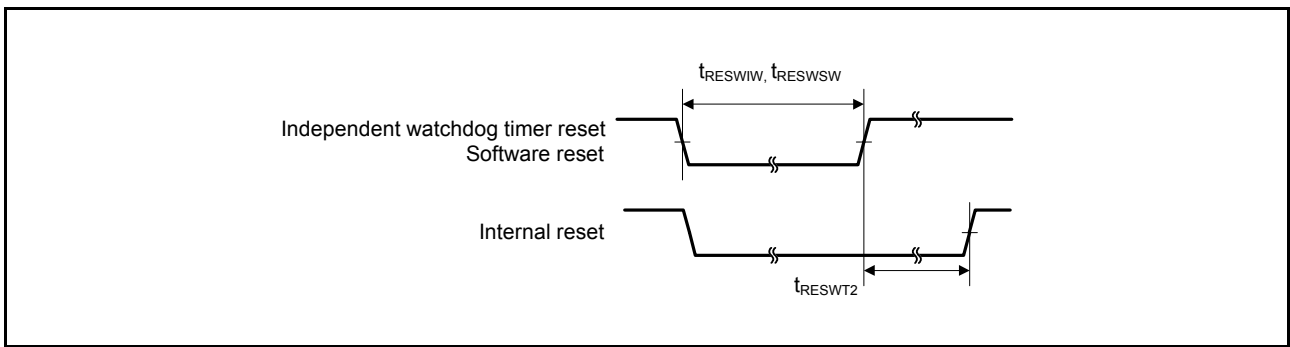


Figure 5.33 Reset Input Timing (2)

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.26 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{SS0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | | |
|--|---|---|---|--------------------|------|------|-----------------|----|-------------|
| Recovery time from software standby mode*1 | High-speed mode | Crystal connected to main clock oscillator | Main clock oscillator operating*2 | t _{SBYMC} | — | 2 | 3 | ms | Figure 5.34 |
| | | | Main clock oscillator and PLL circuit operating*3 | t _{SBYPC} | — | 2 | 3 | ms | |
| | External clock input to main clock oscillator | Main clock oscillator operating*4 | t _{SBYEX} | — | 35 | 50 | μs | | |
| | | Main clock oscillator and PLL circuit operating*5 | t _{SBYPE} | — | 70 | 95 | μs | | |
| | Sub-clock oscillator operating | | t _{SBYSC} | — | 650 | 800 | μs | | |
| | HOCO clock oscillator operating*6 | | t _{SBYHO} | — | 40 | 55 | μs | | |
| | LOCO clock oscillator operating | | t _{SBYLO} | — | 40 | 55 | μs | | |

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. This applies when only the oscillator listed in each item is operating and the other oscillators are stopped.

Note 2. When the frequency of the crystal is 20 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 3. When the frequency of PLL is 32 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 4. When the frequency of the external clock is 20 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 5. When the frequency of PLL is 32 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 6. When the frequency of HOCO is 32 MHz.

When the high-speed clock oscillator wait control register (HOCOWTCR) is set to 05h.

Table 5.27 Timing of Recovery from Low Power Consumption Modes (2)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{SS0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|--|-------------------|---|---|-------------|------|------|------|-----------------|-------------|
| Recovery time from software standby mode*1 | Middle-speed mode | Crystal connected to main clock oscillator | Main clock oscillator operating*2 | t_{SBYMC} | — | 2 | 3 | ms | Figure 5.34 |
| | | | Main clock oscillator and PLL circuit operating*3 | t_{SBYPC} | — | 2 | 3 | ms | |
| | | External clock input to main clock oscillator | Main clock oscillator operating*4 | t_{SBYEX} | — | 3 | 4 | μs | |
| | | | Main clock oscillator and PLL circuit operating*5 | t_{SBYPE} | — | 65 | 85 | μs | |
| | | Sub-clock oscillator operating | | t_{SBYSC} | — | 600 | 750 | μs | |
| | | HOCO clock oscillator operating*6 | | t_{SBYHO} | — | 40 | 50 | μs | |
| | | LOCO clock oscillator operating | | t_{SBYLO} | — | 4.8 | 7 | μs | |

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. This applies when only the oscillator listed in each item is operating and the other oscillators are stopped.

Note 2. When the frequency of the crystal is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 3. When the frequency of PLL is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 4. When the frequency of the external clock is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 5. When the frequency of PLL is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 6. When the frequency of HOCO is 8 MHz.

When the high-speed clock oscillator wait control register (HOCOWTCR) is set to 05h.

Table 5.28 Timing of Recovery from Low Power Consumption Modes (3)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{SS0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--|----------------|--------------------------------|-------------|------|------|------|---------------|-----------------|
| Recovery time from software standby mode*1 | Low-speed mode | Sub-clock oscillator operating | t_{SBYSC} | — | 600 | 750 | μs | Figure 5.34 |

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

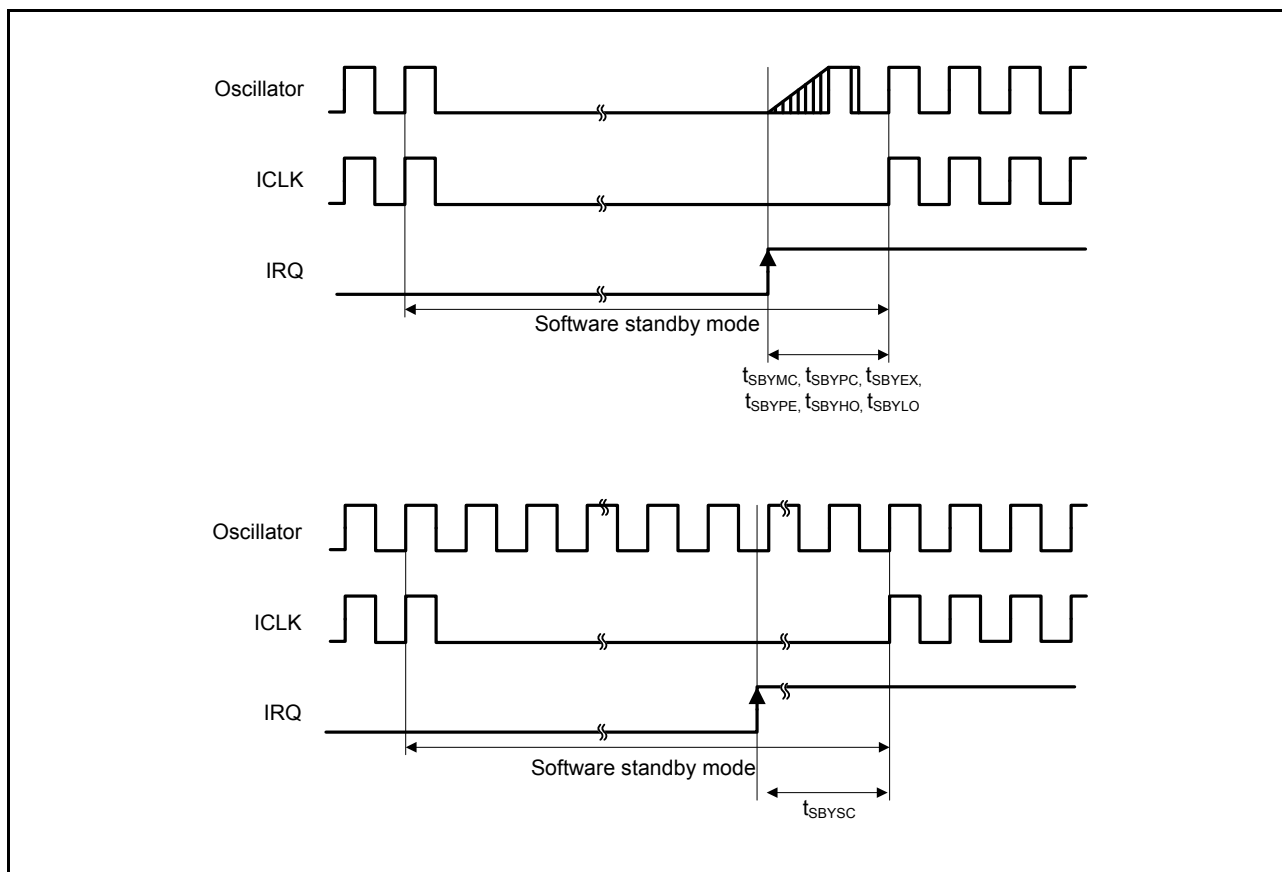


Figure 5.34 Software Standby Mode Cancellation Timing

Table 5.29 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--------------------------------------|---------------------|------|------|------|---------------|-----------------|
| Recovery time from deep sleep mode*1 | High-speed mode*2 | — | 2 | 3.5 | μs | |
| | Middle-speed mode*3 | — | 3 | 4 | μs | |
| | Low-speed mode*4 | — | 400 | 500 | μs | |

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. Oscillators continue oscillating in deep sleep mode.

Note 2. When the frequency of the system clock is 32 MHz.

Note 3. When the frequency of the system clock is 12 MHz.

Note 4. When the frequency of the system clock is 32.768 kHz.

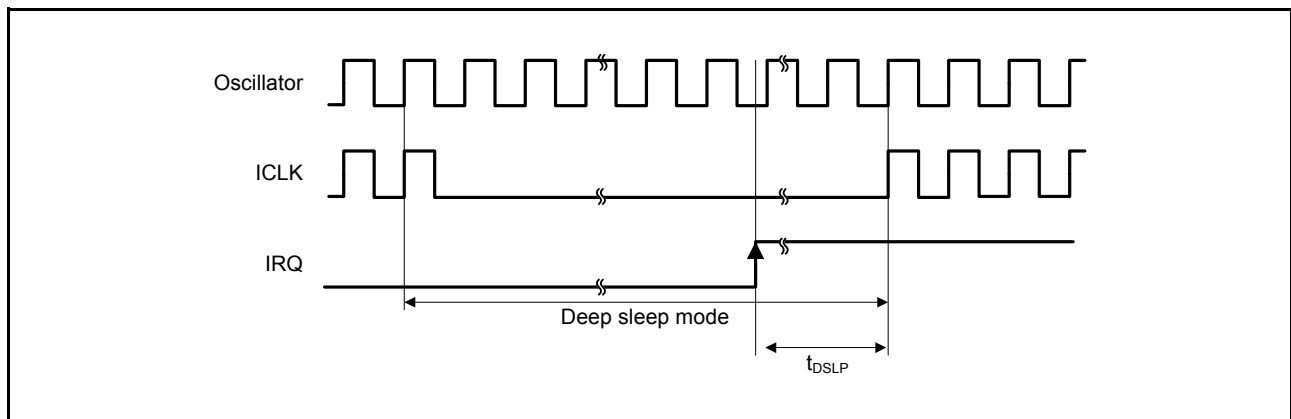


Figure 5.35 Deep Sleep Mode Cancellation Timing

Table 5.30 Timing of Recovery from Low Power Consumption Modes (5) Operating Mode Transition Time

Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Mode before Transition | Mode after Transition | ICLK Frequency | Transition Time | | | Unit |
|--|--|----------------|-----------------|--------|------|---------------|
| | | | Min. | Typ. | Max. | |
| High-speed operating mode | Middle-speed operating mode | 8 MHz | — | 10 | — | μs |
| Middle-speed operating mode | High-speed operating mode | 8 MHz | — | 37.5 | — | μs |
| Low-speed operating mode | Middle-speed operating mode, high-speed operating mode | 32.768 kHz | — | 213.62 | — | μs |
| Middle-speed operating mode, high-speed operating mode | Low-speed operating mode | 32.768 kHz | — | 183.11 | — | μs |

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

5.3.4 Control Signal Timing

Table 5.31 Control Signal Timing

Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|-----------------|------------|-----------------------------|------|------|------|--|---|
| NMI pulse width | t_{NMIW} | 200 | — | — | ns | NMI digital filter disabled (NMIFLTE.NFLTEN = 0) | $t_{Pcyc} \times 2 \leq 200\text{ ns}$ |
| | | $t_{Pcyc} \times 2^{*1}$ | — | — | | | $t_{Pcyc} \times 2 > 200\text{ ns}$ |
| | | 200 | — | — | | NMI digital filter enabled (NMIFLTE.NFLTEN = 1) | $t_{NMICK} \times 3 \leq 200\text{ ns}$ |
| | | $t_{NMICK} \times 3.5^{*2}$ | — | — | | | $t_{NMICK} \times 3 > 200\text{ ns}$ |
| IRQ pulse width | t_{IRQW} | 200 | — | — | ns | IRQ digital filter disabled (IRQFLTE0.FLTENi = 0) | $t_{Pcyc} \times 2 \leq 200\text{ ns}$ |
| | | $t_{Pcyc} \times 2^{*1}$ | — | — | | | $t_{Pcyc} \times 2 > 200\text{ ns}$ |
| | | 200 | — | — | | IRQ digital filter enabled (IRQFLTE0.FLTENi = 1) | $t_{IRQCK} \times 3 \leq 200\text{ ns}$ |
| | | $t_{IRQCK} \times 3.5^{*3}$ | — | — | | | $t_{IRQCK} \times 3 > 200\text{ ns}$ |

Note: • 200 ns minimum in software standby mode.

Note 1. t_{Pcyc} indicates the cycle of PCLKB.

Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.

Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).



Figure 5.36 NMI Interrupt Input Timing



Figure 5.37 IRQ Interrupt Input Timing

5.3.5 Timing of On-Chip Peripheral Modules

Table 5.32 Timing of On-Chip Peripheral Modules (1)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions | |
|---------------------------------|-----------------------------------|------------------------------|------------------------------|----------------------------|------------|-----------------|--------------------------|
| I/O ports | Input data pulse width | t_{PRW} | 1.5 | — | t_{Pcyc} | Figure 5.38 | |
| MTU2 | Input capture input pulse width | Single-edge setting | t_{TICW} | 1.5 | — | t_{Pcyc} | Figure 5.39 |
| | | Both-edge setting | | 2.5 | | | |
| | Timer clock pulse width | Single-edge setting | t_{TCKWH} , t_{TCKWL} | 1.5 | — | t_{Pcyc} | Figure 5.40 |
| | | Both-edge setting | | 2.5 | | | |
| Phase counting mode | | 2.5 | | | | | |
| POE | POE# input pulse width | t_{POEW} | 1.5 | — | t_{Pcyc} | Figure 5.41 | |
| SCI | Input clock cycle | Asynchronous | t_{Scyc} | 4 | — | t_{Pcyc} | Figure 5.42 |
| | | Clock synchronous | | 6 | | | |
| | Input clock pulse width | | t_{SCKW} | 0.4 | 0.6 | t_{Scyc} | |
| | Input clock rise time | | t_{SCKr} | — | 20 | ns | |
| | Input clock fall time | | t_{SCKf} | — | 20 | ns | |
| | Output clock cycle | Asynchronous | t_{Scyc} | 16 | — | t_{Pcyc} | Figure 5.43 C = 30 pF |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | t_{SCKW} | 0.4 | 0.6 | t_{Scyc} | |
| | Output clock rise time | | t_{SCKr} | — | 20 | ns | |
| | Output clock fall time | | t_{SCKf} | — | 20 | ns | |
| | Transmit data delay time (master) | Clock synchronous | | t_{TXD} | — | 40 | ns |
| | Transmit data delay time (slave) | Clock synchronous | 2.7 V or above | | — | 65 | ns |
| | | | 1.8 V or above | — | 100 | ns | |
| | Receive data setup time (master) | Clock synchronous | 2.7 V or above | t_{RXS} | 65 | — | ns |
| 1.8 V or above | | | 90 | | — | ns | |
| Receive data setup time (slave) | Clock synchronous | | | 40 | — | ns | |
| Receive data hold time | Clock synchronous | | | 40 | — | ns | |
| A/D converter | Trigger input pulse width | t_{TRGW} | 1.5 | — | t_{Pcyc} | Figure 5.44 | |
| CAC | CACREF input pulse width | $t_{Pcyc} \leq t_{cac}^{*2}$ | t_{CACREF} | $4.5 t_{cac} + 3 t_{Pcyc}$ | — | ns | |
| | | $t_{Pcyc} > t_{cac}^{*2}$ | | $5 t_{cac} + 6.5 t_{Pcyc}$ | | | |
| CLKOUT | CLKOUT pin output cycle*4 | VCC = 2.7 V or above | t_{Cyc} | 125 | — | ns | |
| | | VCC = 1.8 V or above | | 250 | | | |
| | CLKOUT pin high pulse width*3 | VCC = 2.7 V or above | t_{CH} | 35 | — | ns | |
| | | VCC = 1.8 V or above | | 70 | | | |
| | CLKOUT pin low pulse width*3 | VCC = 2.7 V or above | t_{CL} | 35 | — | ns | |
| | | VCC = 1.8 V or above | | 70 | | | |
| | CLKOUT pin output rise time | VCC = 2.7 V or above | t_{Cr} | — | 15 | ns | |
| | | VCC = 1.8 V or above | | 30 | | | |
| | CLKOUT pin output fall time | VCC = 2.7 V or above | t_{Cf} | — | 15 | ns | |
| | | VCC = 1.8 V or above | | 30 | | | |

Note 1. t_{Pcyc} : PCLK cycle

Note 2. t_{cac} : CAC count clock source cycle

Note 3. When the LOCO is selected as the clock output source (CKOCR.CKOSSEL[2:0] bits = 000b), set the clock output division ratio selection to divided by 2 (CKOCR.CKODIV[2:0] bits = 001b).

Note 4. When the XTAL external clock input or an oscillator is used with divided by 1 (CKOCR.CKOSSEL[2:0] bits = 010b and CKOCR.CKODIV[2:0] bits = 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Table 5.33 Timing of On-Chip Peripheral Modules (2)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{SS0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$, $C = 30\text{ pF}$

| Item | | Symbol | Min. | Max. | Unit | Test Conditions | |
|------|------------------------------------|----------------|---|---|--|-----------------|---------------------------|
| RSPI | RSPCK clock cycle | Master | t_{SPCyc} | 2 | 4096 | t_{Pcyc}^*1 | Figure 5.46 |
| | | Slave | | 8 | 4096 | | |
| | RSPCK clock high pulse width | Master | t_{SPCKWH} | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | — | ns | |
| | | Slave | | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2$ | — | | |
| | RSPCK clock low pulse width | Master | t_{SPCKWL} | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$ | — | ns | |
| | | Slave | | $(t_{SPCyc} - t_{SPCKr} - t_{SPCKf})/2$ | — | | |
| | RSPCK clock rise/fall time | Output | 2.7 V or above | t_{SPCKr} | — | 10 | ns |
| | | | | 1.8 V or above | t_{SPCKf} | — | 15 |
| | | Input | | | — | 1 | μs |
| | Data input setup time | Master | 2.7 V or above | t_{SU} | 10 | — | ns |
| | | | | 1.8 V or above | | 30 | — |
| | | Slave | | | $25 - t_{Pcyc}$ | — | |
| | Data input hold time | Master | RSPCK set to a division ratio other than PCLKB divided by 2 | t_H | t_{Pcyc} | — | ns |
| | | | RSPCK set to PCLKB divided by 2 | t_{HF} | 0 | — | |
| | | Slave | | t_H | $20 + 2 \times t_{Pcyc}$ | — | |
| | SSL setup time | Master | t_{LEAD} | $-30 + N \times 2 \times t_{SPCyc}$ | — | ns | |
| | | Slave | | 2 | — | t_{Pcyc} | |
| | SSL hold time | Master | t_{LAG} | $-30 + N \times 3 \times t_{SPCyc}$ | — | ns | |
| | | Slave | | 2 | — | t_{Pcyc} | |
| | Data output delay time | Master | 2.7 V or above | t_{OD} | — | 14 | ns |
| | | | | 1.8 V or above | | — | 30 |
| | | Slave | 2.7 V or above | | | — | $3 \times t_{Pcyc} + 65$ |
| | | | | 1.8 V or above | | — | $3 \times t_{Pcyc} + 105$ |
| | Data output hold time | Master | 2.7 V or above | | t_{OH} | 0 | — |
| | | | | 1.8 V or above | | -20 | — |
| | | Slave | | | 0 | — | |
| | Successive transmission delay time | Master | t_{TD} | $t_{SPCyc} + 2 \times t_{Pcyc}$ | $8 \times t_{SPCyc} + 2 \times t_{Pcyc}$ | ns | |
| | | Slave | | $4 \times t_{Pcyc}$ | — | | |
| | MOSI and MISO rise/fall time | Output | 2.7 V or above | t_{Dr}, t_{Df} | — | 10 | ns |
| | | | | 1.8 V or above | | — | 20 |
| | | Input | | | — | 1 | μs |
| | SSL rise/fall time | Output | t_{SSLr}, t_{SSLf} | — | 20 | ns | |
| | | Input | | — | 1 | μs | |
| | Slave access time | 2.7 V or above | t_{SA} | | — | 6 | t_{Pcyc} |
| | | | | 1.8 V or above | | — | 7 |
| | Slave output release time | 2.7 V or above | t_{REL} | | | — | 5 |
| | | | | 1.8 V or above | | — | 6 |

Note 1. t_{Pcyc} : PCLK cycle

Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)

Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

Table 5.34 Timing of On-Chip Peripheral Modules (3)

Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$, $C = 30\text{ pF}$

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions | |
|-------------------------------|---------------------------------|----------------------|------------------------|-------|------------|-----------------------------|-----------------------------|
| Simple SPI | SCK clock cycle output (master) | t_{SPCyc} | 4 | 65536 | t_{Pcyc} | Figure 5.46 | |
| | SCK clock cycle input (slave) | | 6 | 65536 | | | |
| | SCK clock high pulse width | | t_{SPCKWH} | 0.4 | 0.6 | | t_{SPCyc} |
| | SCK clock low pulse width | | t_{SPCKWL} | 0.4 | 0.6 | | t_{SPCyc} |
| | SCK clock rise/fall time | | t_{SPCKr}, t_{SPCKf} | — | 20 | | ns |
| | Data input setup time (master) | 2.7 V or above | t_{SU} | 65 | — | ns | Figure 5.47, Figure 5.49 |
| | | 1.8 V or above | | 95 | — | | |
| | Data input setup time (slave) | | | 40 | — | | |
| | Data input hold time | | t_H | 40 | — | ns | |
| | SS input setup time | | t_{LEAD} | 3 | — | t_{Pcyc} | |
| | SS input hold time | | t_{LAG} | 3 | — | t_{Pcyc} | |
| | Data output delay time (master) | | t_{OD} | — | 40 | ns | |
| | Data output delay time (slave) | 2.7 V or above | | — | 65 | | |
| | | 1.8 V or above | | — | 85 | | |
| | Data output hold time (master) | 2.7 V or above | t_{OH} | -10 | — | ns | |
| 1.8 V or above | | -20 | | — | | | |
| Data output hold time (slave) | | -10 | | — | | | |
| Data rise/fall time | | t_{Dr}, t_{Df} | — | 20 | ns | | |
| SS input rise/fall time | | t_{SSLr}, t_{SSLf} | — | 20 | ns | | |
| Slave access time | | t_{SA} | — | 6 | t_{Pcyc} | Figure 5.51, Figure 5.52 | |
| Slave output release time | | t_{REL} | — | 6 | t_{Pcyc} | | |

Note 1. t_{Pcyc} : PCLK cycle

Table 5.35 Timing of On-Chip Peripheral Modules (4)

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $2.7\text{ V} \leq AV_{SS0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $f_{PCLKB} \leq 32\text{ MHz}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Symbol | Min.*1 | Max. | Unit | Test Conditions |
|-----------------------------------|---|------------|----------------------------------|--------------------------|------|-----------------|
| RIIC (Standard mode, SMBus) | SCL0 input cycle time | t_{SCL} | $6(12) \times t_{IICcyc} + 1300$ | — | ns | Figure 5.53 |
| | SCL0 input high pulse width | t_{SCLH} | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL0 input low pulse width | t_{SCLL} | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL0, SDA0 input rise time | t_{Sr} | — | 1000 | ns | |
| | SCL0, SDA0 input fall time | t_{Sf} | — | 300 | ns | |
| | SCL0, SDA0 input spike pulse removal time | t_{SP} | 0 | $1(4) \times t_{IICcyc}$ | ns | |
| | SDA0 input bus free time | t_{BUF} | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | START condition input hold time | t_{STAH} | $t_{IICcyc} + 300$ | — | ns | |
| | Repeated START condition input setup time | t_{STAS} | 1000 | — | ns | |
| | STOP condition input setup time | t_{STOS} | 1000 | — | ns | |
| | Data input setup time | t_{SDAS} | $t_{IICcyc} + 50$ | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| | SCL0, SDA0 capacitive load | C_b | — | 400 | pF | |
| RIIC (Fast mode) | SCL0 input cycle time | t_{SCL} | $6(12) \times t_{IICcyc} + 600$ | — | ns | Figure 5.53 |
| | SCL0 input high pulse width | t_{SCLH} | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL0 input low pulse width | t_{SCLL} | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL0, SDA0 input rise time | t_{Sr} | —*2 | 300 | ns | |
| | SCL0, SDA0 input fall time | t_{Sf} | —*2 | 300 | ns | |
| | SCL0, SDA0 input spike pulse removal time | t_{SP} | 0 | $1(4) \times t_{IICcyc}$ | ns | |
| | SDA0 input bus free time | t_{BUF} | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | START condition input hold time | t_{STAH} | $t_{IICcyc} + 300$ | — | ns | |
| | Repeated START condition input setup time | t_{STAS} | 300 | — | ns | |
| | STOP condition input setup time | t_{STOS} | 300 | — | ns | |
| | Data input setup time | t_{SDAS} | $t_{IICcyc} + 50$ | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| | SCL0, SDA0 capacitive load | C_b | — | 400 | pF | |

Note: • t_{IICcyc} : RIIC internal reference count clock (IIC ϕ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. The minimum t_{sr} and t_{sf} specifications for fast mode are not set.

Table 5.36 Timing of On-Chip Peripheral Modules (5)

Conditions: $2.7\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $2.7\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $fPCLKB \leq 32\text{ MHz}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|--|---|------------|------|--------------------------|------|-----------------|
| Simple I ² C (Standard mode) | SDA0 input rise time | t_{Sr} | — | 1000 | ns | Figure 5.53 |
| | SDA0 input fall time | t_{Sf} | — | 300 | ns | |
| | SDA0 input spike pulse removal time | t_{SP} | 0 | $4 \times t_{pcyc}^{*1}$ | ns | |
| | Data input setup time | t_{SDAS} | 250 | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| | SCL0, SDA0 capacitive load | C_b | — | 400 | pF | |
| Simple I ² C (Fast mode) | SCL0, SDA0 input rise time | t_{Sr} | — | 300 | ns | Figure 5.53 |
| | SCL0, SDA0 input fall time | t_{Sf} | — | 300 | ns | |
| | SCL0, SDA0 input spike pulse removal time | t_{SP} | 0 | $4 \times t_{pcyc}^{*1}$ | ns | |
| | Data input setup time | t_{SDAS} | 100 | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| | SCL0, SDA0 capacitive load | C_b | — | 400 | pF | |

Note: • t_{pcyc} : PCLK cycle

Note 1. This applies when the SMR.CKS[1:0] bits = 00b and the SNFR.NFCS[2:0] bits = 010b while the SNFR.NFE bit = 1 and the digital filter is enabled.

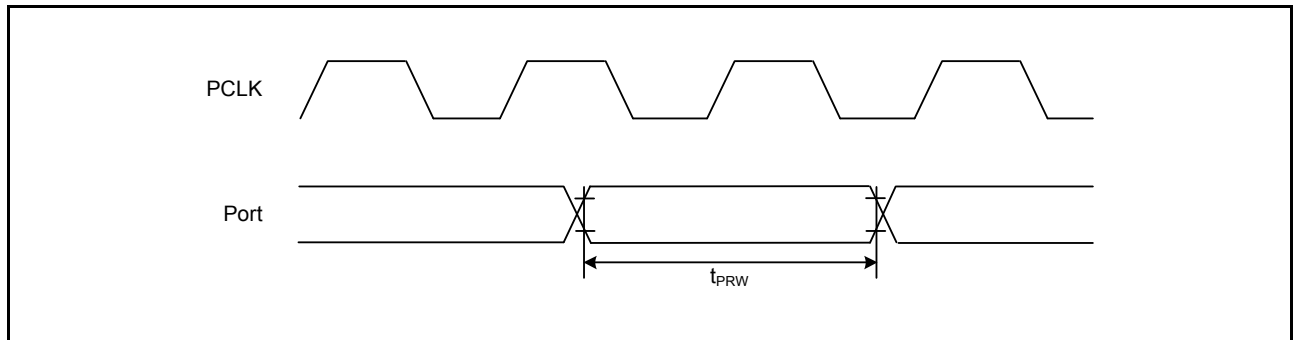


Figure 5.38 I/O Port Input Timing

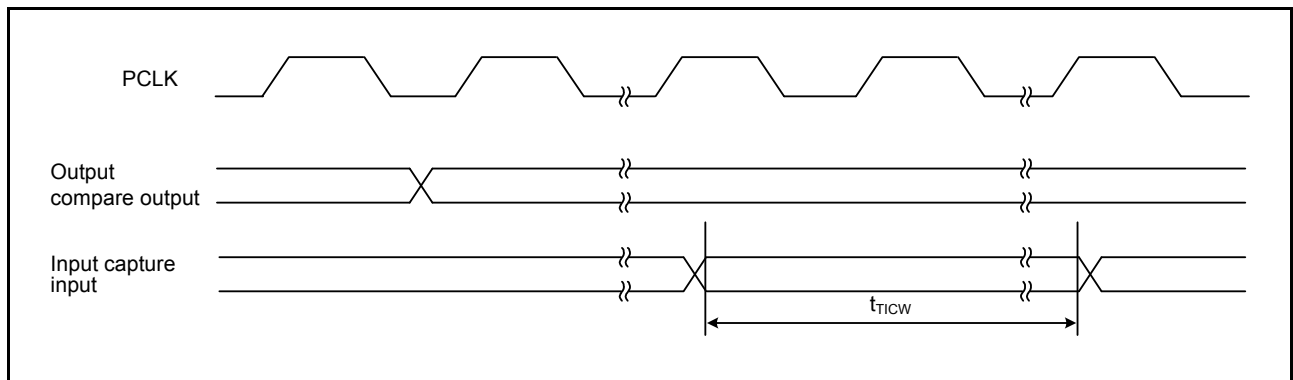


Figure 5.39 MTU2 Input/Output Timing



Figure 5.40 MTU2 Clock Input Timing



Figure 5.41 POE# Input Timing



Figure 5.42 SCK Clock Input Timing



Figure 5.43 SCI Input/Output Timing: Clock Synchronous Mode



Figure 5.44 A/D Converter External Trigger Input Timing



Figure 5.45 CLKOUT Output Timing

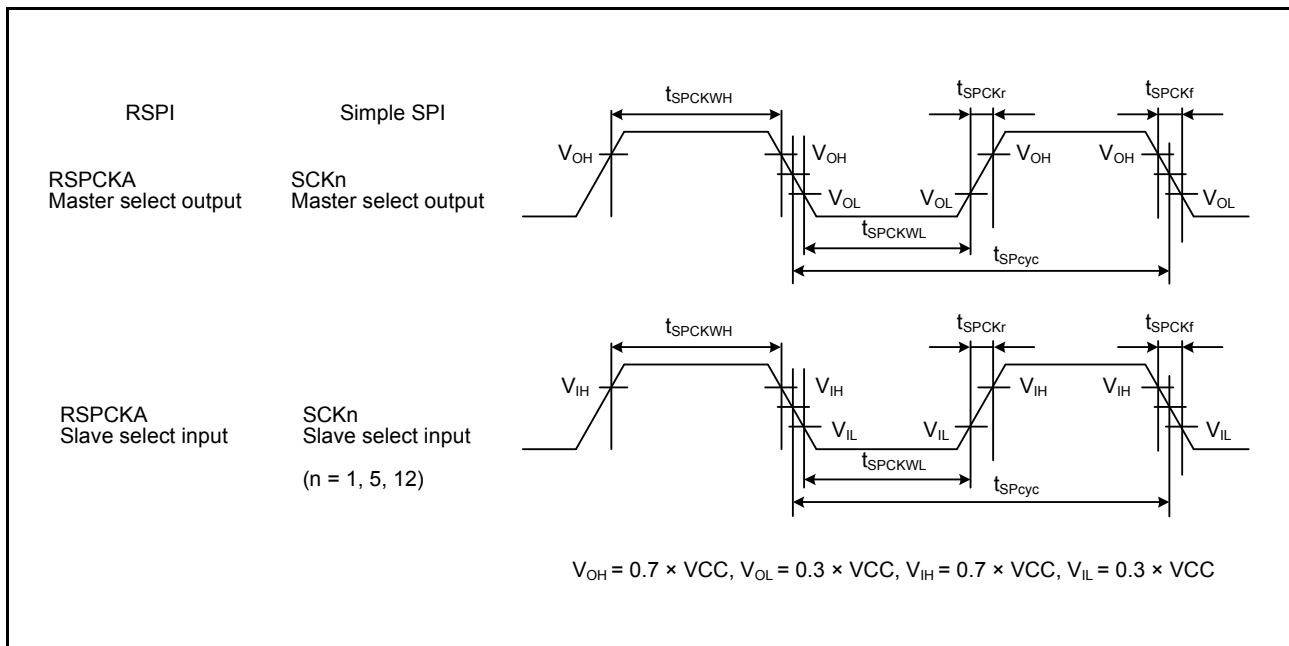


Figure 5.46 RSPI Clock Timing and Simple SPI Clock Timing

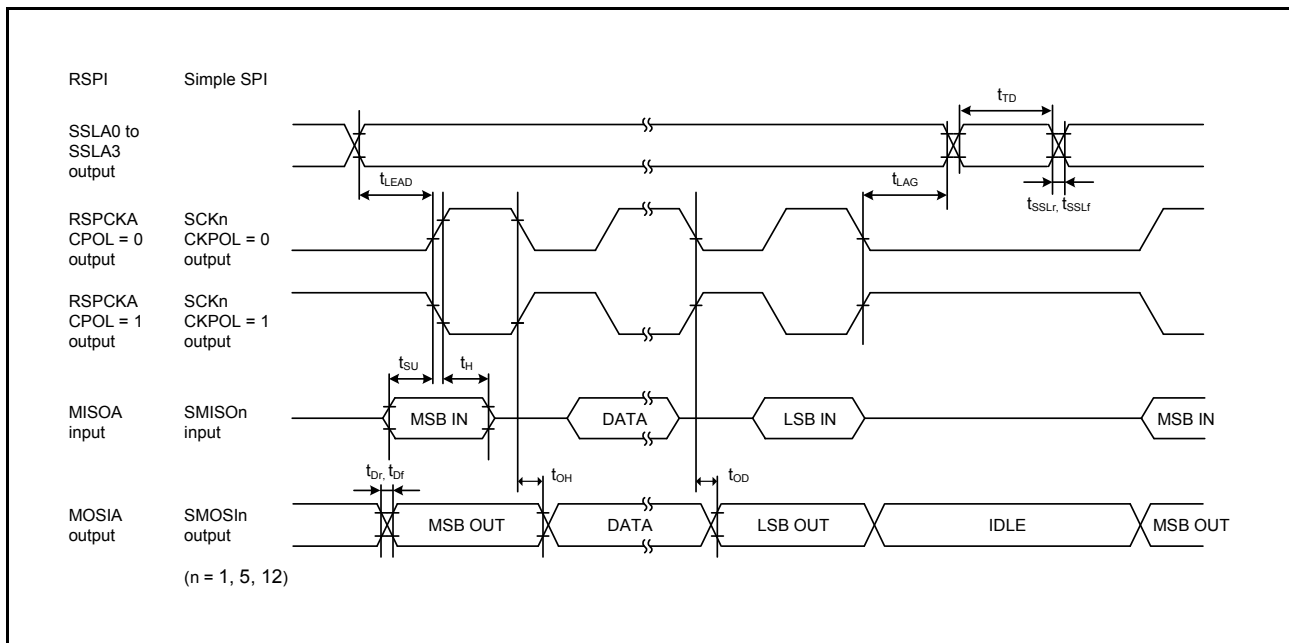


Figure 5.47 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 1)



Figure 5.48 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2)



Figure 5.49 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 0)



Figure 5.50 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Divided by 2)



Figure 5.51 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

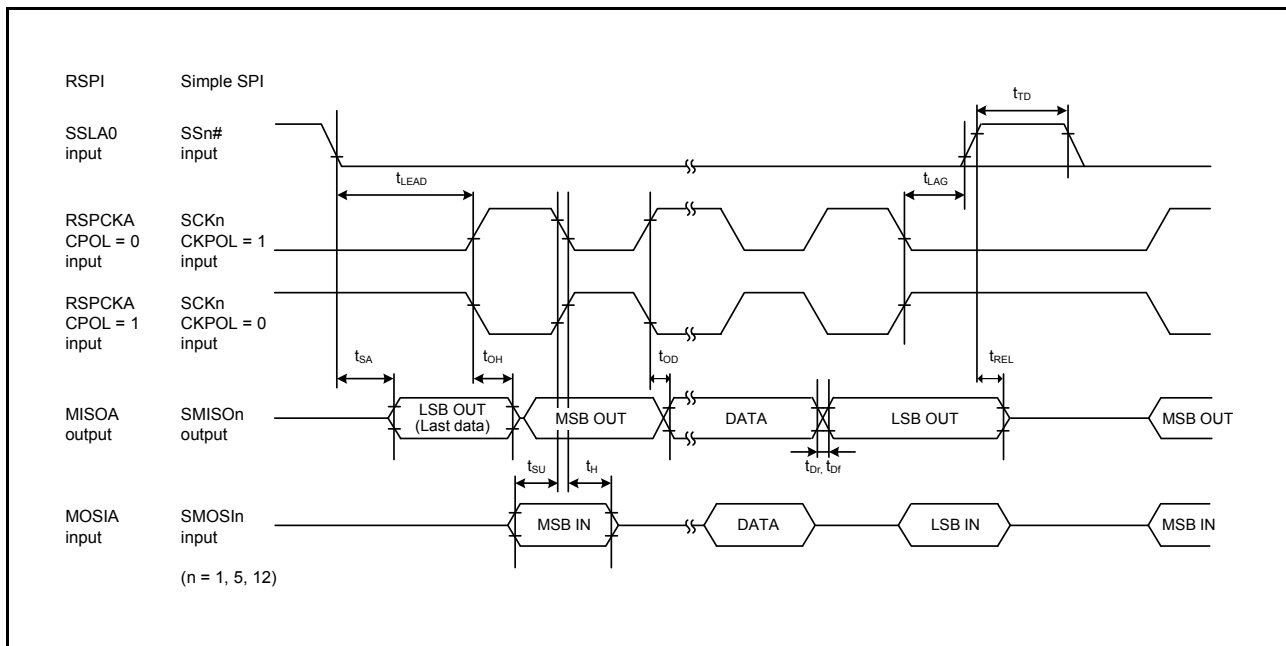


Figure 5.52 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

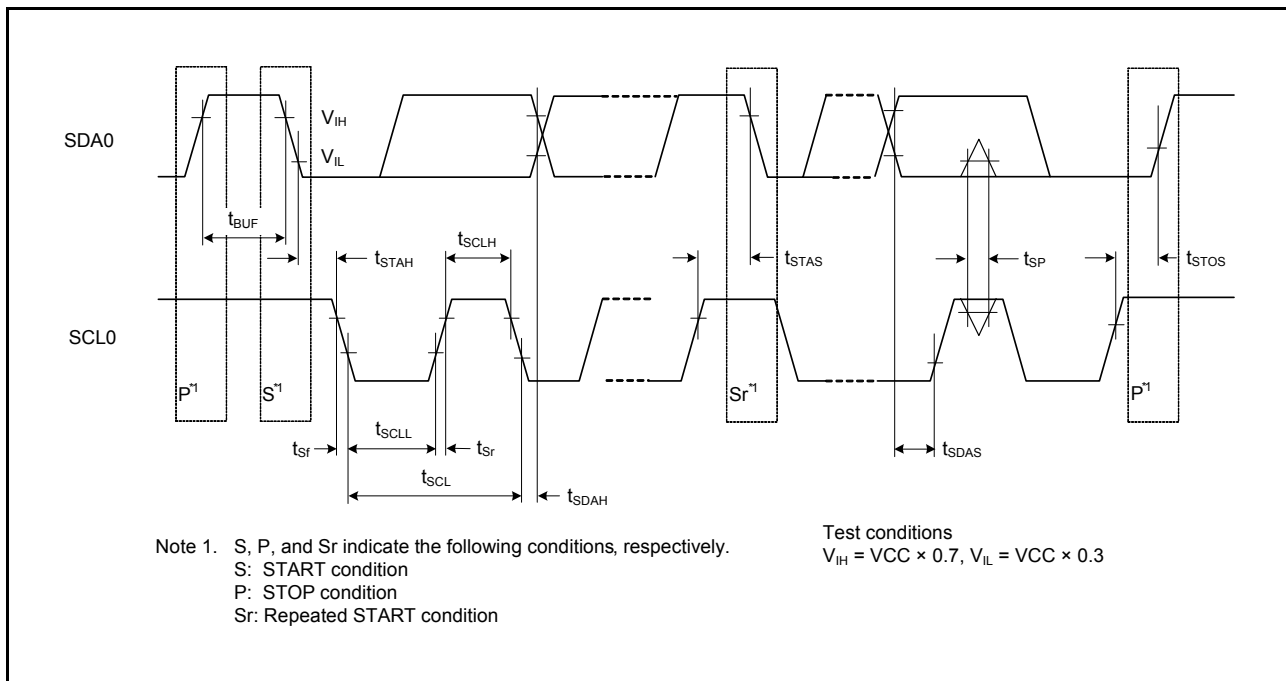


Figure 5.53 I2C Bus Interface Input/Output Timing and Simple I2C Bus Interface Input/Output Timing

5.4 USB Characteristics

Table 5.37 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics)

Conditions: $3.0\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $3.0\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Symbol | Min. | Max. | Unit | Test Conditions | |
|--|----------------------------------|----------------|------------------|------------------|---------------|------------------------------------|---|
| Input characteristics | Input high level voltage | V_{IH} | 2.0 | — | V | | |
| | Input low level voltage | V_{IL} | — | 0.8 | V | | |
| | Differential input sensitivity | V_{DI} | 0.2 | — | V | USB0_DP – USB0_DM | |
| | Differential common mode range | V_{CM} | 0.8 | 2.5 | V | | |
| Output characteristics | Output high level voltage | V_{OH} | 2.8 | VCC_USB | V | $I_{OH} = -200\ \mu\text{A}$ | |
| | Output low level voltage | V_{OL} | 0.0 | 0.3 | V | $I_{OL} = 2\ \text{mA}$ | |
| | Cross-over voltage | | V_{CRS} | 1.3 | 2.0 | V | Figure 5.54 Figure 5.55 |
| | Rise time | FS | t_r | 4 | 20 | ns | |
| | | LS | | 75 | 300 | | |
| | Fall time | FS | t_f | 4 | 20 | ns | |
| | | LS | | 75 | 300 | | |
| | Rise/fall time ratio | FS | t_r/t_f | 90 | 111.11 | % | |
| | | LS | | 80 | 125 | | |
| | Output resistance | | Z_{DRV} | 28 | 44 | Ω | (Adjusting the resistance of external elements is not necessary.) |
| VBUS characteristics | VBUS input voltage | V_{IH} | $VCC \times 0.8$ | — | V | | |
| | | V_{IL} | — | $VCC \times 0.2$ | V | | |
| | VBUS (P16) input leakage current | $ I_{VBUSIN} $ | — | 10 | μA | USB0_VBUS = 5.5V | |
| Pull-up, pull-down | Pull-down resistor | R_{PD} | 14.25 | 24.80 | k Ω | | |
| | Pull-up resistor | R_{PUI} | 0.9 | 1.575 | k Ω | During idle state | |
| | | R_{PUA} | 1.425 | 3.09 | k Ω | During reception | |
| Battery Charging Specification Ver 1.2 | USB0_DP sink current | I_{DP_SINK} | 25 | 175 | μA | | |
| | USB0_DM sink current | I_{DM_SINK} | 25 | 175 | μA | | |
| | DCD source current | I_{DP_SRC} | 7 | 13 | μA | | |
| | Data detection voltage | V_{DAT_REF} | 0.25 | 0.4 | V | | |
| | USB0_DP source current | V_{DP_SRC} | 0.5 | 0.7 | V | Output current = 250 μA | |
| | USB0_DM source current | V_{DM_SRC} | 0.5 | 0.7 | V | Output current = 250 μA | |

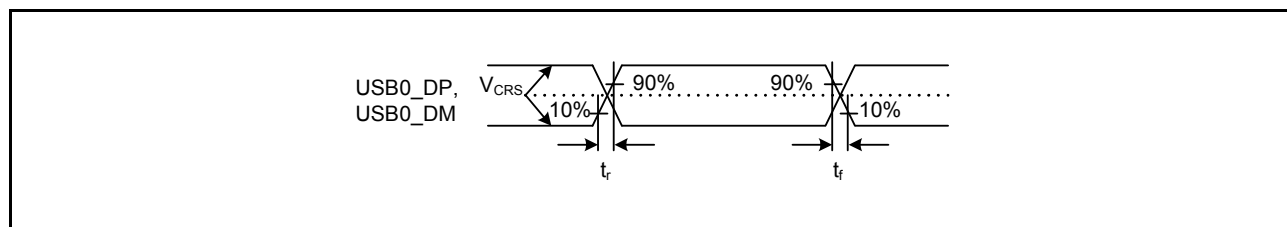


Figure 5.54 USB0_DP and USB0_DM Output Timing



Figure 5.55 Test Circuit

5.5 A/D Conversion Characteristics

Table 5.38 A/D Conversion Characteristics (1)

Conditions: $2.7\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $2.7\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $2.7\text{ V} \leq V_{REFH0} \leq AV_{CC0}$,
 $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|--|--------------------|------------|-----------|---------------|--|
| Frequency | | 4 | — | 32 | MHz | |
| Resolution | | — | — | 12 | Bit | |
| Conversion time*1 (Operation at PCLKD = 32 MHz) | Permissible signal source impedance (Max.) = 0.3 k Ω | 1.031 (0.313)*2 | — | — | μs | High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 09h |
| | | 1.375 (0.641)*2 | — | — | | Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 14h |
| Analog input effective range | | 0 | — | VREFH0 | V | |
| Offset error | | — | ± 0.5 | ± 4.5 | LSB | High-precision channel PJ6PFS.ASEL bit = 1 PJ7PFS.ASEL bit = 1 |
| | | | | ± 6.0 | LSB | Other than above |
| Full-scale error | | — | ± 0.75 | ± 4.5 | LSB | High-precision channel PJ6PFS.ASEL bit = 1 PJ7PFS.ASEL bit = 1 |
| | | | | ± 6.0 | LSB | Other than above |
| Quantization error | | — | ± 0.5 | — | LSB | |
| Absolute accuracy | | — | ± 1.25 | ± 5.0 | LSB | High-precision channel PJ6PFS.ASEL bit = 1 PJ7PFS.ASEL bit = 1 |
| | | | | ± 8.0 | LSB | Other than above |
| DNL differential nonlinearity error | | — | ± 1.0 | — | LSB | |
| INL integral nonlinearity error | | — | ± 1.0 | ± 3.0 | LSB | |

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.



Figure 5.56 AVCC0 to AVREFH0 Voltage Range

Table 5.39 A/D Conversion Characteristics (2)

Conditions: $2.4\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $2.4\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $2.4\text{ V} \leq V_{REFH0} \leq AV_{CC0}$, $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

| Item | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|--|--------------------|------------|-----------|---------------|--|
| Frequency | | 4 | — | 16 | MHz | |
| Resolution | | — | — | 12 | Bit | |
| Conversion time*1 (Operation at PCLKD = 16 MHz) | Permissible signal source impedance (Max.) = 1.0 k Ω | 2.062 (0.625)*2 | — | — | μs | High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 09h |
| | | 2.750 (1.313)*2 | — | — | μs | Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn.SST[7:0] bits = 14h |
| Analog input effective range | | 0 | — | VREFH0 | V | |
| Offset error | | — | ± 0.5 | ± 6.0 | LSB | |
| Full-scale error | | — | ± 1.25 | ± 6.0 | LSB | |
| Quantization error | | — | ± 0.5 | — | LSB | |
| Absolute accuracy | | — | ± 3.0 | ± 8.0 | LSB | |
| DNL differential nonlinearity error | | — | ± 1.0 | — | LSB | |
| INL integral nonlinearity error | | — | ± 1.5 | ± 3.0 | LSB | |

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.40 A/D Conversion Characteristics (3)

Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $1.8\text{ V} \leq V_{REFH0} \leq AV_{CC0}$, $V_{SS} = AV_{SS0} = V_{REFL0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

| Item | | Min. | Typ. | Max. | Unit | Test Conditions |
|--|--|--------------------|------------|------------|---------------|--|
| Frequency | | 1 | — | 8 | MHz | |
| Resolution | | — | — | 12 | Bit | |
| Conversion time*1 (Operation at PCLKD = 8 MHz) | Permissible signal source impedance (Max.) = 5.0 k Ω | 4.875 (1.250)*2 | — | — | μs | High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 09h |
| | | 6.250 (2.625)*2 | — | — | μs | Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 14h |
| Analog input effective range | | 0 | — | VREFH0 | V | |
| Offset error | | — | ± 0.5 | ± 24.0 | LSB | |
| Full-scale error | | — | ± 1.25 | ± 24.0 | LSB | |
| Quantization error | | — | ± 0.5 | — | LSB | |
| Absolute accuracy | | — | ± 2.75 | ± 32.0 | LSB | |
| DNL differential nonlinearity error | | — | ± 1.0 | — | LSB | |
| INL integral nonlinearity error | | — | ± 1.25 | ± 12.0 | LSB | |

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.41 A/D Converter Channel Classification

| Classification | Channel | Conditions | Remarks |
|--|----------------------------|----------------------|---|
| High-precision channel | AN000 to AN004, AN006 | AVCC0 = 1.8 to 3.6 V | Pins AN000 to AN004 and AN006 cannot be used as digital outputs when the A/D converter is in use. |
| Normal-precision channel | AN008 to AN015 | | |
| Internal reference voltage input channel | Internal reference voltage | AVCC0 = 2.0 to 3.6 V | |
| Temperature sensor input channel | Temperature sensor output | AVCC0 = 2.0 to 3.6 V | |

Table 5.42 A/D Internal Reference Voltage Characteristics

Conditions: $2.0\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $2.0\text{ V} \leq AVCC0 \leq 3.6\text{ V}^*1$, $VSS = AVSS0 = VREFL0 = VSS_USB = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|--|------|------|------|------|-----------------|
| Internal reference voltage input channel*2 | 1.36 | 1.43 | 1.50 | V | |

Note 1. The internal reference voltage cannot be selected for input channels when $AVCC0 < 2.0\text{ V}$.

Note 2. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.



Figure 5.57 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage ($V_{REFH0} = 3.072 \text{ V}$), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = $\pm 5 \text{ LSB}$ means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.6 D/A Conversion Characteristics

Table 5.43 D/A Conversion Characteristics

Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVCC0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $fPCLKB \leq 32\text{ MHz}$,
 $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------------|------------------------------------|------|-----------|---------------|-----------------------------|
| Resolution | — | — | 8 | Bit | |
| Conversion time | $VCC = 2.7\text{ to }3.6\text{ V}$ | — | 3.0 | μs | 35-pF capacitive load |
| | $VCC = 1.6\text{ to }2.7\text{ V}$ | — | 6.0 | | |
| Absolute accuracy | $VCC = 2.4\text{ to }3.6\text{ V}$ | — | ± 3.0 | LSB | 2-M Ω resistive load |
| | $VCC = 1.8\text{ to }2.4\text{ V}$ | — | ± 3.5 | | |
| | $VCC = 2.4\text{ to }3.6\text{ V}$ | — | ± 2.0 | LSB | 4-M Ω resistive load |
| | $VCC = 1.8\text{ to }2.4\text{ V}$ | — | ± 2.5 | | |
| RO output resistance | — | 6.4 | — | k Ω | |

5.7 Temperature Sensor Characteristics

Table 5.44 Temperature Sensor Characteristics

Conditions: $2.0\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $2.0\text{ V} \leq AVCC0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--|--------------------|------|-----------|------|----------------------|----------------------|
| Relative accuracy | — | — | ± 1.5 | — | $^\circ\text{C}$ | 2.4 V or above |
| | | — | ± 2.0 | — | | Below 2.4 V |
| Temperature slope | — | — | -3.65 | — | mV/ $^\circ\text{C}$ | |
| Output voltage (at 25 $^\circ\text{C}$) | — | — | 1.05 | — | V | $VCC = 3.3\text{ V}$ |
| Temperature sensor start time | t_{START} | — | — | 5 | μs | |
| Sampling time | — | 5 | — | — | μs | |

5.8 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.45 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|-------------------------|------------------------------------|---------------|------|------|------|-----------------|------------------------------------|
| Voltage detection level | Power-on reset (POR) | V_{POR} | 1.35 | 1.50 | 1.65 | V | Figure 5.58, Figure 5.59 |
| | Voltage detection circuit (LVD1)*1 | V_{det1_4} | 3.00 | 3.10 | 3.20 | V | Figure 5.60 At falling edge VCC |
| V_{det1_5} | | 2.91 | 3.00 | 3.09 | | | |
| V_{det1_6} | | 2.81 | 2.90 | 2.99 | | | |
| V_{det1_7} | | 2.70 | 2.79 | 2.88 | | | |
| V_{det1_8} | | 2.60 | 2.68 | 2.76 | | | |
| V_{det1_9} | | 2.50 | 2.58 | 2.66 | | | |
| V_{det1_A} | | 2.40 | 2.48 | 2.56 | | | |
| V_{det1_B} | | 1.99 | 2.06 | 2.13 | | | |
| V_{det1_C} | | 1.90 | 1.96 | 2.02 | | | |
| | V_{det1_D} | 1.80 | 1.86 | 1.92 | | | |

Note: • These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol V_{det1_n} denotes the value of the LVDLVL[3:0] bits.

Table 5.46 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)Conditions: $1.8\text{ V} \leq V_{CC} = V_{CC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{CC0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$, $T_a = -40$ to $+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|--|------------------|------|------|------|-----------------|--|
| Voltage detection level | Voltage detection circuit (LVD2)*1 | V_{det2_0} | 2.71 | 2.90 | 3.09 | V | Figure 5.61 At falling edge VCC |
| | | V_{det2_1} | 2.43 | 2.60 | 2.77 | | |
| | | V_{det2_2} | 1.87 | 2.00 | 2.13 | | |
| | | V_{det2_3} *2 | 1.69 | 1.80 | 1.91 | | |
| Wait time after power-on reset cancellation | At normal startup*3 | t_{POR} | — | 9.1 | — | ms | Figure 5.59 |
| | During fast startup time*4 | t_{POR} | — | 1.6 | — | | |
| Wait time after voltage monitoring 1 reset cancellation | Power-on voltage monitoring 1 reset disabled*3 | t_{LVD1} | — | 568 | — | μs | Figure 5.60 |
| | Power-on voltage monitoring 1 reset enabled*4 | | — | 100 | — | | |
| Wait time after voltage monitoring 2 reset cancellation | | t_{LVD2} | — | 100 | — | μs | Figure 5.61 |
| Response delay time | | t_{det} | — | — | 350 | μs | Figure 5.58 |
| Minimum VCC down time*5 | | t_{VOFF} | 350 | — | — | μs | Figure 5.58, VCC = 1.0 V or above |
| Power-on reset enable time | | $t_{W(POR)}$ | 1 | — | — | ms | Figure 5.59, VCC = below 1.0 V |
| LVD operation stabilization time (after LVD is enabled) | | $T_{d(E-A)}$ | — | — | 300 | μs | Figure 5.60, Figure 5.61 |
| Hysteresis width (LVD1 and LVD2) | | V_{LVH} | — | 70 | — | mV | Vdet1_4 selected |
| | | | — | 60 | — | | Vdet1_5 to 9, LVD2 selected |
| | | | — | 50 | — | | When selection is from among Vdet1_A to B. |
| | | | — | 40 | — | | When selection is from among Vdet1_C to D. |

Note: • These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol V_{det2_n} denotes the value of the LVDLVL[3:0] bits.

Note 2. V_{det2_3} selection can be used only when the CMPA2 pin input voltage is selected and cannot be used when the power supply voltage (VCC) is selected.

Note 3. When OFS1.(STUPLVD1REN, FASTSTUP) = 11b.

Note 4. When OFS1.(STUPLVD1REN, FASTSTUP) \neq 11b.

Note 5. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det0} , V_{det1} , and V_{det2} for the POR/LVD.

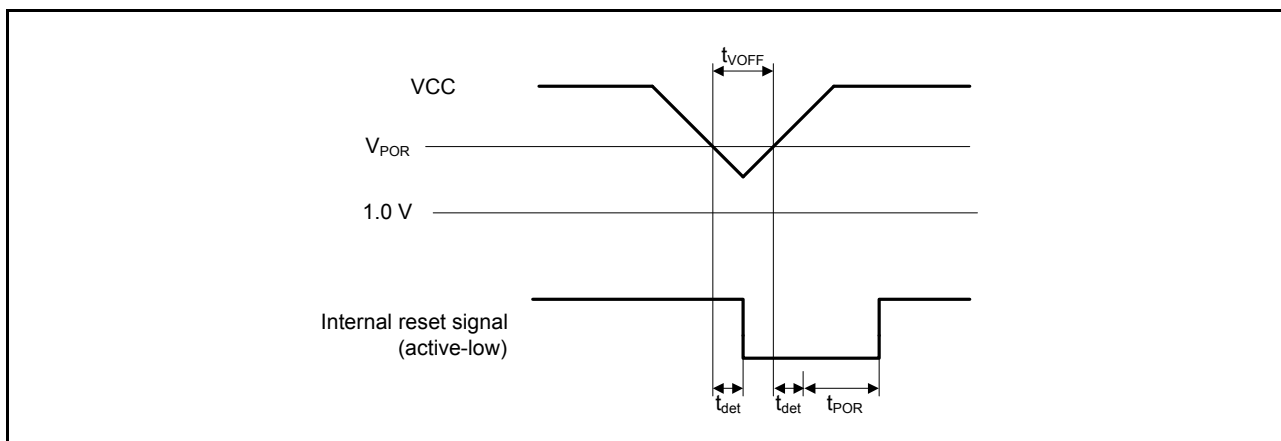
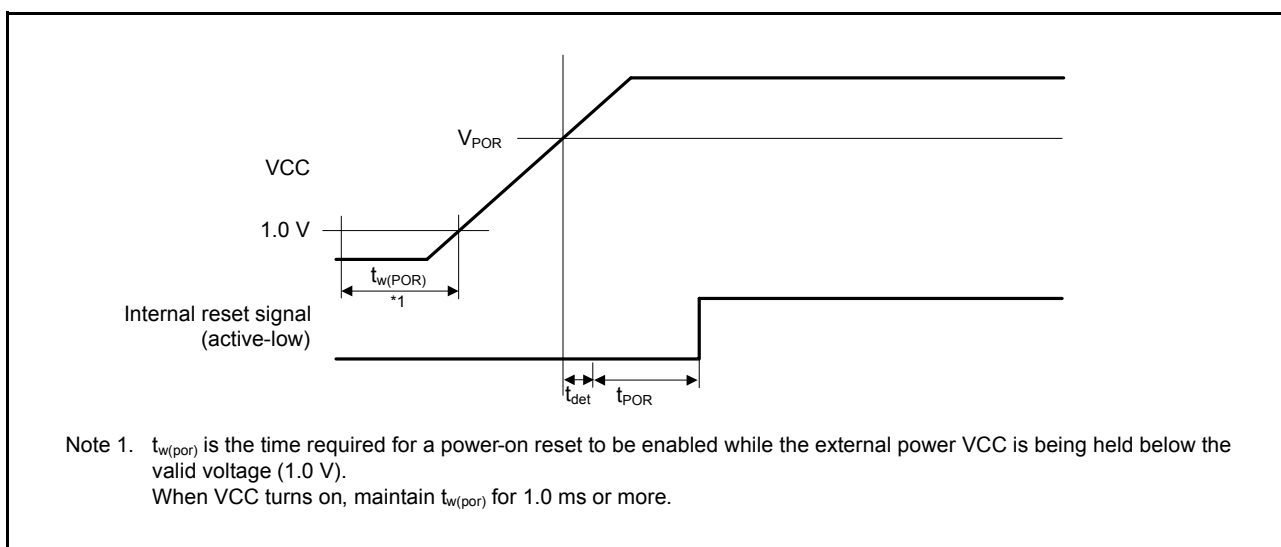


Figure 5.58 Voltage Detection Reset Timing



Note 1. t_{w(por)} is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain t_{w(por)} for 1.0 ms or more.

Figure 5.59 Power-On Reset Timing

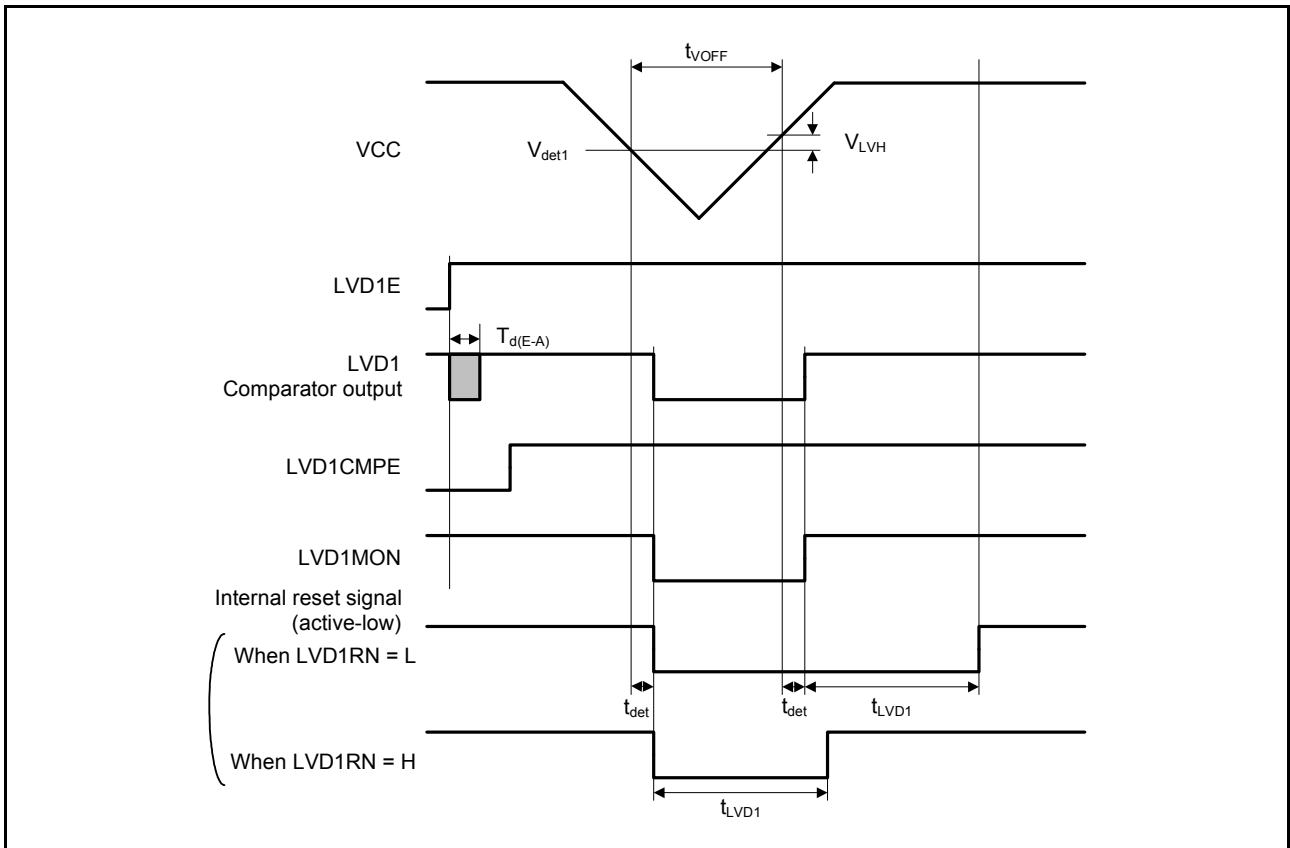


Figure 5.60 Voltage Detection Circuit Timing (V_{det1})

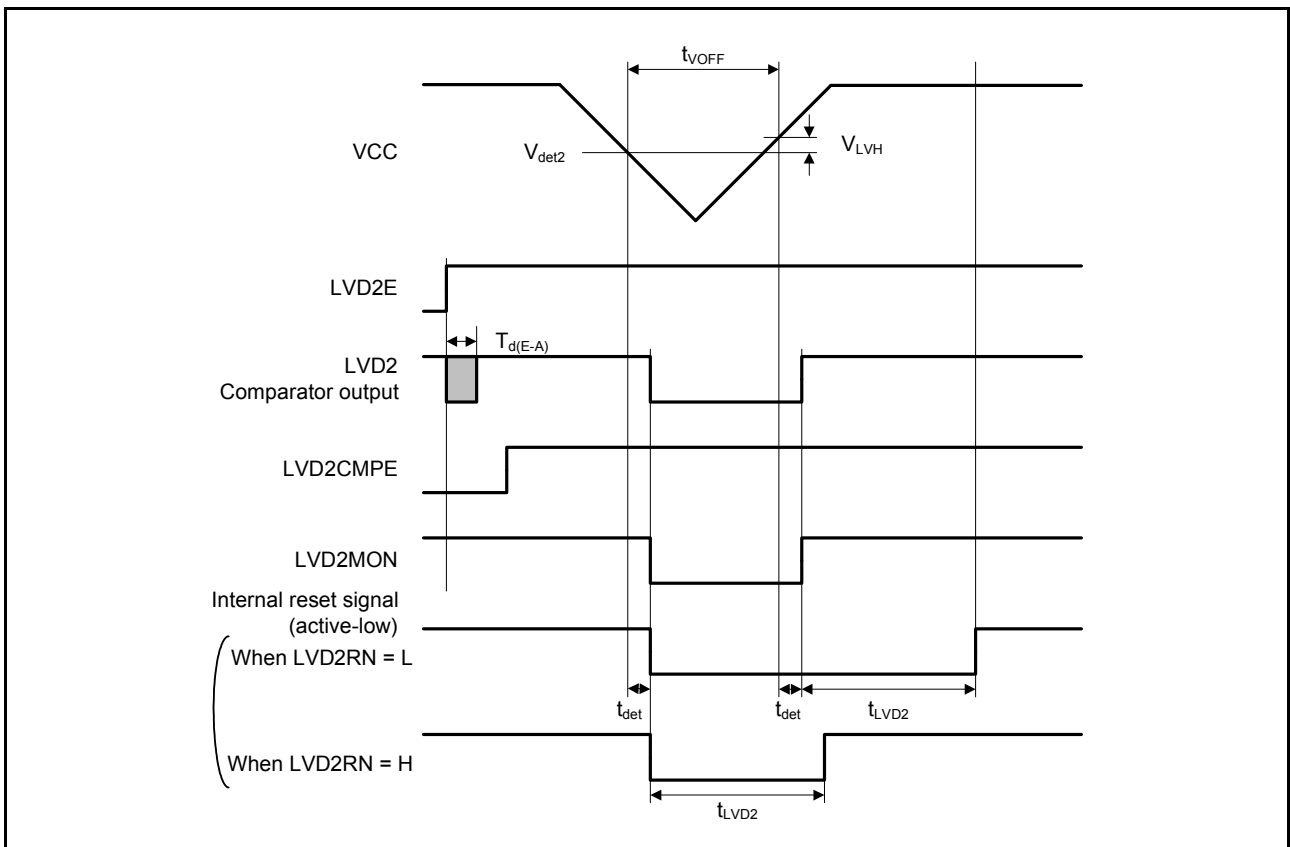


Figure 5.61 Voltage Detection Circuit Timing (V_{det2})

5.9 Oscillation Stop Detection Timing

Table 5.47 Oscillation Stop Detection Circuit Characteristics

Conditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------|----------|------|------|------|------|-----------------|
| Detection time | t_{dr} | — | — | 1 | ms | Figure 5.62 |

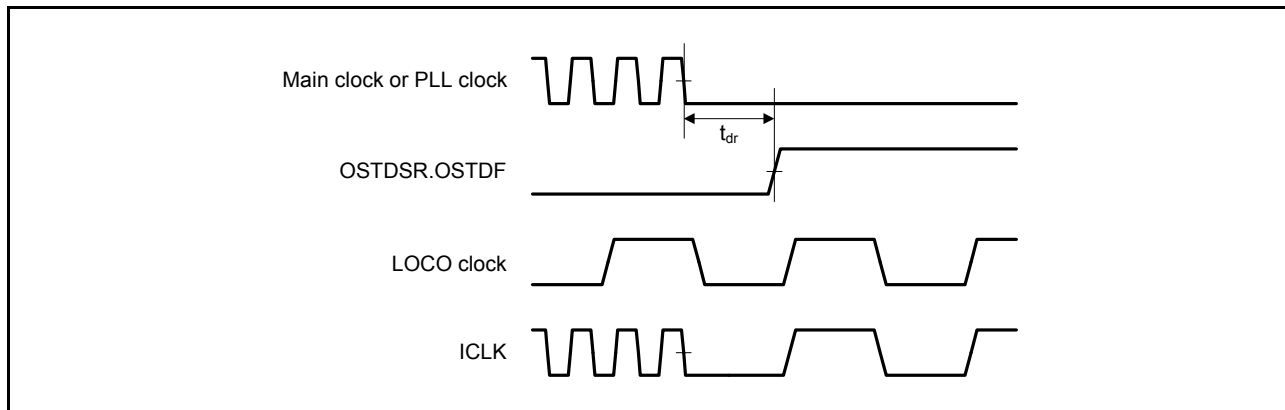


Figure 5.62 Oscillation Stop Detection Timing

5.10 ROM (Flash Memory for Code Storage) Characteristics

Table 5.48 ROM (Flash Memory for Code Storage) Characteristics (1)

| Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|-------------------------------|-------------------------------|-----------|----------|------|-------|---------------------------|
| Reprogramming/erasure cycle*1 | N_{PEC} | 1000 | — | — | Times | |
| Data hold time | After 1000 times of N_{PEC} | t_{DRP} | 20*2, *3 | — | Year | $T_a = +85^\circ\text{C}$ |

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 1000$), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 5.49 ROM (Flash Memory for Code Storage) Characteristics (2)

High-speed operating mode Conditions: $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $2.7\text{ V} \leq AVSS0 \leq 3.6\text{ V}$, $V_{SS} = AVSS0 = V_{SS_USB} = 0\text{ V}$

Temperature range for the programming/erasure operation: $T_a = -40$ to $+105^\circ\text{C}$

| Item | Symbol | FCLK = 1 MHz | | | FCLK = 32 MHz | | | Unit | |
|--------------------------------------|-----------|--------------|------|------|---------------|------|------|-------|---------------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Programming time | 4-byte | t_{P4} | — | 103 | 931 | — | 52 | 489 | μs |
| Erasure time | 1-Kbyte | t_{E1K} | — | 8.23 | 267 | — | 5.48 | 214 | ms |
| | 256-Kbyte | t_{E256K} | — | 407 | 925 | — | 39 | 457 | ms |
| Blank check time | 4-byte | t_{BC4} | — | — | 48 | — | — | 15.9 | μs |
| | 1-Kbyte | t_{BC1K} | — | — | 1.58 | — | — | 0.127 | ms |
| Erase operation forcible stop time | | t_{SED} | — | — | 21.6 | — | — | 12.8 | μs |
| Start-up area switching setting time | | t_{SAS} | — | 12.6 | 543 | — | 6.16 | 432 | ms |
| Access window time | | t_{AWS} | — | 12.6 | 543 | — | 6.16 | 432 | ms |
| ROM mode transition wait time 1 | | t_{DIS} | 2 | — | — | 2 | — | — | μs |
| ROM mode transition wait time 2 | | t_{MS} | 5 | — | — | 5 | — | — | μs |

Note: • Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: • The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: • The frequency accuracy of FCLK should be $\pm 3.5\%$. Confirm the frequency accuracy of the clock source.

Table 5.50 ROM (Flash Memory for Code Storage) Characteristics (3)Middle-speed operating mode Conditions: $1.8\text{ V} \leq \text{VCC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVSS0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$ Temperature range for the programming/erasure operation: $T_a = -40$ to $+85^\circ\text{C}$

| Item | | Symbol | FCLK = 1 MHz | | | FCLK = 8 MHz | | | Unit |
|--------------------------------------|-----------|-------------|--------------|------|------|--------------|------|-------|---------------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time | 4-byte | t_{P4} | — | 143 | 1330 | — | 96.8 | 932 | μs |
| Erasure time | 1-Kbyte | t_{E1K} | — | 8.3 | 269 | — | 5.85 | 219 | ms |
| | 256-Kbyte | t_{E256K} | — | 407 | 928 | — | 93 | 520 | ms |
| Blank check time | 4-byte | t_{BC4} | — | — | 78 | — | — | 50 | μs |
| | 1-Kbyte | t_{BC1K} | — | — | 1.61 | — | — | 0.369 | ms |
| Erase operation forcible stop time | | t_{SED} | — | — | 33.6 | — | — | 25.6 | μs |
| Start-up area switching setting time | | t_{SAS} | — | 13.2 | 549 | — | 7.6 | 445 | ms |
| Access window time | | t_{AWS} | — | 13.2 | 549 | — | 7.6 | 445 | ms |
| ROM mode transition wait time 1 | | t_{DIS} | 2 | — | — | 2 | — | — | μs |
| ROM mode transition wait time 2 | | t_{MS} | 3 | — | — | 3 | — | — | μs |

Note: • Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: • The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: • The frequency accuracy of FCLK should be $\pm 3.5\%$. Confirm the frequency accuracy of the clock source.

5.11 E2 DataFlash Characteristics

Table 5.51 E2 DataFlash Characteristics (1)

| Item | | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|-------------------------------|-----------------------------------|------------|----------|---------|------|-------|-----------------------------|
| Reprogramming/erasure cycle*1 | | N_{DPEC} | 100000 | 1000000 | — | Times | |
| Data hold time | After 10000 times of N_{DPEC} | t_{DDRP} | 20*2, *3 | — | — | Year | $T_a = +85^{\circ}\text{C}$ |
| | After 100000 times of N_{DPEC} | | 5*2, *3 | — | — | Year | |
| | After 1000000 times of N_{DPEC} | | — | 1*2, *3 | — | Year | $T_a = +25^{\circ}\text{C}$ |

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 100000$), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in 1-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristics when using the flash memory programmer and the self-programming library provided from Renesas Electronics.

Note 3. These results are obtained from reliability testing.

**Table 5.52 E2 DataFlash Characteristics (2)
: high-speed operating mode**

Conditions: $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $2.7\text{ V} \leq AV_{SS0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$

Temperature range for the programming/erasure operation: $T_a = -40$ to $+105^{\circ}\text{C}$

| Item | | Symbol | FCLK = 1 MHz | | | FCLK = 32 MHz | | | Unit |
|------------------------------------|---------|-------------|--------------|------|------|---------------|------|-------|---------------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time | 1-byte | t_{DP1} | — | 86 | 761 | — | 40.5 | 374 | μs |
| Erasure time | 1-Kbyte | t_{DE1K} | — | 17.4 | 456 | — | 6.15 | 228 | ms |
| | 8-Kbyte | t_{DE8K} | — | 60.4 | 499 | — | 9.3 | 231 | ms |
| Blank check time | 1-byte | t_{DBC1} | — | — | 48 | — | — | 15.9 | μs |
| | 1-Kbyte | t_{DBC1K} | — | — | 1.58 | — | — | 0.127 | μs |
| Erase operation forcible stop time | | t_{DSED} | — | — | 21.5 | — | — | 12.8 | μs |
| DataFlash STOP recovery time | | t_{DSTOP} | 5 | — | — | 5 | — | — | μs |

Note: • Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: • The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: • The frequency accuracy of FCLK should be $\pm 3.5\%$. Confirm the frequency accuracy of the clock source.

**Table 5.53 E2 DataFlash Characteristics (3)
: middle-speed operating mode**

Conditions: $1.8\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, $1.8\text{ V} \leq AV_{SS0} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS0} = V_{SS_USB} = 0\text{ V}$

Temperature range for the programming/erasure operation: $T_a = -40$ to $+85^{\circ}\text{C}$

| Item | | Symbol | FCLK = 1 MHz | | | FCLK = 8 MHz | | | Unit |
|------------------------------------|---------|-------------|--------------|------|------|--------------|------|-------|---------------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time | 1-byte | t_{DP1} | — | 126 | 1160 | — | 85.4 | 818 | μs |
| Erasure time | 1-Kbyte | t_{DE1K} | — | 17.5 | 457 | — | 7.76 | 259 | ms |
| | 8-Kbyte | t_{DE8K} | — | 60.5 | 500 | — | 16.7 | 267.6 | ms |
| Blank check time | 1-byte | t_{DBC1} | — | — | 78 | — | — | 50 | μs |
| | 1-Kbyte | t_{DBC1K} | — | — | 1.61 | — | — | 0.369 | ms |
| Erase operation forcible stop time | | t_{DSED} | — | — | 33.5 | — | — | 25.5 | μs |
| DataFlash STOP recovery time | | t_{DSTOP} | 720 | — | — | 720 | — | — | ns |

Note: • Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: • The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: • The frequency accuracy of FCLK should be $\pm 3.5\%$. Confirm the frequency accuracy of the clock source.

5.12 Usage Notes

5.12.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU to adjust automatically to the optimum level. A 4.7- μF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and VSS pin. Figure 5.63 to Figure 5.64 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin. Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor to the MCU power supply pins as close as possible. Use a recommended value of 0.1 μF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 30, 12-Bit A/D Converter (S12ADb) in the User's Manual: Hardware.

For notes on designing the printed circuit board, see the descriptions of the application note "Hardware Design Guide" (R01AN1411EJ). The latest version can be downloaded from Renesas Electronics Website.



Figure 5.63 Connecting Capacitors (64 Pins)



Figure 5.64 Connecting Capacitors (48-pin LQFP)

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.



Figure A 64-Pin LFQFP (PLQP0064KB-A)

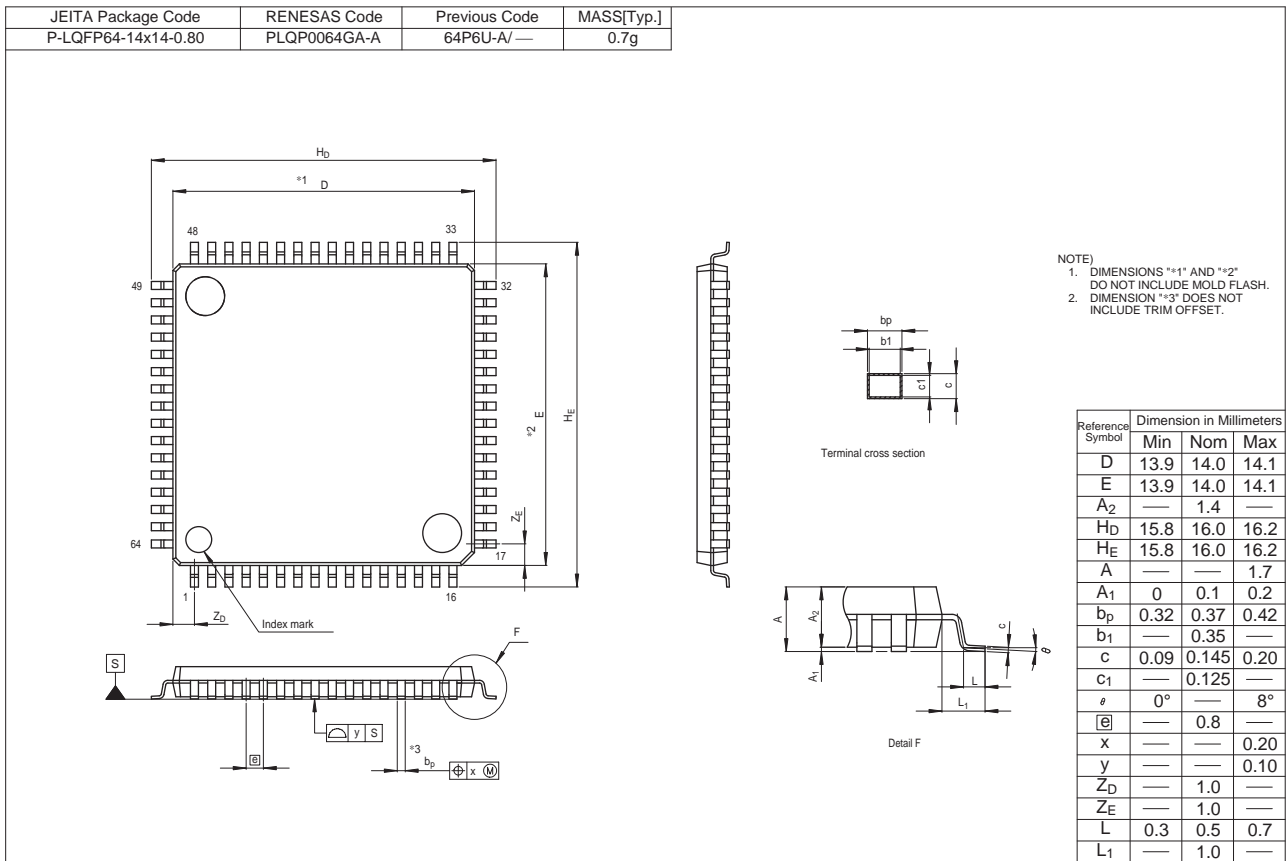


Figure B 64-Pin LQFP (PLQP0064GA-A)



Figure C 64-Pin WFLGA (PWLG0064KA-A)

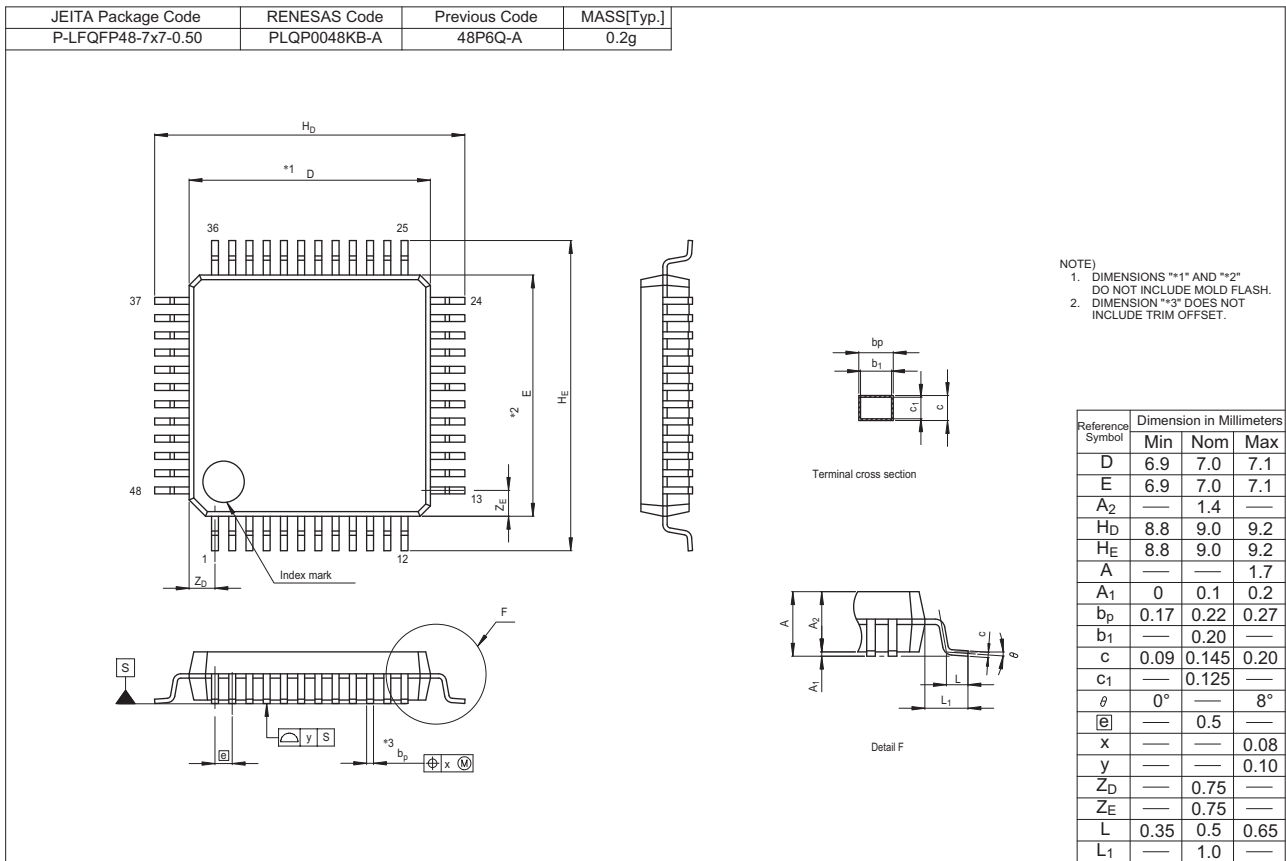


Figure D 48-Pin LFQFP (PLQP0048KB-A)

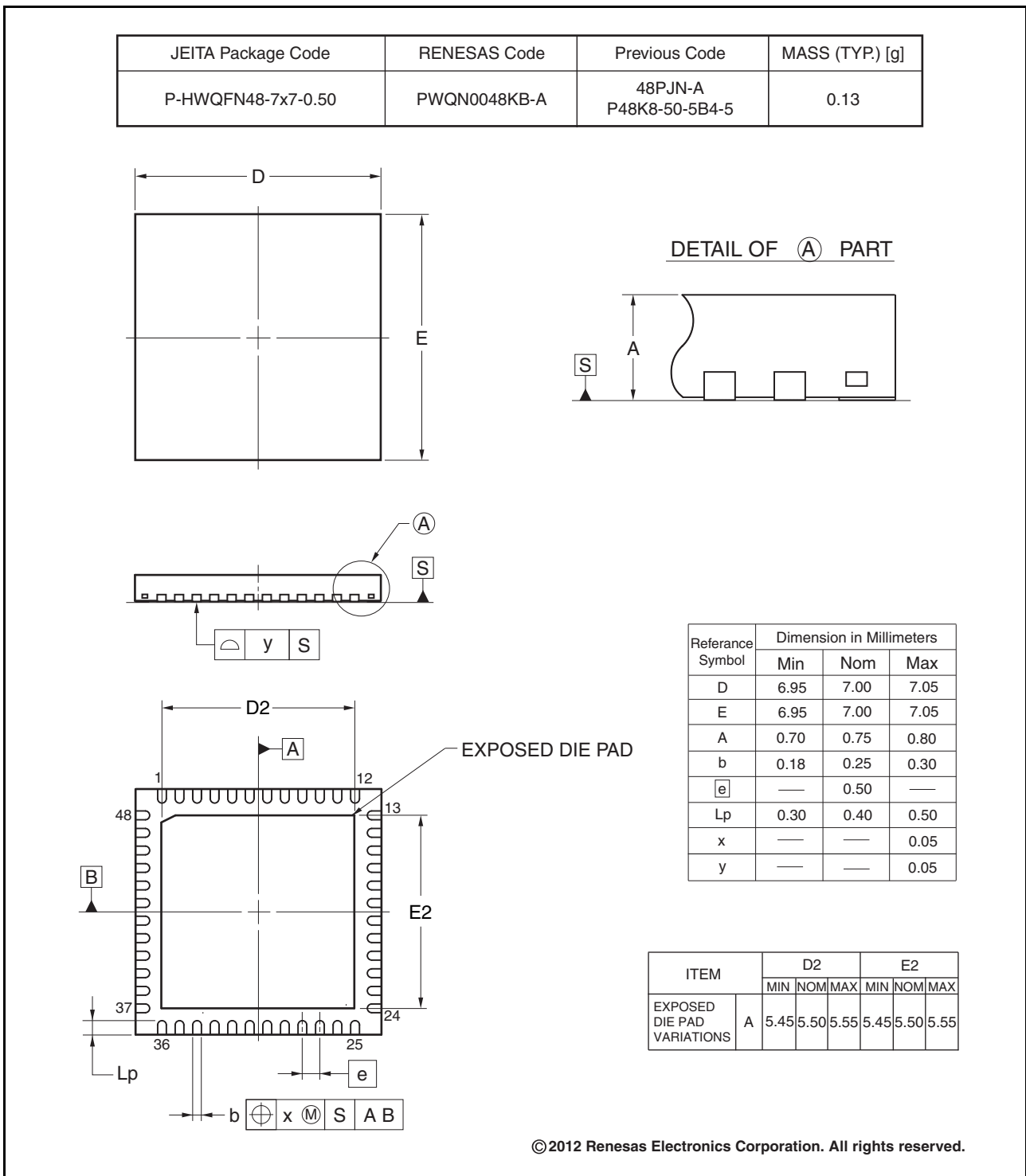


Figure E 48-Pin HWQFN (PWQN0048KB-A)

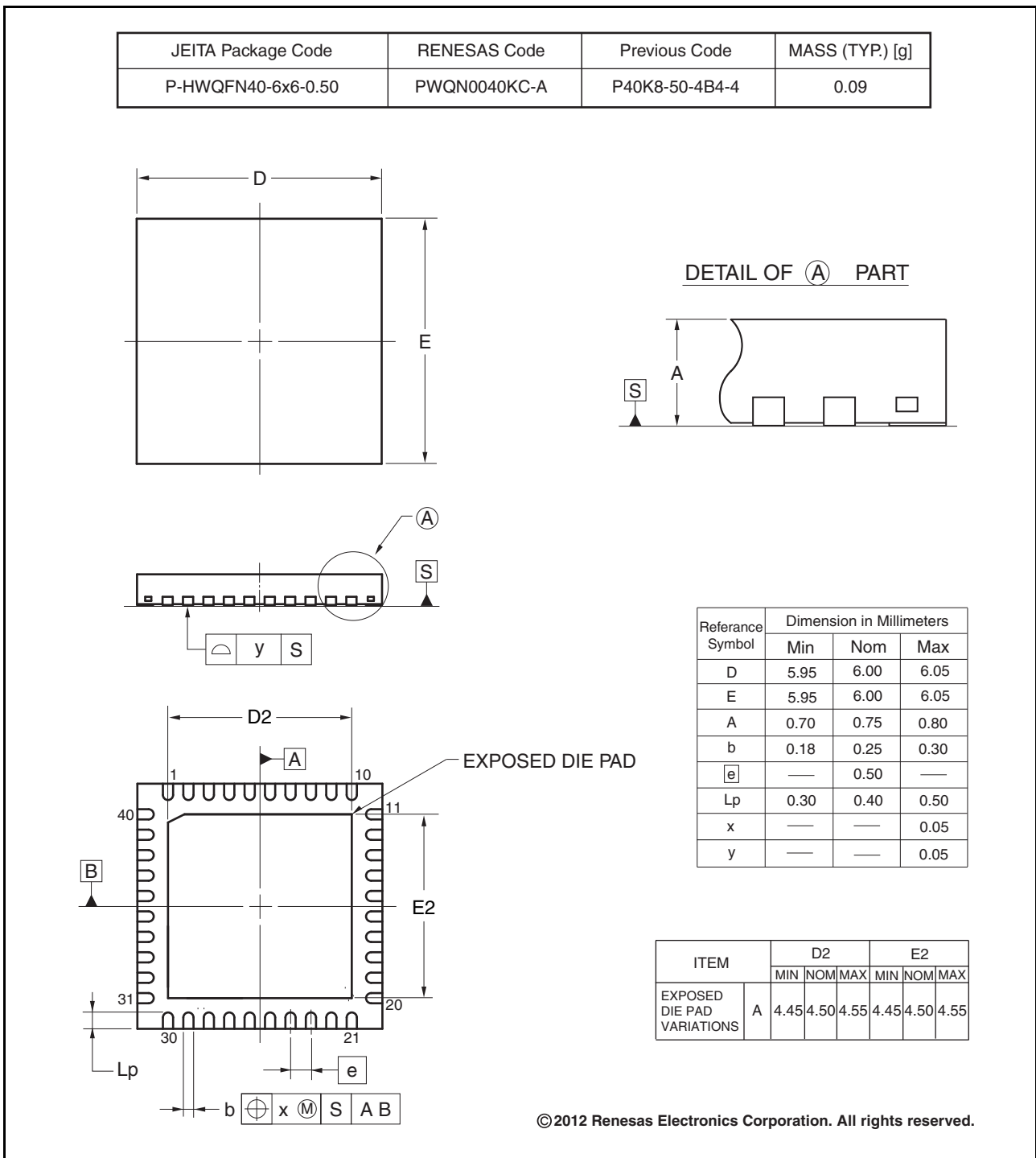


Figure F 40-Pin HWQFN (PWQN0040KC-A)

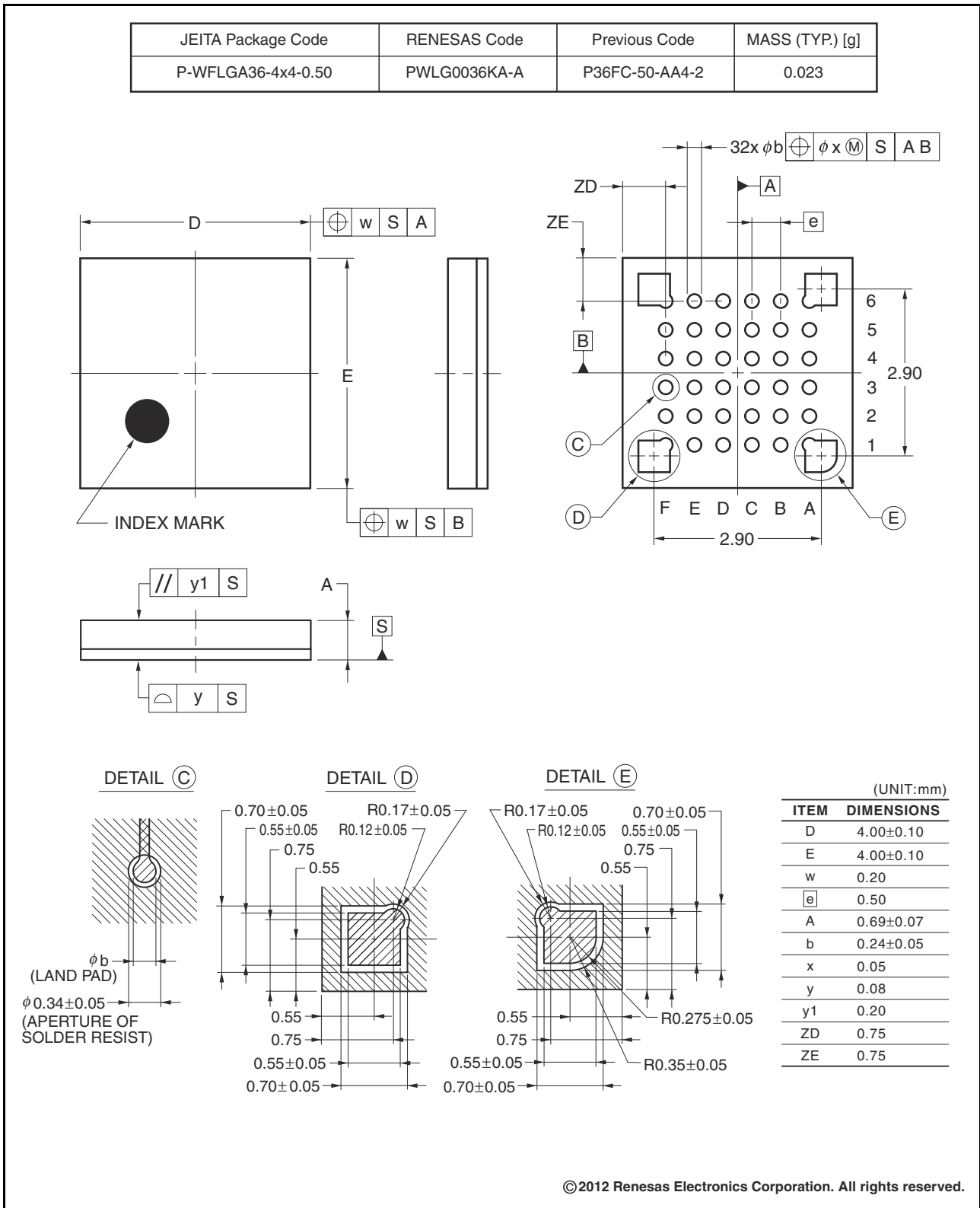


Figure G 36-Pin WFLGA (PWLG0036KA-A)

| | |
|------------------|-----------------------|
| REVISION HISTORY | RX111 Group Datasheet |
|------------------|-----------------------|

| Rev. | Date | Description | |
|----------|---|-------------------------------|--|
| | | Page | Summary |
| 0.60 | Apr 15, 2013 | — | First edition, issued |
| 0.90 | May 15, 2013 | Features | |
| | | 1 | Changed |
| | | 1. Overview | |
| | | 2 to 4 | Table 1.1 Outline of Specifications changed |
| | | 10 to 12 | Table 1.4 Pin Functions changed |
| | | 13 | Figure 1.3 Pin Assignments of the 64-Pin LQFP changed |
| | | 14 | Figure 1.4 Pin Assignments of the 64-Pin WFLGA changed |
| | | 15 | Figure 1.5 Pin Assignments of the 48-Pin LQFP/HWQFN changed |
| | | 18, 19 | Table 1.5 List of Pins and Pin Functions (64-Pin LQFP) changed, Note 1 added |
| | | 20, 21 | Table 1.6 List of Pins and Pin Functions (64-Pin WFLGA) changed, Note 1 added |
| | | 22, 23 | Table 1.7 List of Pins and Pin Functions (48-Pin LQFP/HWQFN) changed, Note 1 added |
| | | 24, 25 | Table 1.8 List of Pins and Pin Functions (40-Pin HWQFN) changed, Note 1 added |
| | | 26 | Table 1.9 List of Pins and Pin Functions (36-Pin WFLGA) changed, Note 1 added |
| | | 4. I/O Registers | |
| 33 to 48 | Table 5.1 List of I/O Registers (Address Order) changed | | |
| 1.00 | Jun 19, 2013 | 1. Overview | |
| | | 9 | Figure 1.2 Block Diagram changed |
| | | 20, 21 | Table 1.6 List of Pins and Pin Functions (64-Pin WFLGA) changed |
| | | 26 | Table 1.9 List of Pins and Pin Functions (36-Pin WFLGA) changed |
| | | 4. I/O Registers | |
| | | 33 to 48 | Table 4.1 List of I/O Registers (Address Order) changed |
| | | 5. Electrical Characteristics | |
| 49 to 99 | Added | | |
| 1.20 | Sep 29, 2014 | 1. Overview | |
| | | 2 to 4 | Table 1.1 Outline of Specifications: ROM capacity and RAM capacity changed, Unique ID added |
| | | 6, 7 | Table 1.3 List of Products, changed |
| | | 8 | Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed |
| | | 9 | Figure 1.2 Block Diagram changed |
| | | 10 | Table 1.4 Pin Functions changed |
| | | 15 | Figure 1.5 Pin Assignments of the 48-Pin LQFP/HWQFN: Note added |
| | | 16 | Figure 1.6 Pin Assignments of the 40-Pin HWQFN: Note added |
| | | 3. Address Space | |
| | | 30 | Figure 3.1 Memory Map, changed |
| | | 4. I/O Registers | |
| | | 33 to 48 | Table 4.1 List of I/O Registers (Address Order), changed |
| | | 5. Electrical Characteristics | |
| | | 49 | Table 5.1 Absolute Maximum Ratings, Table 5.2 Recommended Operating Conditions, changed |
| | | 50 | Table 5.3 DC Characteristics (1) and Table 5.4 DC Characteristics (2), changed |
| | | 51 | Table 5.5 DC Characteristics (3), changed |
| | | 55, 56 | Table 5.8 DC Characteristics (6), added |
| | | 56 | Table 5.9 DC Characteristics (7), changed |
| | | 58 | Table 5.10 DC Characteristics (8), added |
| | | 59 | Table 5.13 DC Characteristics (11), changed |
| | | 61 | Table 5.19 Output Values of Voltage (1) and Table 5.20 Output Values of Voltage (2), changed |
| | | 68 | Table 5.22 Operation Frequency Value (Middle-Speed Operating Mode) changed, Note 4 added |
| | | 69 | Table 5.24 Clock Timing, changed |
| 78 | Table 5.32 Timing of On-Chip Peripheral Modules (1) changed | | |
| 81 | Table 5.35 Timing of On-Chip Peripheral Modules (4), changed | | |
| 82 | Table 5.36 Timing of On-Chip Peripheral Modules (5): Note 2 deleted | | |
| 83 | Figure 5.37 SCK Clock Input Timing changed | | |
| 84 | Figure 5.38 SCI Input/Output Timing: Clock Synchronous Mode changed | | |

| Rev. | Date | Description | |
|------|--------------|-------------------------------|---|
| | | Page | Summary |
| 1.20 | Sep 29, 2014 | 85 | Figure 5.41 RSPI Clock Timing and Simple SPI Clock Timing, Figure 5.42 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 1) changed |
| | | 86 | Figure 5.43 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Divided by 2) added, Figure 5.44 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 0) changed |
| | | 87 | Figure 5.45 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Set to Divided by 2) added, Figure 5.46 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1) changed |
| | | 88 | Figure 5.47 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0) changed |
| | | 89 | Table 5.37 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics) and Figure 5.49 USB0_DP and USB0_DM Output Timing, changed |
| | | 90 | Figure 5.50 Test Circuit, changed |
| | | 91 | Table 5.38 A/D Conversion Characteristics (1), Figure 5.51 AVCC0 to AVREFH0 Voltage Range, changed |
| | | 92 | Table 5.39 A/D Conversion Characteristics (2), Table 5.40 A/D Conversion Characteristics (3) changed |
| | | 101 | Table 5.49 ROM (Flash Memory for Code Storage) Characteristics (2) and Table 5.50 ROM (Flash Memory for Code Storage) Characteristics (3), changed |
| | | 102 | Table 5.52 E2 DataFlash Characteristics (2), Table 5.53 E2 DataFlash Characteristics (3) changed |
| 1.21 | Dec 09, 2014 | 1. Overview | |
| | | 2 to 4 | Table 1.1 Outline of Specifications Unique ID, changed |
| | | 5. Electrical Characteristics | |
| | | 51 | Table 5.3 DC Characteristics (1) and Table 5.4 DC Characteristics (2), changed |
| | | 61 | Table 5.19 Output Voltage (1) and Table 5.20 Output Voltage (2), changed |
| | | 102 | Table 5.52 E2 DataFlash Characteristics (2): high-speed operating mode and Table 5.53 E2 DataFlash Characteristics (3): middle-speed operating mode, changed |

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update

- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

| Rev. | Date | Description | | Classification |
|------|---|-------------------------------|--|----------------|
| | | Page | Summary | |
| 1.30 | May 31, 2016 | 1. Overview | | |
| | | 18 to 26 | Table 1.5 to 1.9 Note 2 regarding I/O power source is AVCC0 for the ports (P4, PJ6, and PJ7), added | |
| | | 5. Electrical Characteristics | | |
| | | 49 | Table 5.1 Absolute Maximum Ratings, Analog power supply voltage added | |
| | | 49 | Table 5.2 Recommended Operating Conditions, VREFH0 / VREFL0 added | |
| | | 58 | Figure 5.4 Voltage Dependency in High-Speed Operating Mode (Reference Data) added | |
| | | 59 | Figure 5.5 Voltage Dependency in Middle-Speed Operating Mode (Reference Data) added | |
| | | 59 | Figure 5.6 Voltage Dependency in Low-Speed Operating Mode (Reference Data) added | |
| | | 60 | Table 5.9 DC Characteristics (7), Increment for IWDT operation added | |
| | | 62 | Table 5.10 DC Characteristics (8), Increment for IWDT operation added | |
| | | 62 | Figure 5.9 Voltage Dependency in Software Standby Mode (Reference Data) added | |
| | | 63 | Figure 5.10 Temperature Dependency in Software Standby Mode (Reference Data) added | |
| | | 63 | Table 5.11 DC Characteristics (9) added | TN-RX*-A134A/E |
| | | 64 | Table 5.12 DC Characteristics (10), LDV1, 2 added | |
| | | 66, 67 | Table 5.18 Permissible Output Currents is divided into D version and G version | TN-RX*-A134A/E |
| | | 110 | Table 5.49 ROM (Flash Memory for Code Storage) Characteristics (2), Erasure time - 256-Kbyte added | TN-RX*-A132A/E |
| | | 111 | Table 5.50 ROM (Flash Memory for Code Storage) Characteristics (3), Temperature range for the programming/erasure operation changed and Erasure time - 256-Kbyte added | TN-RX*-A132A/E |
| | | 112 | Table 5.52 E2 DataFlash Characteristics (2), Low speed FCLK changed and Erasure time - 8-Kbyte added | TN-RX*-A132A/E |
| 112 | Table 5.53 E2 DataFlash Characteristics (3), Temperature range for the programming/erasure operation changed, Low speed FCLK changed and Erasure time - 8-Kbyte added | TN-RX*-A132A/E | | |
| | 113, 114 | 5.12 Usage Notes added | | |

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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