ICL3207E, ICL3217E

+/- 15kV ESD Protected, +3V to +5.5V, Low Power, 250kbps, RS-232 Transmitters/Receivers

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The Intersil ICL32X7E devices are 3V to 5.5V powered RS-232 transmitters (five)/receivers (three) which meet EIA/TIA-232 and V.28/V.24 specifications, even at V_{CC} = 3.0V. Additionally, they provide ±15kV ESD protection (IEC61000-4-2 Air Gap) and ±15kV Human Body Model protection on transmitter outputs and receiver inputs (RS-232 pins). Targeted applications are ISDN Terminal Adaptors, PDAs, Palmtops, peripherals, and notebook and laptop computers where the low operational, and even lower standby, power consumption is critical. The ICL3217E's efficient on-chip charge pumps, coupled with an automatic powerdown function, reduces the standby supply current to a 1µA trickle. Small footprint packaging, and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250kbps are guaranteed at worst case load conditions. This family is fully compatible with 3.3V-only systems, mixed 3.3V and 5V systems, and 5V-only systems, and is a lower power, pin-for-pin replacement for '207E and '237E type devices.

The **ICL3217E** features an ***automatic powerdown*** function which powers down the on-chip power-supply and driver circuits. This occurs when an attached peripheral device is shut off or the RS-232 cable is removed, conserving system power automatically, without changes to the hardware or operating system. The ICL3217E powers up again when a valid RS-232 voltage is applied to any receiver input.

Table 1 summarizes the features of the devices represented by this data sheet, while application Note AN9863 summarizes the features of each device comprising the ICL32XXE 3V family.

Features

- Pb-Free Available as an Option (see Ordering Info)
- ESD Protection for RS-232 I/O Pins to ±15kV (IEC61000)
- 5V Lower Power Replacement for MAX207E, HIN207E, HIN237E
- Meets EIA/TIA-232 and V.28/V.24 Specifications at 3V
- Latch-Up Free
- On-Chip Voltage Converters Require Only Four External 0.1µF Capacitors
- RS-232 Compatible with V_{CC} = 2.7V
- Automatic Powerdown (I_{CC} = 1µA, ICL3217E Only)
- Receiver Hysteresis For Improved Noise Immunity
- Guaranteed Minimum Data Rate 250kbps
- Guaranteed Minimum Slew Rate 6V/µs
- Wide Power Supply Range . . . . . Single +3V to +5.5V

Applications

- Battery Powered, Hand-Held, and Portable Equipment
- Laptop Computers, Notebooks, Palmtops
- Modems, Printers and other Peripherals
- ISDN Terminal Adaptors and Set Top Boxes
- Related Literature
  - Technical Brief TB363, *Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)*

Pinout

ICL3207E, ICL3217E (SOIC, SSOP)
TOP VIEW

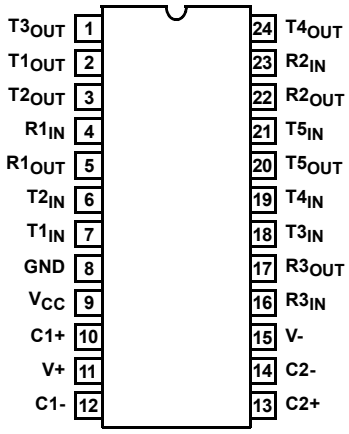


TABLE 1. SUMMARY OF FEATURES

PART NUMBER	NO. OF TX	NO. OF RX	NO. OF MONITOR RX (R_{OUTB})	DATA RATE (kbps)	RX ENABLE FUNCTION?	MANUAL POWER- DOWN?	AUTOMATIC POWERDOWN FUNCTION?
ICL3207E	5	3	0	250	NO	NO	NO
ICL3217E **(No longer available or supported)**	5	3	0	250	NO	NO	YES

Pin Descriptions

PIN	FUNCTION
V_{CC}	System power supply input (3.0V to 5.5V).
V+	Internally generated positive transmitter supply (+5.5V).
V-	Internally generated negative transmitter supply (-5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	External capacitor (voltage doubler) is connected to this lead.
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	External capacitor (voltage inverter) is connected to this lead.
T_{IN}	TTL/CMOS compatible transmitter inputs.
T_{OUT}	±15kV ESD Protected, RS-232 level (nominally ±5.5V) transmitter outputs.
R_{IN}	±15kV ESD Protected, RS-232 compatible receiver inputs.
R_{OUT}	TTL/CMOS level receiver outputs.

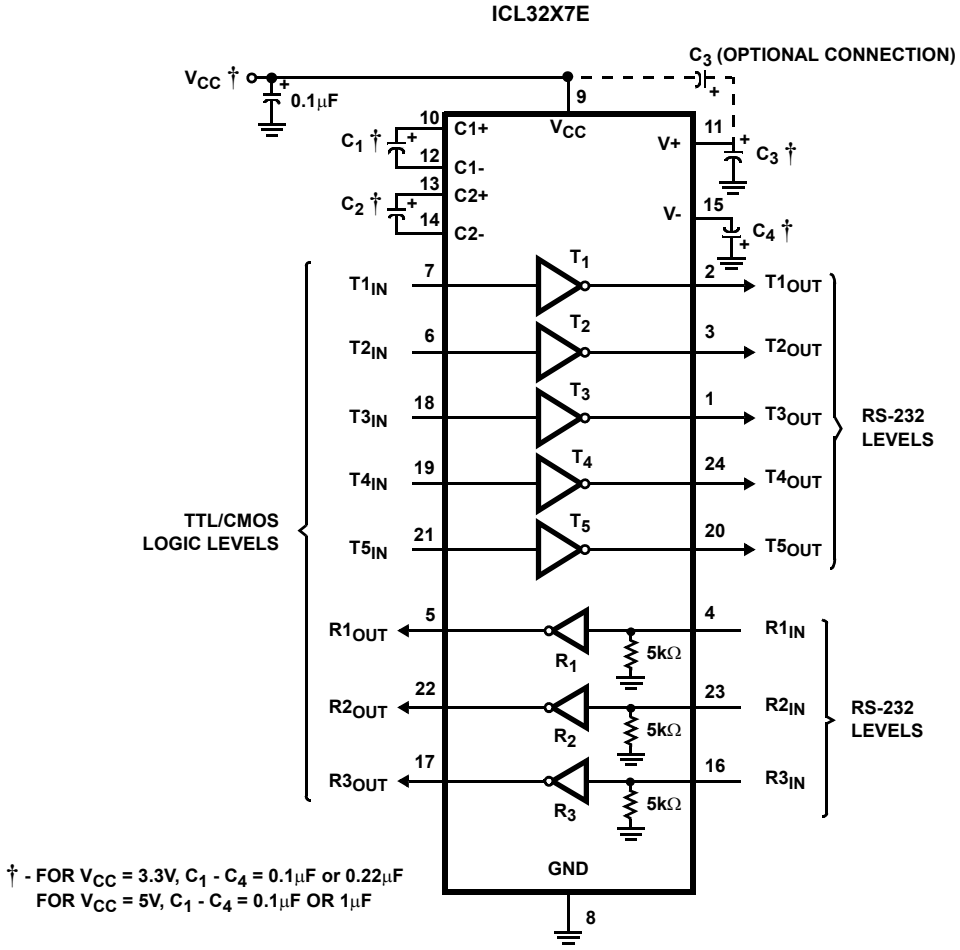
Ordering Information

PART NUMBER (Notes 1, 2)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ICL3207ECAZ	0 to 70	24 Ld SSOP	M24.209
ICL3207ECBZ	0 to 70	24 Ld SOIC	M24.3
ICL3217ECAZ **(No longer available, recommended replacement: ICL3238ECAZ)**	0 to 70	24 Ld SSOP	M24.209
ICL3217ECBZ **(No longer available, recommended replacement: ICL3238ECAZ)**	0 to 70	24 Ld SOIC	M24.3
ICL3217EIAZ **(No longer available, recommended replacement: ICL3238ECAZ)**	-40 to 85	24 Ld SSOP	M24.209
ICL3217EIBZ **(No longer available, recommended replacement: ICL3238ECAZ)**	-40 to 85	24 Ld SOIC	M24.3

NOTES:

1. Most surface mount devices are available on tape and reel; add “-T” to suffix.
2. Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Typical Operating Circuit



Absolute Maximum Ratings

V_{CC} to Ground . . . . . -0.3V to 6V
V+ to Ground . . . . . -0.3V to 7V
V- to Ground . . . . . +0.3V to -7V
V+ to V- 14V
Input Voltages
T_{IN} . . . . . -0.3V to 6V
R_{IN} . . . . . ±25V
Output Voltages
T_{OUT} . . . . . ±13.2V
R_{OUT} . . . . . -0.3V to V_{CC} + 0.3V
Short Circuit Duration
T_{OUT} . . . . . Continuous
ESD Rating . . . . . See Specification Table

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°/W)
24 Ld SOIC Package	75
24 Ld SSOP Package	100

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

Operating Conditions

Temperature Range
ICL32X7ECX . . . . . 0°C to 70°C
ICL32X7EIX . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; Unless Otherwise Specified. Typicals are at T_A = 25°C

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Supply Current, Automatic Powerdown	All R_{IN} Open (ICL3217E Only)		25	-	1.0	10	µA
Supply Current, Automatic Powerdown Disabled	All Outputs Unloaded		25	-	0.3	1.0	mA
TRANSMITTER INPUTS AND RECEIVER OUTPUTS							
Input Logic Threshold Low	T_{IN}		Full	-	-	0.8	V
Input Logic Threshold High	T_{IN}	V_{CC} = 3.3V	Full	2.0	-	-	V
		V_{CC} = 5.0V	Full	2.4	-	-	V
Input Leakage Current	T_{IN}		Full	-	±0.01	±1.0	µA
Output Leakage Current (ICL3217E Only)			Full	-	±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC}-0.6	V_{CC}-0.1	-	V
AUTOMATIC POWERDOWN (ICL3217E Only)							
Receiver Input Thresholds to Enable Transmitters	ICL3217E Powers Up (Figure 4)		Full	-2.7	-	2.7	V
Receiver Input Thresholds to Disable Transmitters	ICL3217E Powers Down (Figure 4)		Full	-0.3	-	0.3	V
Receiver Threshold to Transmitters Enabled Delay (t_{WU})			25	-	100	-	µs
Receiver Positive or Negative Threshold to Transmitters Disabled Delay			25	-	30	-	µs
RECEIVER INPUTS							
Input Voltage Range			Full	-25	-	25	V
Input Threshold Low	V_{CC} = 3.3V		25	0.6	1.2	-	V
	V_{CC} = 5.0V		25	0.8	1.5	-	V
Input Threshold High	V_{CC} = 3.3V		25	-	1.5	2.4	V
	V_{CC} = 5.0V		25	-	1.8	2.4	V

Electrical Specifications Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; Unless Otherwise Specified. Typicals are at T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
Input Hysteresis			25	-	0.3	-	V
Input Resistance			25	3	5	7	kΩ
TRANSMITTER OUTPUTS							
Output Voltage Swing	All Transmitter Outputs Loaded with 3kΩ to Ground		Full	±5.0	±5.4	-	V
Output Resistance	V_{CC} = V+ = V- = 0V, Transmitter Output = ±2V		Full	300	10M	-	Ω
Output Short-Circuit Current			Full	-	±35	±60	mA
Output Leakage Current (ICL3217E Only)	V_{OUT} = ±12V, V_{CC} = 0V or 3V to 5.5V In Automatic Powerdown		Full	-	-	±25	µA
TIMING CHARACTERISTICS							
Maximum Data Rate (One Transmitter Switching)	V_{CC} = 3.15V, C_1 - C_4 = 0.1µF, R_L = 3kΩ, C_L = 1000pF		Full	250	500	-	kbps
	V_{CC} = 3.0V, C_1 - C_4 = 0.22µF, R_L = 3kΩ, C_L = 1000pF		Full	250	286	-	kbps
	$V_{CC} \geq$ 4.5V, C_1 - C_4 = 0.1µF, R_L = 3kΩ, C_L = 1000pF		Full	250	310	-	kbps
Receiver Propagation Delay	Receiver Input to Receiver Output, C_L = 150pF	t_{PHL}	25	-	0.3	-	µs
		t_{PLH}	25	-	0.3	-	µs
Transmitter Skew	t_{PHL} - t_{PLH}		Full	-	200	1000	ns
Receiver Skew	t_{PHL} - t_{PLH}		Full	-	100	500	ns
Transition Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, Measured From +3V to -3V or -3V to +3V	C_L = 200pF to 2500pF	25	4	15	30	V/µs
		C_L = 200pF to 1000pF	25	6	15	30	V/µs
ESD PERFORMANCE							
RS-232 Pins (T_{OUT}, R_{IN})	IEC61000-4-2, Air-Gap Discharge Method		25	-	±15	-	kV
	IEC61000-4-2, Contact Discharge Method		25	-	±8	-	kV
	Human Body Model		25	-	±15	-	kV
All Other Pins	Human Body Model		25	-	±2	-	kV

Detailed Description

The ICL32X7E interface ICs operate from a single +3V to +5.5V power supply, guarantee a 250kbps minimum data rate, require only four small external 0.1µF capacitors, feature low power consumption, and meet all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: charge pump, transmitters and receivers.

Charge-Pump

Intersil's new ICL32XXE family utilizes regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3V. This allows these devices to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external 0.1µF capacitors for the voltage doubler and inverter functions at V_{CC} = 3.3V. See the *Capacitor Selection* section, and Table 3 for capacitor recommendations for other operating conditions. The charge pumps operate discontinuously (i.e., they turn off as soon as the V+ and V- supplies are pumped up to the nominal values), resulting in significant power savings.

Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. Coupled with the on-chip ±5.5V supplies, these transmitters deliver true RS-232 levels over a wide range of single supply system voltages.

ICL3217E transmitter outputs disable and assume a high impedance state when the device enters the automatic powerdown mode. These outputs may be driven to ±12V when disabled.

Both devices guarantee a 250kbps data rate for full load conditions (3kΩ and 1000pF), $V_{CC} \geq$ 3.0V, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq$ 3.3V, R_L = 3kΩ, and C_L = 250pF, one transmitter easily operates at 800kbps.

Transmitter inputs float if left unconnected, and may cause I_{CC} increases. Connect unused inputs to GND for the best performance.

Receivers

The ICL32X7E each contain inverting receivers that convert RS-232 signals to CMOS output levels and accept inputs up to ±25V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 1) even if the power is off (V_{CC} = 0V). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions.

Receivers on the ICL3207E are always active. The ICL3217E receivers disable when in the automatic powerdown state, thereby eliminating the possible current path through a shutdown peripheral's input protection diode (see Figures 2 and 3).

Low Power Operation

These 3V devices require a nominal supply current of 0.3mA, even at V_{CC} = 5.5V, during normal operation (not in powerdown mode). This is considerably less than the 11mA current required by comparable 5V RS-232 devices, allowing users to reduce system power simply by replacing the old style device with the ICL3207E.

Low Power, Pin Compatible Replacement

Pin compatibility with existing 5V products (e.g., MAX207E), coupled with the wide operating supply range, make the ICL32X7E potential lower power, higher performance drop-in replacements for existing '2X7E 5V applications. As long as the ±5V RS-232 output swings are acceptable, the ICL32X7E devices should work in most 5V applications.

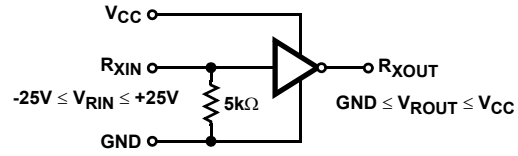


FIGURE 1. INVERTING RECEIVER CONNECTIONS

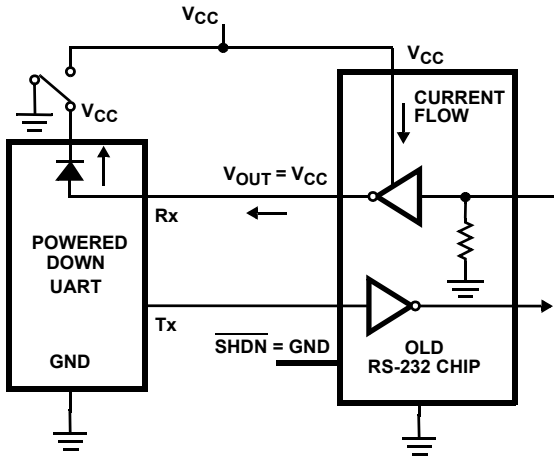


FIGURE 2. POWER DRAIN THROUGH POWERED DOWN PERIPHERAL

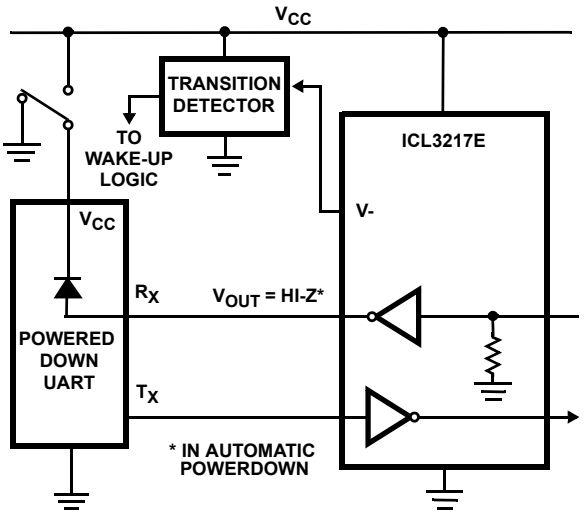


FIGURE 3. DISABLED RECEIVERS PREVENT POWER DRAIN

When replacing a '207E or '237E device in an existing 5V application, it is acceptable to terminate C_3 to V_{CC} as shown on the *Typical Operating Circuit*. Nevertheless, terminate C_3 to GND if possible, as slightly better performance results from this configuration.

Automatic Powerdown (ICL3217E Only)

Even greater power savings is available by using the ICL3217E which features an automatic powerdown function. When no valid RS-232 voltages (see Figure 4) are sensed on any receiver input for 30µs, the ICL3217E *automatically* enters its powerdown state (see Figure 5). In powerdown, supply current drops to 1µA, because the on-chip charge pump turns off (V+ collapses to V_{CC}, V- collapses to GND), and the receiver and transmitter outputs three-state (see Table 2). This micro-power mode makes the ICL3217E ideal for battery powered and portable applications. Invalid receiver levels occur whenever the driving peripheral's outputs are shut off (powered down) or when the RS-232 interface cable is disconnected. The ICL3217E powers back up whenever it detects a valid RS-232 voltage level on any receiver input (such as when the RS-232 cable is reconnected). The time to recover from automatic powerdown mode is typically 100µs.

TABLE 2. ICL3217E AUTOMATIC POWERDOWN OPERATION

RS-232 SIGNAL PRESENT AT RECEIVER INPUT?	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	MODE OF OPERATION
YES	Active	Active	Normal Operation
NO	High-Z	High-Z	Powerdown Due to Auto Powerdown Logic

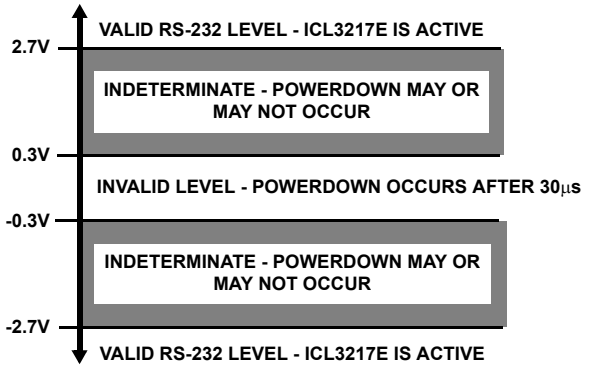


FIGURE 4. DEFINITION OF VALID RS-232 RECEIVER LEVELS

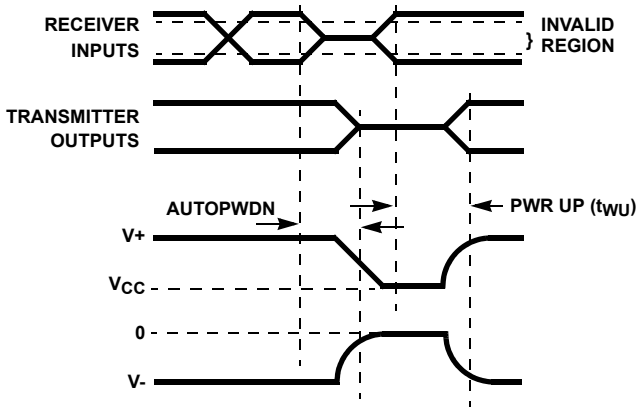


FIGURE 5. AUTOMATIC POWERDOWN TIMING DIAGRAM

This automatic powerdown feature provides additional system power savings without changes to the existing operating system or hardware.

Utilizing power management circuitry, to power down the rest of the communication circuitry (e.g., the UART) when the ICL3217E powers down, produces even greater power savings. Connecting a transition detector to the V- pin (see Figure 3) is an easy way for the power management logic to determine when the ICL3217E enters and exits powerdown.

Capacitor Selection

The charge pumps require 0.1µF, or greater, capacitors for 3.3V operation. With 0.1µF capacitors, five percent tolerance supplies (e.g., 3.14V minimum) deliver greater than ±5V transmitter swings at full data rate, while ten percent tolerance supplies (e.g., 2.97V minimum) deliver ±4.95V transmitter swings. If greater than ±5V transmitter swings are required with a 10% tolerance 3.3V supply, 0.22µF capacitors are recommended (see Table 3). Existing 5V applications typically utilize either 0.1µF or 1µF capacitors, and the ICL32X7E works well with either value. New 5V designs should use 0.22µF capacitors for the best results. For other supply voltages refer to Table 3 for capacitor values. Do not use values smaller than those listed in Table 3. Increasing the capacitor values (by a factor of two) reduces ripple on the transmitter outputs and slightly reduces power consumption. C_2, C_3, and C_4 can be increased without increasing C_1's value, however, do not increase C_1 without also increasing C_2, C_3, and C_4 to maintain the proper ratios (C_1 to the other capacitors).

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V+ and V-.

TABLE 3. REQUIRED CAPACITOR VALUES

V_{CC} (V)	C_1 (µF)	C_2, C_3, C_4 (µF)
3.15 to 3.6	0.1	0.1
3.0 to 3.6	0.22	0.22
4.5 to 5.5	0.1 to 1.0	0.1 to 1.0
3.0 to 5.5	0.22	0.22

Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

Transmitter Outputs when Exiting Powerdown

Figure 6 shows the response of two ICL3217E transmitter outputs when exiting powerdown mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V.

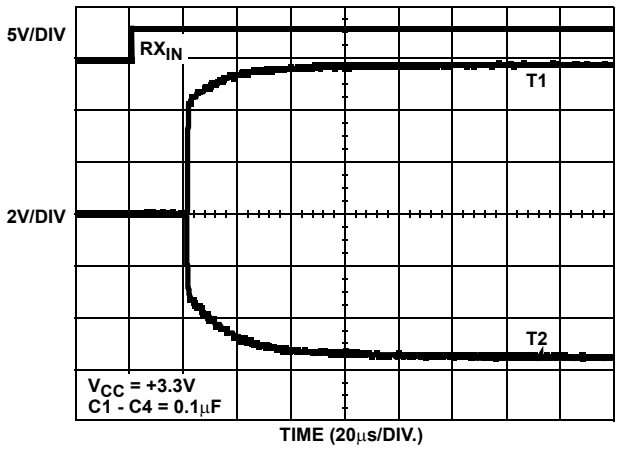


FIGURE 6. TRANSMITTER OUTPUTS WHEN EXITING POWERDOWN (ICL3217E ONLY)

Operation down to 2.7V

ICL32X7E transmitter outputs meet RS-562 levels (±3.7V) with V_{CC} as low as 2.7V. RS-562 levels typically ensure inter operability with RS-232 devices.

High Data Rates

The ICL32XX maintain the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 7 details a transmitter loopback test circuit, and Figure 8 illustrates the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120kbps. Figure 9 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

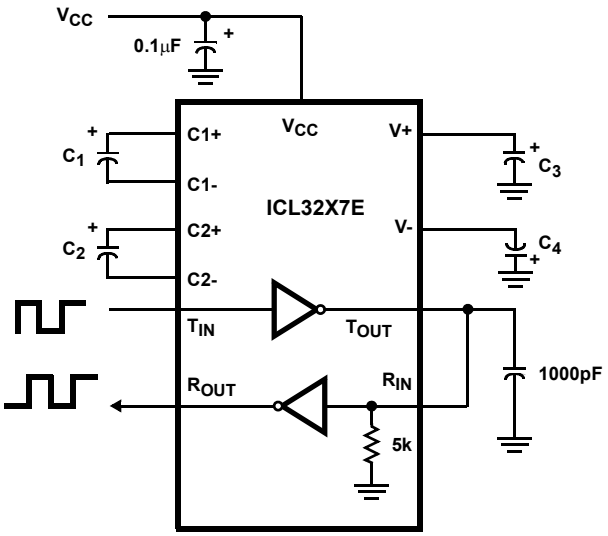


FIGURE 7. TRANSMITTER LOOPBACK TEST CIRCUIT

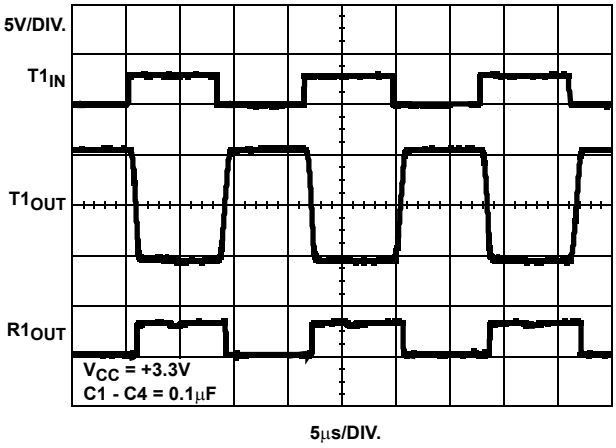


FIGURE 8. LOOPBACK TEST AT 120kbps

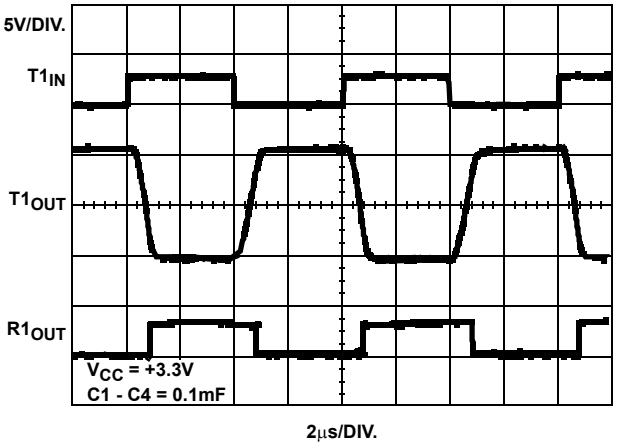


FIGURE 9. LOOPBACK TEST AT 250kbps

Interconnection with 3V and 5V Logic

The ICL32X7E directly interface with 5V CMOS and TTL logic families. Nevertheless, with the ICL32X7E at 3.3V, and the logic supply at 5V, AC, HC, and CD4000 outputs can drive ICL32X7E inputs, but ICL32X7E outputs do not reach the minimum V_{IH} for these logic families. See Table 4 for more information.

TABLE 4. LOGIC FAMILY COMPATIBILITY WITH VARIOUS SUPPLY VOLTAGES

SYSTEM POWER-SUPPLY VOLTAGE (V)	V_{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. ICL32X7E outputs are incompatible with AC, HC, and CD4000 CMOS inputs.

±15kV ESD Protection

All pins on ICL32XX devices include ESD protection structures, but the ICL32X7***E*** incorporate advanced structures which allow the RS-232 pins (transmitter outputs and receiver inputs) to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and don't interfere with RS-232 signals as large as ±25V.

Human Body Model (HBM) Testing

As the name implies, this test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor, making the test less severe than the IEC61000 test which utilizes a 330Ω limiting resistor. The HBM method determines an ICs ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on “E” family devices can withstand HBM ESD events to ±15kV.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device’s RS-232 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-232 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The “E” device RS-232 pins withstand ±15kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. All “E” family devices survive ±8kV contact discharges on the RS-232 pins.

Typical Performance Curves V_{CC} = 3.3V, T_A = 25°C

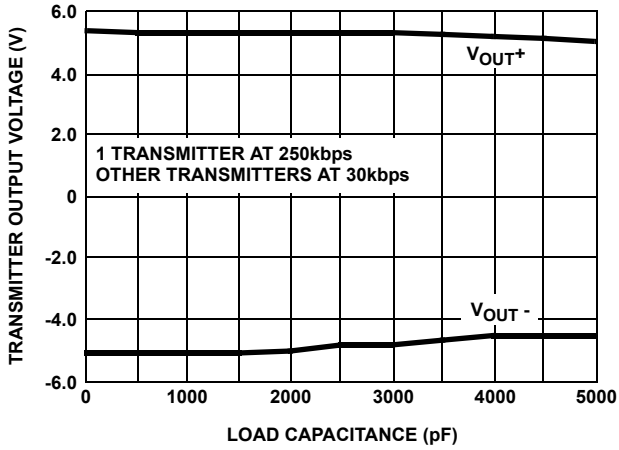


FIGURE 10. TRANSMITTER OUTPUT VOLTAGE vs LOAD CAPACITANCE

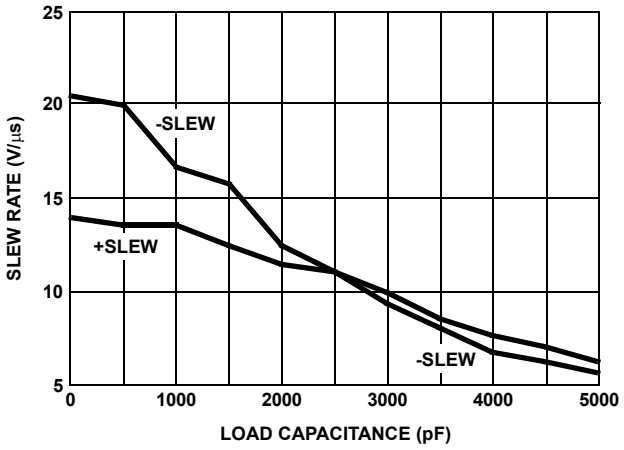


FIGURE 11. SLEW RATE vs LOAD CAPACITANCE

Typical Performance Curves V_{CC} = 3.3V, T_A = 25°C **(Continued)**

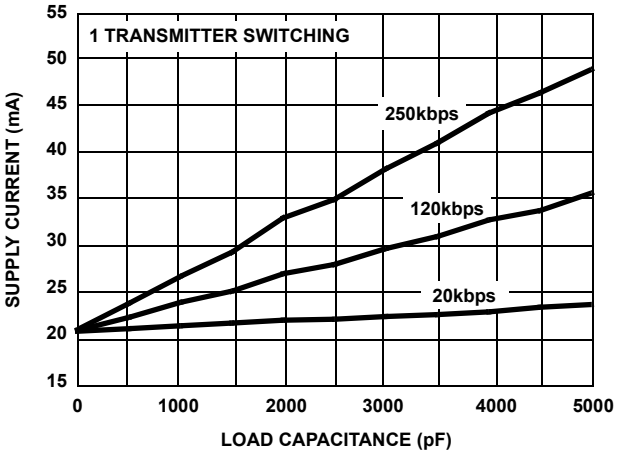


FIGURE 12. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

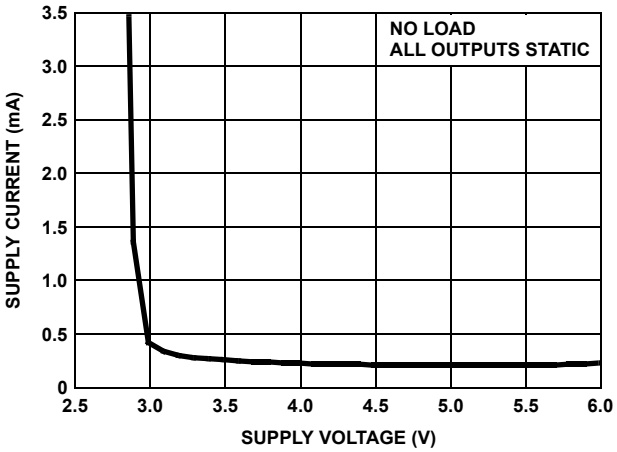


FIGURE 13. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

ICL3207E: 469

ICL3217E: 488

PROCESS:

Si Gate CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 21, 2015	FN4914.6	Updated Ordering Information table on page 2. Added Revision History and About Intersil sections. Updated Package Outline Drawing M24.3 to the latest revision updates are as follows: -Revision 0 to Revision 1, Removed µ symbol which is overlapping the alpha symbol in the diagram. -Revision 1 to Revision 2, Updated to new POD standard by removing table listing dimensions and putting dimensions on drawing. Added Land Pattern.

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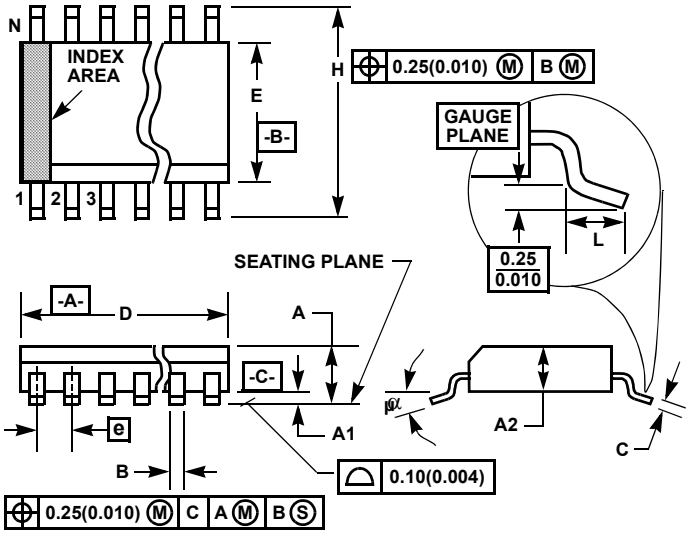
Shrink Small Outline Plastic Packages (SSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.209 **(JEDEC MO-150-AG ISSUE B)**
24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.312	0.334	7.90	8.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

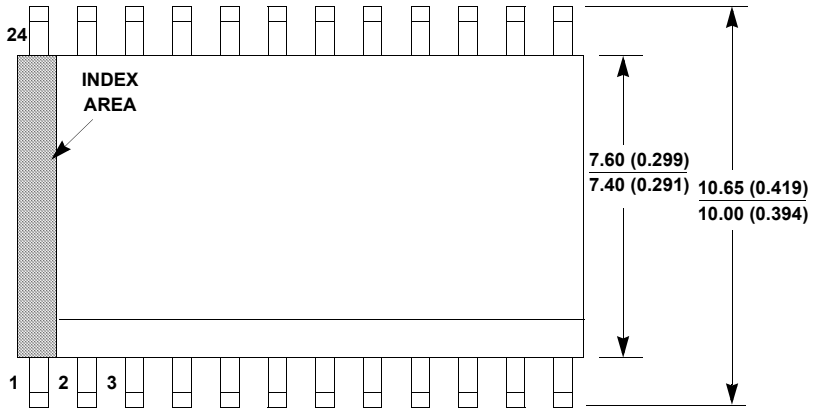
Rev. 1 3/95

Package Outline Drawing

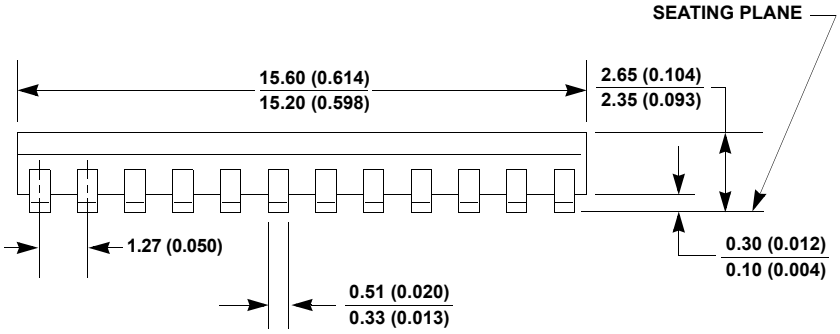
M24.3

24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOIC)

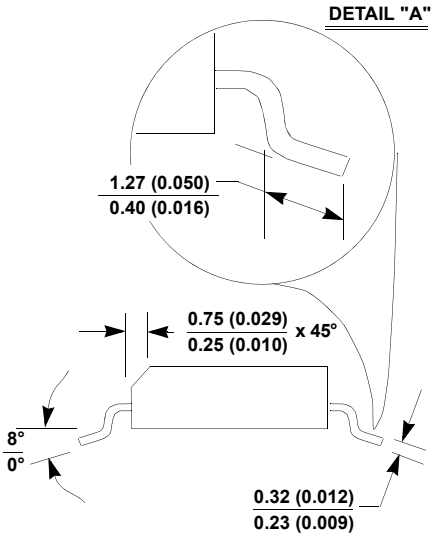
Rev 2, 3/11



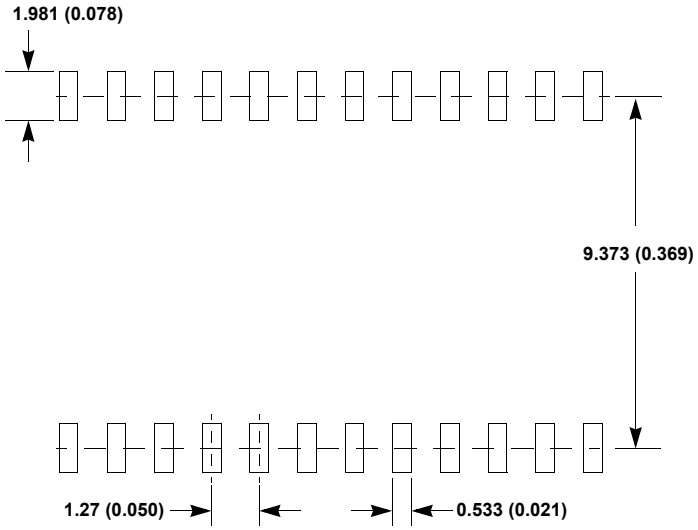
TOP VIEW



SIDE VIEW “A”



SIDE VIEW “B”



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions in ( ) are not necessarily exact.
8. This outline conforms to JEDEC publication MS-013-AD ISSUE C.

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