VND5E012AY-E

Double channel high-side driver with analog current sense for automotive applications

Datasheet - production data

PowerSSO-36

Features

Max transient supply voltage	V_{CC}	41V
Operating voltage range	V_{CC}	4.5 to 28V
Max on-state resistance (per ch.)	R_{ON}	12 mΩ
Current limitation (typ)	I_{LIMH}	74 A
Off-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected

- General:
  - Inrush current active management by power limitation
  - Very low standby current
  - 3.0 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC european directive
  - Proportional load current sense
  - High current sense precision for wide range current
  - Very low current sense leakage
- Diagnostic functions:
  - Off-state open-load detection
  - Current sense disable
  - Thermal shutdown indication
  - Output short to V_{CC} detection
  - Overload and short to ground (power limitation) indication
- Protection:
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Thermal shutdown
  - Reverse battery protection with self switch of the Power MOS
  - Electrostatic discharge protection

Applications

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

Description

The VND5E012AY-E is a device made using STMicroelectronics® VIPower® M0-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes.

This device integrates an analog current sense which delivers a current proportional to the load current when CS_DIS high leads the current sense pin in high impedance.

Fault conditions such as overload, overtemperature or openload are reported via the current sense pin.

Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shutdown intervention. Thermal shutdown with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

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1 Block diagram and pin description

Figure 1. Block diagram

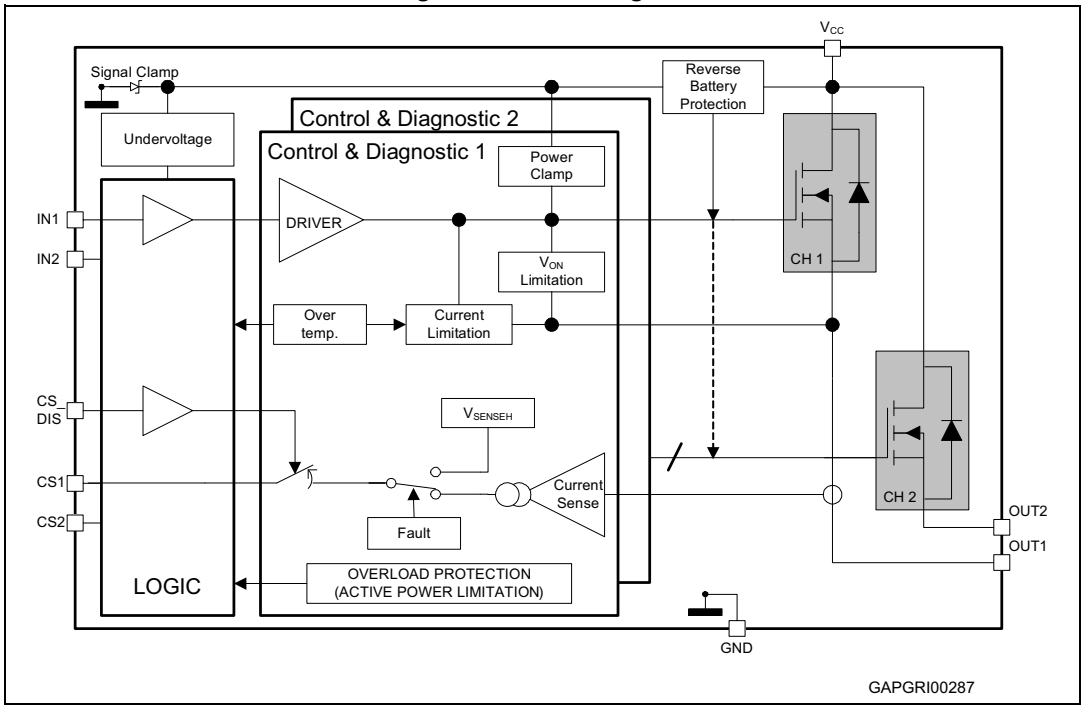


Table 1. Pin function

Name	Function
V_{CC}	Battery connection
$OUT_{1,2}$	Power output
GND	Ground connection
$IN_{1,2}$	Voltage controlled input pin with hysteresis, CMOS compatible; controls output switch state
$CS_{1,2}$	Analog current sense pin delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 2. Configuration diagram (top view)

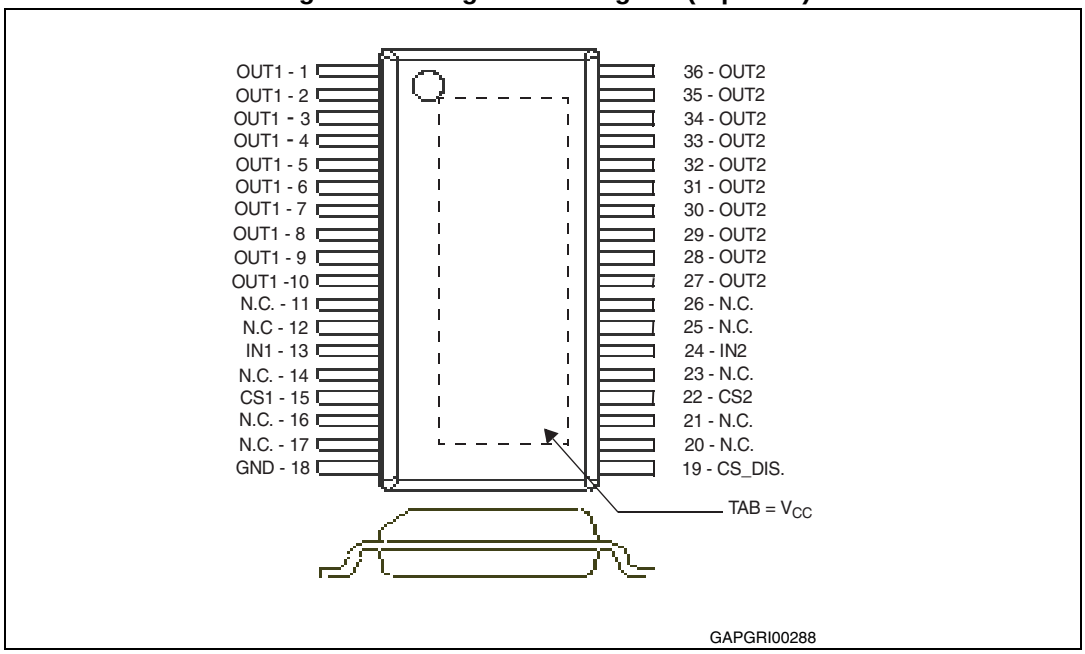
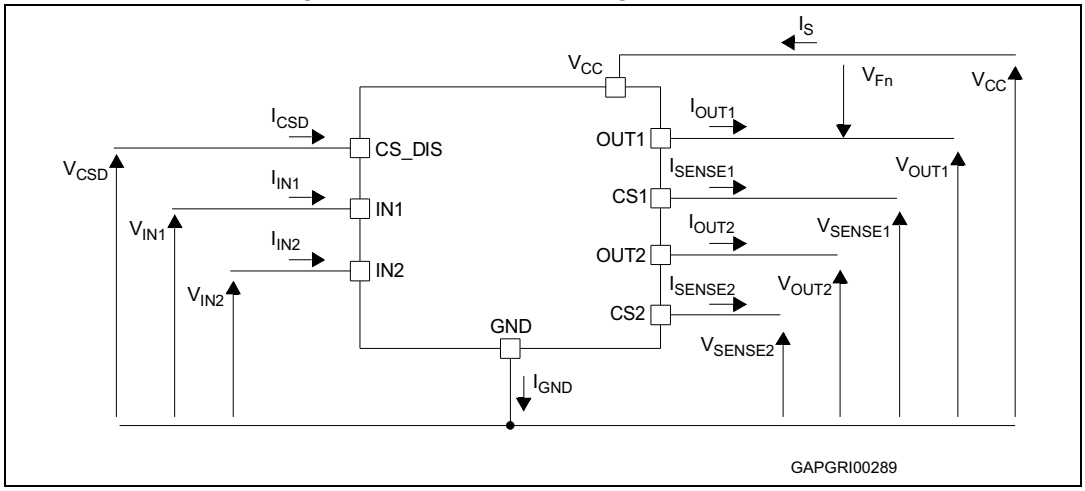


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	Not connected	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 KΩ resistor	X	Not allowed	Through 10 KΩ resistor	Through 10 KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Applying stress which exceeds the ratings listed in the*Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	28	V
V_{CCPK}	Transient supply voltage (T<400 ms, R_{LOAD} > 0.5 Ω)	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
V_{CC_LSC}	Maximum supply voltage for full protection to short-circuit (acc. AEC-Q100-012)	18	V
$- I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$- I_{OUT}$	Reverse DC output current	50	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC Reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC}-41 $+V_{CC}$	V V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy (single pulse) (L = 0.47 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_{OUT} = I_{limL}(Typ.))	110	mJ
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) – V_{CC}, OUTPUT – INPUT, CS_DIS – CURRENT SENSE	 5000 4000 2000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Maximum value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (With one channel ON)	2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	See *Figure 36* in the thermal section	°C/W

2.3 Electrical characteristics

8V<V_{CC}<28V; -40°C< T_j <150°C, unless otherwise specified

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance	I_{OUT}=5A; T_j=25°C		11	16	
		I_{OUT}=5A; T_j=150°C			24	mΩ
		I_{OUT}=5A; V_{CC}=5V; T_j=25°C			16	mΩ
$R_{ON\ REV}$	Reverse battery on-state resistance	V_{CC}=-13V; I_{OUT}=-5A; T_j=25°C			12	mΩ
V_{clamp}	Clamp voltage	I_S=20 mA	41	46	52	V
I_S	Supply current	Off-state; V_{CC}=13V; T_j=25°C;				
		V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0 V		2 (1)	5(1)	µA
		On-state; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A		3.5	6.5	mA
$I_{L(off)}$	Off-state output current (2)	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=25°C	0	0.01	3	
		V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=125°C	0		5	µA

1. PowerMOS leakage included
2. For each channel

Table 6. Switching (V_{CC} = 13V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L=2.6Ω (see *Figure 8*)	-	30	-	µs
$t_{d(off)}$	Turn-off delay time	R_L=2.6Ω (see *Figure 8*)	-	20	-	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L=2.6Ω	-	See *Figure 28*	-	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L=2.6Ω	-	See *Figure 29*	-	V/µs
W_{ON}	Switching energy losses during t_{WON}	R_L=2.6Ω (see *Figure 8*)	-	1	-	mJ
W_{OFF}	Switching energy losses during t_{WOFF}	R_L=2.6Ω (see *Figure 8*)	-	0.5	-	mJ

Table 7. Current sense (8V<V_{CC}<18V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT}=0.25A; V_{SENSE}=0.5V T_j= -40°C...150°C	2615	5130	7770	
K_1	I_{OUT}/I_{SENSE}	I_{OUT}=5A; V_{SENSE}=0.5V T_j=-40°C...150°C T_j=25°C...150°C	4155 4530	5330 5330	6650 6130	
dK_1/K_1(1)	Current sense ratio drift	I_{OUT}=5A; V_{SENSE}= 0.5V; V_{CSD}=0V; T_J= -40 °C to 150 °C	-8		8	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT}=10A; V_{SENSE}=4V T_j=-40°C...150°C T_j=25°C...150°C	4705 4865	5290 5290	5950 5715	
dK_2/K_2(1)	Current sense ratio drift	I_{OUT}= 10 A; V_{SENSE}= 4 V; V_{CSD}=0V; T_J= -40 °C to 150 °C	-5		5	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT}=25A; V_{SENSE}=4V T_j=-40°C...150°C T_j=25°C...150°C	4935 4985	5250 5250	5565 5515	
dK_3/K_3(1)	Current sense ratio drift	I_{OUT}= 25 A; V_{SENSE}= 4 V; V_{CSD}= 0V; T_J= -40 °C to 150 °C	-4		4	%
I_{SENSE0}	Analog sense leakage current	I_{OUT}=0A; V_{SENSE}=0V; V_{CSD}=5V; V_{IN}=0V; T_j=-40°C...150°C V_{CSD}=0V; V_{IN}=5V; T_j=-40°C...150°C I_{OUT}=5A; V_{SENSE}=0V; V_{CSD}=V_{IN}=5V;	0 0 0		1 2 1	µA µA µA
V_{SENSE}	Max analog sense output voltage	I_{OUT}=15A; V_{CSD}=0V	5			V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	V_{CC}=13V; R_{SENSE}=10KΩ		8		V
I_{SENSEH}	Analog sense output current in overtemperature condition	V_{CC}=13V; V_{SENSE}=5V		9		mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE}<4V, 1.5A<Iout<25A I_{SENSE}=90% of $I_{SENSE\ max}$ (see fig *Figure 4*)		50	100	µs

Table 7. Current sense (8V<V_{CC}<18V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE1L}$	Delay Response time from rising edge of CS_DIS pin	V_{SENSE}<4V, 1.5A<Iout<25A I_{SENSE}=10% of $I_{SENSE\ max}$ (see fig *Figure 4*)		5	20	µs
$t_{DSENSE2H}$	Delay Response time from rising edge of INPUT pin	V_{SENSE}<4V, 1.5A<Iout<25A I_{SENSE}=90% of $I_{SENSE\ max}$ (see fig *Figure 4*)		70	300	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4V, I_{SENSE} = 90% of $I_{SENSEMAX}$, I_{OUT} = 90% of I_{OUTMAX} I_{OUTMAX}= 5A (see *Figure 9*)			300	µs
$t_{DSENSE2L}$	Delay Response time from falling edge of INPUT pin	V_{SENSE}<4V, 1.5A<Iout<25A I_{SENSE}=10% of $I_{SENSE\ max}$ (see fig *Figure 4*)		100	250	µs

1. Parameter guaranteed by design; it is not tested.

Table 8. Open-load detection (8V<V_{CC}<18V)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{OL}	Openload off-state voltage detection threshold	V_{IN} = 0V	2	-	4	V
t_{DSTKON}	Output short circuit to V_{cc} detection delay at turn-off	see *Figure 5*	180	-	1200	µs
$I_{L(off2)r}$	Off-state output current at V_{OUT} = 4 V	V_{IN} = 0 V; V_{SENSE} = 0 V V_{OUT} rising from 0 V to 4 V	-120	-	90	µA
$I_{L(off2)f}$	Off-state output current at V_{OUT} = 2V	V_{IN} = 0 V; V_{SENSE} = V_{SENSEH} V_{OUT} falling to V_{CC} to 2 V	-50	-	90	µA

Table 9. Protections (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC Short circuit current	V_{CC}=13V 5V<V_{CC}<18V	52	74	104 104	A A
I_{limL}	Short circuit current during thermal cycling	V_{CC}=13V; T_R<T_j<T_{TSD}		18.5		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C

Table 9. Protections (1) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT}=2A; V_{IN}=0; L=6mH	V_{CC}-28	V_{CC}-31	V_{CC}-35	V
V_{ON}	Output voltage drop limitation	I_{OUT}=0.4A; T_j=-40°C...150°C (see fig. *Figure 10*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Table 10. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN}=0.9V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN}=2.1V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN}=1mA I_{IN}=-1mA	5.5	 -0.7	7	V V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	V_{CSD}=0.9V	1			µA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	V_{CSD}=2.1V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD}=1mA I_{CSD}=-1mA	5.5	 -0.7	7	V V

Figure 4. Current sense delay characteristics

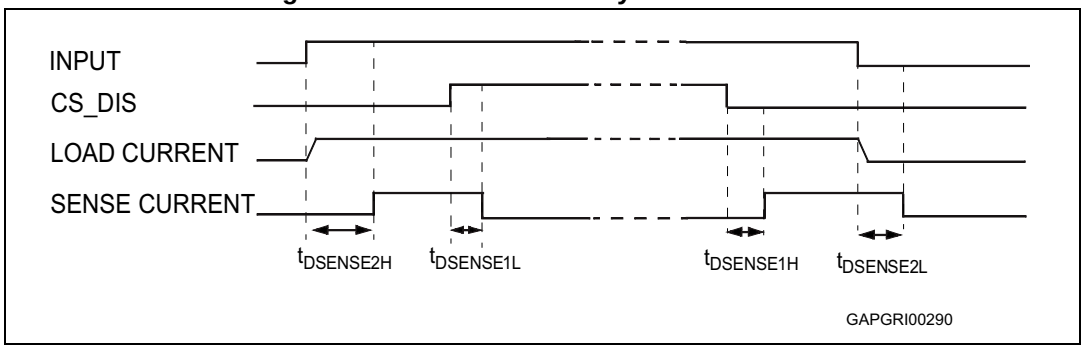


Figure 5. Open-load off-state delay timing

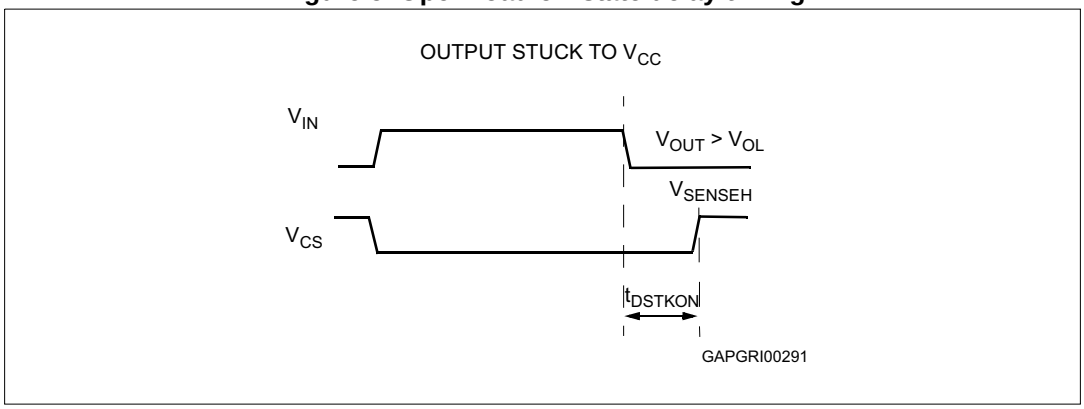
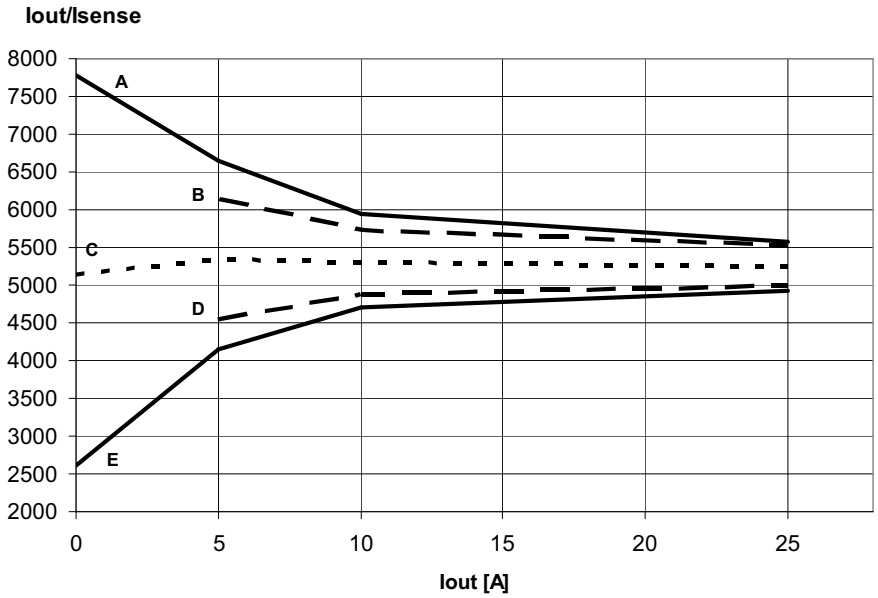


Figure 6. I_{OUT}/I_{SENSE} vs I_{OUT}



A: Max, Tj = -40 °C to 150 °C
B: Max, Tj = 25 °C to 150 °C
C: Typical, Tj = -40 °C to 150 °C
D: Min, Tj = 25 °C to 150 °C
E: Min, Tj = -40 °C to 150 °C

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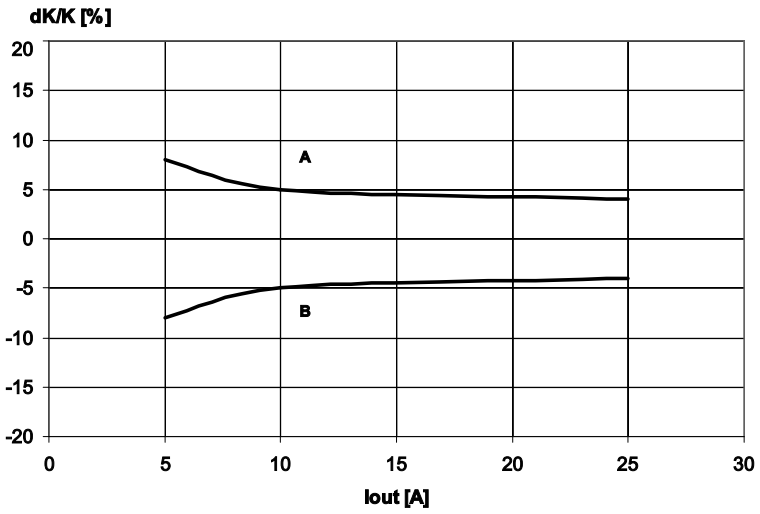
Figure 7. Maximum current sense ratio drift vs load current



A: Max, Tj = -40 °C to 150 °C
B: Min, Tj = -40 °C to 150 °C

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Table 11. Truth table

Conditions	Input	Output	Sense(V_{CSD}=0V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overload	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short circuit to GND (Power limitation)	L H	L L	0 V_{SENSEH}
Open load off-state (with external pull up)	L	H	V_{SENSEH}
Short circuit to V_{CC} (external pull up disconnected)	L H	H H	V_{SENSEH} < Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance; its potential depends on leakage currents and external circuit

Figure 8. Switching characteristics

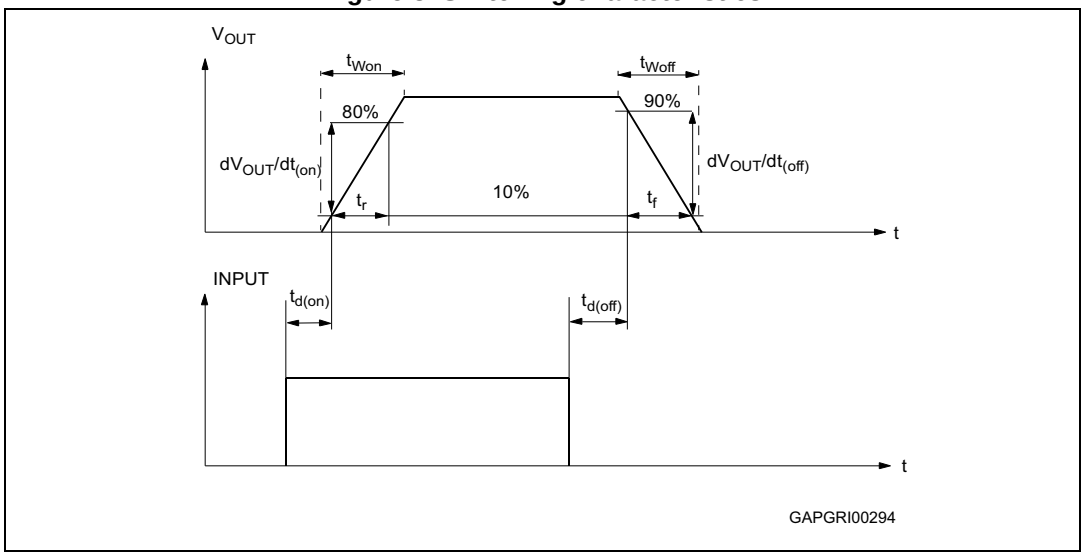


Figure 9. Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled)

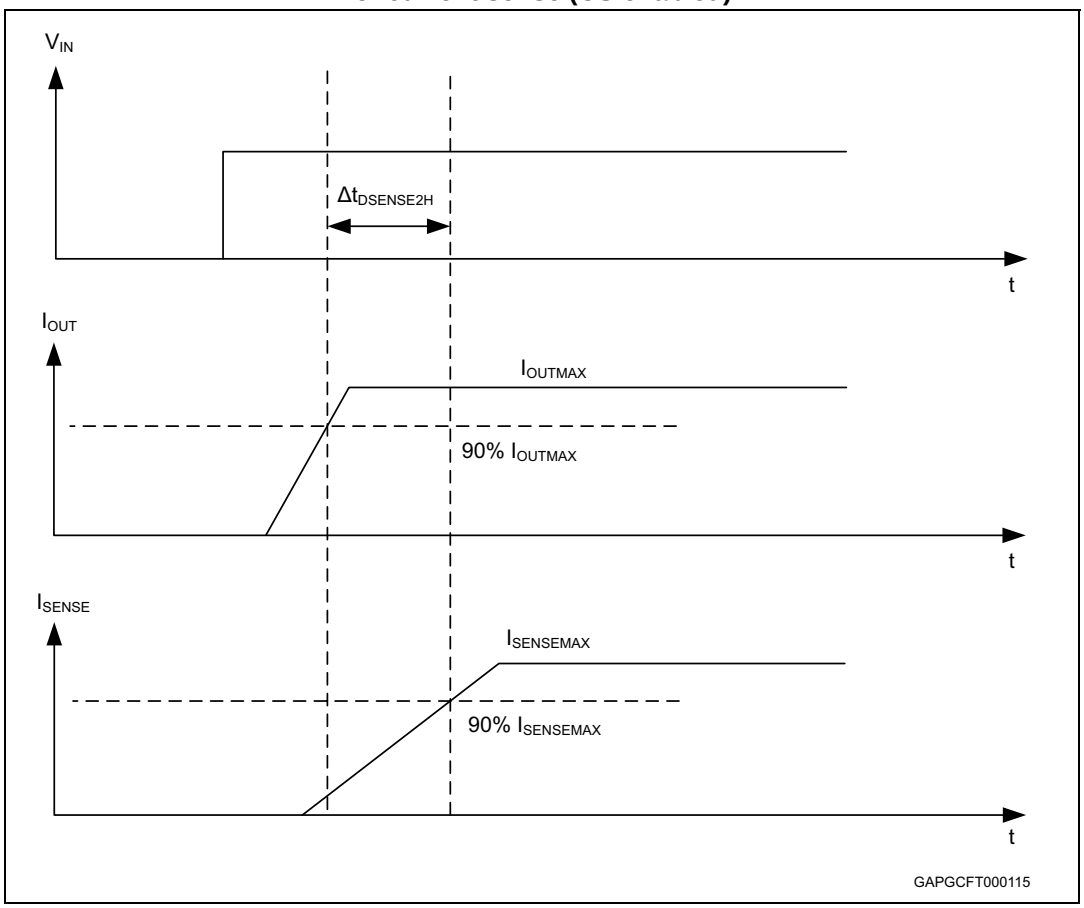


Figure 10. Output voltage drop limitation

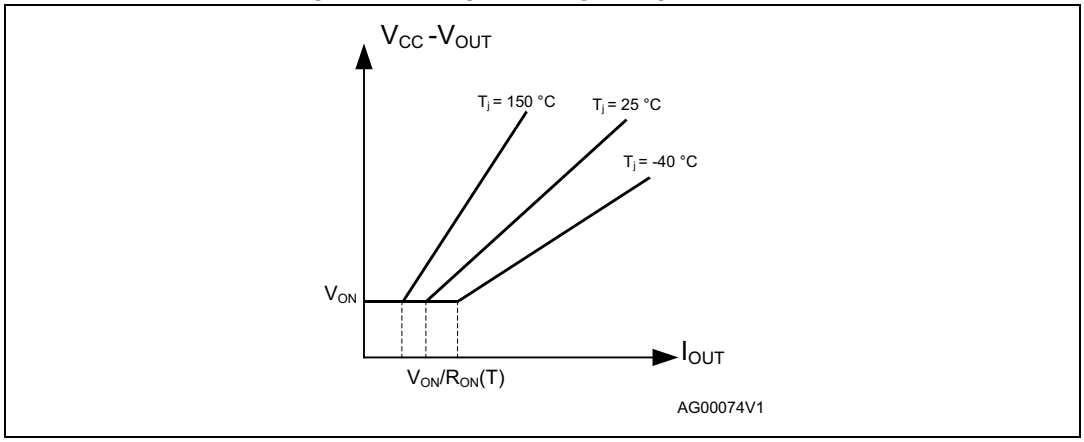


Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test Pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2) (3)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in *Table 3: Absolute maximum ratings*

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 11. Normal operation

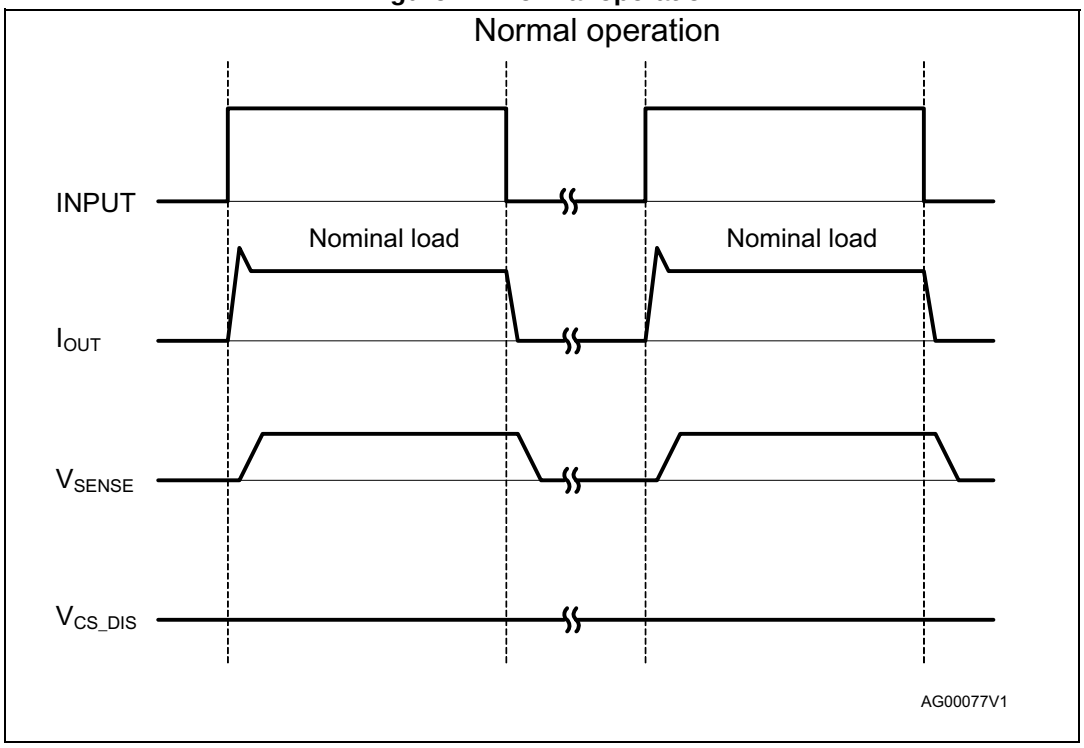


Figure 12. Overload or short to GND

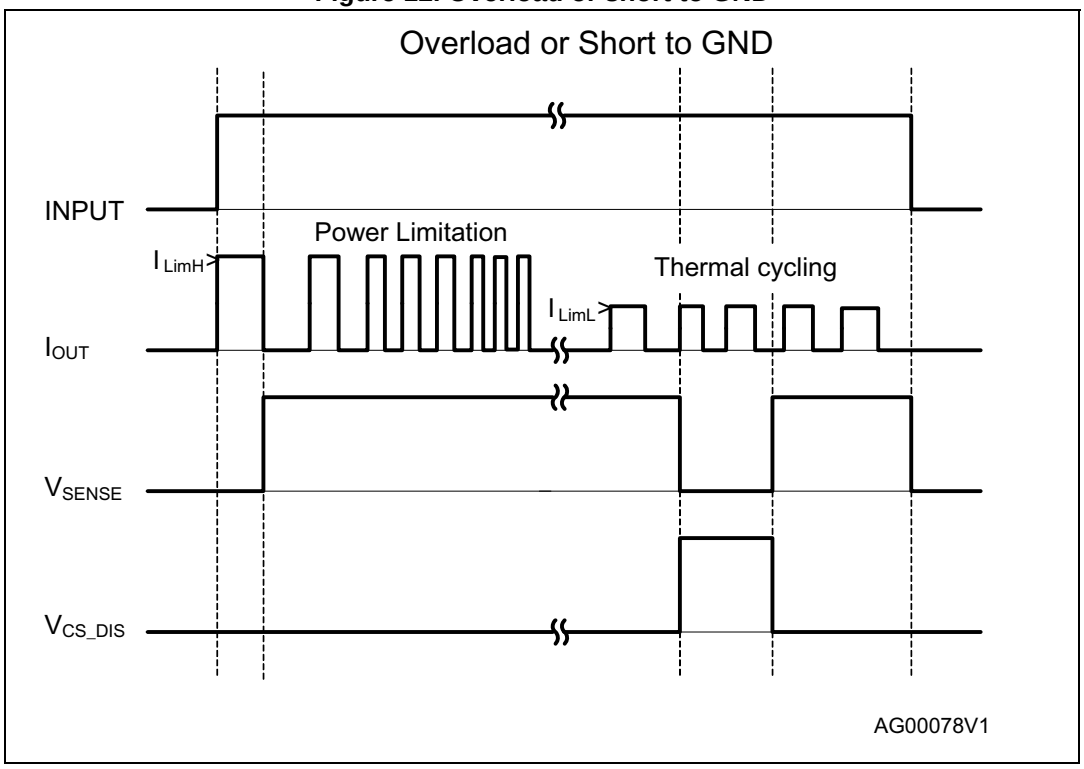


Figure 13. Intermittent overload

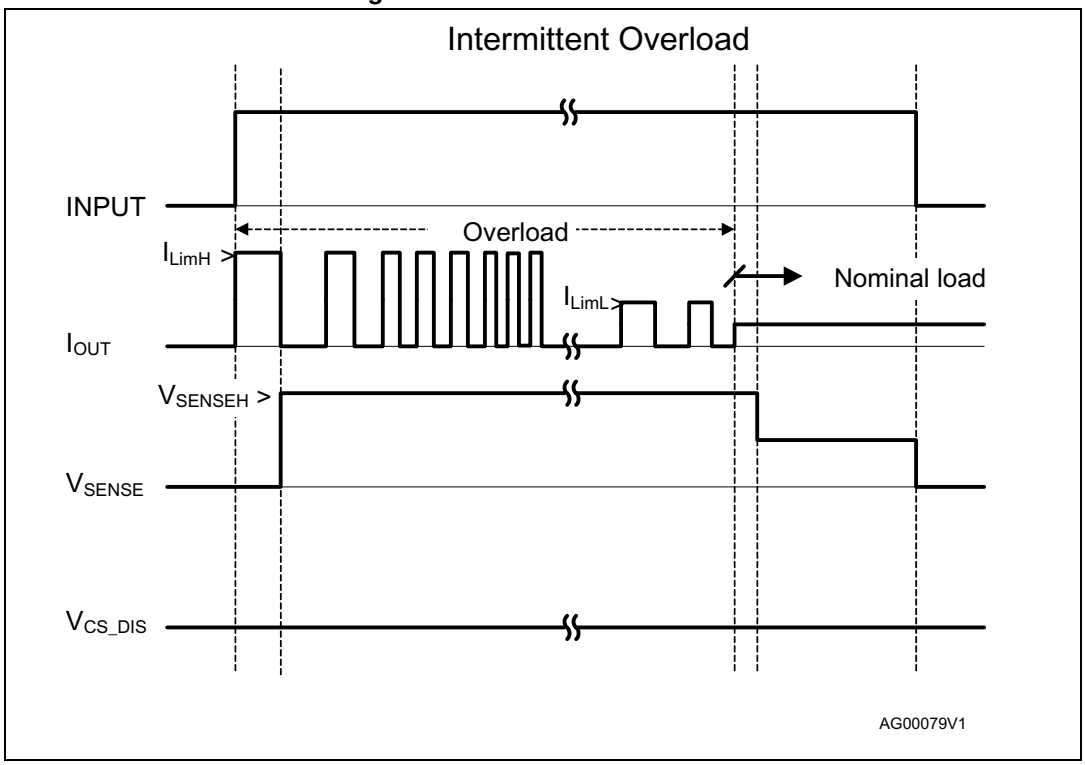


Figure 14. Off-state open-load with external circuitry

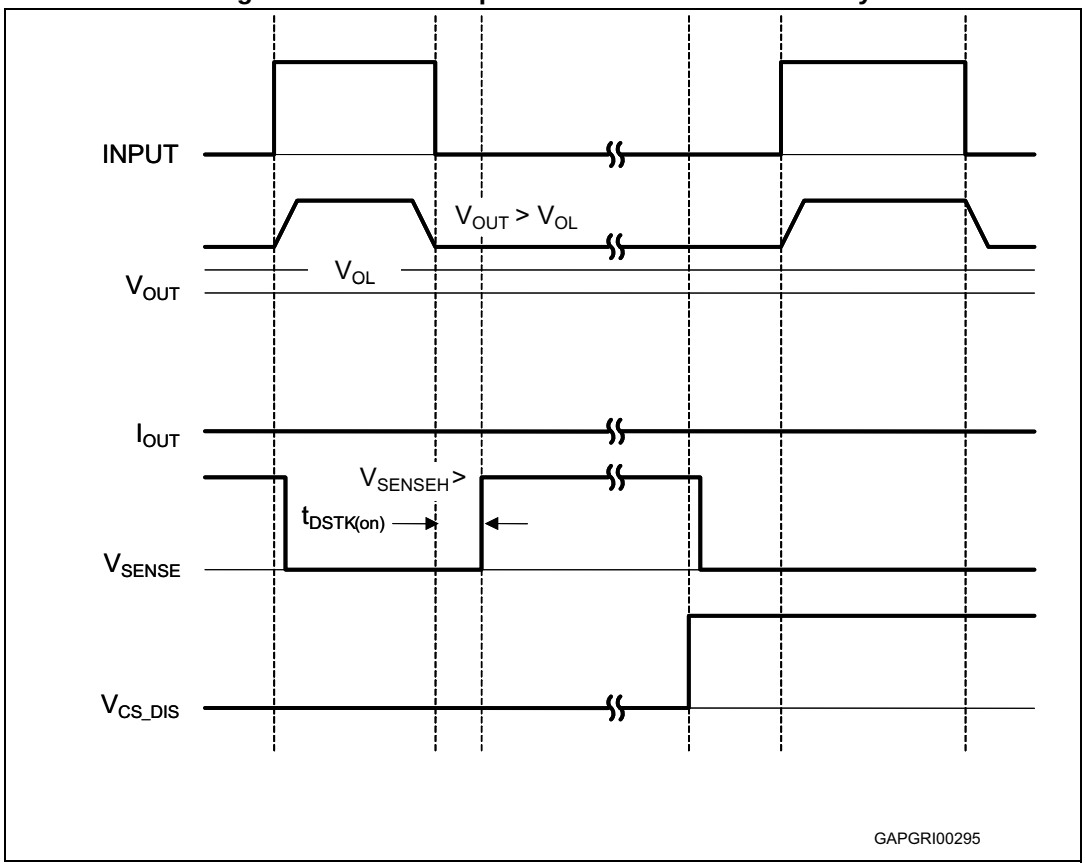


Figure 15. Short to V_{CC}

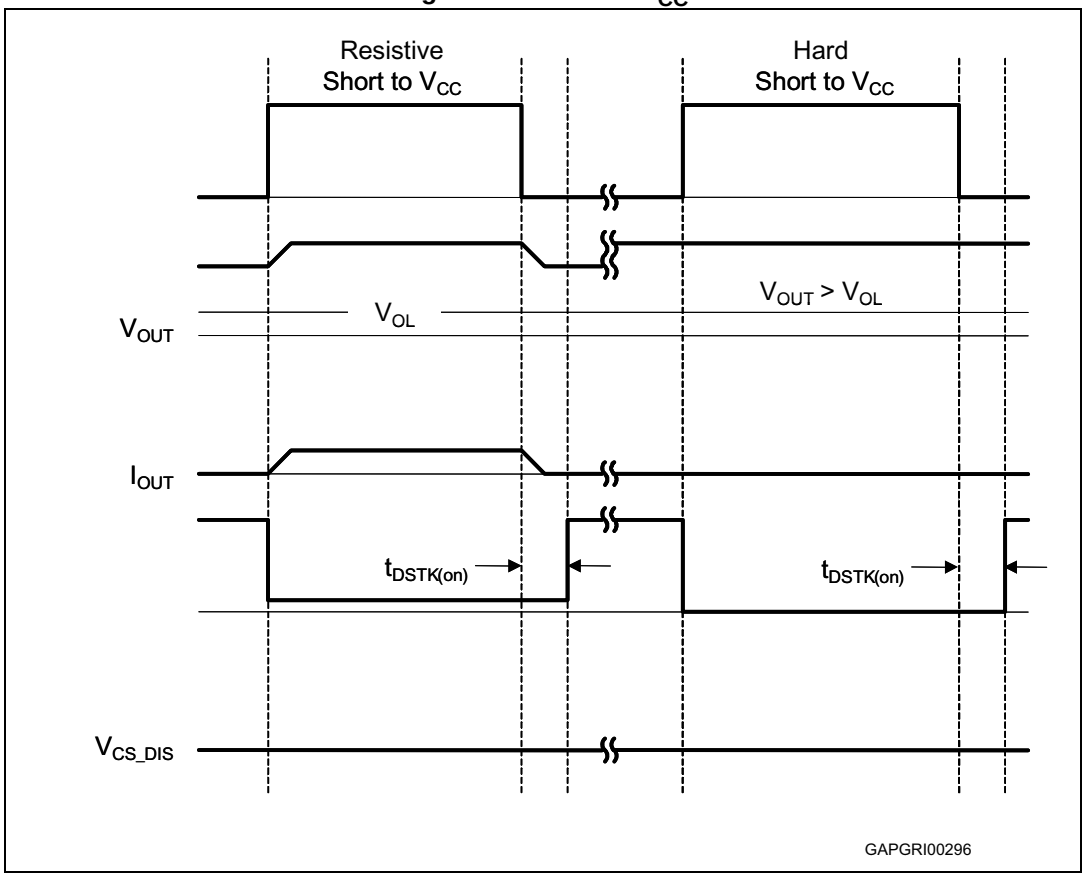
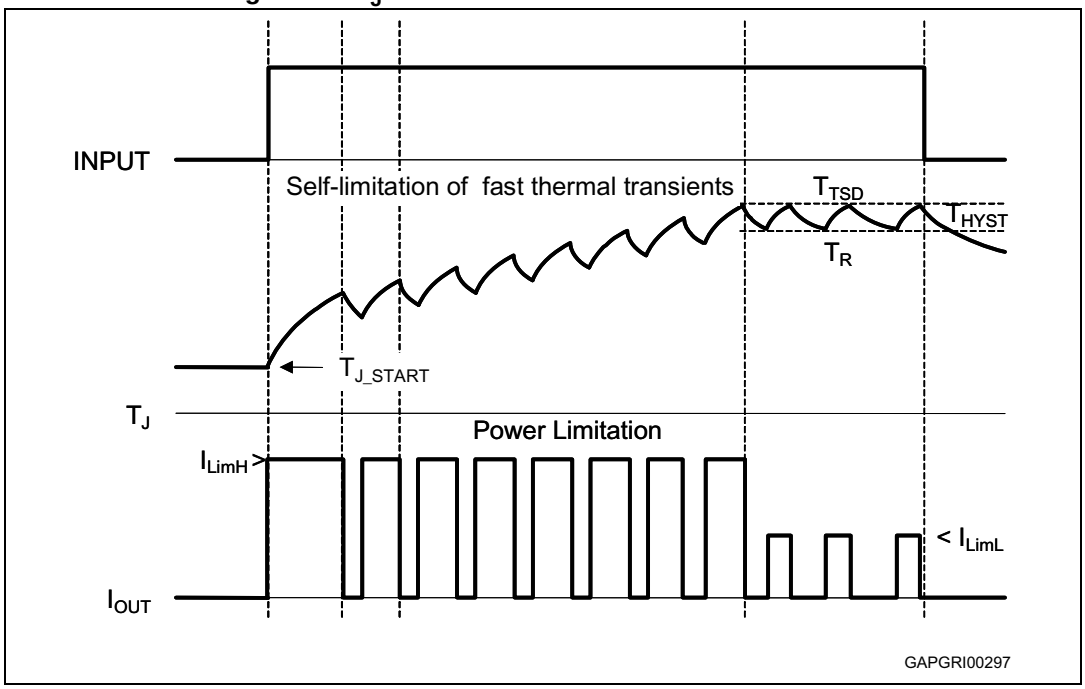


Figure 16. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. Off-state output current

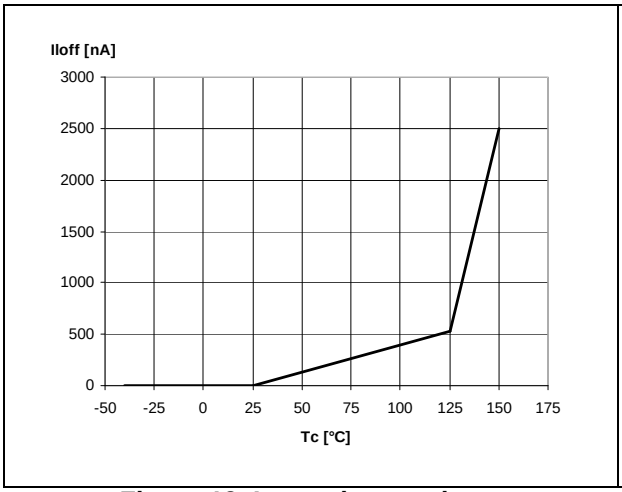


Figure 18. High level input current

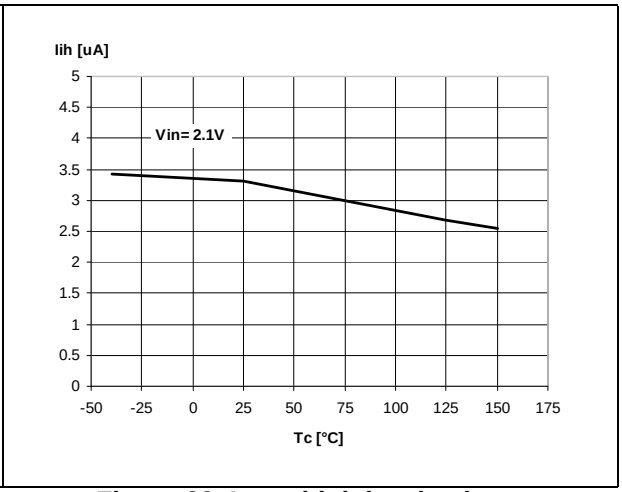


Figure 19. Input clamp voltage

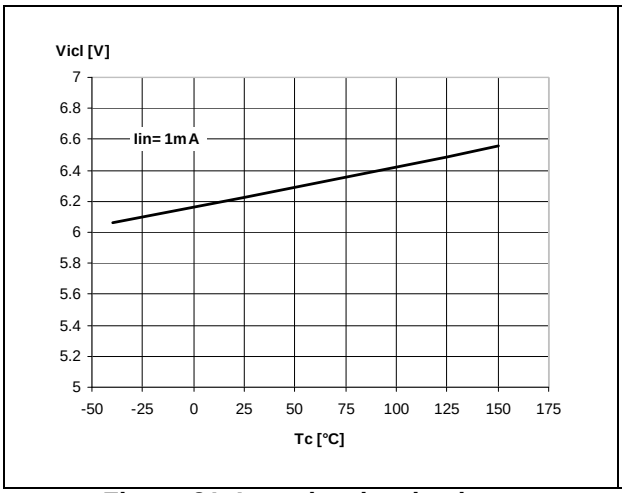


Figure 20. Input high level voltage

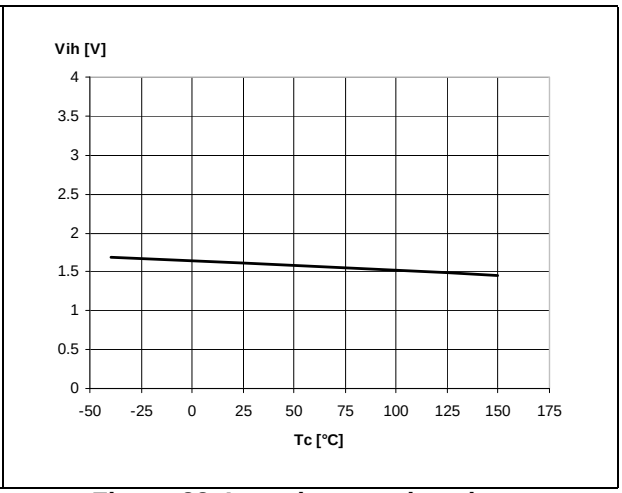


Figure 21. Input low level voltage

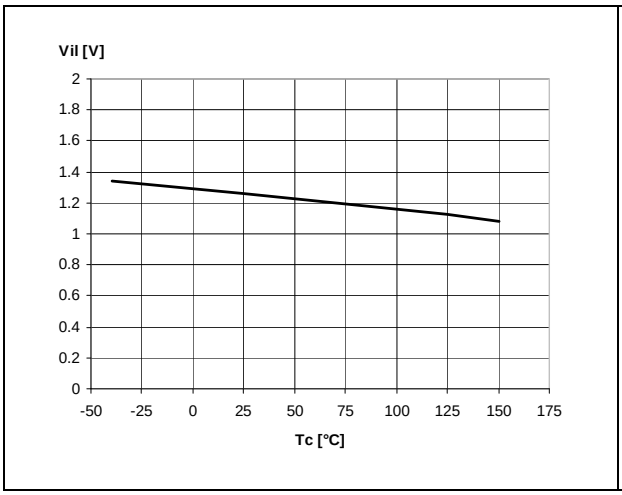


Figure 22. Input hysteresis voltage

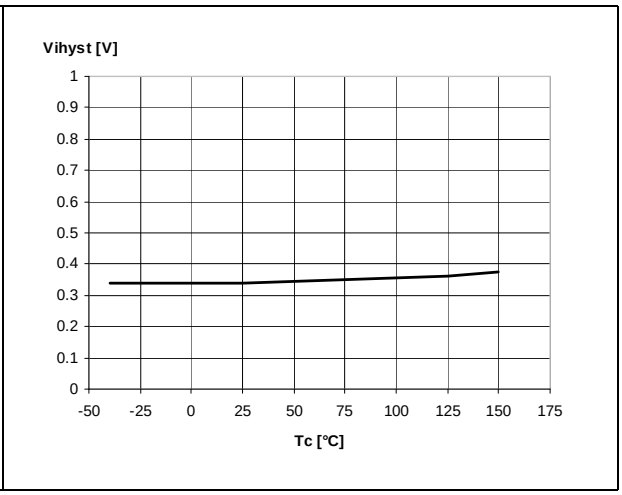


Figure 23. On-state resistance vs T_{case}

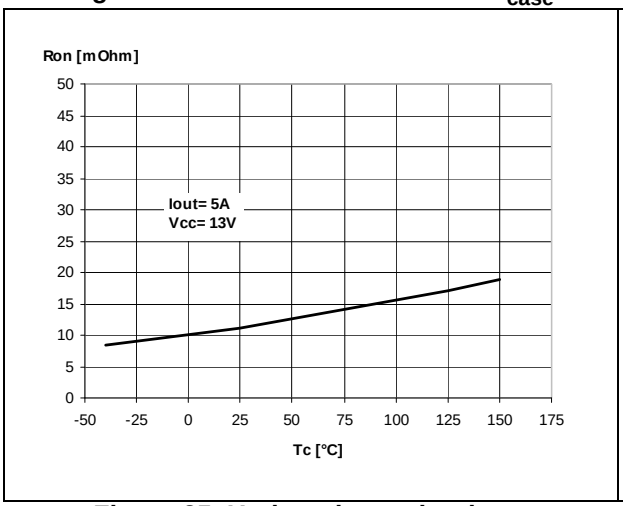


Figure 24. On-state resistance vs V_{CC}

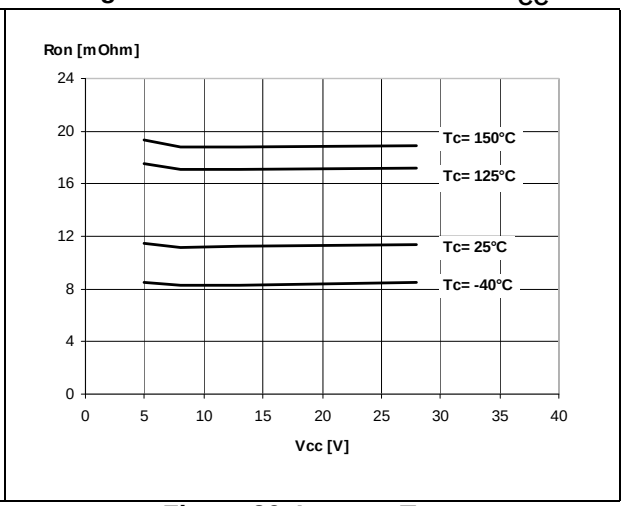


Figure 25. Undervoltage shutdown

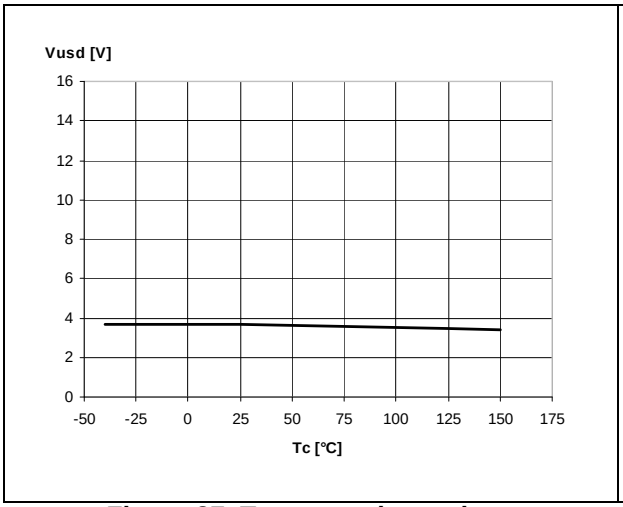


Figure 26. I_{LIMH} vs T_{case}

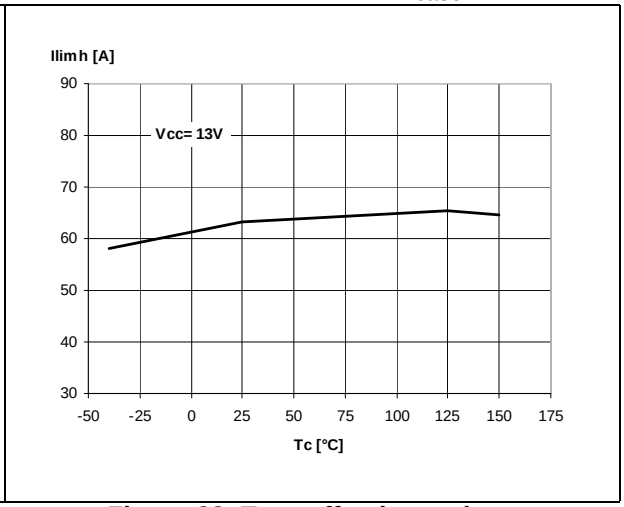


Figure 27. Turn-on voltage slope

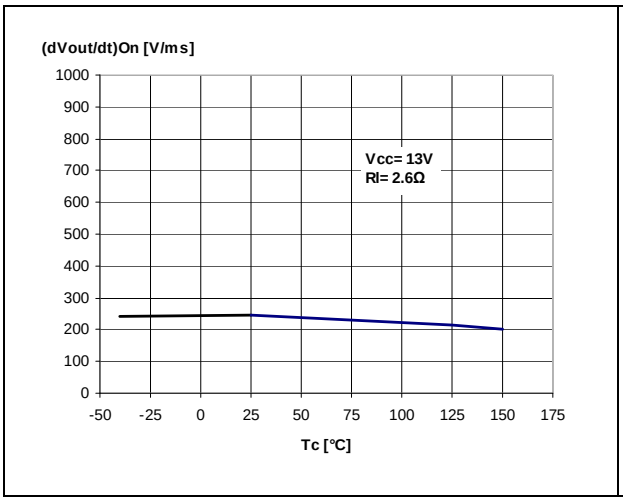


Figure 28. Turn-off voltage slope

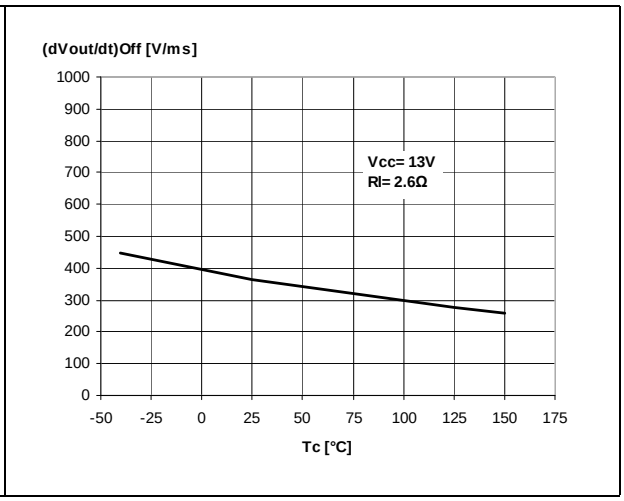


Figure 29. CS_DIS clamp voltage

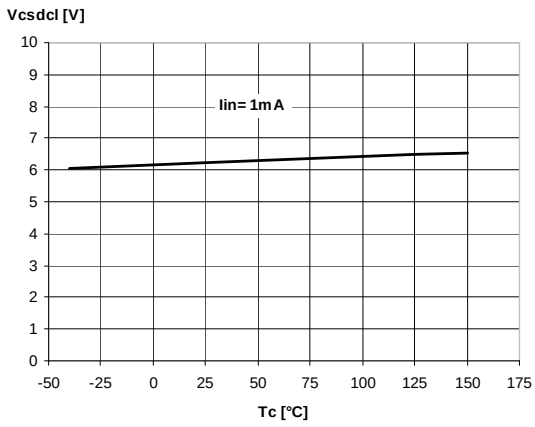


Figure 30. Low level CS_DIS voltage

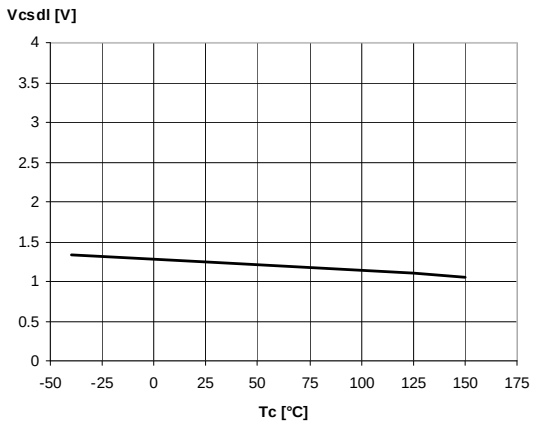
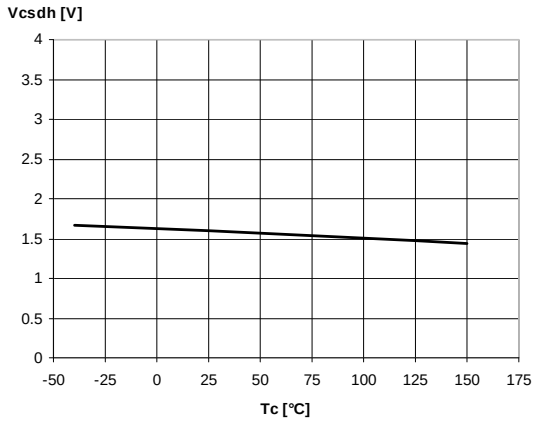
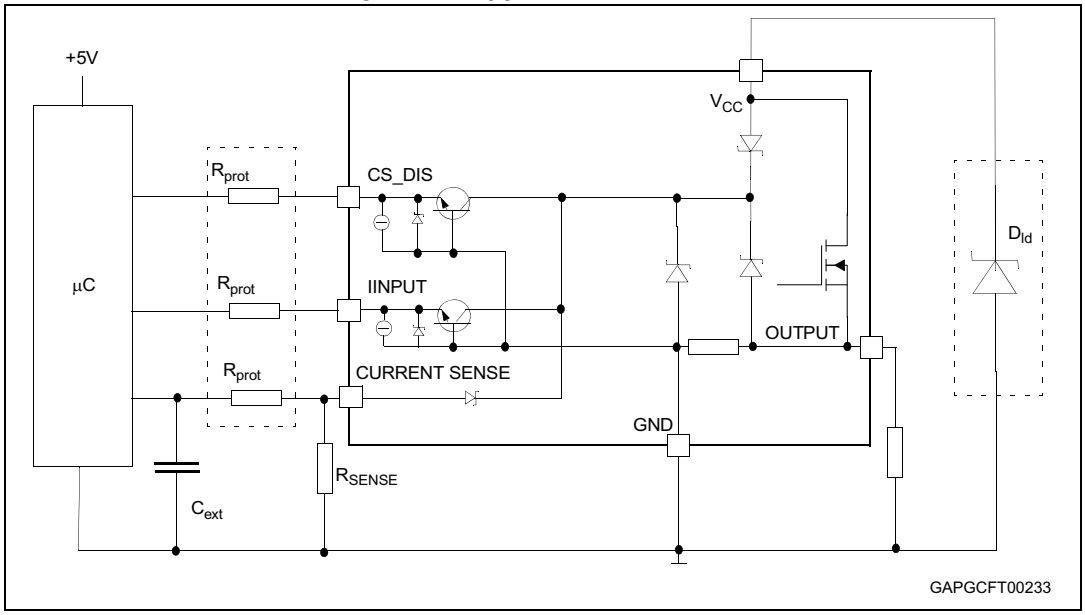


Figure 31. High level CS_DIS voltage



3 Application information

Figure 32. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CCPK} max rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.2 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pin is pulled negative to approximately -1.5 V. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/Os pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$$v_{ccpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH})/I_{IHmax}$$

Calculation example:

For V_{CCpeak} = - 1.5 V; $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

$$75\ \Omega \leq R_{prot} \leq 240\ k\Omega.$$

Recommended values: R_{prot} =10 kΩ, C_{EXT} =10 nF.

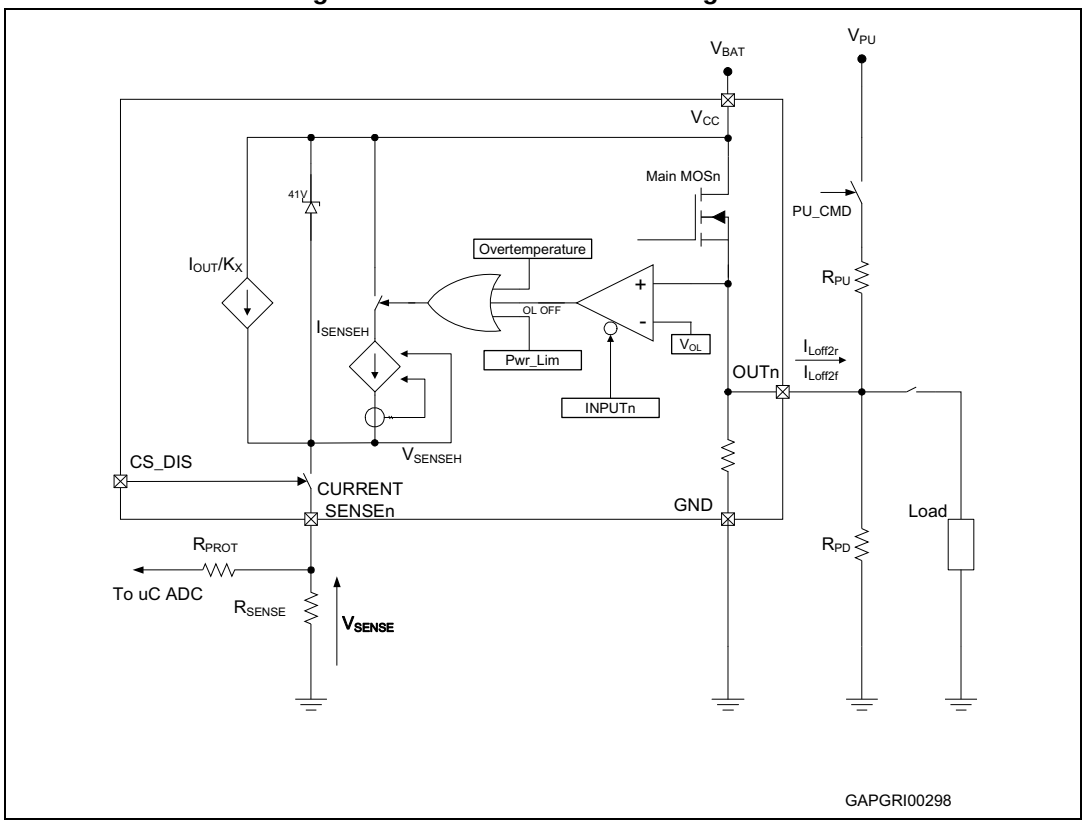
3.3 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 33: Current sense and diagnostic*):

- **Current mirror of the load current in normal operation,** delivering a current proportional to the load one according to a know ratio $\mathbf{K_X}$.
  The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE}. Linearity between I_{OUT} and V_{SENSE} is ensured up to 5 V minimum (see parameter V_{SENSE} in *Table 7: Current sense (8V<V_{CC}<18V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 7: Current sense (8V<V_{CC}<18V)*).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Table 11: Truth table*):
  - Power limitation activation
  - Overtemperature
  - Short to V_{CC} in off-state
  - Open load in off-state with additional external components.

A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high-impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 33. Current sense and diagnostic



3.3.1 Short to V_{CC} and off-state open-load detection

Short to V_{CC}

A short-circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device OFF-state. Small or no current is delivered by the current sense during the ON-state depending on the nature of the short-circuit.

Off-state open-load with external circuitry

Detection of an open load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

An external pull-down resistor R_{PD} connected between output and GND is mandatory to avoid misdetection in case of floating outputs in off-state (see *Figure 33: Current sense and diagnostic*).

R_{PD} must be selected in order to ensure $V_{OUT} < V_{OLmin}$ unless pulled-up by the external circuitry:

Equation 2

$$v_{out}\big|_{Pull-up\_off} = R_{PD} \cdot I_{L(off2)f} < V_{OLmin} = 2V$$

$R_{PD} \leq 22\ k\Omega$ is recommended.

For proper open load detection in off-state, the external pull-up resistor must be selected according to the following formula:

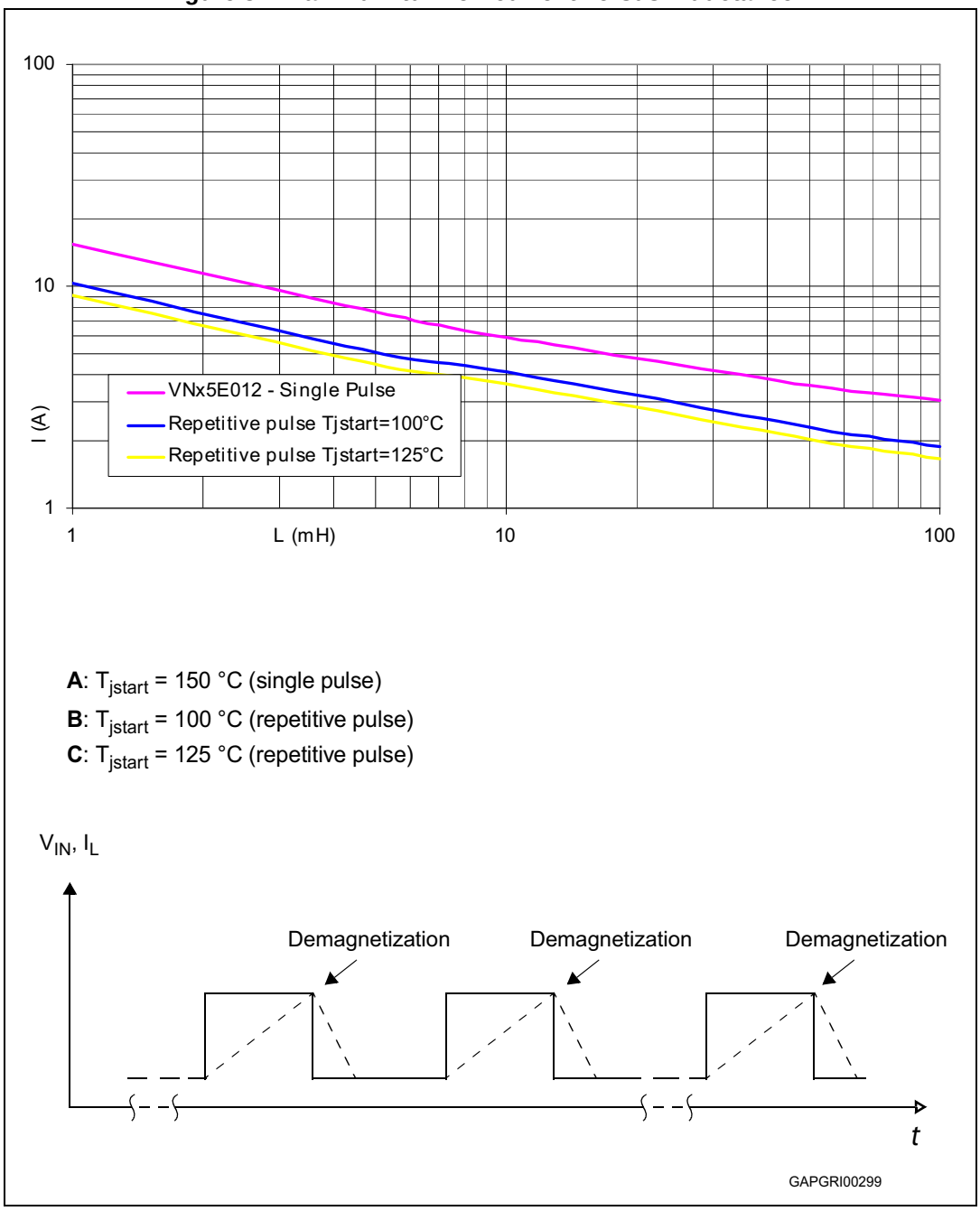
Equation 3

$$V_{OUT}\big|_{Pull-up\_ON} = \frac{(R_{PD} \cdot V_{PU}) - (R_{PU} \cdot R_{PD} \cdot I_{L(off2)r})}{(R_{PU} + R_{PD})} > V_{OLmax} = 4\,V$$

For the values of V_{OLmin} ,V_{OLmax}, $I_{L(off2)r}$ and $I_{L(off2)f}$ (see *Table 8: Open-load detection (8V<V_{CC}<18V)*).

3.4 Maximum demagnetization energy (V_{CC} = 13.5 V)

Figure 34. Maximum turn-off current versus inductance(1)



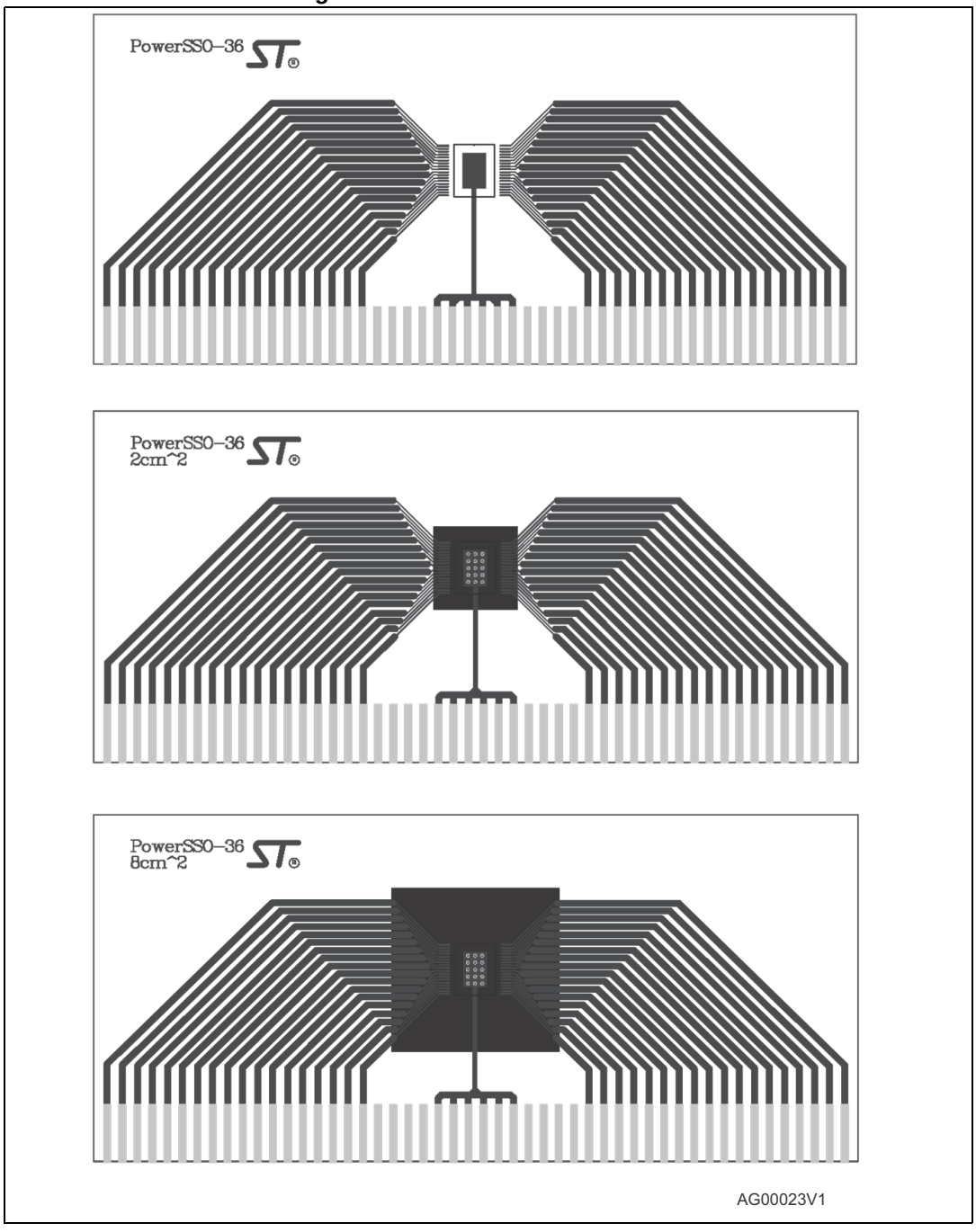
1. Values are generated with R_L = 0 Ω.

   In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-36 thermal data

Figure 35. PowerSSO-36 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 129mm x 60mm, PCB thickness=1.6mm, Cu thickness=70µm (front and back side), Copper areas: from minimum pad lay-out to 8cm^2).

Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

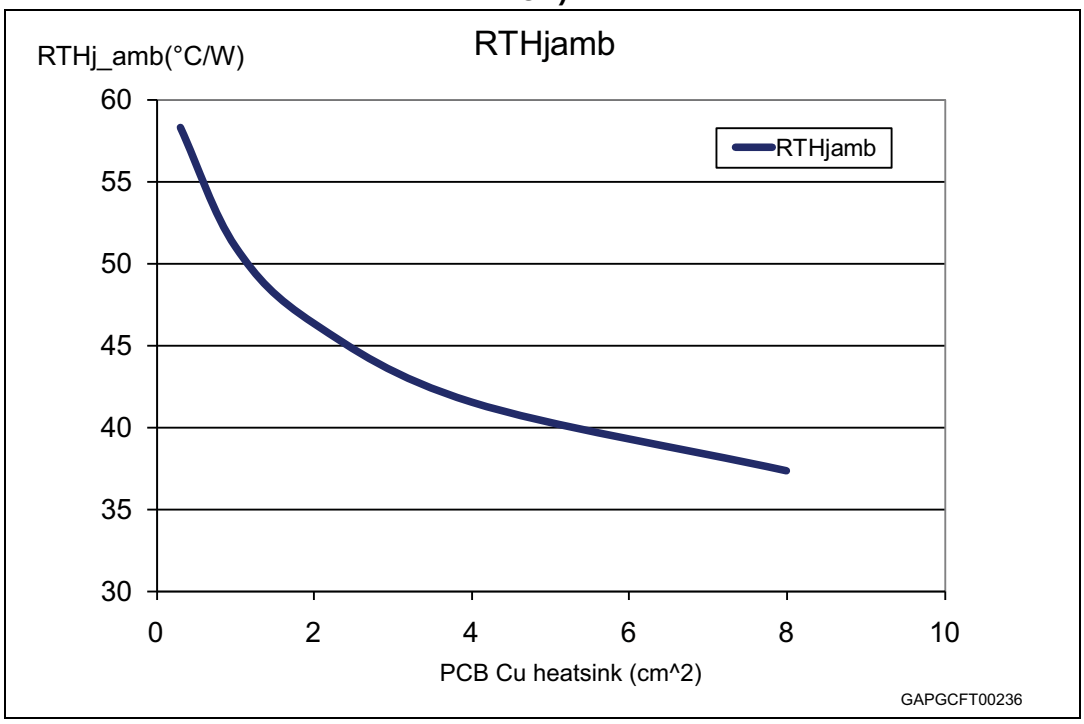


Figure 37. PowerSSO-36 Thermal impedance junction ambient single pulse (one channel ON)

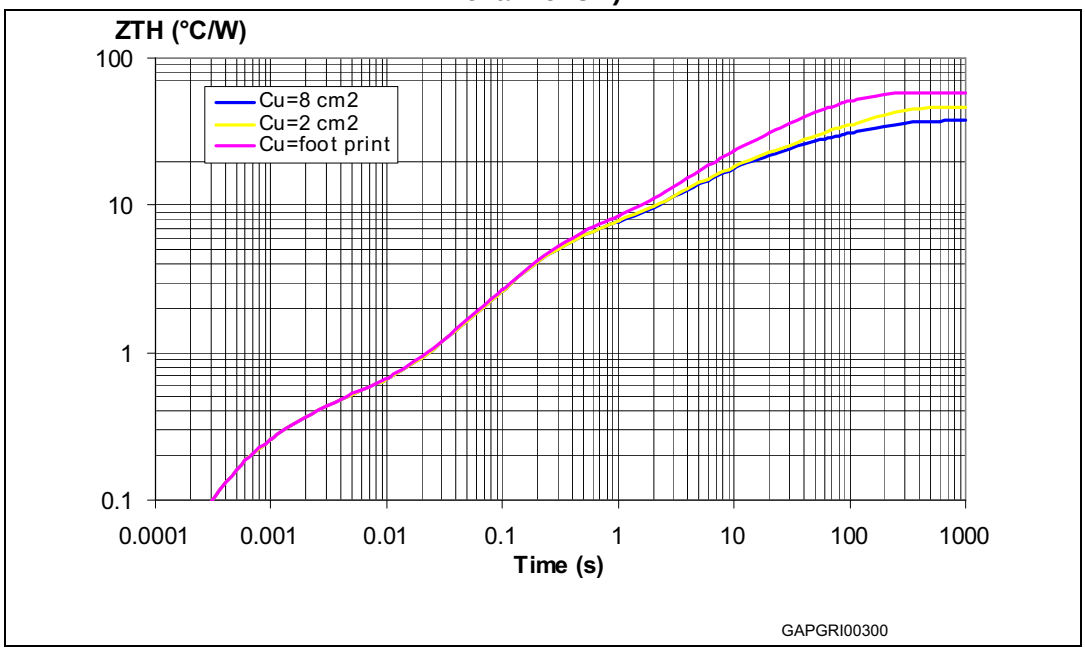
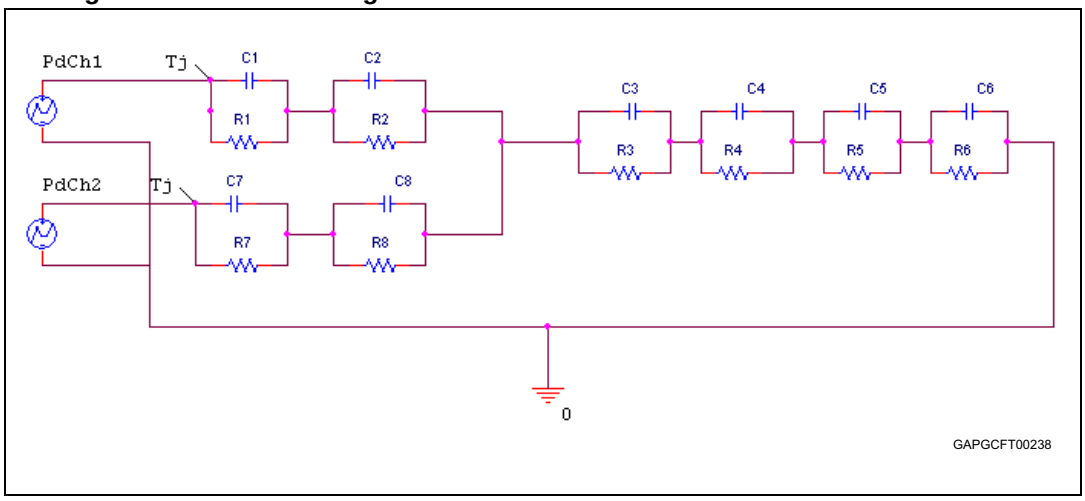


Figure 38. Thermal fitting model of a double channel HSD in PowerSSO-36(1)



1. The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered

Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where:

Equation 5

$$\delta = t_p / T$$

Table 15. Thermal parameter

Area/island (cm^2)	Footprint	2	8
R1 (°C/W)	0.1		
R2 (°C/W)	0.3		
R3 (°C/W)	5		
R4 (°C/W)	8		
R5 (°C/W)	18	10	10
R6 (°C/W)	27	23	14
R7 (°C/W)	0.1		
R8 (°C/W)	0.3		
C1 (W.s/°C)	0.0025		
C2 (W.s/°C)	0.005		
C3 (W.s/°C)	0.04		
C4 (W.s/°C)	0.5		
C5 (W.s/°C)	1	2	2
C6 (W.s/°C)	3	6	9

Table 15. Thermal parameter (continued)

Area/island (cm^2)	Footprint	2	8
C7 (W.s/°C)	0.0025		
C8 (W.s/°C)	0.005		

5 Package information

5.1 ECOPACK® package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

5.2 PowerSSO-36 mechanical data

Figure 39. PowerSSO-36 package dimensions

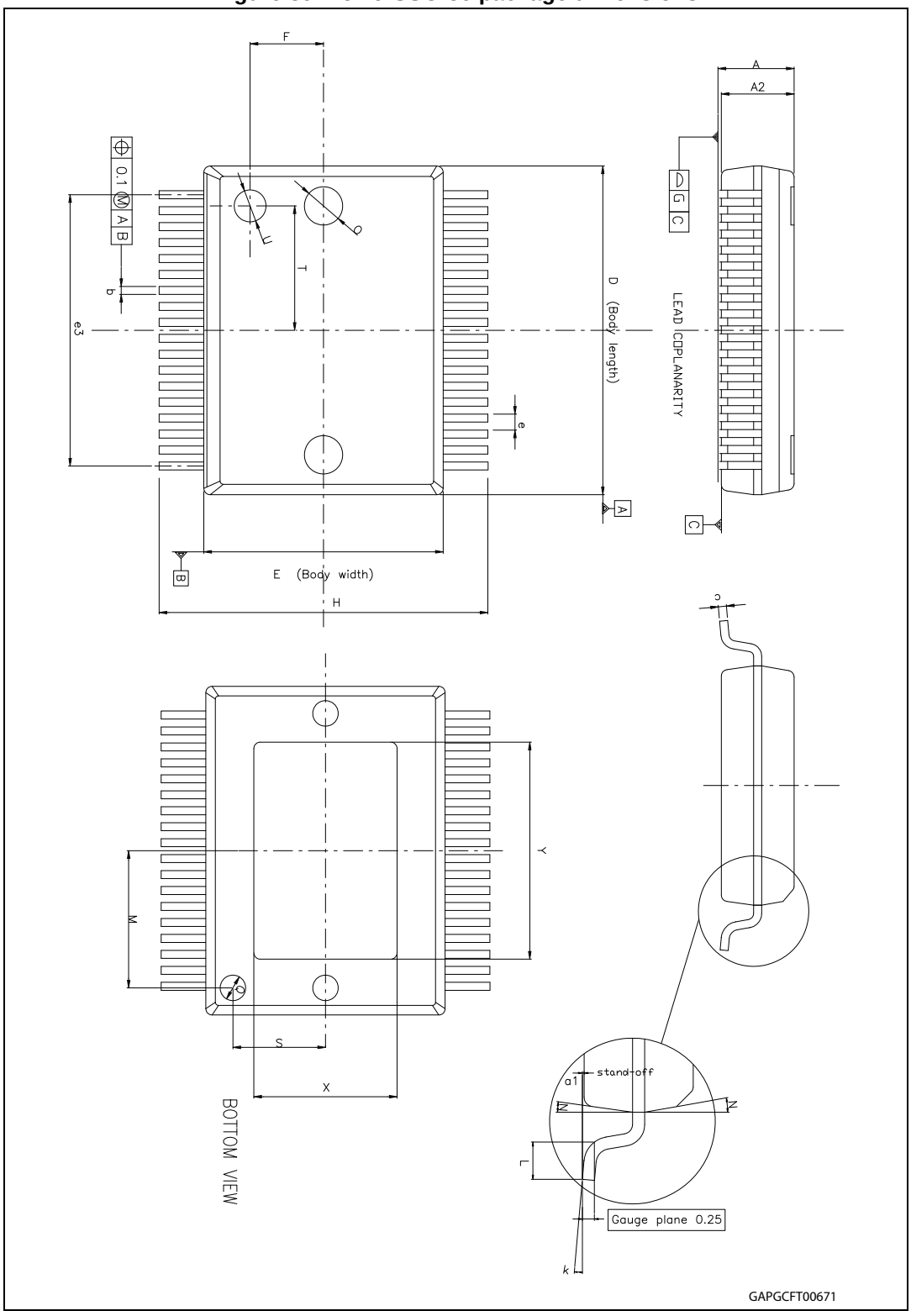
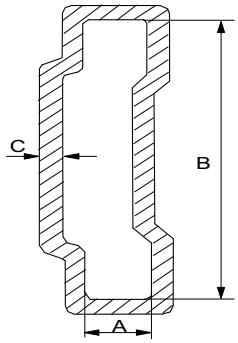


Table 16. PowerSSO-36 mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	2.15	-	2.47
A2	2.15	-	2.40
a1	0	-	0.075
b	0.18	-	0.36
c	0.23	-	0.32
D	10.10	-	10.50
E	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
G	-	-	0.1
G1	-	-	0.06
H	10.1	-	10.5
h	-	-	0.4
L	0.55	-	0.85
N	-	-	10 deg
X	4.1	-	4.7
Y	6.5	-	7.1

5.3 Packing information

Figure 40. PowerSSO-36 tube shipment (no suffix)

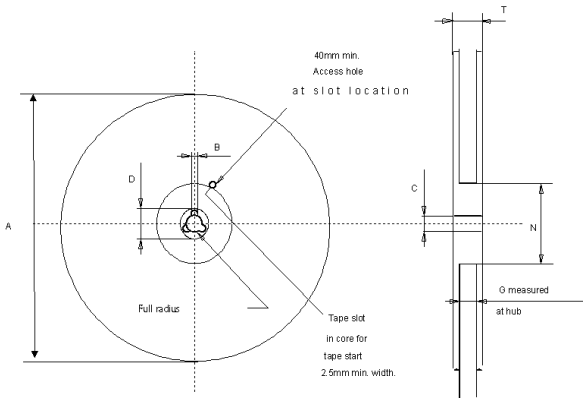


GAPGCFT00002

Base Q.ty	49
Bulk Q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 41. PowerSSO-36 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

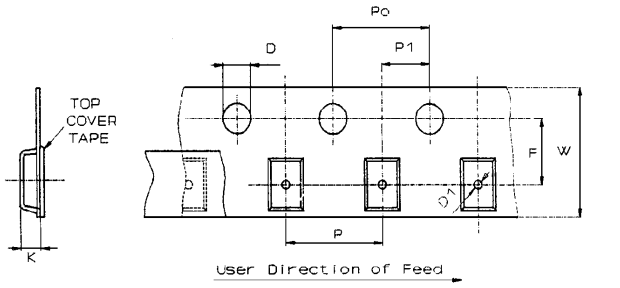
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	100
T (max)	30.4

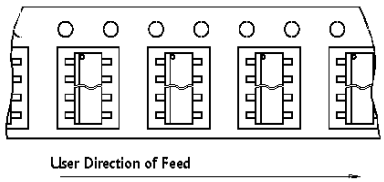
TAPE DIMENSIONS

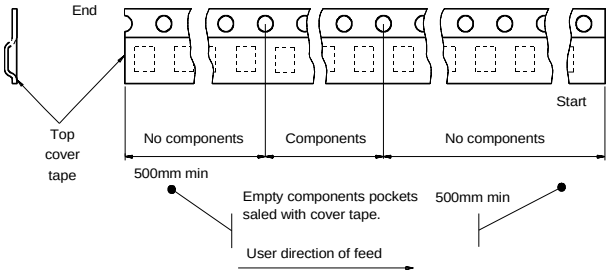
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Order codes

Table 17. Device summary

package	Order codes	
	Tube	Tape and reel
PowerSSO-36	VND5E012AY-E	VND5E012AYTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
05-Jun-2007	1	Initial release.
21-Oct-2009	2	Updated *Figure 3: Current and voltage conventions*. Updated following tables: – *Table 3: Absolute maximum ratings* – *Table 4: Thermal data* – *Table 5: Power section* – *Table 6: Switching (VCC = 13V; Tj = 25°C)* – *Table 7: Current sense (8V<V_{CC}<18V)* – *Table 8: Open-load detection (8V<V_{CC}<18V)* Added following figures: – *Figure 7: Maximum current sense ratio drift vs load current* – *Figure 8: Switching characteristics* – *Figure 9: Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled)* Added *Section 2.4: Waveforms* and *Section 2.5: Electrical characteristics curves*. Apdated *Chapter 3: Application information*. Updated *Section 4.1: PowerSSO-36 thermal data*: – Added *Figure 35: PowerSSO-36 PC board*, *Figure 36: Rthj-amb vs PCB copper area in open box free air condition (one channel ON)* and *Figure 37: PowerSSO-36 Thermal impedance junction ambient single pulse (one channel ON)* – Updated *Figure 38: Thermal fitting model of a double channel HSD in PowerSSO-36*(1) – Added *Table 15: Thermal parameter*. Updated *Section 5.1: ECOPACK® package*.
03-Dec-2009	3	Updated *Section 4.1: PowerSSO-36 thermal data*
09-July-2012	4	Updated *Figure 39: PowerSSO-36 package dimensions*
20-Sep-2013	5	Updated Disclaimer
28-Oct-2013	6	Updated footnote 2 into the *Table 12: Electrical transient requirements (part 1)* and *Table 13: Electrical transient requirements (part 2)*.

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