

# NB3N108K

## 3.3V Differential 1:8 Fanout Clock Data Driver with HCSL Outputs

### Description

The NB3N108K is a differential 1:8 Clock fanout buffer with High-speed Current Steering Logic (HCSL) outputs optimized for ultra low propagation delay variation. The NB3N108K is designed with HCSL PCI Express clock distribution and FBDIMM applications in mind.

Inputs can directly accept differential LVPECL, LVDS, HCSL signals per Figures 7, 8, and 9. Single-ended LVPECL, HCSL, LVCMOS, or LVTTTL levels are accepted with a proper external  $V_{th}$  reference supply per Figures 4 and 10. Input pins incorporate separate internal 50  $\Omega$  termination resistors allowing additional single ended system interconnect flexibility.

Output drive current is set by connecting a 475  $\Omega$  resistor from IREF (Pin 1) to GND per Figure 6. Outputs can also interface to LVDS receivers when terminated per Figure 11.

The NB3N108K specifically guarantees low output-to-output skews. Optimal design, layout, and processing minimize skew within a device and from device to device. System designers can take advantage of the NB3N108K's performance to distribute low skew clocks across the backplane or the motherboard.

### Features

- Typical Input Clock Frequency 100, 133, 166, or 400 MHz
- 220 ps Typical Rise and Fall Times
- 800 ps Typical Propagation Delay
- $\Delta t_{pd}$  100 ps Maximum Propagation Delay Variation Per Each Diff Pair
- 0.1 ps Typical Integrated Phase Jitter RMS
- Operating Range:  $V_{CC} = 3.0$  V to 3.6 V with  $V_{EE} = 0$  V
- Differential HCSL Output Levels
- LVDS Output Levels with Interface Termination
- These are Pb-Free Devices

### Applications

- Clock Distribution
- PCIe I, II, III
- Networking and Communications
- High End Computing
- Routers

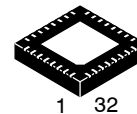
### End Products

- Servers
- FBDIMM Memory Card
- Ethernet Switch/Routers



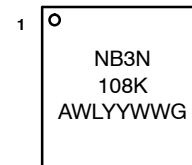
ON Semiconductor®

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QFN32  
MN SUFFIX  
CASE 488AM

### MARKING DIAGRAM\*



- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*For additional marking information, refer to

Application Note AND8002/D.

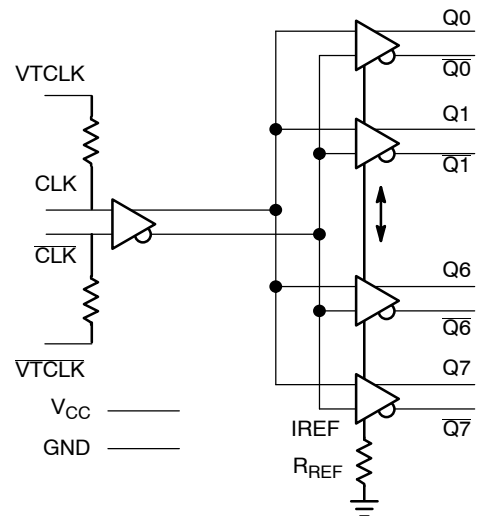
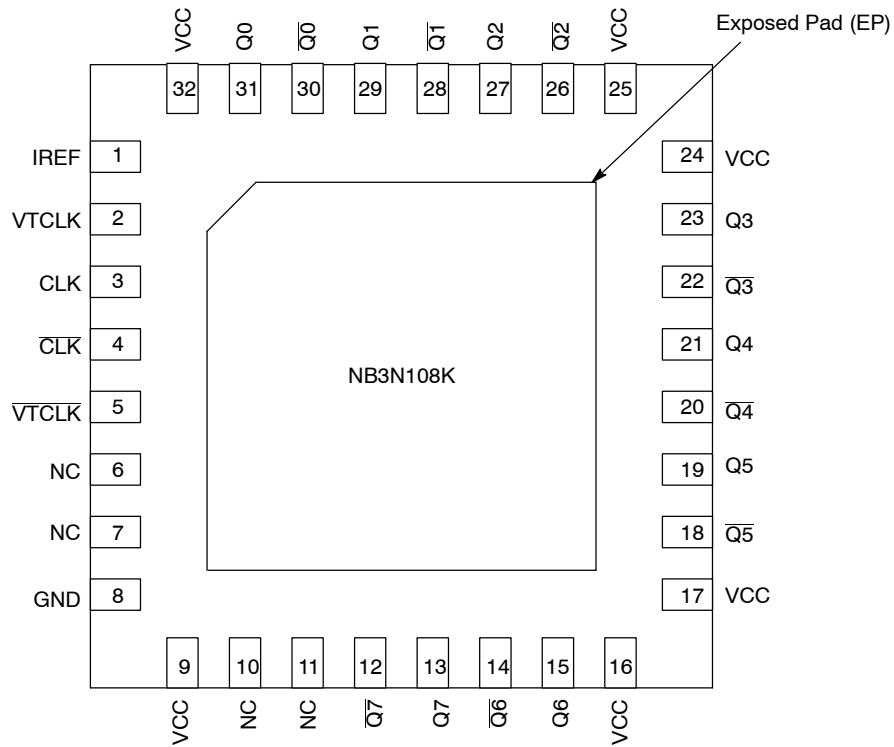


Figure 1. Simplified Logic Diagram

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

# NB3N108K



**Figure 2. Pinout Configuration (Top View)**

**Table 1. PIN DESCRIPTION**

Pin	Name	I/O	Description
1	IREF		Use the IREF pin to set the output drive. Connect a 475 $\Omega$ RREF resistor from the IREF pin to GND to produce 2.6 mA of IREF current. A current mirror multiplies IREF by a factor of 5.4x to force 14 mA through a 50 $\Omega$ output load. See Figures 6 and 12.
2, 5	VTCLK, VTCLK	-	Internal 50 $\Omega$ Termination Resistor connection Pins. In the differential configuration when the input termination pins are connected to the common termination voltage, and if no signal is applied then the device may be susceptible to self-oscillation.
3	CLK	LVPECL HCSL, LVDS Input	Clock (TRUE) Input
4	$\overline{\text{CLK}}$	LVPECL HCSL, LVDS Input	Clock (INVERT) Input
12, 14, 18, 20, 22, 26, 28, 30	Q[7-0]b	HCSL or LVDS (Note 1) Output	Output (INVERT) (Note 1)
13, 15, 19, 21, 23, 27, 29, 31	Q[7-0]	HCSL or LVDS (Note 1) Output	Output (TRUE) (Note 1)
6, 7, 10, 11	NC		No Connect
8	GND	-	Supply Ground. GND pin must be externally connected to power supply to guarantee proper operation.
9, 16, 17, 24, 25, 32	VCC	-	Positive Voltage Supply pin. VCC pins must be externally connected to a power supply to guarantee proper operation.
Exposed Pad	EP	GND	Exposed Pad. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a sufficient heat-sinking conduit for proper thermal operation and electrically connected to the circuit board ground (GND).

1. Outputs can also interface to LVDS receiver when terminated per Figure 11.

# NB3N108K

**Table 2. ATTRIBUTES**

Characteristic		Value
ESD Protection	Human Body Model	>2 kV
	Machine Model	200 V
Moisture Sensitivity (Note 2)	QFN-52	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		286
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS** (Note 3)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		4.6	V
V <sub>I</sub>	Positive Input	GND = 0 V		GND - 0.3 ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	V
I <sub>OUT</sub>	Output Current	Continuous Surge		50 100	mA mA
T <sub>A</sub>	Operating Temperature Range	QFN32		-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfpm 500 lfpm	QFN32 QFN32	31 27	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	2S2P (Note 3)	QFN32	12	°C/W
T <sub>sol</sub>	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard 51-6, multilayer board - 2S2P (2 signal, 2 power) with eight filled thermal vias under exposed pad.

# NB3N108K

**Table 4. DC CHARACTERISTICS** ( $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$  Note 4)

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{GND}$	GND Supply Current (All Outputs Loaded)		60	90	mA
$I_{CC}$	Power Supply Current (All Outputs Loaded)		190	230	mA
$I_{IH}$	Input HIGH Current		2.0	150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150	-2.0		$\mu\text{A}$
$R_{TIN}$	Internal Input Termination Resistor	45	50	55	$\Omega$

## DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED

$V_{th}$	Input Threshold Reference Voltage Range (Note 5)	350		$V_{CC} - 1000$	mV
$V_{IH}$	Single – Ended Input HIGH Voltage	$V_{th} + 150$		$V_{CC}$	mV
$V_{IL}$	Single – Ended Input LOW Voltage	GND		$V_{th} - 150$	mV

## DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 7, 8 and 9)

$V_{IHD}$	Differential Input HIGH Voltage	425		$V_{CC} - 850$	mV
$V_{ILD}$	Differential Input LOW Voltage	GND		$V_{CC} - 1000$	mV
$V_{ID}$	Differential Input Voltage ( $V_{IHD} - V_{ILD}$ )	150		$V_{CC} - 850$	mV
$V_{CMR}$	Input Common Mode Range	350		$V_{CC} - 1000$	mV

## HCSL OUTPUTS (Figure 4)

$V_{OH}$	Output HIGH Voltage	600	740	900	mV
$V_{OL}$	Output LOW Voltage	-150	0	150	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Measurements taken with with outputs loaded  $50\ \Omega$  to GND, see Figure 6. Connect a  $475\ \Omega$  resistor from IREF (Pin 1) to GND per Figure 6.
- $V_{th}$  is applied to the complementary input when operating in single ended mode per Figure 4.

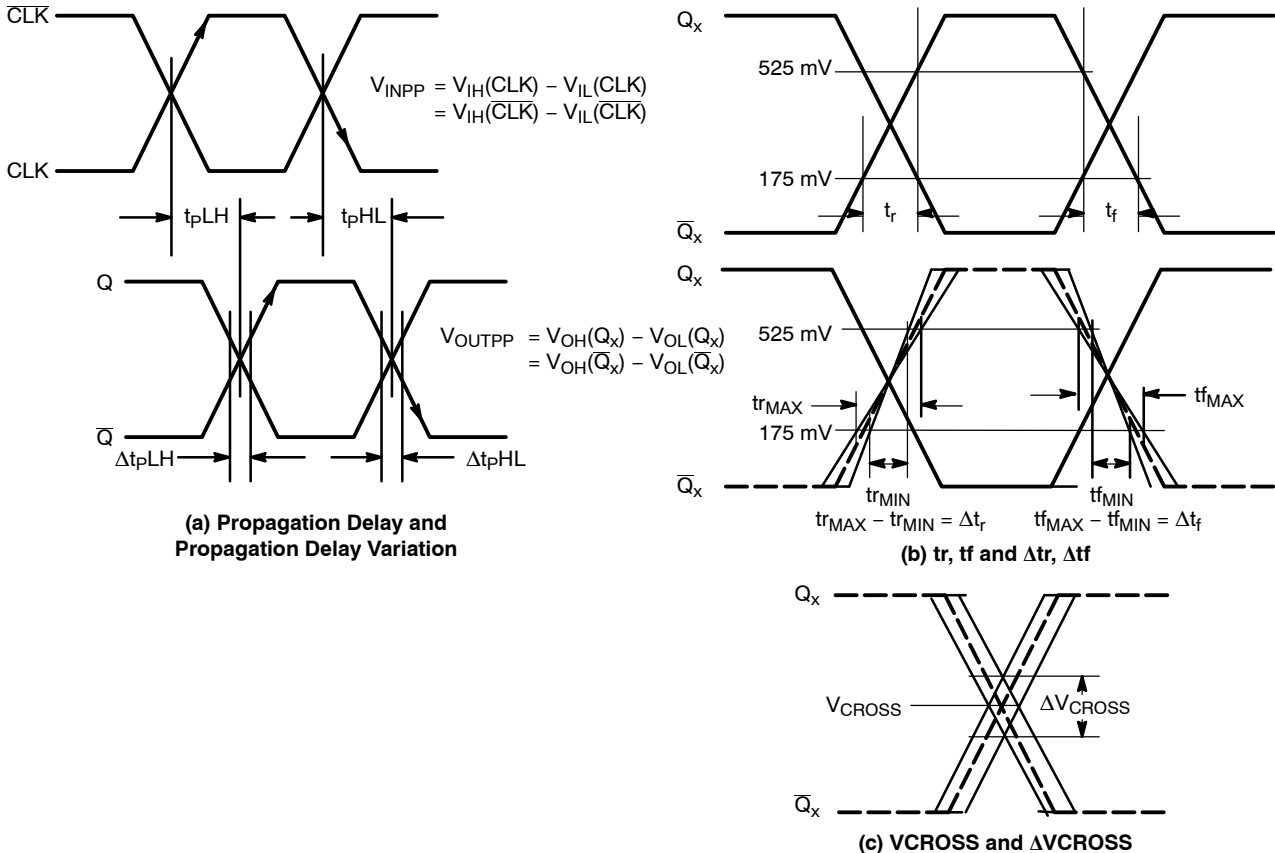
# NB3N108K

**Table 5. AC CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ ;  $-40^{\circ}\text{C to }+85^{\circ}\text{C}$  (Note 6)

Symbol	Characteristic	Min	Typ	Max	Unit
$V_{OUTPP}$	Output Voltage Amplitude (@ $V_{INPPmin}$ ) $f_{in} \leq 400\text{ MHz}$		725	1000	mV
$t_{PLH}$ , $t_{PHL}$	Propagation Delay (See Figure 3a) CLK/CLK to $Q_x/\bar{Q}_x$	550	800	1100	ps
$\Delta t_{PLH}$ , $\Delta t_{PHL}$	Propagation Delay Variation Per Each Diff Pair (Note 7) (See Figure 3a) CLK/CLK to $Q_x/\bar{Q}_x$			100	ps
$t_{SKEW}$	Duty Cycle Skew (Note 8) Within -Device Skew Device to Device Skew (Note 9)			20 100 150	ps
$t_{JIT\phi}$	Integrated Phase Jitter RMS (Note 10)		0.1		ps
$V_{INPP}$	Input Voltage Swing/Sensitivity (Differential Configuration)	0.150		$V_{CC} - 0.85$	V
$V_{CROSS}$	Absolute Crossing Magnitude Voltage (See Figure 3b)	250		550	mV
$\Delta V_{CROSS}$	Variation in Magnitude of $V_{CROSS}$ (See Figure 3b)			150	mV
$t_r, t_f$	Absolute Magnitude in Output Risetime and Falltime (from 175 mV to 525 mV) (See Figure 3b) $Q_x, \bar{Q}_x$	150	220	400	ps
$\Delta t_r, \Delta t_f$	Variation in Magnitude of Risetime and Falltime (Single-Ended) (See Figure 3b) $Q_x, \bar{Q}_x$			125	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Measured by forcing  $V_{INPP}$  (MIN) from a 50% duty cycle. Measurement taken with all outputs loaded  $50\ \Omega$  to GND per Figure 6. Connect a  $475\ \Omega$  resistor from IREF (Pin 1) to GND per Figure 6.
7. Measured from the input pair crosspoint to each single output pair crosspoint across temp and voltage ranges per Figure 3.
8. Duty cycle skew is measured between differential outputs using the deviations of the sum of  $T_{pw-}$  and  $T_{pw+}$ .
9. Skew is measured between outputs under identical transition conditions @ 50 MHz.
10. Phase noise integrated from 12 kHz to 20 MHz.



**Figure 3. AC Reference Measurement**

# NB3N108K

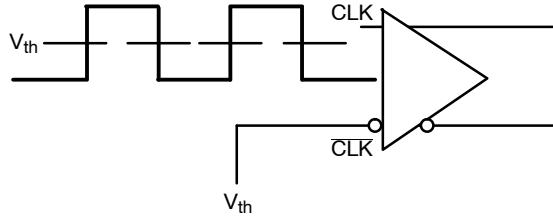


Figure 4. Single-Ended Interconnect  $V_{th}$  Reference Voltage

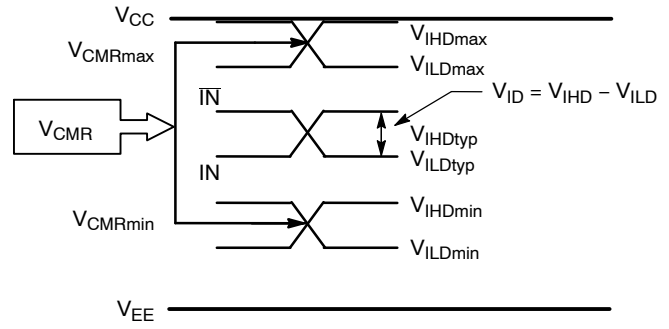
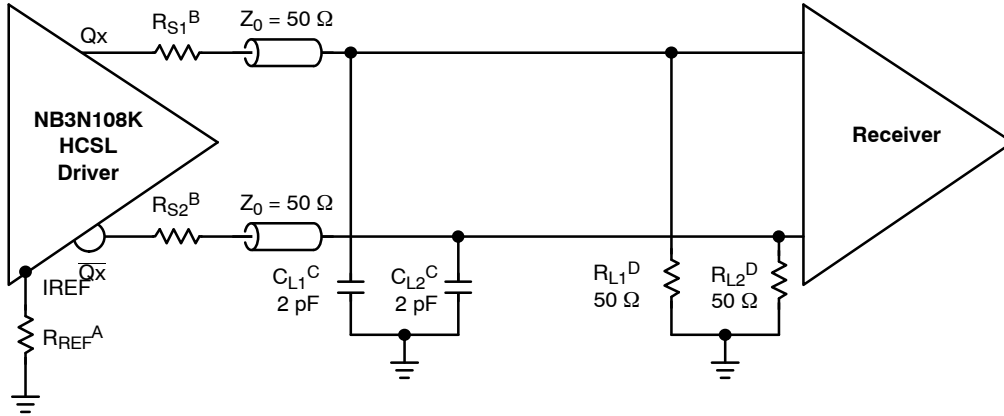
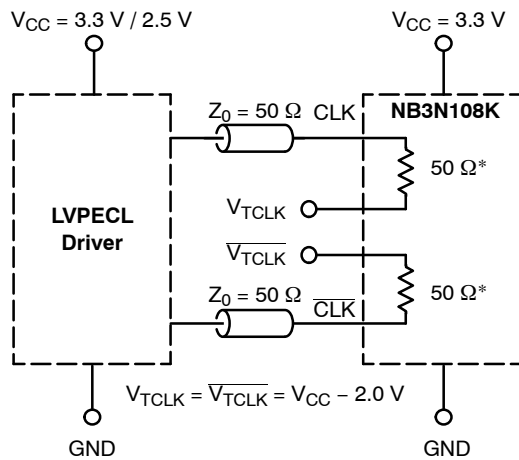


Figure 5.  $V_{th}$  Diagram



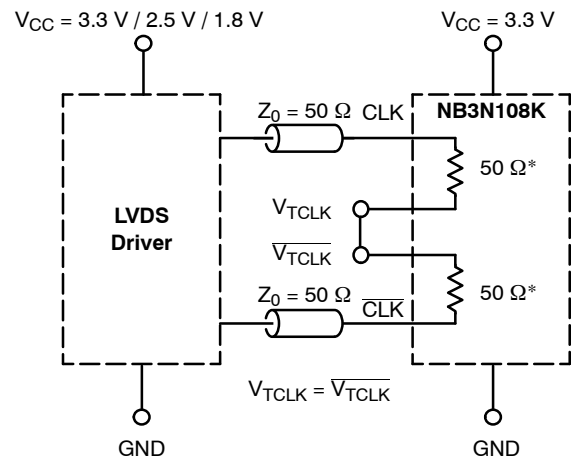
- A. Connect 475  $\Omega$  resistor RREF from IREF pin to GND.
- B.  $R_{S1}$ ,  $R_{S2}$ : 0  $\Omega$  for Test and Evaluation. Select to Minimizing Ringing.
- C.  $C_{L1}$ ,  $C_{L2}$ : Receiver Input Simulation (for test only not added to application circuit).
- D.  $D_{L1}$ ,  $D_{L2}$  Termination and Load Resistors Located at Received Inputs.

Figure 6. Typical Termination Configuration for Output Driver and Device Evaluation



\*RTIN, Internal Input Termination Resistor

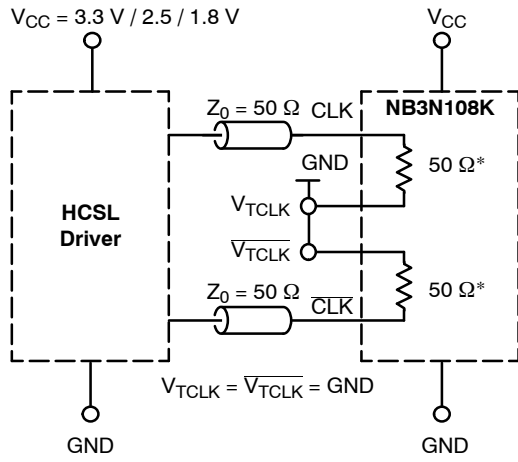
Figure 7. LVPECL Interface



\*RTIN, Internal Input Termination Resistor

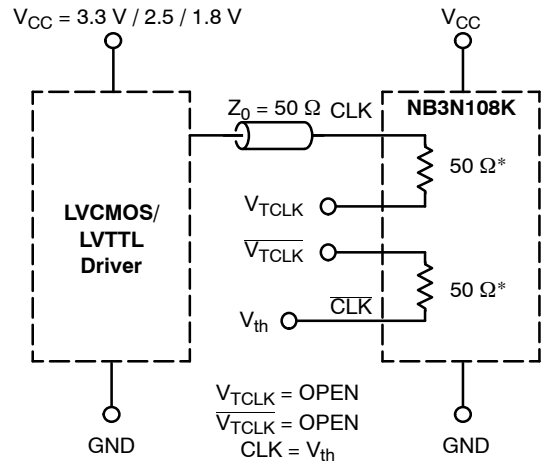
Figure 8. LVDS Interface

# NB3N108K



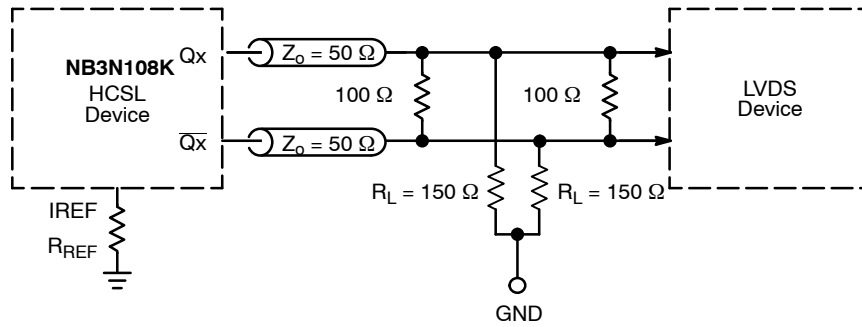
\*RTIN, Internal Input Termination Resistor

**Figure 9. Standard 50  $\Omega$  Load HCSL Interface**

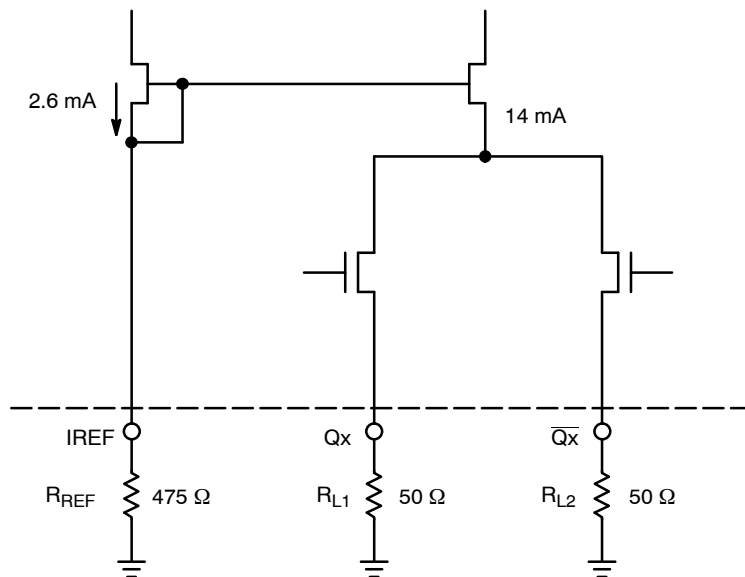


\*RTIN, Internal Input Termination Resistor

**Figure 10. LVCMOS/LVTTL Interface**



**Figure 11. HCSL Interface Termination to LVDS**



**Figure 12. HCSL Simplified Output Structure**

# NB3N108K

## ORDERING INFORMATION

Device	Package	Shipping†
NB3N108KMNG	QFN32 (Pb-Free)	74 Units / Rail
NB3N108KMNR4G	QFN32 (Pb-Free)	1000 / Tape & Reel

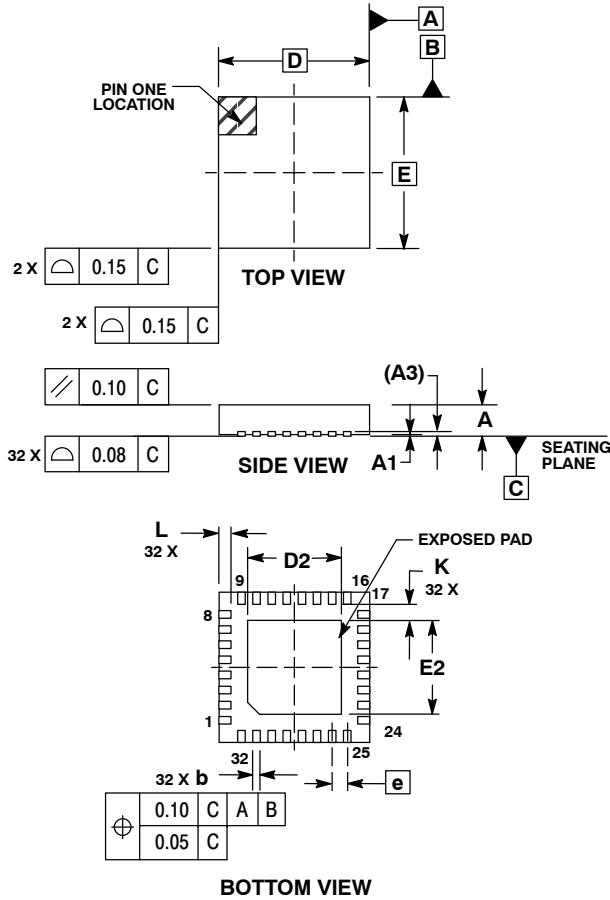
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



# NB3N108K

## PACKAGE DIMENSIONS

QFN32 5\*5\*1 0.5 P  
CASE 488AM-01  
ISSUE 0

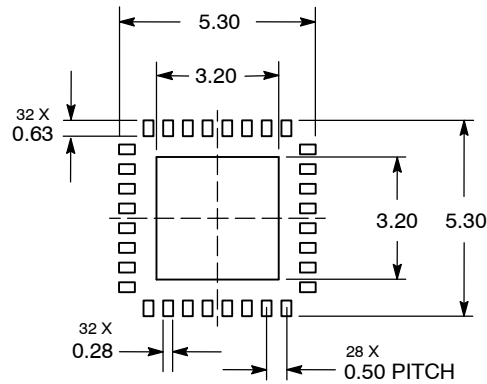


**NOTES:**

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3	0.200 REF		
b	0.180	0.250	0.300
D	5.00 BSC		
D2	2.950	3.100	3.250
E	5.00 BSC		
E2	2.950	3.100	3.250
e	0.500 BSC		
K	0.200	---	---
L	0.300	0.400	0.500

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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