TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TCK401G, TCK402G

External FET Driver IC

The TCK401G and TCK402G are 28 V high input voltage External FET driver IC. It has wide input voltage operation. And this features a slew rate control driver with small package WCSP6E (0.8 mm x 1.2 mm, t: 0.55 mm). Also it can block reverse current if switch turned off by using external series FET. Thus this is suitable for power management selector such as Battery Charge application.

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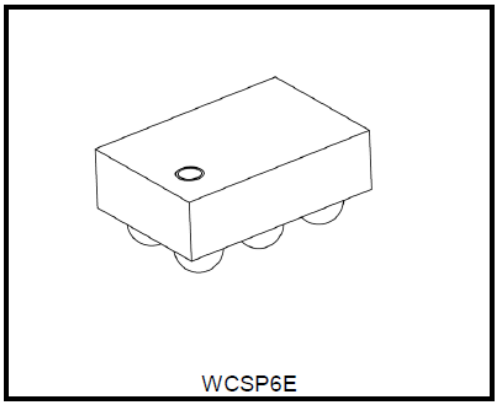
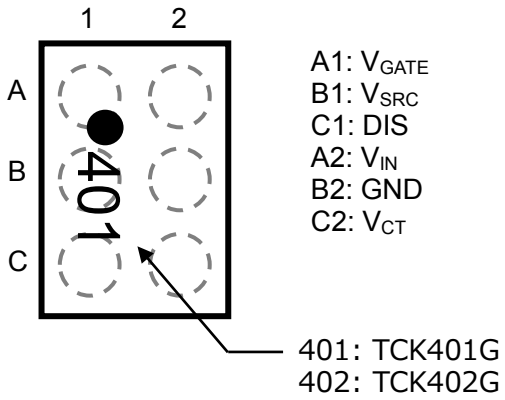


Weight: 1 mg(typ.)

Feature

- High maximum input voltage: $V_{IN\ max}$ = 40 V
- Wide input voltage operation: V_{IN} = 2.7 to 28 V
- Auto output discharge terminal
- Charge pump circuit
- Inrush current reducing circuit.
- Over Voltage lock out (Over 28 V)
- Under Voltage lock out (Under 2.7 V)
- Reverse Current Protection by External Back to Back MOSFET

Top marking (Top view)



Start of commercial production
2017-10

- **Absolute Maximum Ratings (Ta = 25°C)**

Characteristics	Symbol	Rating	Unit
Input voltage	V_{IN}	-0.3 to 40	V
Control voltage	V_{CT}	-0.3 to 6	V
Output GATE voltage	V_{GATE}	-0.3 to V_{IN}_opr + V_{GS}	V
SRC voltage	V_{SRC}	-0.3 to V_{GATE}	V
DIS voltage	V_{DIS}	-0.3 to 40	V
Power dissipation	P_D	800 (Note 1)	mW
Operating temperature range	T_{opr}	−40 to 85	°C
Junction temperature	Tj	150	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

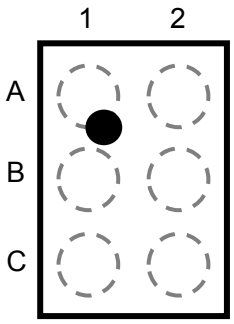
Note1: Rating at mounting on a board: FR4 board. (40 mm × 40 mm × 1.6 mm, Cu 4 layer)

- **Recommended Operating Conditions**

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Input operation voltage	V_{IN} _opr	2.7	5.0	28	V
Capacitance	C_{IN}	0.1	1	—	μF
	C_{GATE}	—	2000	—	pF
CONTROL High-level input voltage	V_{IH}	1.6	—	—	V
CONTROL Low-level input voltage	V_{IL}	—	—	0.4	V

- **Pin Assignment (Top view)**

- **WCSP6E**

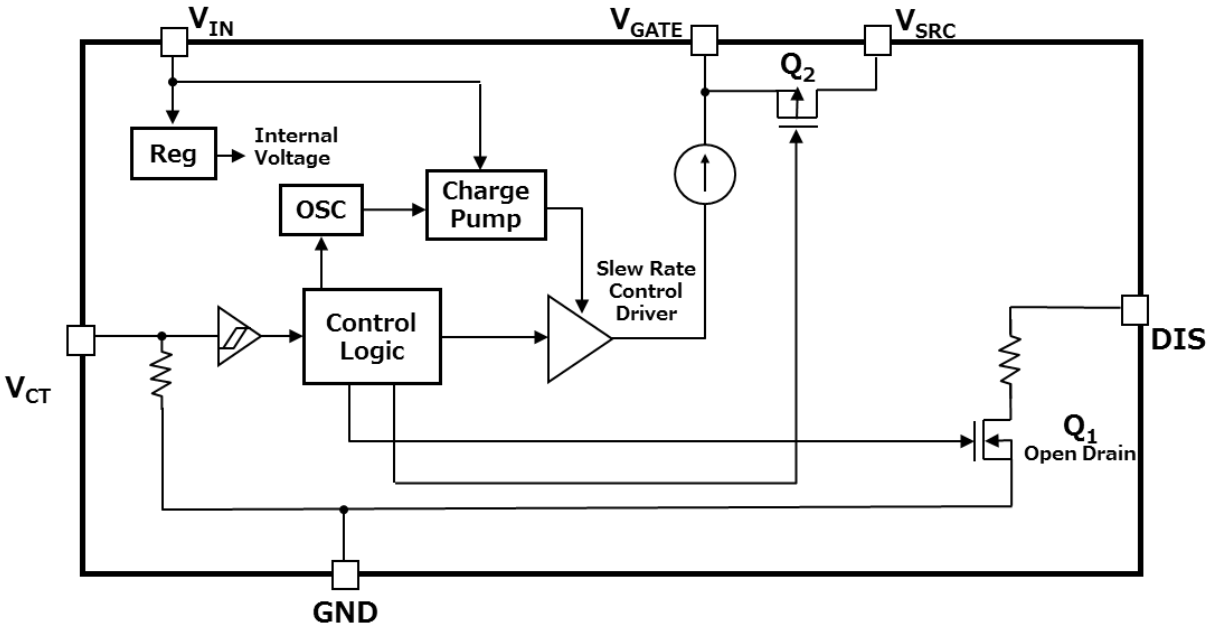


Pin #	Name	Pin #	Name
A1	V_{GATE}	A2	V_{IN}
B1	V_{SRC}	B2	GND
C1	DIS	C2	V_{CT}

- **Product list**

Part number	VCT function	VCT resistance
TCK401G	Active High	Pull down
TCK402G	Active Low	Pull down

- **Block Diagram**



TCK401G PIN Description

PIN	Name	Description
A1	V_{GATE}	Gate-Driver Output.
A2	V_{IN}	Supply voltage input.
B1	V_{SRC}	Recommend connecting V_{SRC} terminal to the common source connection of the external MOSFETs.
B2	GND	Ground
C1	DIS	Output Discharge terminal.
C2	V_{CT}	Mode control input terminal. When V_{CT}=High turn the external MOSFETs on, V_{CT}=Low, turn the external MOSFETs off.

- ## TCK402G PIN Description

PIN	Name	Description
A1	V_{GATE}	Gate-Driver Output.
A2	V_{IN}	Supply voltage input.
B1	V_{SRC}	Recommend connecting V_{SRC} terminal to the common source connection of the external MOSFETs.
B2	GND	Ground
C1	DIS	Output Discharge terminal.
C2	V_{CT}	Mode control input terminal. When V_{CT}=Low turn the external MOSFETs on, V_{CT}=High, turn the external MOSFETs off.

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TCK401G Operation Status Table

2.7V ≤ V_{IN} ≤ 28 V (Ta = -40 to 85°C)

V_{CT}	V_{GATE}	Discharge Q1	comment
High	ON (V_{IN} + V_{GS})	OFF	Driver ON mode
Open	OFF	ON	Driver OFF mode
Low			

TCK402G Operation Status Table

2.7V ≤ V_{IN} ≤ 28 V (Ta = -40 to 85°C)

V_{CT}	V_{GATE}	Discharge Q1	comment
Low	ON (V_{IN} + V_{GS})	OFF	Driver ON mode
Open			
High	OFF	ON	Driver OFF mode

DC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C (Note 2)		Unit
				Min.	Typ.	Max.	Min	Max	
Input quiescent current (ON state)	$I_{Q(ON)}$	TCK401G	V_{CT}: High, V_{IN} = 5.0 V	—	121	—	—	222	μA
			V_{CT}: High, V_{IN} = 9.0 V	—	144	—	—	283	μA
			V_{CT}: High, V_{IN} = 12 V	—	159	—	—	294	μA
			V_{CT}: High, V_{IN} = 20 V	—	198	—	—	376	μA
		TCK402G	V_{CT}: Low, V_{IN} = 5.0 V	—	121	—	—	222	μA
			V_{CT}: Low, V_{IN} = 9.0 V	—	144	—	—	283	μA
			V_{CT}: Low, V_{IN} = 12 V	—	159	—	—	294	μA
			V_{CT}: Low, V_{IN} = 20 V	—	198	—	—	376	μA
Standby current (OFF state)	$I_{Q(OFF)}$	TCK401G	V_{CT}: Low, V_{IN} = 5.0 V	—	3.0	—	—	4.8	μA
			V_{CT}: Low, V_{IN} = 9.0 V	—	5.9	—	—	8.2	μA
			V_{CT}: Low, V_{IN} = 12 V	—	8.0	—	—	11.2	μA
			V_{CT}: Low, V_{IN} = 20 V	—	13.8	—	—	19.2	μA
		TCK402G	V_{CT}: High, V_{IN} = 5.0 V	—	3.0	—	—	4.8	μA
			V_{CT}: High, V_{IN} = 9.0 V	—	5.9	—	—	8.2	μA
			V_{CT}: High, V_{IN} = 12 V	—	8.0	—	—	11.2	μA
			V_{CT}: High, V_{IN} = 20 V	—	13.8	—	—	19.2	μA
GATE Drive voltage(V_{GATE}-V_{IN})	V_{GS}	V_{IN} = 3 V		—	4.0	—	2.8	5.1	V
		V_{IN} = 5 V		—	6.5	—	5.1	7.9	V
		VIN = 9.0 V		—	6.5	—	5.1	7.9	V
		12 V ≤ V_{IN} ≤ 28 V		—	8.5	—	6.9	10.0	V
Output current	$I_{GATE(ON)}$	V_{IN} = 5 V		—	38	—	——	—	μA
DIS resistance	R_{DIS}	—		—	21	—	—	—	kΩ
Control pull down resistance	R_{CT}	V_{CT}= 5 V		—	600	—	—	—	kΩ

Note 2: This parameter is warranted by design.

- **AC Characteristics (Ta = 25°C, V_{IN}=5V, C_{GATE}=2000pF)**

Characteristics	Symbol	Test Condition (Figure 1,2)	Min.	Typ.	Max.	Unit
V_{GATE} ON time	t_{ON}	Initial startup time of V_{GATE} (Note 3) voltage from 0V to V_{IN} +1V	—	0.58	0.8	ms
V_{GATE} OFF time	t_{OFF}	V_{GATE} =0.5V	—	16.6	—	μs
V_{GATE} rise time	t_r	V_{GATE} rising from V_{IN} +1V to V_{IN} +3V	—	0.2	—	ms
V_{GATE} fall time	t_f	V_{GATE} falling from V_{IN} +3V to V_{IN} +1V	—	1.5	—	μs

- **AC Characteristics (Ta = 25°C, V_{IN}=9V, C_{GATE}=2000pF)**

Characteristics	Symbol	Test Condition (Figure 1,2)	Min.	Typ.	Max.	Unit
V_{GATE} ON time	t_{ON}	Initial startup time of V_{GATE} (Note 3) voltage from 0V to V_{IN} +1V	—	0.78	1.0	ms
V_{GATE} OFF time	t_{OFF}	V_{GATE}=0.5V	—	19.7	—	μs
V_{GATE} rise time	t_r	V_{GATE} rising from V_{IN} +1V to V_{IN} +4V	—	0.35	—	ms
V_{GATE} fall time	t_f	V_{GATE} falling from V_{IN} +4V to V_{IN} +1V	—	1.6	—	μs

- **AC Characteristics (Ta = 25°C, V_{IN}=12V, C_{GATE}=2000pF)**

Characteristics	Symbol	Test Condition (Figure 1,2)	Min.	Typ.	Max.	Unit
V_{GATE} ON time	t_{ON}	Initial startup time of V_{GATE} (Note 3) voltage from 0V to V_{IN} +1V	—	0.92	1.2	ms
V_{GATE} OFF time	t_{OFF}	V_{GATE}=0.5V	—	21.3	—	μs
V_{GATE} rise time	t_r	V_{GATE} rising from V_{IN} +1V to V_{IN} +5V	—	0.6	—	ms
V_{GATE} fall time	t_f	V_{GATE} falling from V_{IN} +5V to V_{IN} +1V	—	1.7	—	μs

Note 3: This parameter is warranted by design.

Timing chart

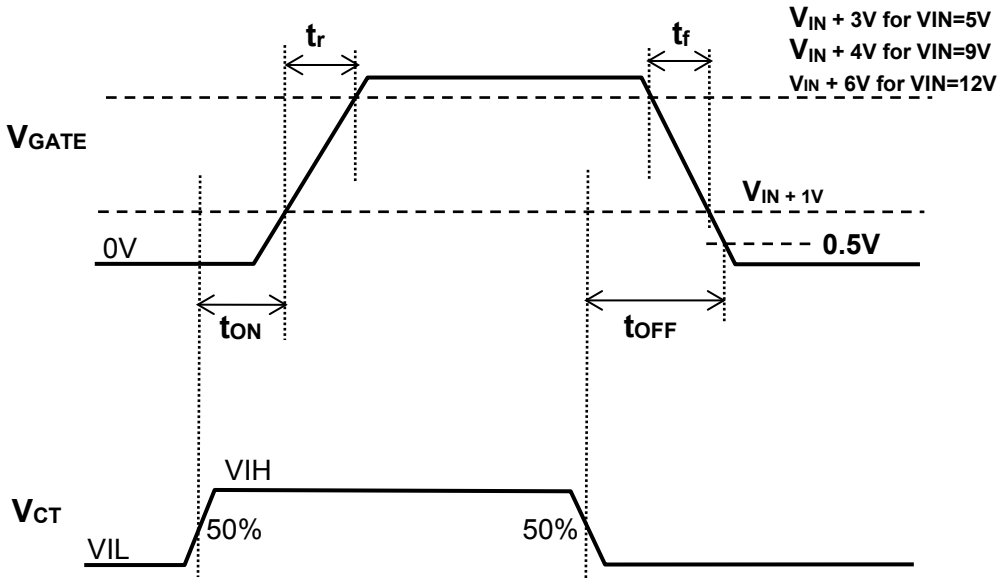


Fig.1 Active High (TCK401G)

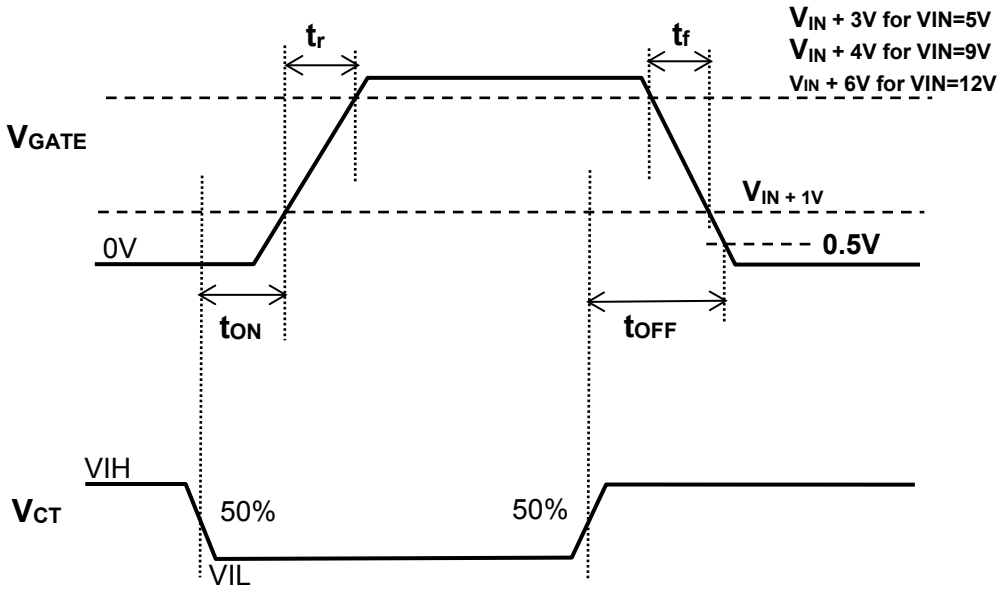
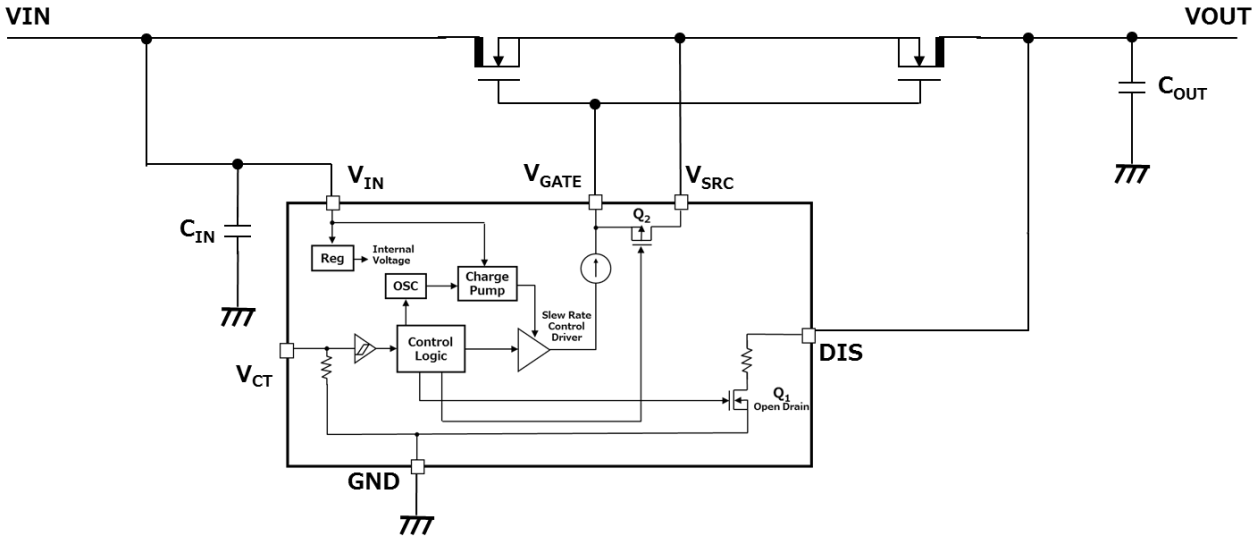


Fig.2 Active Low (TCK402G)

- **Application Note**
  - **Application circuit example**



1) Input and Output capacitor

An input capacitor (C_{IN}) and an output capacitor (C_{OUT}) is recommended for the stable operation of TCK401G and TCK402G. And it is effective to reduce voltage overshoot or undershoot due to sharp changes in output current and also for improved stability of the power supply. When used, place C_{IN} and C_{OUT} more than 1.0μF as close to V_{IN} pin to improve stability of the power supply.

2) V_{CT} pin

V_{CT} pin for TCK401G and TCK402G is operated by the control voltage and Schmitt trigger. V_{CT} pin has a tolerant function such that it can be used even if the control voltage is higher than the input voltage.

3) SRC Pin

For Dual MOSFET Driver, V_{SRC} work for short between V_{GATE} and MOSFET source when Driver IC Turn off.
If there are enough margins of V_{GS} of MOSFET, V_{SRC} terminal Open state is no problem.
For Single MOSFET Driver, if there are enough margins of V_{GS} of MOSFET, V_{SRC} pin Open state is no problem. If there are not enough margins, we recommend connecting V_{SRC} and V_{OUT}. If connect V_{SRC} and V_{OUT}, tOFF time become longer because of C_{OUT}. Therefore, please consider enough margins for MOSFET selection.

4) DIS Pin

If need Discharge function when Driver IC Turn off, please connect DIS Pin to V_{OUT}. If no need, DIS Pin Open state is no problem.

5) Over Voltage Protection off time (t_{OVP})

Over Voltage (V_{IN} is over V_{IN}_opr max) Protection off time (t_{OVP}) is similar V_{GATE} OFF time (t_{OFF}).

Timing chart

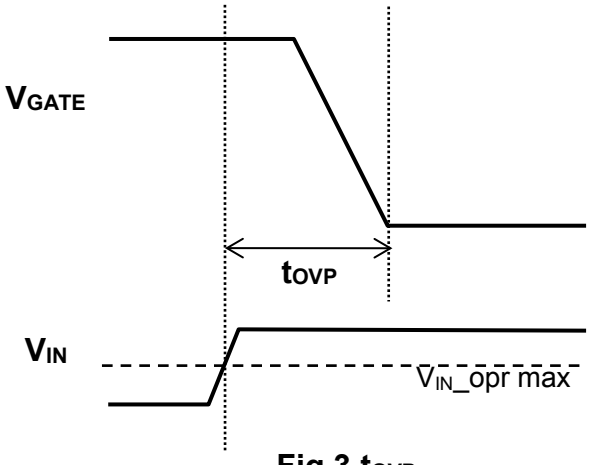
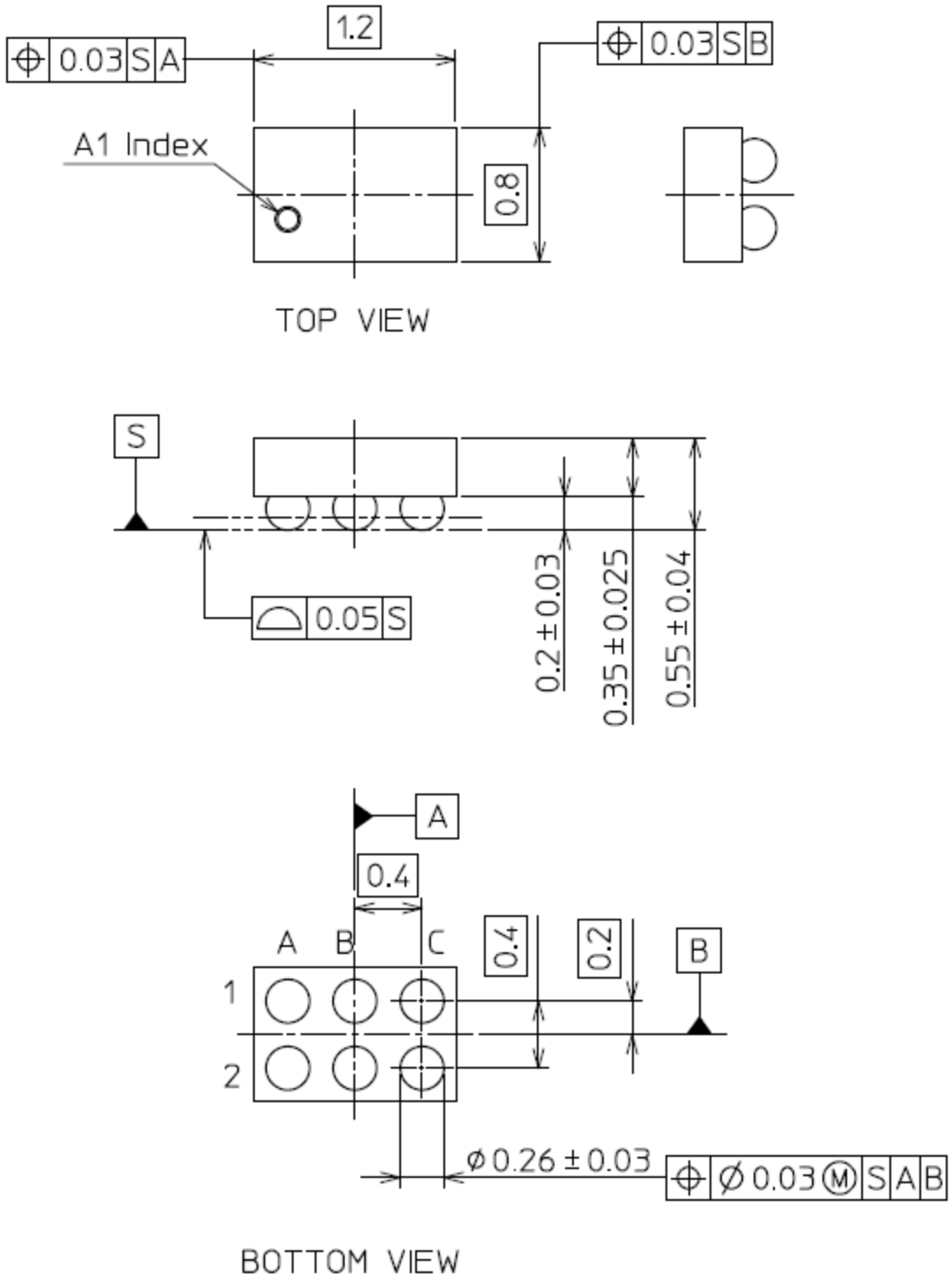


Fig.3 t_{OVP}

- **Package dimension**

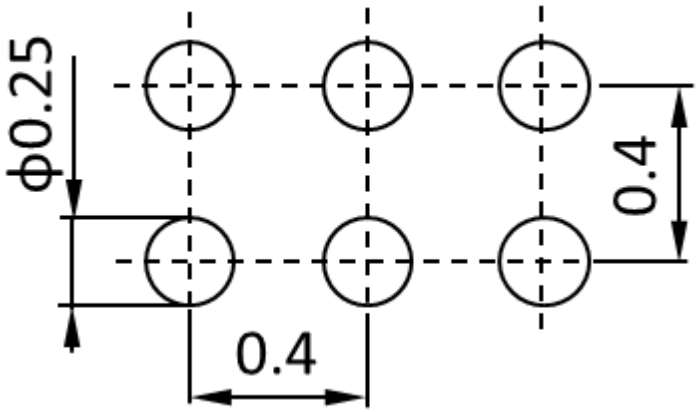
Unit: mm



Weight: 1 mg (typ.)

Land pattern dimensions (for reference only)

Unit: mm



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