SP705-SP708-SP813L

Low Power Microprocessor Supervisory Circuits

June 2011 Rev. 2.1.0

GENERAL DESCRIPTION

The SP705-708/813L series is a family of microprocessor (µP) supervisory circuits that integrate myriad components involved in discrete solutions which monitor power-supply and battery in mP and digital systems.

The SP705-708/813L series will significantly improve system reliability and operational efficiency when compared to solutions obtained with discrete components. The features of the SP705-708/813L series include a watchdog timer, a µP reset, a Power Fail Comparator, and a manual-reset input.

The SP705-708/813L series is ideal for applications in automotive systems, computers, controllers, and intelligent instruments. The SP705-708/813L series is an ideal solution for systems in which critical monitoring of the power supply to the µP and related digital components is demanded.

APPLICATIONS

- **Processors & DSPs Based Systems**
- **Industrial & Medical Instruments**

FEATURES

- **Precision Voltage Monitor**
  - SP705/SP707/SP813L: 4.65V
  - SP706/SP708: 4.40V
- **200ms RESET Pulse Width**
- **Independent Watchdog Timer**
  - 1.6s Timeout (SP705/SP706/SP813L)
- **60µA Maximum Supply Current**
- **Debounced TTL/CMOS Manual Reset Input**
- **$\overline{\text{RESET}}$ Asserted Down to V_{CC}=1.1V**
- **Voltage Monitor for Power Failure or Low Battery Warning**
- **8-Pin PDIP, NSOIC and MSOP Packages**
- **Pin Compatible with Industry Standards 705-708-813L Series**
- **Functionally Compatible to Industry Standard 1232 Series**

Part Number	RESET Threshold	RESET Active	Manual RESET	Watchdog	PFI Accuracy
SP705	4.65V	Low	Yes	Yes	4%
SP706	4.40V	Low	Yes	Yes	4%
SP707	4.65V	Low and High	Yes	No	4%
SP708	4.40V	Low and High	Yes	No	4%
SP813L	4.65V	High	Yes	Yes	4%

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} .....-0.3V to 6.0V
All Other Inputs (Note 1).....-0.3V to (V_{CC}+0.3V)
Input Current
  VCC.....20mA
  GND 20mA
  Output Current (All outputs) 20mA
ESD Rating (HBM - Human Body Model) 4kV
Continuous Power Dissipation
  Plastic DIP (derate 9.09mW/°C above +70°C)....727mW
  SO (derate 5.88mW/°C above +70°C).....471mW
  Mini SO (derate 4.10mW/°C above +70°C) 330mW
Storage Temperature .....-65°C to 160°C
Lead Temperature (Soldering, 10 sec) .....300°C

ELECTRICAL SPECIFICATIONS

Unless otherwise indicated, V_{CC} = 4.75V to 5.5V (SP705-SP707-SP813L), V_{CC} = 4.50V to 5.5V (SP706-SP708), T_A= T_{MIN} to T_{MAX}, typical at 25°C.

Parameter	Min.	Typ.	Max.	Units		Conditions
Operating Voltage Range V_{CC}	1.1		5.5	V		
Supply Current I_{SUPPLY}		40	60	µA		$\overline{MR}$=V_{CC} or floating, WDI floating
Reset Threshold	4.50	4.65	4.75	V		SP705, SP707, SP813L
	4.25	4.40	4.50			SP706, SP708 (Note 2)
Reset Threshold Hysteresis		40		mV		Note 2
Reset Pulse Width t_{RS}	140	200	280	ms		Note 2
RESET Output Voltage	V_{CC}-1.5			V		I_{SOURCE}=800µA, Note 2
	0.8					I_{SOURCE}=4µA, V_{CC}=1.1V, Note 2
			0.4			I_{SINK}=3.2mA, Note 2
			0.3			I_{SINK}=100µA, V_{CC}=1.2V, Note 2
Watchdog Timeout Period t_{WD}	1.00	1.60	2.25	s		SP705, SP707, SP813L
WDI Pulse Width t_{WP}	100			ns		V_{IL}=0.4V, V_{IH}=0.8xV_{CC}
WDI Input Threshold Low			0.8	V		SP705, SP707, SP813L V_{CC}=5V
WDI Input Threshold High	3.5			V		
WDI Input Current		30	75	µA		SP705, SP707, SP813L, WDI=V_{CC}
	-75	-20		µA		SP705, SP707, SP813L, WDI=0V
$\overline{WDO}$ Output Voltage	V_{CC}-1.5			V		I_{SOURCE}=800µA
			0.4			I_{SINK}=3.2mA
$\overline{MR}$ Pull-up Current	100	250	600	µA		$\overline{MR}$ = 0V
$\overline{MR}$ Pulse Width t_{MR}	150			ns		
$\overline{MR}$ Input Threshold Low			0.8	V		
$\overline{MR}$ Input Threshold High	2.0					
$\overline{MR}$ to Reset Out Delay t_{MD}			250	ns		Note 2
PFI Input Threshold	1.20	1.25	1.30	V		V_{CC}=5V
PFI Input Current	-25.00	0.01	25.00	nA		
$\overline{PFO}$ Output Voltage	V_{CC}-1.5			V		I_{SOURCE}=800µA
			0.4			I_{SINK}=3.2mA

Note 1: The input voltage limits on PFI and $\overline{MR}$ can be exceeded if the input current is less than 10mA.
Note 2: Applies to both $\overline{RESET}$ in the SP705-SP708 and RESET in the SP707/708/813L/813M.

BLOCK DIAGRAM

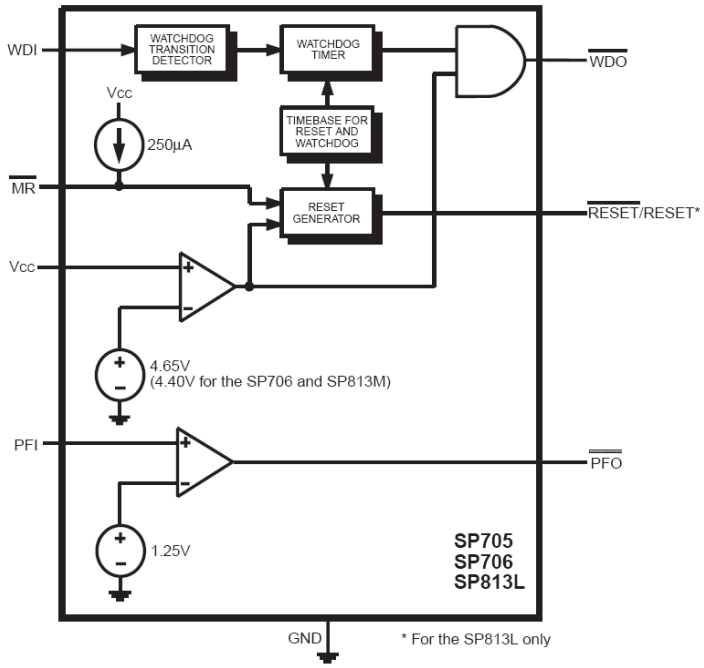


Fig. 1: SP705-SP706-SP813L Block Diagram

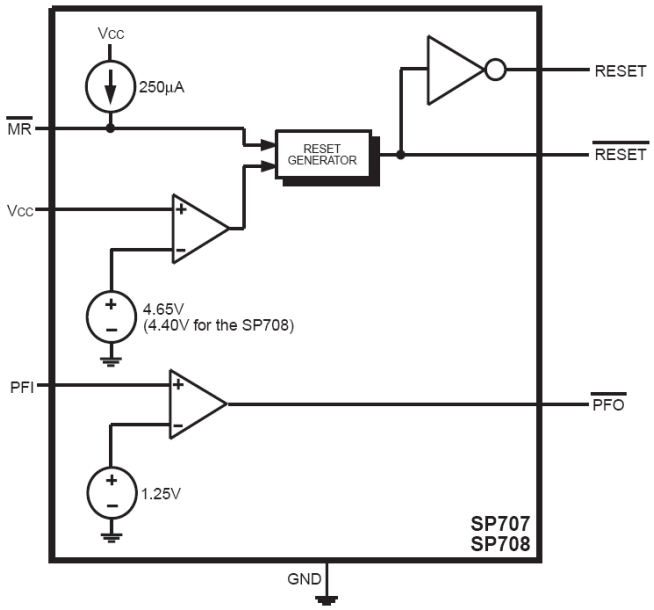


Fig. 2: SP707-SP708 Block Diagram

PIN ASSIGNMENT

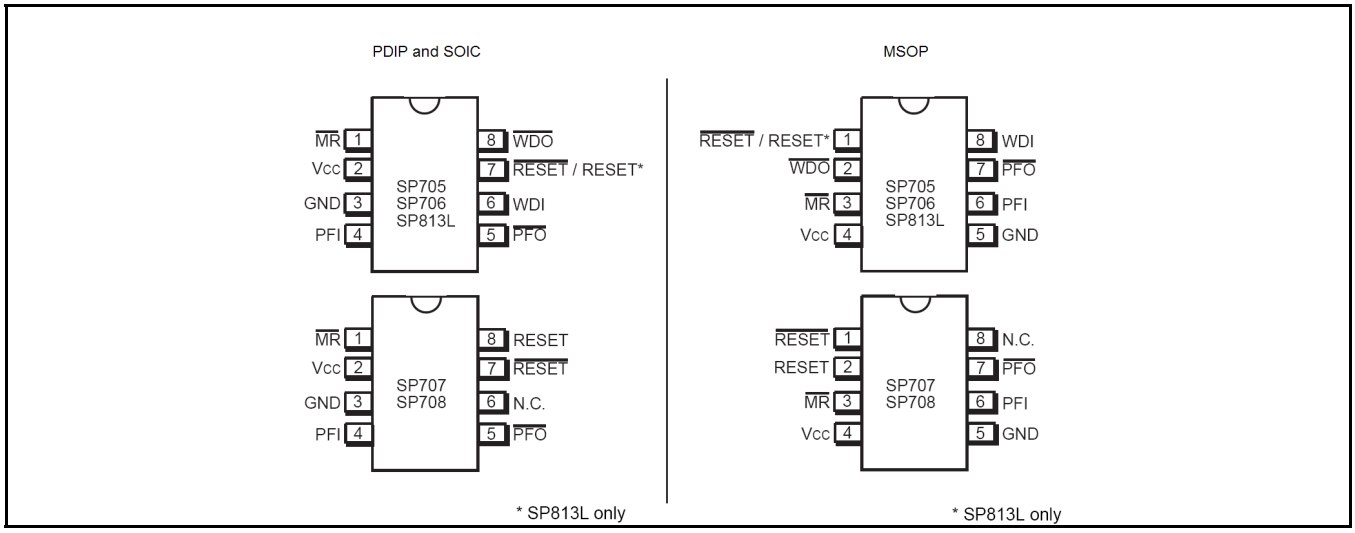


Fig. 3: Pin Assignment

PIN DESCRIPTION

Name	Pin Number					Description
	SP705-SP706		SP707-SP708		SP813L	
	SOIC	MSOP	SOIC	MSOP	DIP SOIC	
$\overline{MR}$	1	3	1	3	1	Manual Reset This input triggers a reset pulse when pulled below 0.8V. This active LOW input has an internal 250µA pull-up current. It can be driven from a TTL or CMOS logic line or shorted to ground with a switch.
V_{CC}	2	4	2	4	2	+5V power supply
GND	3	5	3	5	3	Ground reference for all signals
PFI	4	6	4	6	4	Power-Fail Input When this voltage monitor input is less than 1.25V, $\overline{PFO}$ goes LOW. Connect PFI to ground or V_{CC} when not in use.
$\overline{PFO}$	5	-	5	7	5	Power-Fail Output This output is LOW until PFI is less then 1.25V
WDI	6	8	-	-	6	Watchdog Input If this input remains HIGH or LOW for 1.6s, the internal watchdog timer times out and $\overline{WDO}$ goes LOW. Floating WDI or connecting WDI to a high-impedance tri-state buffer disables the watchdog feature. The internal watchdog timer clears whenever $\overline{RESET}$ is asserted, WDI is tri-stated, or whenever WDI sees a rising or falling edge.
N.C.	-	-	6	8	-	No Connect
$\overline{RESET}$	7	1	7	1	-	Active-LOW $\overline{RESET}$ Output This output pulses LOW for 200ms when triggered and stays LOW whenever V_{CC} is below the reset threshold (4.65V for the SP705/707/813L and 4.40V for the SP706/708). It remains LOW for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from LOW to HIGH. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.

Name	Pin Number					Description
	SP705-SP706		SP707-SP708		SP813L	
	SOIC	MSOP	SOIC	MSOP	DIP SOIC	
$\overline{WDO}$	8	2	-	-	8	Watchdog Output This output pulls LOW when the internal watchdog timer finishes its 1.6s count and does not go HIGH again until the watchdog is cleared. $\overline{WDO}$ also goes LOW during low-line conditions. Whenever V_{CC} is below the reset threshold, WDO stays LOW. However, unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width. As soon as V_{CC} is above the reset threshold, $\overline{WDO}$ goes HIGH with no delay.
RESET	-	-	8	2	7	Active-HIGH RESET Output This output is the complement of $\overline{RESET}$. Whenever RESET is HIGH, $\overline{RESET}$ is LOW and vice-versa. Note that the SP813L has a reset output only.

ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
SP705CN-L	0°C≤T_A≤+70°C	SP705C YYWWL #	8-pin NSOIC	Bulk	Lead Free	
SP705CN-L/TR	0°C≤T_A≤+70°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP705EN-L	-40°C≤T_A≤+85°C	SP705E YYWWL #	8-pin NSOIC	Bulk	Lead Free	
SP705EN-L/TR	-40°C≤T_A≤+85°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP705CU-L	0°C≤T_A≤+70°C	705C # YWW	8-pin MSOP	Bulk	Lead Free	
SP705CU-L/TR	0°C≤T_A≤+70°C		8-pin MSOP	2.5K/Tape & Reel	Lead Free	
SP706CN-L	0°C≤T_A≤+70°C	SP706C YYWWL #	8-pin NSOIC	Bulk	Lead Free	
SP706CN-L/TR	0°C≤T_A≤+70°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP706EN-L	-40°C≤T_A≤+85°C	SP706E YYWWL #	8-pin NSOIC	Bulk	Lead Free	
SP706EN-L/TR	-40°C≤T_A≤+85°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP706CU-L	0°C≤T_A≤+70°C	706C # YWW	8-pin MSOP	Bulk	Lead Free	
SP706CU-L/TR	0°C≤T_A≤+70°C		8-pin MSOP	2.5K/Tape & Reel	Lead Free	
SP707CN-L	0°C≤T_A≤+70°C	SP707C YYWWL #	8-pin NSOIC	Bulk	Lead Free	
SP707CN-L/TR	0°C≤T_A≤+70°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP707EN-L	-40°C≤T_A≤+85°C	SP707E YYWWL #	8-pin NSOIC	Bulk	Lead Free	
SP707EN-L/TR	-40°C≤T_A≤+85°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP707CU-L	0°C≤T_A≤+70°C	707C # YWW	8-pin MSOP	Bulk	Lead Free	
SP707CU-L/TR	0°C≤T_A≤+70°C		8-pin MSOP	2.5K/Tape & Reel	Lead Free	
SP708CN-L	0°C≤T_A≤+70°C	SP708C YYWWL #	8-pin NSOIC	Bulk	Lead Free	
SP708CN-L/TR	0°C≤T_A≤+70°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP708EN-L	-40°C≤T_A≤+85°C	SP708E YYWWL #	8-pin NSOIC	Bulk	Lead Free	
SP708EN-L/TR	-40°C≤T_A≤+85°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP813LCN-L	0°C≤T_A≤+70°C	SP813LC YYWWL #	8-pin NSOIC	Bulk	Lead Free	
SP813LCN-L/TR	0°C≤T_A≤+70°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP813LEN-L	-40°C≤T_A≤+85°C	SP813LE YYWWL #	8-pin NSOIC	Bulk	Lead Free	
SP813LEN-L/TR	-40°C≤T_A≤+85°C		8-pin NSOIC	2.5K/Tape & Reel	Lead Free	
SP813LCP-L	0°C≤T_A≤+70°C	SP813LC YWWL#	8-pin PDIP	Bulk	Lead Free	
SP813LEP-L	-40°C≤T_A≤+85°C	SP813LE YWWL#	8-pin PDIP	Bulk	Lead Free	

"YY" = Year – "WW" = Work Week – "#" = Lot Number

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at V_{IN} = 2.7V to 5.5V, $T_J = T_A$ = 25°C, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

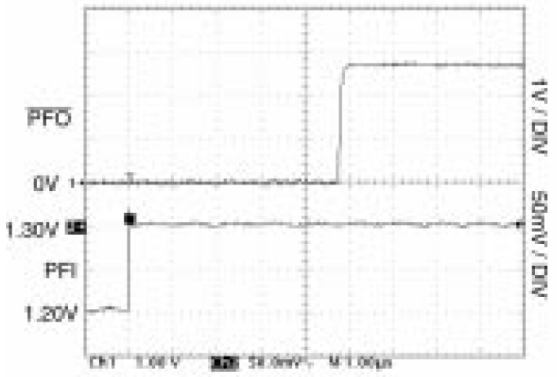


Fig. 4: Power-Fail Comparator
De-Assertion Response Time

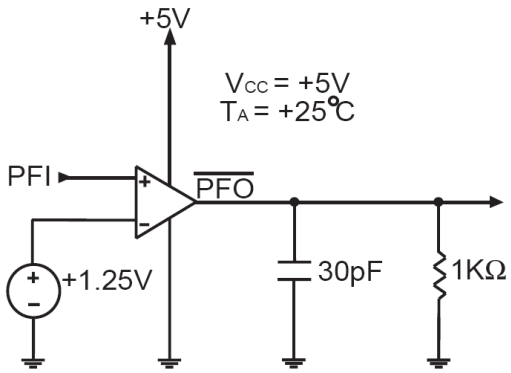


Fig. 5: Power-Fail Comparator
De-Assertion Response Time Circuit

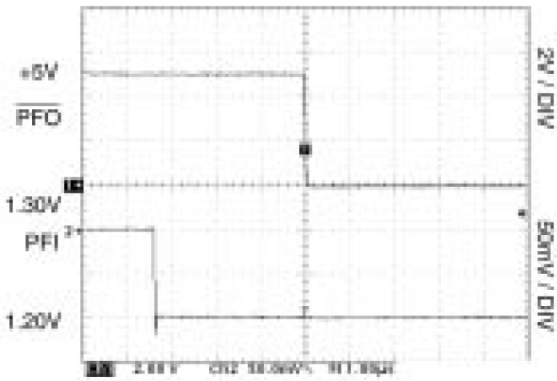


Fig. 6: Power-Fail Comparator
Assertion Response Time

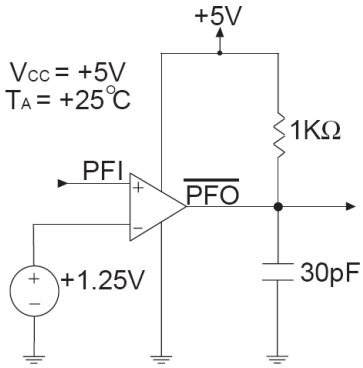


Fig. 7: Power-Fail Comparator
Assertion Response Time Circuit

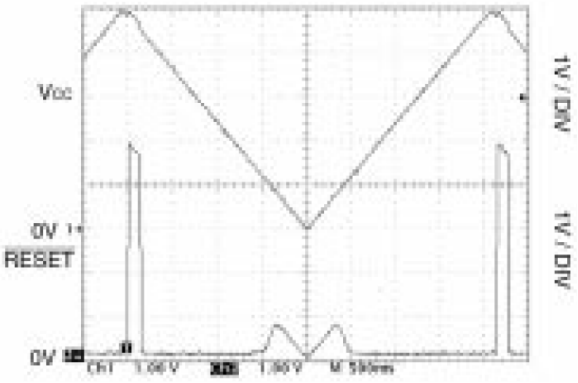


Fig. 8: SP705/707 $\overline{\text{RESET}}$ Output Voltage
vs. Supply Voltage

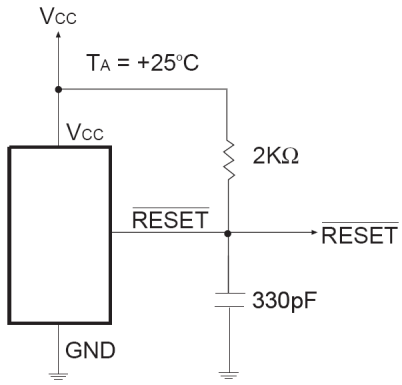


Fig. 9: SP705/707 $\overline{\text{RESET}}$ Output Voltage
vs. Supply Voltage Circuit

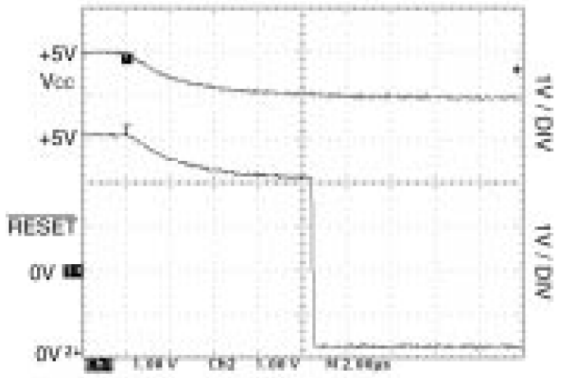


Fig. 10: SP705/707 $\overline{\text{RESET}}$ Response Time

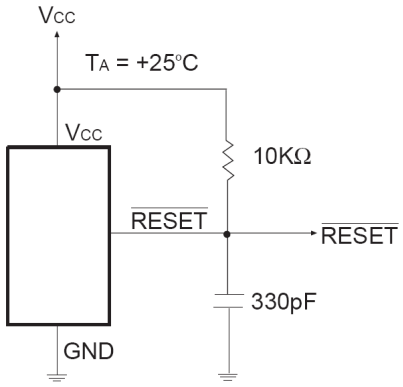


Fig. 11: SP705/707 $\overline{\text{RESET}}$ Response Time Circuit

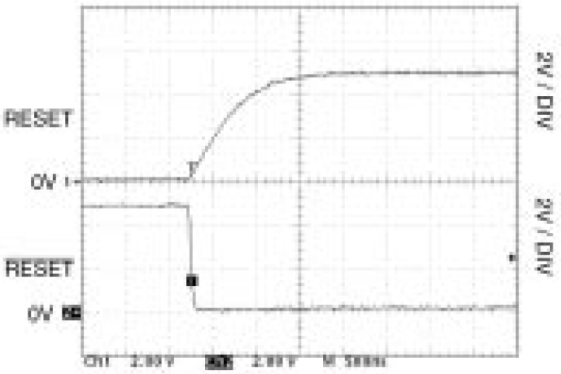


Fig. 12: SP707 RESET and $\overline{\text{RESET}}$ Assertion

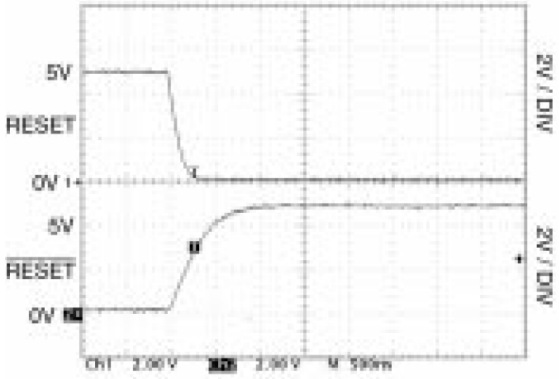


Fig. 13: SP707 RESET and $\overline{\text{RESET}}$ De-Assertion

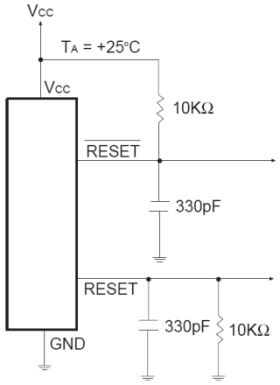


Fig. 14: SP707 RESET and $\overline{\text{RESET}}$ Assertion and De-Assertion Circuit

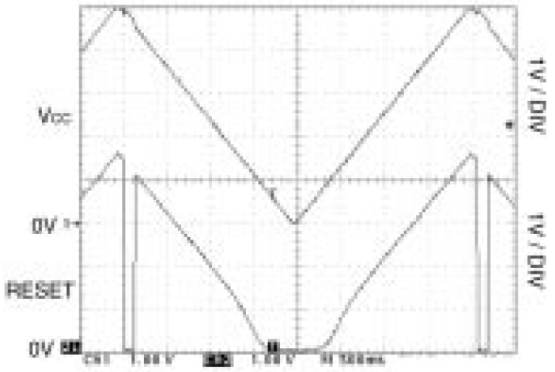


Fig. 15: SP707/708/813L RESET Output Voltage vs. Supply Voltage

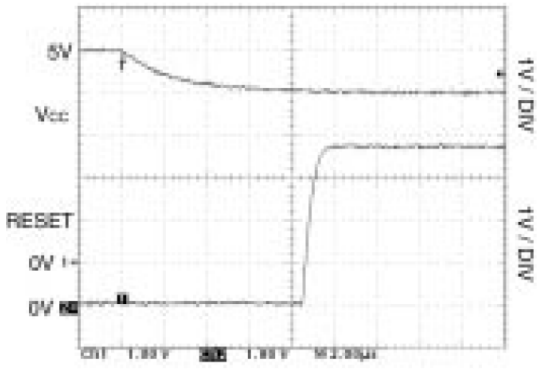


Fig. 16: SP813L RESET Response Time

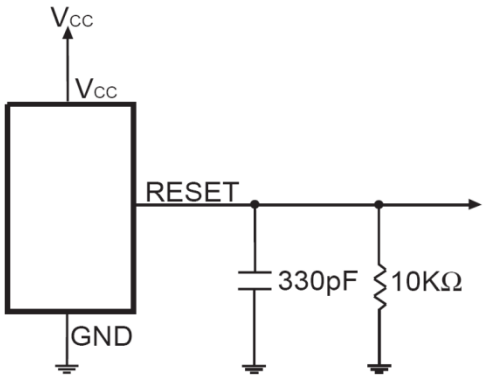


Fig. 17: SP707/708/813L RESET Output Voltage vs. Supply Voltage and SP813L RESET Response Time Circuit

FEATURES

The SP705-708/813L series provides four key functions:

1. A reset output during power-up, power-down and brownout conditions.

2. An independent watchdog output that goes LOW if the watchdog input has not been toggled within 1.6 seconds.

3. A 1.25V threshold detector for power-fail warning, low battery detection, or monitoring a power supply other than +5V.

4. An active-LOW manual-reset that allows RESET to be triggered by a pushbutton switch.

The SP707/708 devices are the same as the SP705/706 devices except for the active-HIGH RESET substitution of the watchdog timer. The SP813L is the same as the SP705 except an active-HIGH RESET is provided rather than an active-LOW $\overline{\text{RESET}}$. The SP705/707/813L devices generate a reset when the supply voltage drops below 4.65V. The SP706/708 devices generate a reset below 4.40V.

The SP705-708/813L series is ideally suited for applications in automotive systems, intelligent instruments, and battery-powered computers and controllers. The SP705-708/813L series is ideally applied in environments where monitoring of power supply to a µP and its related components is critical.

THEORY OF OPERATION

The SP705-708/813L series is a microprocessor (µP) supervisory circuit that monitors the power supplied to digital circuits such as microprocessors, microcontrollers, or memory. The series is an ideal solution for portable, battery-powered equipment that requires power supply monitoring. Implementing this series will reduce the number of components and overall complexity. The watchdog functions of this product family will continuously oversee the operational status of a system. The operational features and benefits of the SP705-708/813L series are described in more detail below.

RESET OUTPUT

A microprocessor's reset input starts the µP in a known state. The SP705-708/813L series asserts reset during power-up and prevents code execution errors during power down or brownout conditions.

On power-up, once V_{CC} reaches 1.1V, $\overline{\text{RESET}}$ is a guaranteed logic LOW of 0.4V or less. As V_{CC} rises, $\overline{\text{RESET}}$ stays LOW. When V_{CC} rises above the reset threshold, an internal timer releases $\overline{\text{RESET}}$ after 200ms. $\overline{\text{RESET}}$ pulses LOW whenever V_{CC} dips below the reset threshold, such as in a brownout condition. When a brownout condition occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power down, once V_{CC} falls below the reset threshold, $\overline{\text{RESET}}$ stays LOW and is guaranteed to be 0.4V or less until V_{CC} drops below 1.1V.

The SP707/708/813L active-HIGH RESET output is simply the complement of the $\overline{\text{RESET}}$ output and is guaranteed to be valid with V_{CC} down to 1.1V. Some µPs, such as Intel's 80C51, require an active-HIGH reset pulse.

WATCHDOG TIMER

The SP705/706/813L watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6 seconds and WDI is not tri-stated, $\overline{\text{WDO}}$ goes LOW. As long as $\overline{\text{RESET}}$ is asserted or the WDI input is tri-stated, the watchdog timer will stay cleared and will not count. As soon as $\overline{\text{RESET}}$ is released and WDI is driven HIGH or LOW, the timer will start counting. Pulses as short as 50ns can be detected.

Typically, $\overline{\text{WDO}}$ will be connected to the non-maskable interrupt input (NMI) of a µP. When V_{CC} drops below the reset threshold, $\overline{\text{WDO}}$ will go LOW whether or not the watchdog timer had timed out. Normally this would trigger an NMI but $\overline{\text{RESET}}$ goes LOW simultaneously and thus overrides the NMI.

If WDI is left unconnected, $\overline{\text{WDO}}$ can be used as a low-line output. Since floating WDI disables the internal timer, $\overline{\text{WDO}}$ goes LOW only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

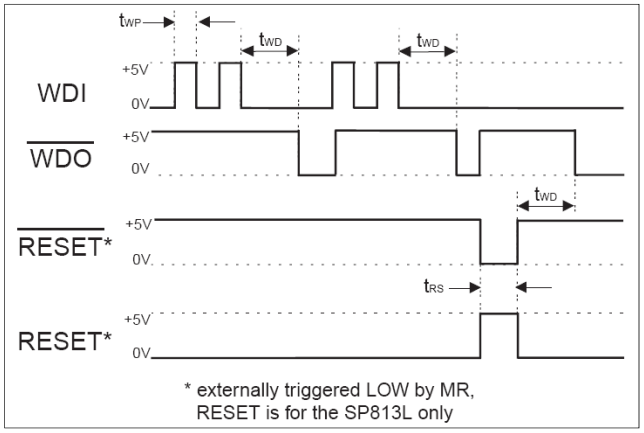


Fig. 18: SP705/706/813L Watchdog Timing Waveforms

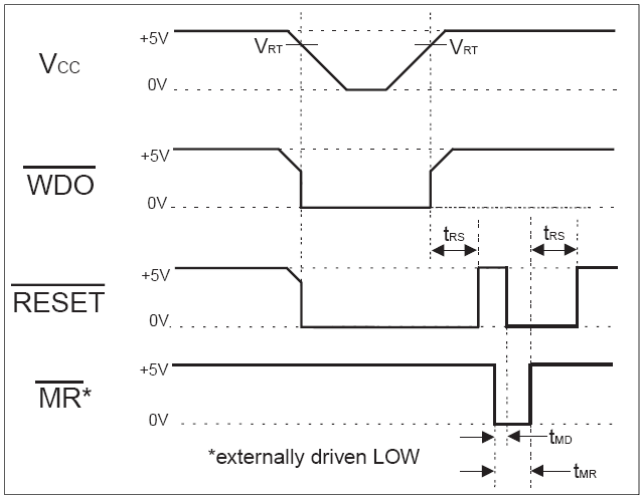


Fig. 19: SP705/706 Timing Diagrams with WDI tri-stated.

POWER-FAIL COMPARATOR

The power-fail comparator can be used for various purposes because its output and non inverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider as shown in Figure 20. Choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. Use $\overline{PFO}$ to interrupt the µP so it can prepare for an orderly power-down.

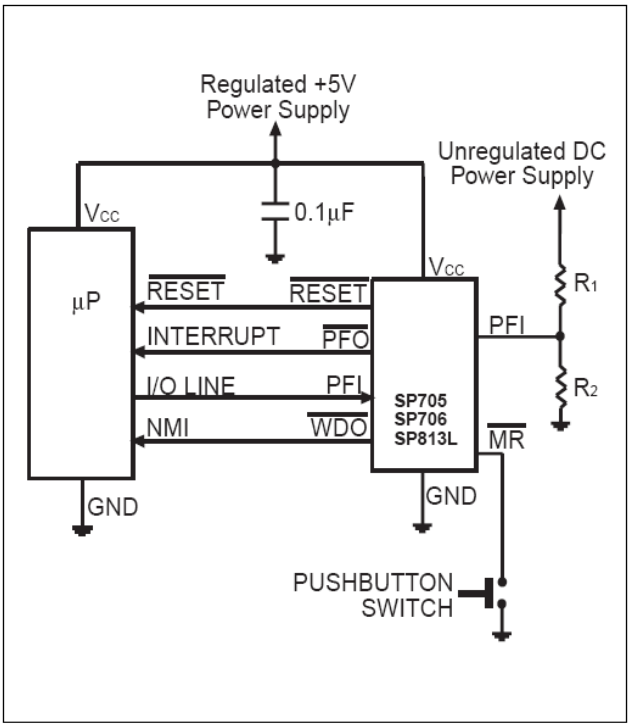


Fig. 20: Typical Operating Circuit

MANUAL RESET

The manual-reset input ($\overline{MR}$) allows RESET to be triggered by a pushbutton switch. The switch is effectively debounced by the 140ms minimum RESET pulse width. $\overline{MR}$ is TTL/CMOS logic compatible, so it can be driven by an external logic line. $\overline{MR}$ can be used to force a watchdog timeout to generate a RESET pulse in the SP705/706/813L. Simply connect $\overline{WDO}$ to $\overline{MR}$.

Ensuring a Valid Reset Output Down to V_{CC}=0V

When V_{CC} falls below 1.1V, the SP705/706/707/708 $\overline{RESET}$ output no longer sinks current, it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the $\overline{RESET}$ pin, any stray charge or leakage currents will be shunted to ground, holding $\overline{RESET}$ LOW. The resistor value is not critical. It should be about 100KW, large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

MONITORING VOLTAGES OTHER THAN THE UNREGULATED DC INPUT

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and PFO. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. RESET can be used to monitor voltages other than the +5V V_{CC} line. Connect PFO to MR to initiate a RESET pulse when PFI drops below 1.25V. Figure 21 shows the SP705/706/707/708 configured to assert RESET when the +5V supply falls below the RESET threshold, or when the +12V supply falls below approximately 11V.

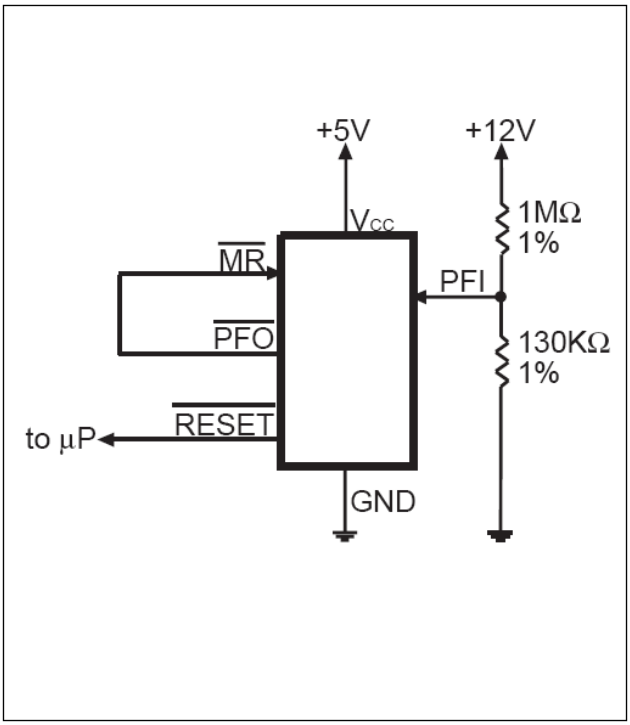


Fig. 21: Monitoring +5V and +12V Power Supplies

MONITORING A NEGATIVE VOLTAGE SUPPLY

The power-fail comparator can also monitor a negative supply rail, shown in Figure 22. When the negative rail is good (a negative voltage of large magnitude), PFO is LOW. By adding the resistors and transistor as shown, a HIGH PFO triggers RESET. As long as PFO remains HIGH, the SP705-708/813L will keep RESET asserted (where RESET = LOW and RESET = HIGH). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.

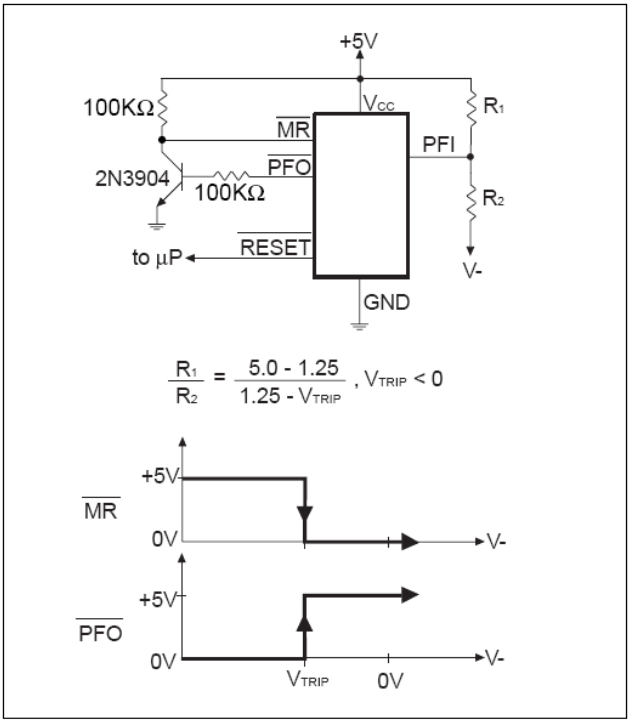


Fig. 22: Monitoring a Negative Voltage Supply

INTERFACING TO µPS WITH BIDIRECTIONAL RESET PINS

µPs with bidirectional RESET pins, such as the Motorola 68HC11 series, can contend with the SP705/706/707/708 RESET output. If, for example, the RESET output is driven HIGH and the µP wants to pull it LOW, indeterminate logic levels may result. To correct this, connect a 4.7KΩ resistor between the RESET output and the µP reset I/O, as shown if Figure 23. Buffer the RESET output to other system components.

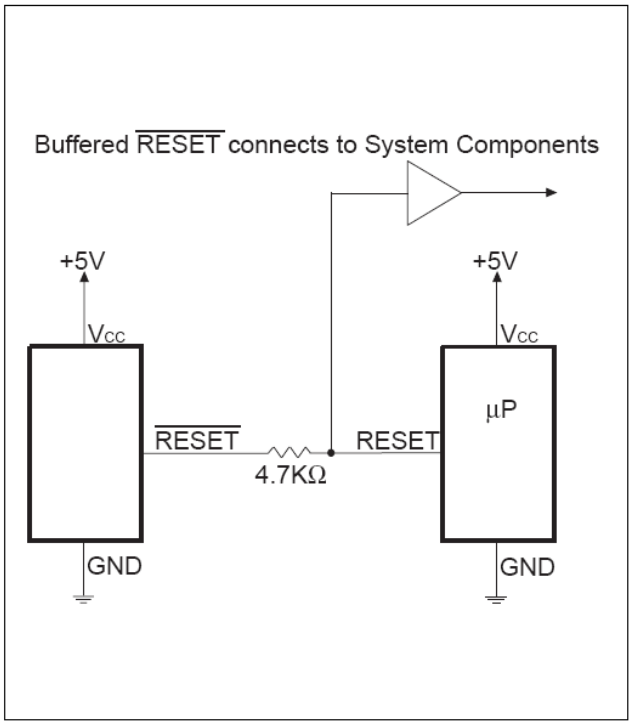


Fig. 23: Interfacing to Microprocessors
with Bidirectional REST I/O (SP705/706/708)

APPLICATIONS

The SP705-708/813L series offers unmatched performance and the lowest power consumption for these industry standard devices. Refer to Figures 24 and 25 for supply current performance characteristics rated against temperature and supply voltages.

Table 2 shows how the SP705-708/813L series can be used instead of the Dallas Semiconductor DS1232LP/LPS. Table 2 illustrates to a designer the advantages and tradeoffs of the SP705-708/813L series compared to the Dallas Semiconductor device. While the names of the pin descriptions may differ, the functions are the same or very similar. Unlike the DS1232, the SP705-708/813L series has a separate watchdog output pin $\overline{WDO}$ which can be simply connected to the $\overline{MR}$ input to generate a Reset signal. The DS1232 has pin selectable features, while the SP705-708/813L series has more fixed functions of reset threshold and watchdog time-out delay. For most applications, the fixed functions will be preferred, with the benefit of reduced cost due to a less complex part. In addition, the SP705-708/ 813L series has a power fail input and output function not available with the DS1232 that is useful for monitoring systems with unregulated supply voltages. The SP705-708/813L series is available in one of the industry's smallest space-saving package sizes, the MSOP.

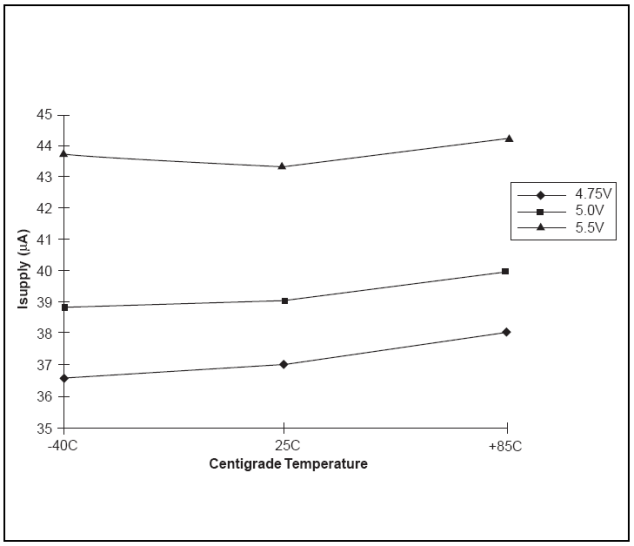


Fig. 24: Supply Current vs. Temperature

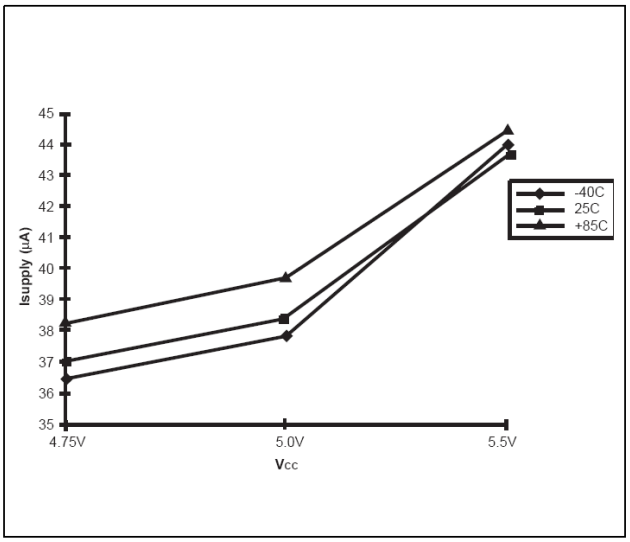


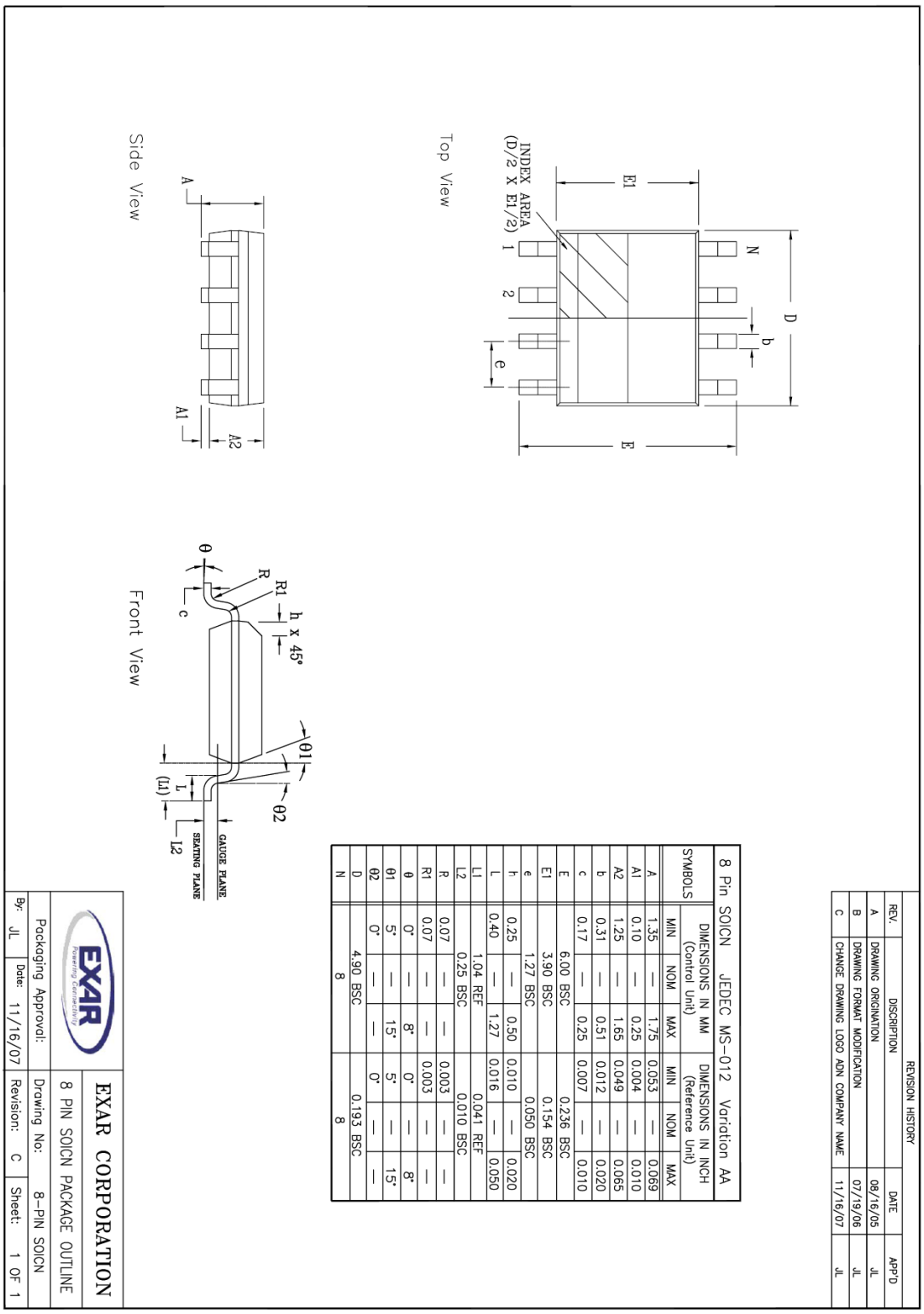
Fig. 25: Supply Current vs. Supply Voltage

Function	Dallas DS1232LP/LPS		Exar Alternative Part Number			
	Pin Number DIP or SOIC	Pin Description	Exar Part Number	Pin Number		Pin Description
				DIP or SOIC	MSOP	
Manual Reset	1	$\overline{\text{PBRST}}$	SP705-708/ 813L	1	3	$\overline{\text{MR}}$
WDI Time Delay Set	2	TD	SP705-708/ 813L	N/A	N/A	1.6sec by design
V_{cc} Trip 4.6V	3	TOL=GND	SP705/707/ 813L	N/A	N/A	4.6V by design
V_{cc} Trip 4.4V	3	TOL=V_{cc}	SP706/708/	N/A	N/A	4.4V by design
Ground	4	GND	SP705-708/ 813L	3	5	GND
Reset Active HIGH	5	RST	SP707/708	8	2	RESET
Reset Active HIGH	5	RST	SP813L	7	1	RESET
Reset Active LOW	6	$\overline{\text{RST}}$	SP705-708	7	1	$\overline{\text{RESET}}$
Watchdog Input	7	$\overline{\text{ST}}$ (H to L)	SP705/706/ 813L	6	8	WDI (any trans.)
Voltage Input	8	V_{cc}	SP705-708/ 813L	2	4	V_{cc}
Power Fail Input	N/A	N/A	SP705-708/ 813L	4	6	PFI
Power Fail Output	N/A	N/A	SP705-708/ 813L	5	7	$\overline{\text{PFO}}$
Watchdog Output	N/A	N/A	SP705/706/ 813L	8	2	$\overline{\text{WDO}}$

Fig. 26: Device Overviw on Maxim/Dallas Semiconductor

PACKAGE SPECIFICATION

8-PIN NSOIC



REVISION HISTORY

REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/16/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	CHANGE DRAWING LOGO ADN COMPANY NAME	11/16/07	JL

8 Pin SOICN JEDEC MS-012 Variation AA

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		

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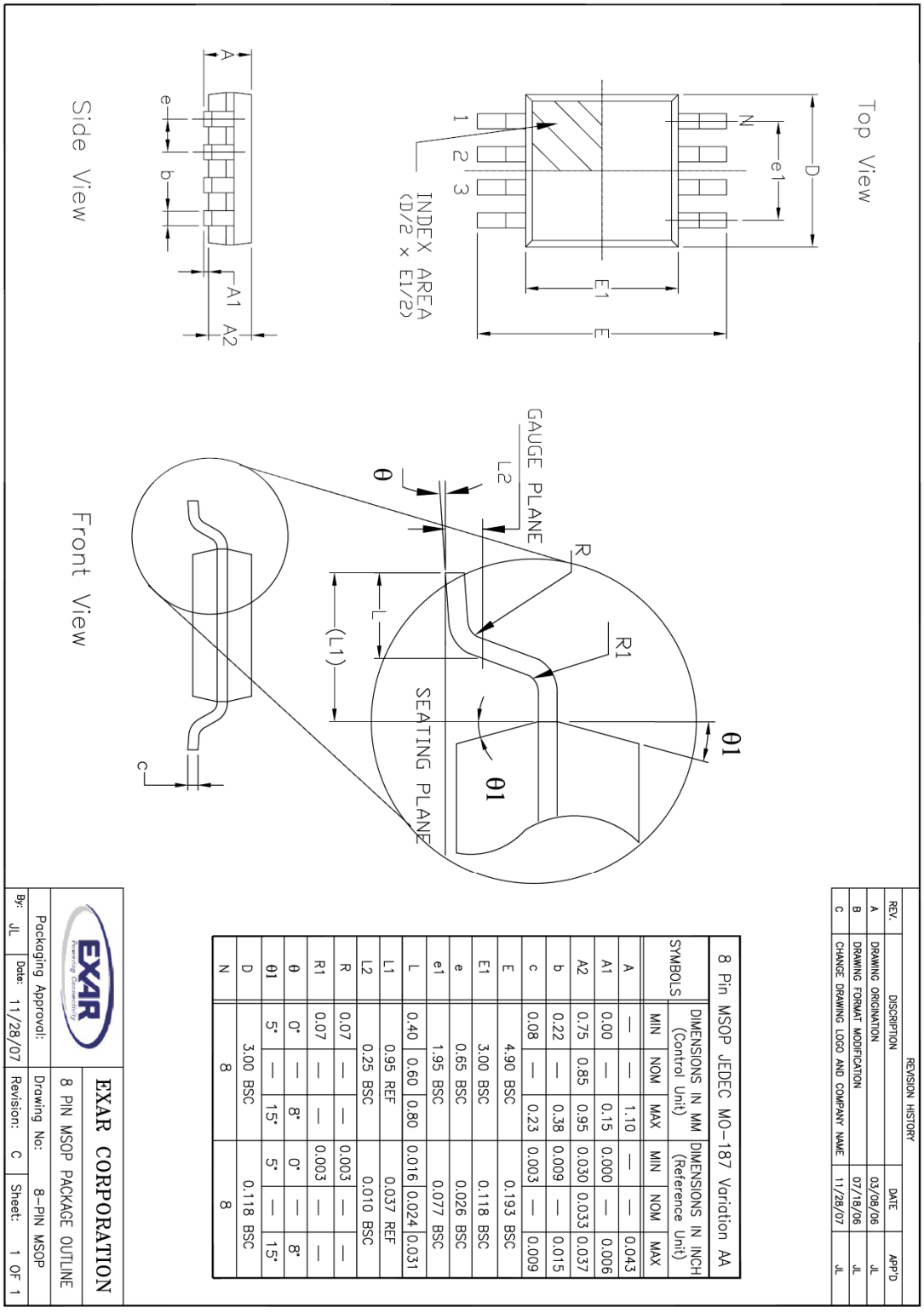
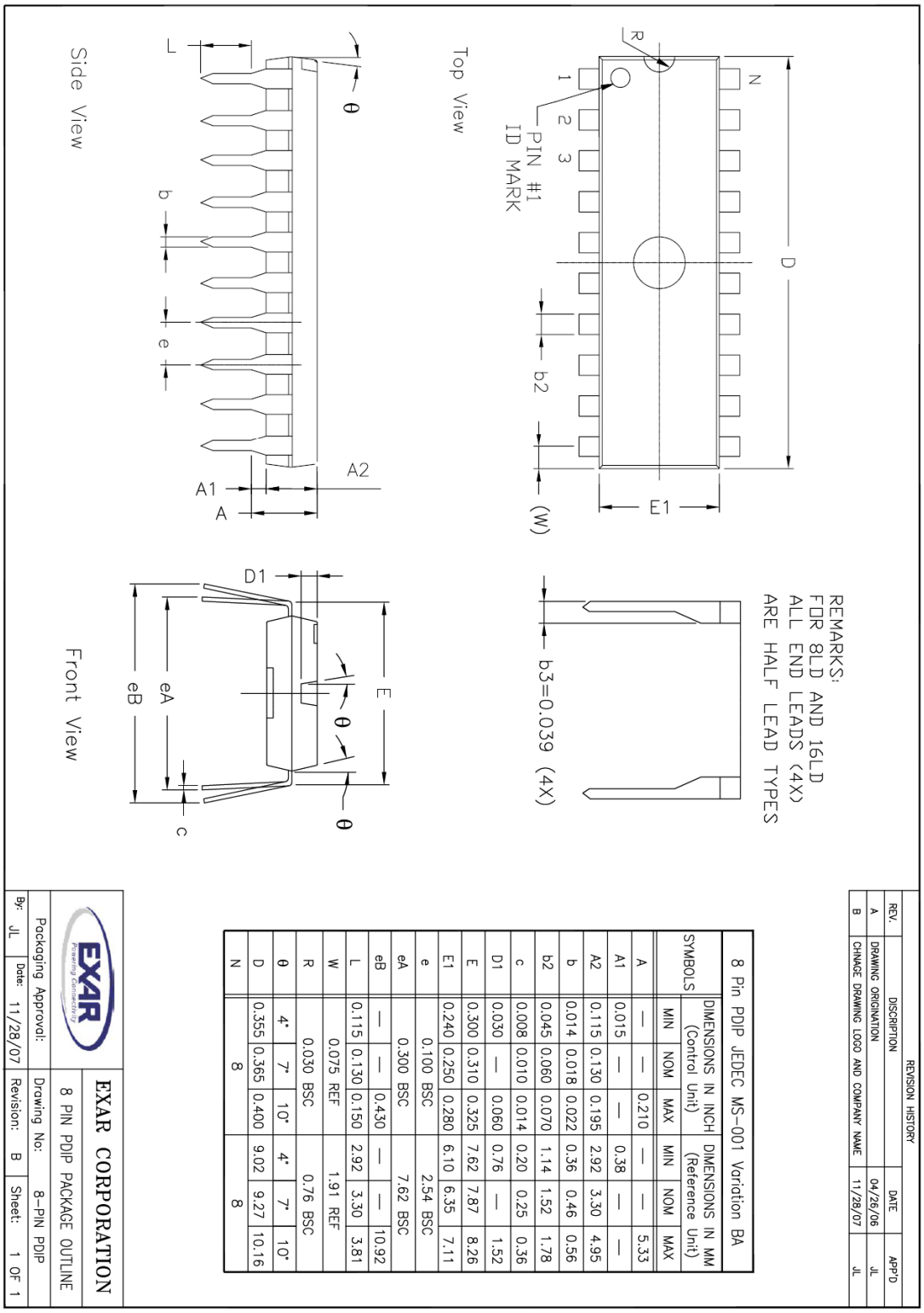
8 PIN SOICN PACKAGE OUTLINE

Packaging Approval:	Drawing No: 8-PIN SOICN
By: JL Date: 11/16/07	Revision: C Sheet: 1 OF 1

8-PIN MSOP


Top View
Side View
Front View
INDEX AREA
(D/2 x E1/2)
GAUGE PLANE
SEATING PLANE
REVISION HISTORY
REV. DESCRIPTION DATE APP'D
A DRAWING ORIGINATION 03/08/06 JL
B DRAWING FORMAT MODIFICATION 07/18/06 JL
C CHANGE DRAWING LOGO AND COMPANY NAME 11/28/07 JL
8 Pin MSOP JEDEC MO-187 Variation AA
SYMBOLS
DIMENSIONS IN MM (Control Unit)
DIMENSIONS IN INCH (Reference Unit)
MIN NOM MAX MIN NOM MAX
A — — 1.10 — — 0.043
A1 0.00 — 0.15 0.000 — 0.006
A2 0.75 0.85 0.95 0.030 0.033 0.037
b 0.22 — 0.38 0.009 — 0.015
c 0.08 — 0.23 0.003 — 0.009
E 4.90 BSC 0.193 BSC
E1 3.00 BSC 0.118 BSC
e 0.65 BSC 0.026 BSC
e1 1.95 BSC 0.077 BSC
L 0.40 0.60 0.80 0.016 0.024 0.031
L1 0.95 REF 0.037 REF
L2 0.25 BSC 0.010 BSC
R 0.07 — — 0.003 — —
R1 0.07 — — 0.003 — —
θ 0° — 8° 0° — 8°
θ1 5° — 15° 5° — 15°
D 3.00 BSC 0.118 BSC
N 8 8
EXAR CORPORATION
8 PIN MSOP PACKAGE OUTLINE
Packaging Approval: Drawing No: 8-PIN MSOP
By: JL Date: 11/28/07 Revision: C Sheet: 1 OF 1

8-PIN PDIP



REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	04/26/06	JL
B	CHNAGE DRAWING LOGO AND COMPANY NAME	11/28/07	JL

8 Pin PDIP JEDEC MS-001 Variation BA

SYMBOLS	DIMENSIONS IN INCH (Control Unit)			DIMENSIONS IN MM (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	0.210	—	—	5.33
A1	0.015	—	—	0.38	—	—
A2	0.115	0.130	0.195	2.92	3.30	4.95
b	0.014	0.018	0.022	0.36	0.46	0.56
b2	0.045	0.060	0.070	1.14	1.52	1.78
c	0.008	0.010	0.014	0.20	0.25	0.36
D1	0.030	—	0.060	0.76	—	1.52
E	0.300	0.310	0.325	7.62	7.87	8.26
E1	0.240	0.250	0.280	6.10	6.35	7.11
e	0.100 BSC			2.54 BSC		
eA	0.300 BSC			7.62 BSC		
eB	—	—	0.430	—	—	10.92
L	0.115	0.130	0.150	2.92	3.30	3.81
W	0.075 REF			1.91 REF		
R	0.030 BSC			0.76 BSC		
θ	4°	7°	10°	4°	7°	10°
D	0.355	0.365	0.400	9.02	9.27	10.16
N	8			8		

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8 PIN PDIP PACKAGE OUTLINE

Packaging Approval:	Drawing No:	8-PIN PDIP
By: JL Date: 11/28/07	Revision: B	Sheet: 1 OF 1

REVISION HISTORY

Revision	Date	Description
2.0.0	06/03/2010	Reformat of datasheet
2.1.0	06/02/2011	Minimum WDI Pulse Width t_{WP} reduced from 1µs to 100ns. Change will be effective with release of Device Product Change Notice.

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