

Improved Quad SPST CMOS Analog Switches

FEATURES

- Low On-Resistance: 45 Ω
- Low Power Consumption: 1.0 mW
- Fast Switching Action— t_{ON} : 120 ns
- Low Charge Injection—Q: -1 pC
- TTL/CMOS-Compatible Logic
- Single Supply Capability

BENEFITS

- Less Signal Errors and Distortion
- Reduced Power Supply Requirements
- Faster Throughput
- Reduced Pedestal Errors
- Simple Interfacing

APPLICATIONS

- Audio Switching
- Data Acquisition
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment
- Medical Instruments

DESCRIPTION

The DG441B/442B are monolithic quad analog switches designed to provide high speed, low error switching of analog and audio signals. The DG441B/442B are upgrades to the original DG441/442.

Combining low on-resistance (45 Ω , typ.) with high speed (t_{ON} 120 ns, typ.), the DG441B/442B are ideally suited for Data Acquisition, Communication Systems, Automatic Test Equipment, or Medical Instrumentation. Charge injection has

been minimized on the drain for use in sample-and-hold circuits.

The DG441B/442B are built using Vishay Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

When on, each switch conducts equally well in both directions and blocks input voltages to the supply levels when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



| TRUTH TABLE | | |
|-------------|--------|--------|
| Logic | DG441B | DG442B |
| 0 | ON | OFF |
| 1 | OFF | ON |

Logic "0" \leq 0.8 V
Logic "1" \geq 2.4 V



ORDERING INFORMATION

| Temp Range | Package | Part Number |
|-------------|--------------------|-------------|
| -40 to 85°C | 16-Pin Plastic DIP | DG441BDJ |
| | | DG442BDJ |
| | 16-Pin Narrow SOIC | DG441BDY |
| | | DG442BDY |
| | 16-Pin QFN 4x4 mm | DG441BDN |
| | | DG442BDN |



ABSOLUTE MAXIMUM RATINGS

| | |
|---|--|
| V+ to V- | 44 V |
| GND to V- | 25 V |
| Digital Inputs ^a V _S , V _D | (V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first |
| Continuous Current (Any Terminal) | 30 mA |
| Current, S or D (Pulsed 1 ms, 10% duty cycle) | 100 mA |
| Storage Temperature | -65 to 125°C |

| | |
|--|--------|
| Power Dissipation (Package) ^b | |
| 16-Pin Plastic DIP ^c | 470 mW |
| 16-Pin Narrow Body SOIC ^d | 900 mW |
| QFN-16 ^d | 850 mW |

Notes:

- Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6 mW/°C above 75°C
- Derate 12 mW/°C above 25°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| SPECIFICATIONS ^a FOR DUAL SUPPLIES | | | | | | | |
|---|----------------------|--|--|-----------------------|------------------|------------------|------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V, V _L = 5 V, V _{IN} = 2.4 V, 0.8 V _F | Temp ^b | Limits -40 to 85°C | | | Unit |
| | | | | Min ^d | Typ ^c | Max ^d | |
| Analog Switch | | | | | | | |
| Analog Signal Range ^e | V _{ANALOG} | | Full | -15 | | 15 | V |
| Drain-Source On-Resistance | r _{DS(on)} | I _S = 1 mA, V _D = ∓10 V | Room Full | | 45 | 80 95 | Ω |
| On-Resistance Match Between Channels ^e | Δr _{DS(on)} | I _S = 1 mA, V _D = ±10 V | Room Full | | 2 | 4 5 | |
| Switch Off Leakage Current | I _{S(off)} | V _D = ±14 V, V _S = ∓14 V | Room Full | -0.5 -5 | ±0.01 | 0.5 5 | nA |
| | I _{D(off)} | | Room Full | -0.5 -5 | ±0.01 | 0.5 5 | |
| Channel On Leakage Current | I _{D(on)} | V _S = V _D = ±14 V | Room Full | -0.5 -10 | ∓0.02 | 0.5 10 | |
| Digital Control | | | | | | | |
| Input Voltage Low | V _{INL} | | Full | | | 0.8 | V |
| Input Voltage High | V _{INH} | | Full | 2.4 | | | |
| Input Current V _{IN} Low | I _{INL} | V _{IN} under test = 0.8 V, All Other = 2.4 V | Full | -1 | -0.01 | 1 | μA |
| Input Current V _{IN} High | I _{INH} | V _{IN} under test = 2.4 V, All Other = 0.8 V | Full | -1 | 0.01 | 1 | |
| Dynamic Characteristics | | | | | | | |
| Turn-On Time | t _{ON} | R _L = 1 kΩ, C _L = 35 pF V _S = 10 V, See Figure 2 | Room | | | 120 | ns |
| Turn-Off Time | t _{OFF} | | Room | | | 65 | |
| Charge Injection ^e | Q | C _L = 1 nF, V _S = 0 V, V _{gen} = 0 V, R _{gen} = 0 Ω | Room | | -1 | | pC |
| Off Isolation ^e | OIRR | R _L = 50 Ω, C _L = 15 pF, V _S = 1 V _{RMS} f = 100 kHz | Room | | | 90 | dB |
| Crosstalk (Channel-to-Channel) | X _{TALK} | | Room | | | 95 | |
| Source Off Capacitance ^e | C _{S(off)} | f = 1 MHz | Room | | | 4 | pF |
| Drain Off Capacitance ^e | C _{D(off)} | | Room | | | 4 | |
| Channel On Capacitance ^e | C _{D(on)} | | V _S = V _D = 0 V, f = 1 MHz | Room | | | |
| Power Supplies | | | | | | | |
| Positive Supply Current | I+ | V+ = 16.5 V, V- = -16.5 V V _{IN} = 0 or 5 V | Room Full | | | 1 5 | μA |
| Negative Supply Current | I- | | Room Full | -1 -5 | | | |

SPECIFICATIONS^a FOR SINGLE SUPPLY

| Parameter | Symbol | Test Conditions Otherwise Unless Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$ | Temp ^b | Limits -40 to 85°C | | | Unit |
|----------------------------------|--------------|---|-------------------|-----------------------|------------------|------------------|---------------|
| | | | | Min ^d | Typ ^c | Max ^d | |
| Analog Switch | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | 0 | | 12 | V |
| Drain-Source On-Resistance | $r_{DS(on)}$ | $I_S = 1\text{ mA}, V_D = 3\text{ V}, 8\text{ V}$ | Room Full | | 90 | 160 200 | Ω |
| Dynamic Characteristics | | | | | | | |
| Turn-On Time | t_{ON} | $R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ $V_S = 8\text{ V}$, See Figure 2 | Room | | 120 | 300 | ns |
| Turn-Off Time | t_{OFF} | | Room | | 60 | 200 | |
| Charge Injection | Q | $C_L = 1\text{ nF}, V_{gen} = 6\text{ V}, R_{gen} = 0\ \Omega$ | Room | | 4 | | pC |
| Power Supplies | | | | | | | |
| Positive Supply Current | I_+ | $V_{IN} = 0\text{ or }5\text{ V}$ | Room Full | | | 1 5 | μA |
| Negative Supply Current | I_- | | Room Full | | -1 -5 | | |

Notes:

- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

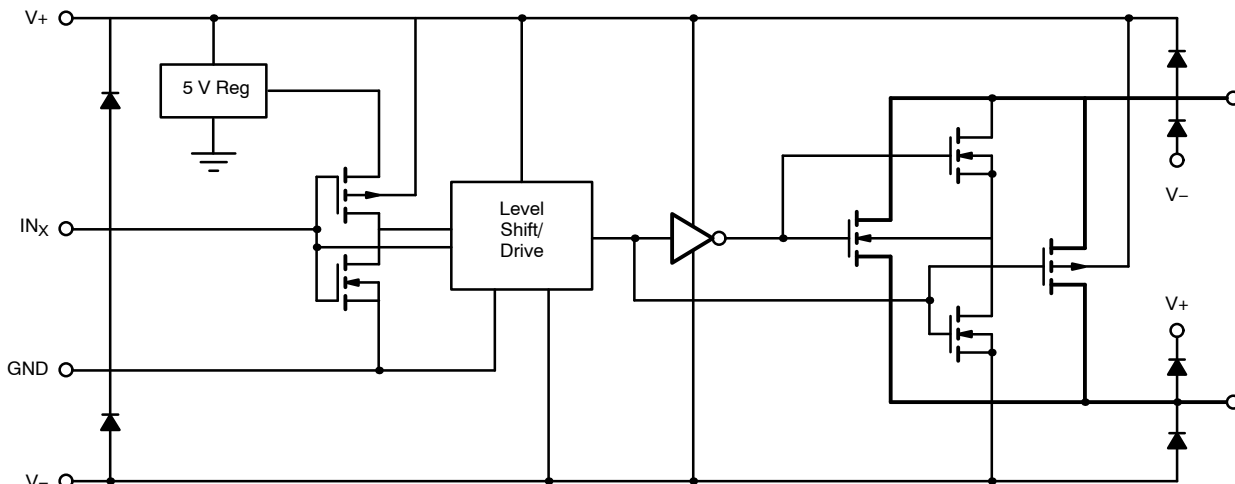
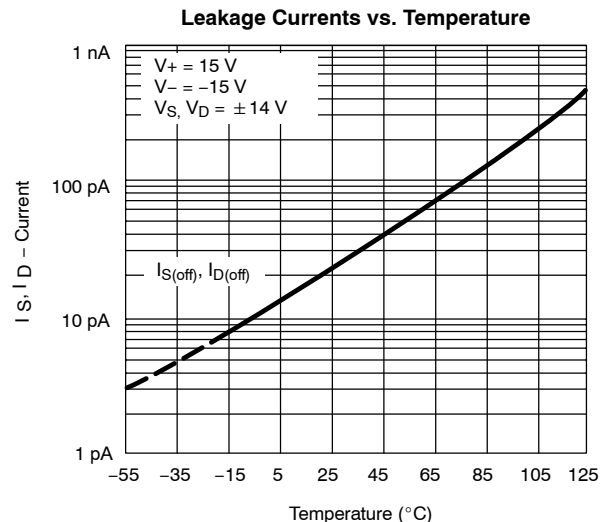
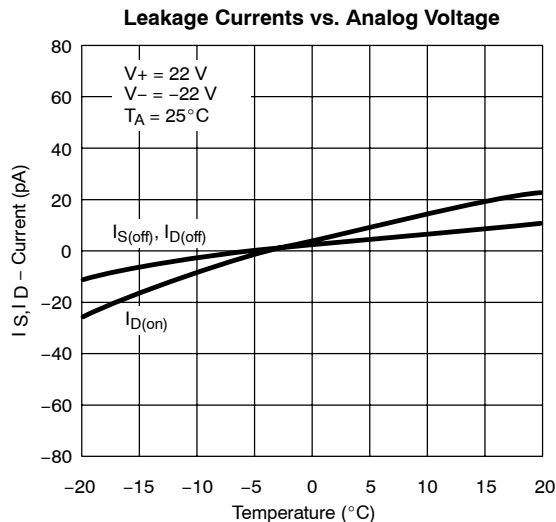
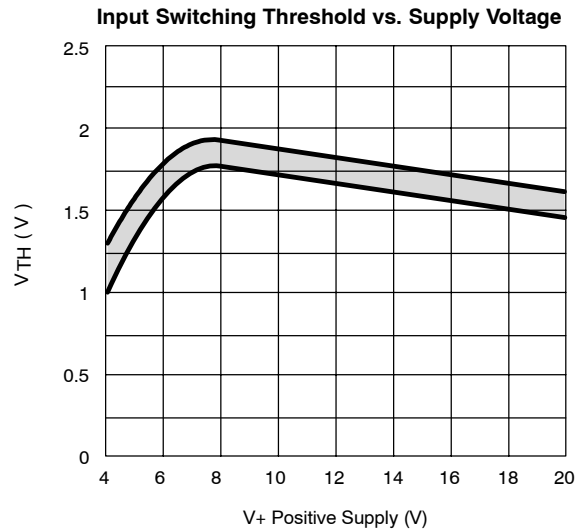
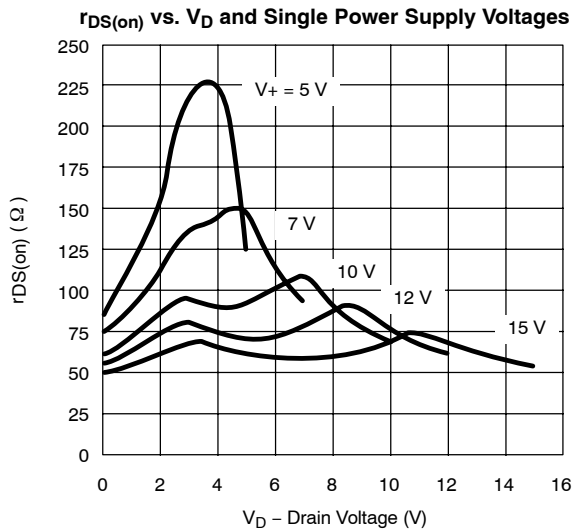
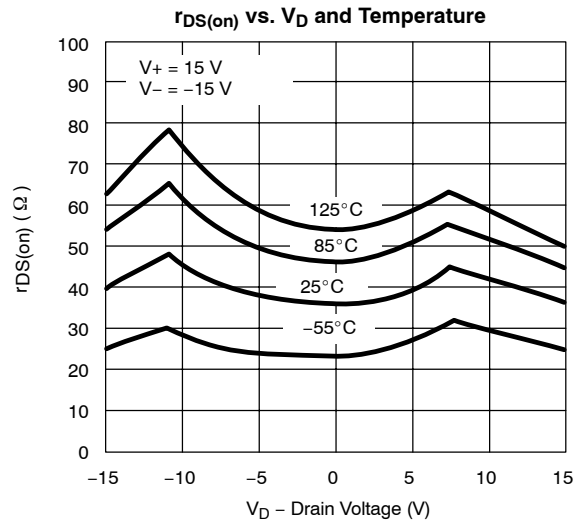
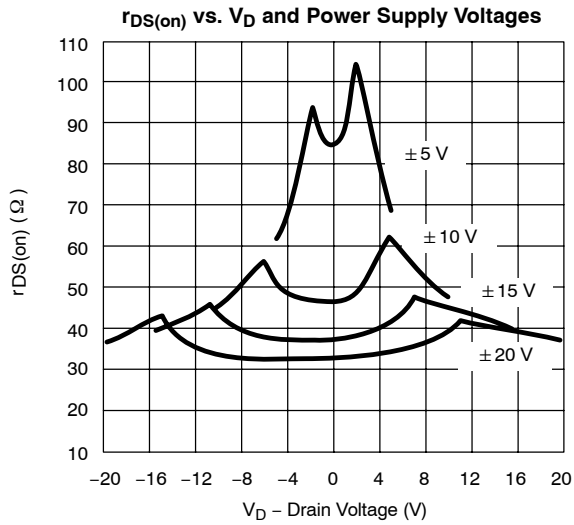


FIGURE 1.

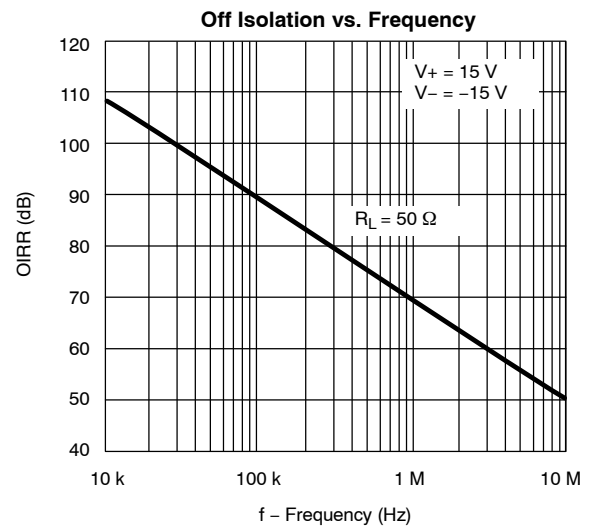
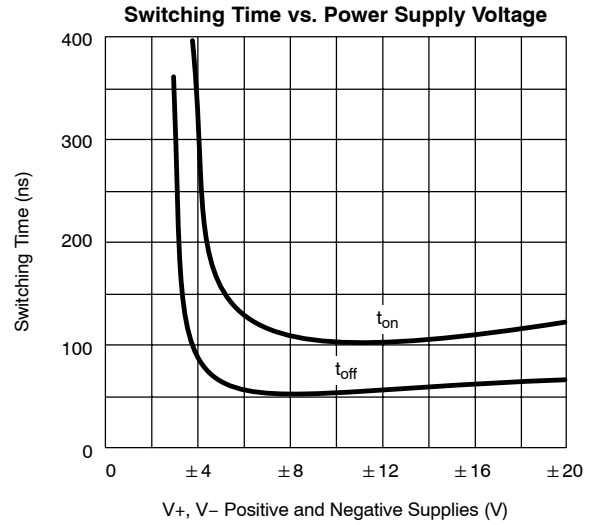


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

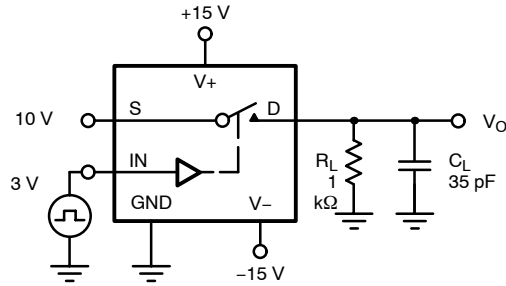




TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TEST CIRCUITS



C_L (includes fixture and stray capacitance)



Note: Logic input waveform is inverted for DG442.

FIGURE 2. Switching Time

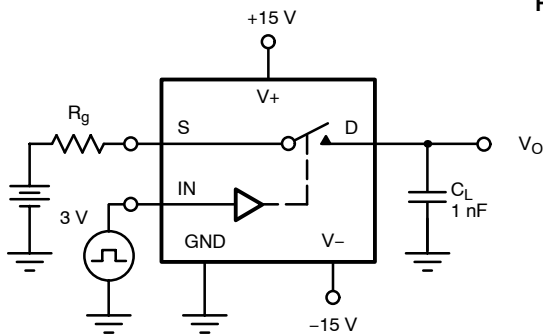


FIGURE 3. Charge Injection

$C = 1 \text{ mF}$ tantalum in parallel with 0.01 mF ceramic



$$X_{\text{TALK Isolation}} = 20 \log \left| \frac{V_S}{V_O} \right|$$

$C = \text{RF bypass}$

FIGURE 4. Crosstalk



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

FIGURE 5. Off Isolation



FIGURE 6. Source/Drain Capacitances

APPLICATIONS

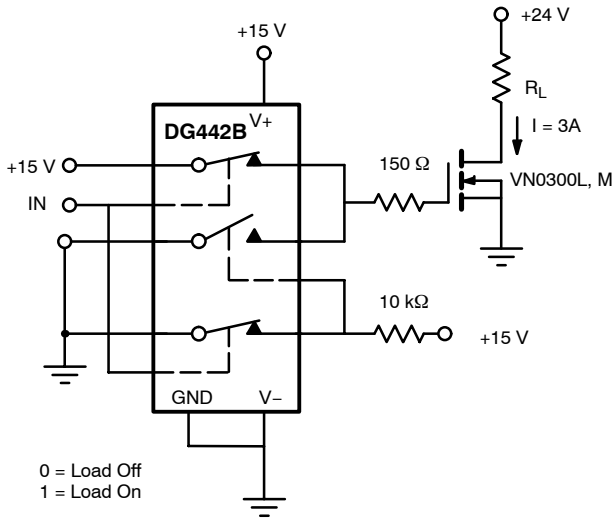


FIGURE 7. Power MOSFET Driver



FIGURE 8. Open Loop Sample-and-Hold

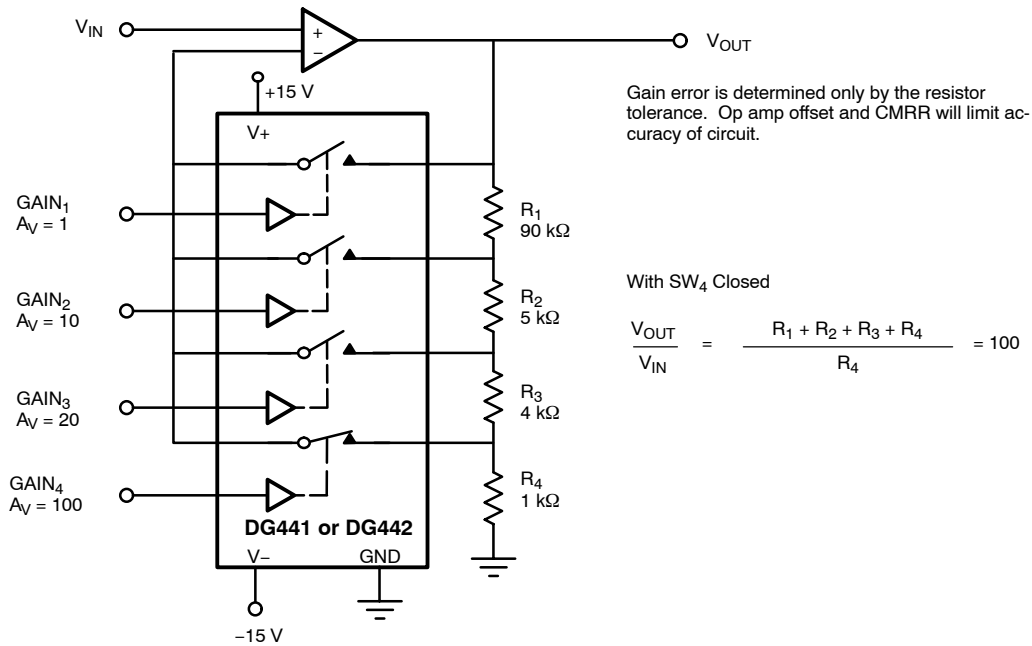


FIGURE 9. Precision-Weighted Resistor Programmable-Gain Amplifier

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