PD671xxx - 8 / 12 / 24-Channel PoE AF and AT DIMM
Data Sheet (Non-confidential)

DESCRIPTION

Microsemi's™ new and unique family of Power over Ethernet (PoE) modules enable next-generation network devices to share data and power over the same cable. The PD671xxx PoE PSE modules are fit / form compatible with the standard plug-in memory modules used in personal computers (Dual Inline Memory Modules - DIMMs) (see Figure 1 and Figure 12). Thus, the use of these modules permit network devices to be designed for up to 96 ports, with fewer ports actually installed. Additional modules can be inserted in the field at any time.

The PD671xxx (8, 12 or 24 ports DIMM) includes a wide range of functions. Some of these modules include the PD69000 micro-controller unit (PoE controller) for Enhanced features and a flexible work environment in a DIMM master or DIMM slave configuration (refer to Ordering Information, page 2).

Microsemi's PoE PD671xxx DIMMs implement real time mechanisms including detection, classification, port real-time protection and system level functions (power management and MIB support).

Microsemi's PD69012 IC, 12-channel PoE Manager IC is at the heart of these modules. PD671xxx DIMMs enable the detection of IEEE802.3at-2009 Type 1 (low power) or Type 2 (high power) Powered Devices (PDs), ensuring safe power feeding and removal over Ethernet ports. The PD69012-based DIMMs detect and disable disconnected ports, using DC or AC disconnection methods. The DIMMs are embedded in multi-port and highly populated Ethernet switches, requiring a minimum of external components.

The PD671xxx DIMM is fully backwards compatible with the PD670xx DIMM and can be dropped into existing designs.

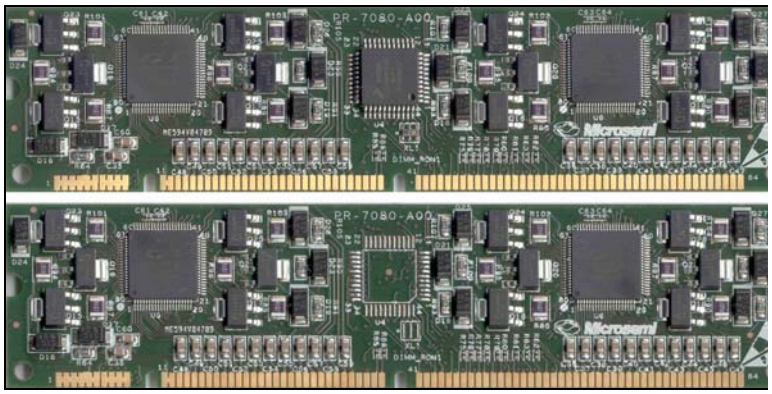

Figure 1: PoE PD67124 DIMM

IMPORTANT: For the most current data, consult Microsemi's website:
http://www.microsemi.com

KEY FEATURES

- IEEE 802.3AT-2009 and IEEE802.3AF-2003 compliant
- Up to 30 W per port power PoE solution
- RoHS compliant
- Supports IETF PoE MIB (RFC 3621)
- Up to 24 power ports per single DIMM
- Up to 96 ports in a system, using master and slave configuration
- Thermal protection per port
- Thermal monitoring capabilities
- Pre-standard detection methods (Cisco Inline Power and Power over LAN Legacy)
- Non-standard terminals supported
- DC disconnect with DC modulation
- AC disconnect function utilizing external diodes
- PD 2-events classification function
- Operates using a single input (44 to 57 VDC)
- I^2C or UART host interface
- Host communication is backward compatible with PD67024M communication, or Marvell® ISSR
- Programmable over current protection per port
- Built-in power management algorithm
- Internal power-on reset mechanism
- Fast port shutdown on power supply failure
- Supports Backplane Power Management
- Automatic on/off sequencer for 96 ports
- Disable/enable power per port
- Continuous port current monitoring
- Serial interface for LED indicator support
- Backwards compatible with PD670xx
- Fit/form compliant with168-pin DIMM JEDEC MO-161F, 3.3 V
- Space efficient compact design
- Factory pre-tested, for plug-and-play integration
- Safety standard compliant: UL / cUL per UL60950-1 (mounted on Microsemi evaluation board)

Ordering Information				
Part Number	**Ports**	**Port Disconnect Method**	**DIMM Master/Slave**	**Mode Enhanced/Auto [3]**
PD67124MDC-gggg [1]	24	DC	Master	Enhanced
PD67124S	24	AC/DC [4]	Slave [2]	Enhanced
PD67112MDC-gggg	12	DC	Master	Enhanced
PD67108MDC-gggg	8	DC	Master	Enhanced
PD67124MAC-gggg	24	AC	Master	Enhanced
PD67112MAC-gggg	12	AC	Master	Enhanced
PD67108MAC-gggg	8	AC	Master	Enhanced
PD67124AM	24	AC/DC [5]	Master	Auto
PD67124AS	24	AC/DC [5]	Slave [2]	Auto
PD67112AM	12	AC/DC [5]	Master	Auto
PD67108AM	8	AC/DC [5]	Master	Auto

Note:
[1] – gggg: MCU software version.
[2] – DIMM Slave should be used in conjunction with DIMM Master (for systems require more than 24 ports).
[3] – Enhanced and Auto mode of operation stand for the PoE system features. The Enhanced mode system includes the PD69000 PoE controller.
[4] – DIMM Slave port disconnection method is determined by the DIMM Master which controllers it.
[5] – DIMM functioning at the Auto Mode Configuration can be configured to AC or DC port disconnection method by the system host. Further details can be found in the Auto Mode User Guide, Catalogue Number 06-1200-056.

APPLICABLE DOCUMENTS

- IEEE 802.3at-2009 standard, DTE Power via MDI
- PD69012 Data Sheet, Catalogue Number 06-0069-058
- PD69000 Data Sheet, Catalogue Number 06-0070-058
- Serial Communication Protocol User Guide 06-0032-056
- Auto Mode User Guide, Catalogue Number 06-1200-056
- Layout Design Guidelines for DIMM-based PoE Systems, AN-132 Catalogue Number 06-0010-080
- Designing a DIMM-based PoE System, AN-133 Catalogue Number 06-0011-080

2381 Morse Avenue, Irvine, CA 92614, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

ABSOLUTE MAXIMUM RATINGS

Vmain	-0.3 to 80 VDC (1)
DGND, AGND, QGND	-0.3 to 0.3 VDC (2)
VPORT_POSx, VPORT_NEGx	-0.3 to 80 VDC (1)
3_3Vout	3.8 VDC
EXT_REG	-0.3 to 6 VDC
I^2C_Addr_M.	-0.3 to (3_3Vout + 0.3 VDC)
MISO, MOSI, SCK, CS, SCL, SDA, SSn, Led_Cs, Asic_Reset	-0.3 to (3_3Vout + 0.3 VDC)
ESD (Human Body Model)	± 2 kV (3)
Storage temperature	-40° to +125° C

Notes: "x" defines port numbers, 0 to 11, inclusive.

(1) 80 VDC is the transient voltage that can be applied for up to one minute.

(2) Maximum voltage value between grounds.

(3) ESD Human Body Model is: (CZap = 100 pF, RZap = 1500 Ω).

Stresses beyond those listed above can cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods could affect device reliability.

CALCULATED MTBF DATA [1]

	Operation mode	Failures per 10^6 Hours	MTBF(Hours)
PD67124M @ 25°C Ambient	IEEE 802.3AT-2009	0.5181	1930000
PD67124M @ 25°C Ambient	IEEE802.3AF-2003	0.5128	1950000

Notes:

[1] – MTBF calculation made for the worst case PoE DIMM populated with 24 fully loaded ports

OPERATING CONDITIONS

PARAMETER	MIN.	NOM.	MAX.	UNIT
Operating ambient temperature	-10		+70	°C
Operating voltage (see Figure 2)	40 to 44	44 to 55	55 to 57	VDC
Operating humidity (non-condensing, Per IEC 68-2-56)			95	%

Notes:
Operating functions depend on the input voltage.
Operating voltage range for IEEE802.3AF is 44 to 57 VDC
Operating voltage range for IEEE802.3AT (High Power) is 50 to 57 VDC

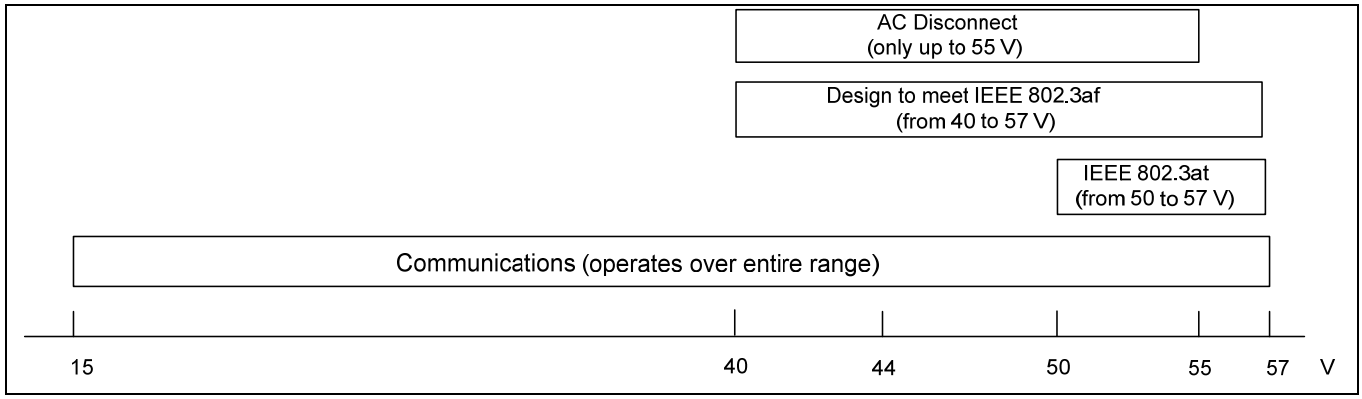

Figure 2: Operational voltage Ranges

Airflow

To prevent overheating, the application designer should supply a minimal airflow to the PD671xxx DIMMs. Figure 3 shows the power handling capability versus air velocities in meter/second, as measured at all points of the DIMM envelope, prior to insertion into the connector(s). As shown in Figure 12, the connectors are spaced by 35 mm; 1 m/s = 197 LFM (linear feet per minute). Maximum allowed temperature is +85° C for the MCU (PD69000) and +125° C for the PD69012.

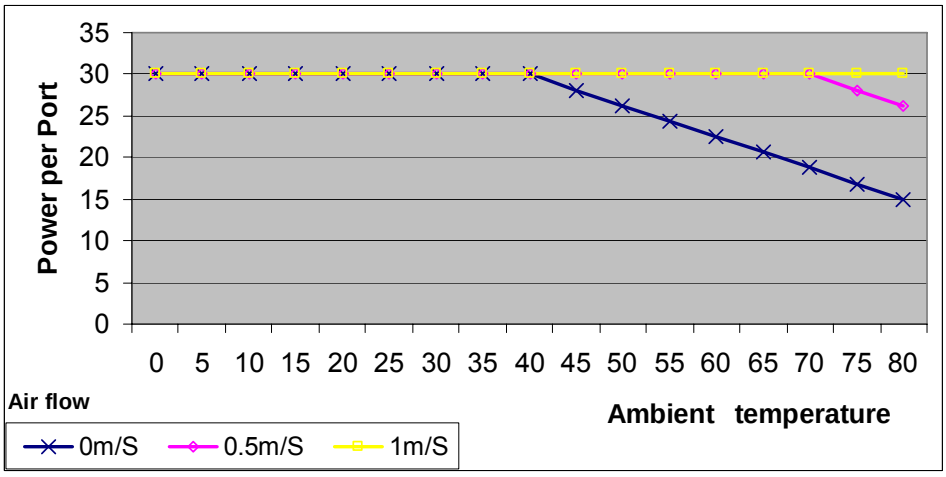

Figure 3: Power per Port for two DIMMs (48 ports)

Electrical Characteristics

The following sections detail the DC and analog characteristics.

DC Characteristics for Digital Inputs and Outputs

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	REMARKS
Pin Name	**SCL, xDisable_Ports, Rx (without internal pull-up/pull-down resistor)**				
Type	**Schmitt Trigger CMOS input, TTL level**				
High level input voltage	V_{IH}	2.0		V	
Low level input voltage	V_{IL}		0.8	V	
Input voltage hysteresis		0.3		V	
Input high current	I_{IH}	-1	+1	µA	
Input low current	I_{IL}	-1	+1	µA	
Pin Name	**MOSI, MISO, CS, Tx (without internal pull-up/down resistor) SCK (with internal resistor)**				
Type	CMOS I/O, TTL level				
High level input voltage	V_{IH}	2.0		V	
Low level input voltage	V_{IL}		0.8	V	
Input voltage hysteresis		0.3		V	
Input high current	I_{IH}	-1	+1	µA	
Input low current	I_{IL}	-1	+1	µA	
High level output voltage		V_{PERI}-0.4V		V	I_{out} = 3 mA
Low level output voltage			0.4	V	I_{out} = 3 mA
Tri state output current		-1	+1	µA	
Pin Name	**xAsic_Reset (with internal resistor) SDA (without internal resistor)**				
Type	CMOS open drain output with Schmitt Trigger input, TTL level				
High level input voltage	V_{IH}	2.0		V	
Low level output voltage	V_{OH}		0.4	V	I_{out} = 3mA
Low level input voltage	V_{IL}		0.8	V	
Input voltage hysteresis		0.3		V	
OFF state output current		-1	+1	µA	

Electrical Characteristics for Analog I/O Pads

PARAMETER	MIN	MAX	UNIT	REMARKS
Pin Name	**VPORT_POSx**			
Operating voltage	44	62	V	
Pin current consumption	-5	+10	µA	Port driver, Vport measurement and AC generator are off
Pin Name	**VPORT_NEGx**			
Operating voltage	0	Vmain	V	Port driver, V_{port} measurement and AC generator are off
Pin current consumption	-5	+10	µA	
Pin Name	**Vmain**			
Operating voltage – AF mode	40	57	V	Recommended Range 48v to 55v
Operating voltage – AT mode	50	57	V	Recommended Range 51v to 55v
V_{main} current consumption		40	mA	Total on V_{main}
Pin Name	**3_3Vout**			
Voltage	3.13	3.46	V	
Output current		6	mA	Without external NPN (see Q1 in Figure 8)
		30	mA	When using external NPN for V_{PERI} (see Q1 in **Figure 8**)

Dynamic Characteristics

The PD671xxx DIMMs utilize three programmable current level thresholds (I_{min}, I_{cut}, I_{lim}) and two timers (T_{min}, T_{cut}), to operate as shown in Figure 4. Loads that consume more than I_{cut} for longer than T_{cut} (OVL_S to OVL) are categorized as 'overloads' and are automatically shutdown. Automatic recovery from overload and no-load conditions is attempted every T_{OVLREC} and T_{UDLREC} periods (typically 5 and 1 seconds, respectively). Output current is limited to I_{lim}, which is the maximum peak current allowed at each port.

DC Disconnect

Output current consumption below I_{min} for more than T_{PMDO} (UDL_S to UDL) is categorized as 'no-load' and is shutdown.

AC Disconnect

A port maintains power if Zac < 27 KΩ

A port shutdowns power if Zac > 1980 KΩ for a time period greater than TPMDO.

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Automatic recovery from	T_{OVLREC} value, measured from port shutdown (can be modified via control port)			5		s
Automatic recovery from no-	T_{UDLREC} value, measured from port shutdown point (can be modified via control port)			1		s
Inrush current	I_{Inrsh}	For t = 50 ms, C_{load} =180 uF max.			750	mA
Output current operating range	I_{port}	Continuous operation after startup period	10		700	mA
Output power available, operating range	P_{port}	Continuous operation after startup period, at port output (@ Vport = 57 VDC)	0.57		30	W
DC disconnect OFF mode	I_{min1}	Must disconnect for **t** greater than T_{UVL}	0		5	mA
	I_{min2}	May or may not disconnect for t greater than T_{UVL}	5	7.5	10	mA
AC Disconnect OFF mode	Zac1	Does not remove power			27	KΩ
	Zac2	Remove power	1980			KΩ
PD power maintenance	T_{PMD}	Buffer period to handle transitions	300		400	ms
Over load current detection range	I_{cut}	Time limited to T_{OVL}	660	680	700	mA
Over load time limit	T_{OVL}	Typical timer accuracy is 2 ms	50		75	ms
Turn on rise time	T_{rise}	From 10% to 90% of V_{port} (specified for PD load consisting of 100 uF capacitor	15			us
Port turn off time	Toff	From V_{port} to 5 Vdc			500	ms

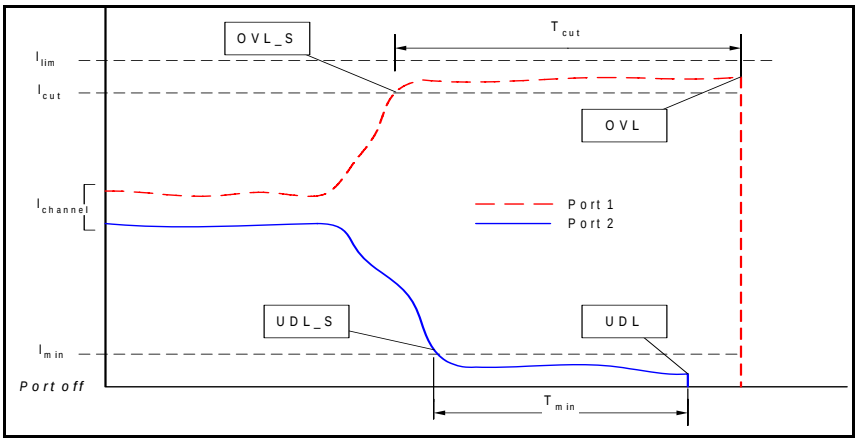

Figure 4: Power Limits

Pin Designations

The PD671xxx DIMMs have a fit/form based on a JEDEC MO-161f outline.

Conventions used in the design are as follows:

- Power and ground connections are reproduced a number of times to carry heavy currents.
- Signals are categorized as analog (input or output) or digital (input, output and I/O).
- All lines which are identified with an "x" prefix are active when logical is low.

Refer to Figure 5.

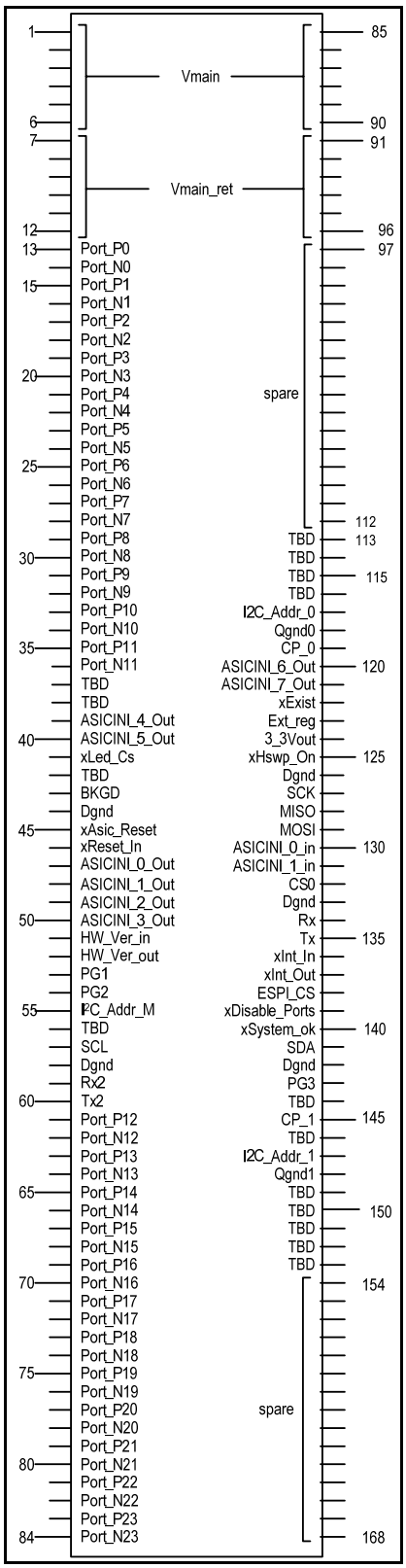

Figure 5: Pinout

Pin Description

Signals are categorized as 'analog' (input or output) or 'digital' (input, output and I/O).

Pin	Pin Name	Pin Type	Pin Description	Pin	Pin Name	Pin Type	Pin Description
1	Vmain	Power input	Main V+ input	85	Vmain	Power input	Main V+ input
2				86			
3				87			
4				88			
5				89			
6				90			
7	Vmain_ret		Main V return	91	Vmain_ret		Main V return
8				92			
9				93			
10				94			
11				95			
12				96			
13	Port_P0	Analog output	Channel 1 positive output	97	Spare		
14	Port_N0		Channel 1 negative output	98			
15	Port_P1		Channel 2 positive output	99			
16	Port_N1		Channel 2 negative output	100			
17	Port_P2		Channel 3 positive output	101			
18	Port_N2		Channel 3 negative output	102			
19	Port_P3		Channel 4 positive output	103			
20	Port_N3		Channel 4 negative output	104			
21	Port_P4		Channel 5 positive output	105			
22	Port_N4		Channel 5 negative output	106			
23	Port_P5		Channel 6 positive output	107			
24	Port_N5		Channel 6 negative output	108			
25	Port_P6		Channel 7 positive output	109			
26	Port_N6		Channel 7 negative output	100			
27	Port_P7		Channel 8 positive output	111			
28	Port_N7		Channel 8 negative output	112			
29	Port_P8		Channel 9 positive output	113	TBD		TBD
30	Port_N8		Channel 9 negative output	114	TBD		TBD
31	Port_P9		Channel 10 positive output	115	TBD		TBD
32	Port_N9		Channel 10 negative output	116	TBD		TBD
33	Port_P10		Channel 11 positive output	117	I2C_Addr_0	Digital input	Auto mode; sets I2C address
34	Port_N10		Channel 11 negative output	118	Qgnd0	Ground	Quiet ground
35	Port_P11		Channel 12 positive output	119	CP_0	Analog output	NC (not in use)
36	Port_N11		Channel 12 negative output	120	ASICINI_6_Out	Analog output	Determine DIMM 4 managers ESPI address
37	TBD		TBD	121	ASICINI_7_Out		
38	TBD		TBD	122	xExist	Digital output	Grounded internally- DIMM is present
39	ASICINI_4_Out	Analog output	Determine DIMM 3 managers ESPI address	123	Ext_reg	Analog output	External regulation for 3.3 V
40	ASICINI_5_Out			124	3_3Vout	Analog output	3.3 V output to support opto couplers (5 V tolerant)
41	xLed_Cs	Digital output	CS for LED support	125	XHswp_On	Digital output	Connect to MCU
42	TBD		TBD	126	DGND	Ground	Digital ground
43	BKGD	Digital input	Factory use only	127	SCK	Digital I/O	SPI clock – PD69012 internal comm
44	DGND	Ground	Digital ground	128	MISO	Digital I/O	SPI I/O – PD69012 internal comm
45	xAsic_Reset	Digital I/O	Internal reset to PD69012	129	MOSI	Digital I/O	SPI I/O – PD69012 internal comm
46	xReset_In	Digital input	A reset signal driven by the Host CPU to PoE DIMM	130	ASICINI_0_In	Analog input	Determine DIMM managers ESPI address
47	ASICINI_0_Out	Analog output	Determine DIMM 1 manager ESPI address	131	ASICINI_1_In	Analog input	Determine DIMM managers ESPI address
48	ASICINI_1_Out	Analog output	Determine DIMM 1 managers ESPI address	132	CS0	Digital I/O	CS for ESPI
49	ASICINI_2_Out	Analog output	Determine DIMM 2 managers ESPI address	133	DGND	Ground	Digital ground

Pin	Pin Name	Pin Type	Pin Description	Pin	Pin Name	Pin Type	Pin Description
50	ASICINI_3_Out			134	Rx	Digital input	UART input
51	HW_Ver_in	Analog input	Receives the hardware version	135	Tx	Digital output	UART output
52	HW_Ver_out	Analog output	Reports on the hardware version	136	xInt_In	Digital input	NC (not in use)
53	PG1	Digital input	Indicates PS 1 is good; low= PS bad.	137	xInt_Out	Digital output	Interrupt out signal
54	PG2	Digital input	Indicates PS 2 is good; low= PS bad.	138	ESPI_CS	Digital I/O	CS for ESPI between DIMMs
55	I2C_Addr_M	Analog input	Enhanced mode – sets I2C address	139	xDisable_Ports	Digital input	Low=disable from host
56	TBD		TBD	140	xSystem_ok	Digital output	Main DC input status indicator; low = Vmain is out of range.
57	SCL	Digital I/O	I2C clock	141	SDA	Digital I/O	I2C data
58	DGND	Ground	Digital ground	142	DGND	Ground	Digital ground
59	Rx2	Digital input	NC (not in use)	143	PG3	Digital input	Indicates PS 3 is good, low= PS bad
60	Tx2	Digital output	NC (not in use)	144	TBD		TBD
61	Port_P12	Analog output	Channel 13 positive output	145	CP_1	Analog output	NC (not in use)
62	Port_N12	Analog output	Channel 13 negative output	146	TBD		TBD
63	Port_P13		Channel 14 positive output	147	I2C_Addr_1	Digital input	Auto mode; sets I2C address
64	Port_N13		Channel 14 negative output	148	Qgnd1	Ground	Quiet ground
65	Port_P14		Channel 15 positive output	149	TBD		TBD
66	Port_N14		Channel 15 negative output	150	TBD		TBD
67	Port_P15		Channel 16 positive output	151	TBD		TBD
68	Port_N15		Channel 16 negative output	152	TBD		TBD
69	Port_P16		Channel 17 positive output	153	TBD		TBD
70	Port_N16		Channel 17 negative output	154			
71	Port_P17		Channel 18 positive output	155			
72	Port_N17		Channel 18 negative output	156			
73	Port_P18		Channel 19 positive output	157			
74	Port_N18		Channel 19 negative output	158			
75	Port_P19		Channel 20 positive output	159			
76	Port_N19		Channel 20 negative output	160			
77	Port_P20		Channel 21 positive output	161	Spare		
78	Port_N20		Channel 21 negative output	162			
79	Port_P21		Channel 22 positive output	163			
80	Port_N21		Channel 22 negative output	164			
81	Port_P22		Channel 23 positive output	165			
82	Port_N22		Channel 23 negative output	166			
83	Port_P23		Channel 24 positive output	167			
84	Port_N23		Channel 24 negative output	168			

Functional Description

The following sections detail the PD671xxx DIMM Master functions.

System Level

Figure 6 illustrates a 24-port Enhanced mode system based on the PD671xxx DIMM Master.

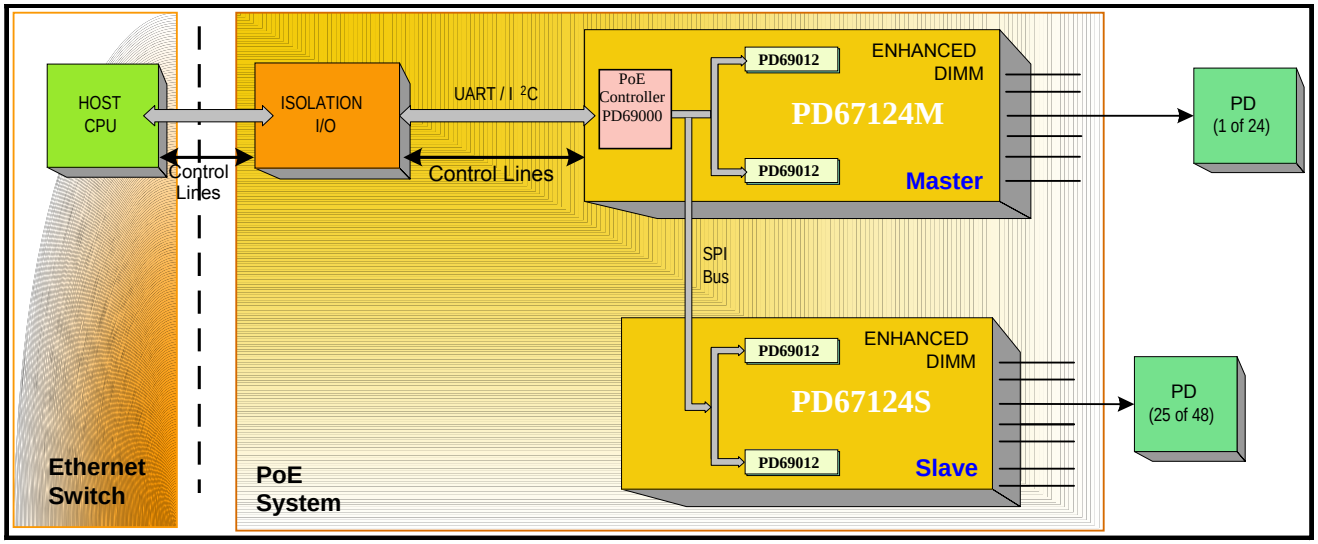

Figure 6: PD67124M/S DIMM Configuration

Figure 7 illustrates a 24-port Auto mode system based on the PD671xxx DIMM Master.

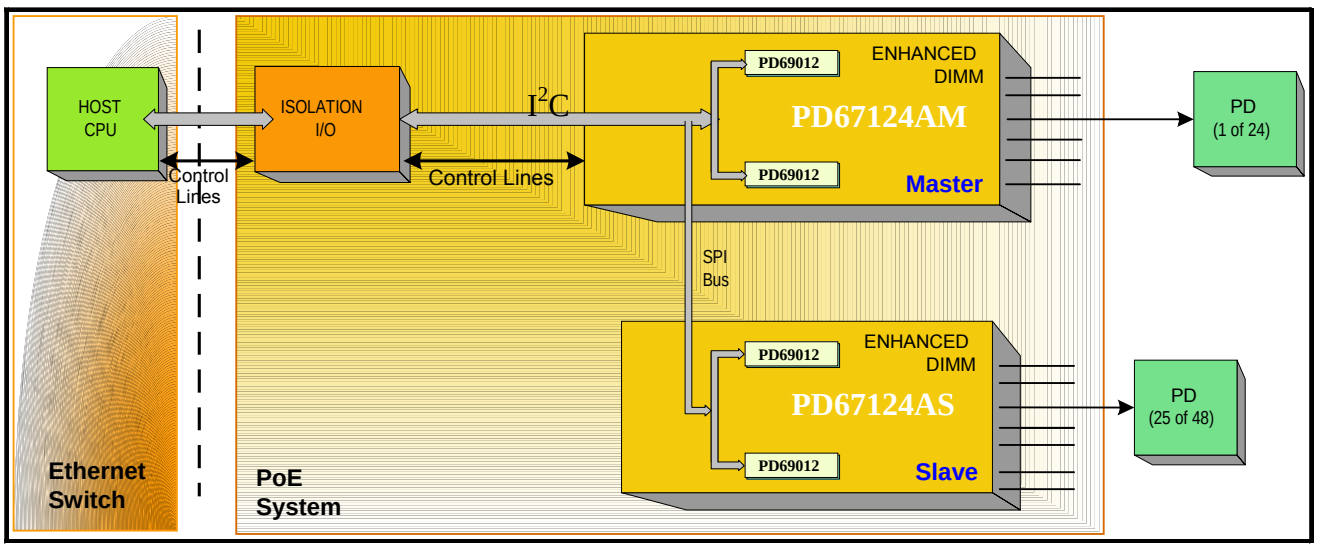

Figure 7: PD67124AM/AS DIMM Configuration

Enhanced Mode PD671xxx DIMM Block Diagram

Figure 8 illustrates the internal circuitry of the Enhanced Mode DIMM Master. PD69012 appears only in one of the 12 port circuits.

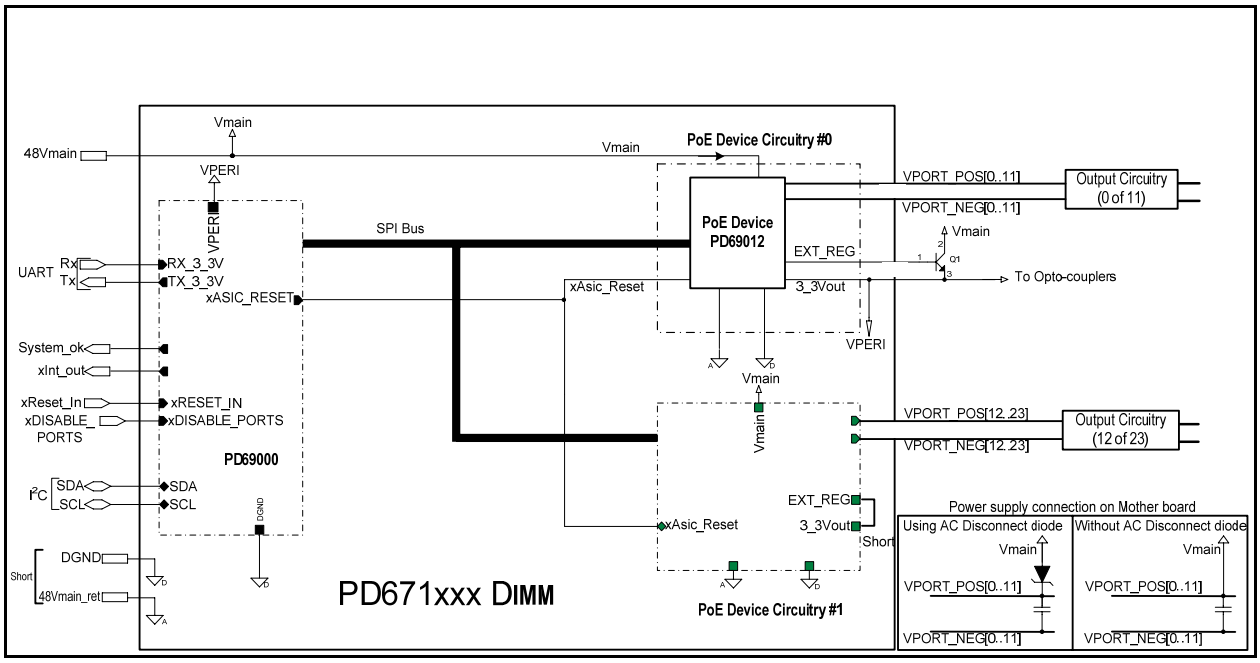

Figure 8: PD67124M DIMM, Internal Block Diagram

Top Assembly Description

The following sections detail the top assembly components.

Power Supply

The entire circuit is powered by a nominal 48 VDC potential (Vmain can range from 44 to 57 VDC for AF mode and 50 to 57 VDC for AT high power mode).

3.3 VDC Regulator

Each of the PD69012 includes a 3.3 VDC regulator (**EXT_REG** and **3_3Vout**) for up to 6 mA. This current is utilized for powering external components in the PoE domain. There is an option of adding a driver to this output to drive higher loads. Q1 provides up to 30 mA to the PoE controller and to the opto-couplers in the interface circuit. The total capacitance on the 3.3 VDC should be less then 4.7 uF (with and without an external driver).

Grounds

The overall circuit includes two physical ground planes, analog and digital, which are electrically connected at a single point on the motherboard (see Figure 9 and Figure 10). This method, used throughout the design, improves noise immunity and coupling. Application note AN-132, Catalogue Number 06-0010-080 provides further details about this design technique.

Control Signals

Several control signals are utilized between the switch and the PoE circuitry:

- **xReset_In:** Driven by the switch circuitry to reset the PoE circuit.
- **xDISABLE_PORTS**: Driven by the switch, to disable all PoE ports immediately.

Indication Signals

- **Int_out:** Enables the Host CPU to reduce the communication volume whenever a PoE event masked by the Host CPU occurs. The PoE Controller sends an interrupt for indication.
- **System_ok: (Enhanced mode only)** An optional hardware single line, driven by the Master DIMM to the Host CPU; this signal provides the Host CPU with a warning that a major failure such as Vmain out of range has occurred.

PD69012 Circuitry

All PD69012s work in slave mode, under control of the PD69000G. The PoE Managers, each controlling 12 output ports, are further detailed in Figure 8. The ports can be disabled by the Ethernet switch via the **xDisable_Ports** signal or by the PoE controller, as required during operation. For further details on the PoE manager, refer to the PoE manager PD69012 Data Sheet, Catalogue Number 06-0072-058.

AC Disconnect Diodes

When deploying an application that utilizes the AC disconnect method, carefully select the diode type and diode location on the mother board. The diode should be located away from the DIMM to prevent mutual heating and the ventilation should be doubled to deal with higher power dissipation. The AC disconnect diode should be connected as shown in Figure 9.

DC Disconnect

Using the DC disconnect method, the mother board should contain a short circuit between Vmain coming from the power supply and Port_P[0-23] as illustrated in Figure 10.

PD671xxx DIMM Evaluation Board

The performance features of Microsemi's PoE DIMMs can be fully appreciated using the PD671xxx - DIMM Evaluation Board.

The Evaluation Board allows the designer to evaluate all of the DIMMs accessible functions. Enhanced mode configuration for up to 48 ports is supported.

Applications

The DIMMs can be integrated into a number of applications, ranging from daughter boards to full integration into Ethernet switches.
Examples of such applications are as follows:

- **Integrated directly into a switch**: Facilitates the entire PoE concept by including the DIMMs on the main switch PCB.
- **Daughter board add-on**: DIMMs are integrated into a small PCB for PoE, mounted on top of the switch's main PCB.
- **Midspan units**: Stand-alone devices, installed between the Ethernet switch and powered devices (telephone, camera, wireless LAN, etc.). These Midspan units include the DIMMs as a PoE control element, injecting power over the communication lines.

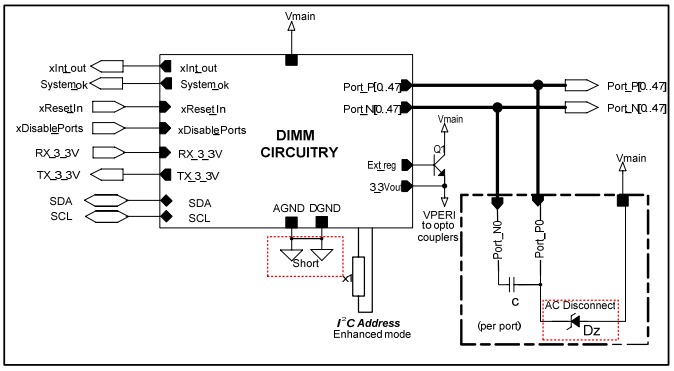

Figure 9: Overall PD671xxx DIMM at AC Disconnect Wiring Diagram

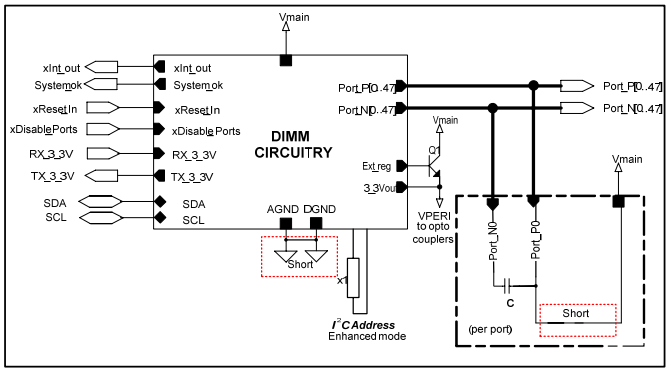

Figure 10: Overall PD671xxx DIMM at DC Disconnect Wiring Diagram

Power Dissipation

The PD671xxx power dissipation is concentrated within a few components distributed along the board as follows. These power dissipation calculations are based on a 24 port DIMM supplied by a 48 VDC power supply and located at ambient temperature of 70° C.

COMPONENT	DESCRIPTION	UNITS	POWER DISSIPATION [W]		
			IEEE802.3AF 0.35A/PORT	IEEE802.3AT 0.6A/PORT	IEEE802.3AT 0.65A/PORT
Rs	Senses resistor	24	1.43	4.21	4.94
Mosfet	PoE switching Mosfet	24	0.56	1.64	1.93
PD69012	PoE manager	2	1.15	1.15	1.15
PD69000	PoE controller	1 *	0.02	0.02	0.02
Total			3.16	7.02	8.04

* Enhanced mode Master board only

Important: When deploying an application utilizing the AC disconnect method, carefully select the diode type and diode location on the mother board. The diode should be located away from the DIMM to prevent mutual heating and the ventilation should be doubled to deal with higher power dissipation.

AC disconnect diodes power dissipation is based on 1 VDC forward voltage.

COMPONENT	DESCRIPTION	UNITS	POWER DISSIPATION [W]		
			IEEE802.3AF 0.35A/PORT	IEEE802.3AT 0.6A/PORT	IEEE802.3AT 0.65A/PORT
Diode	AC disconnect diode	24	8.4	14.4	15.6

Physical Information

Figure 11 shows the PD671xxx DIMM mechanical outline, which can be used in printed circuit layout design. PD671xxx DIMMs are designed to be mounted onto a 168-contact DIMM connector, capable of accepting JEDEC MO-161 modules. All units are in millimeters.

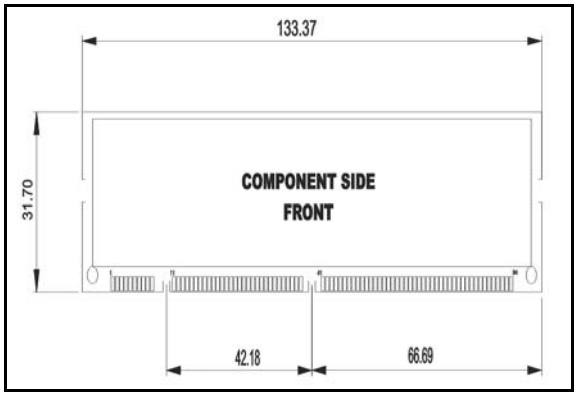

Figure 11: DIMM Dimensions

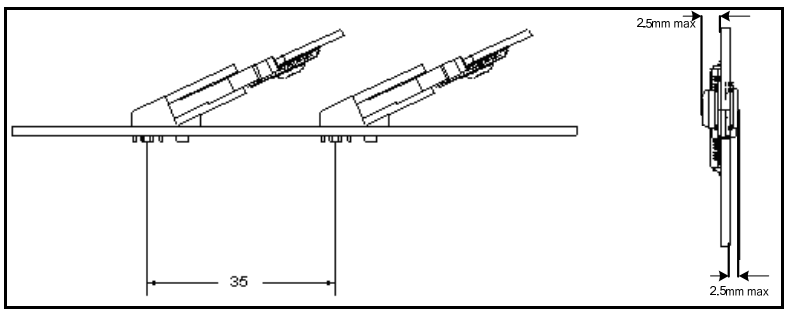

Figure 12: Mechanical Outline of the PD671xxx DIMM

Revision History

Revision Level / Date	Para. Affected	Description
0.1 / Oct. 1 , 2009		Initial release
0.2 / Oct. 29 , 2009	Overall doc	
1.0 / 17-March-10		Formal release

For support contact: sales_AMSG@microsemi.com

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Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А