Low Voltage 2.5V/3.3V Differential LVPECL/HSTL Fanout Buffer

8T33FS6111

DATA SHEET

General Description

The 8T33FS6111 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the 8T33FS6111 supports various applications that require distribution of precisely aligned differential clock signals. Using SiGe:C technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

The 8T33FS6111 is designed for low skew clock distribution systems and supports clock frequencies up to 2.7GHz. The device accepts two clock sources. The CLKA input can be driven by LVPECL compatible signals, the CLKB input accepts HSTL or LVPECL compatible signals. The selected input signal is distributed to 10 identical, LVPECL outputs. If V_{BB} is connected to the CLKA input and bypassed to GND by a 10nF capacitor, the 8T33FS6111 can be driven by single-ended LVPECL signals utilizing the V_{BB} bias voltage output.

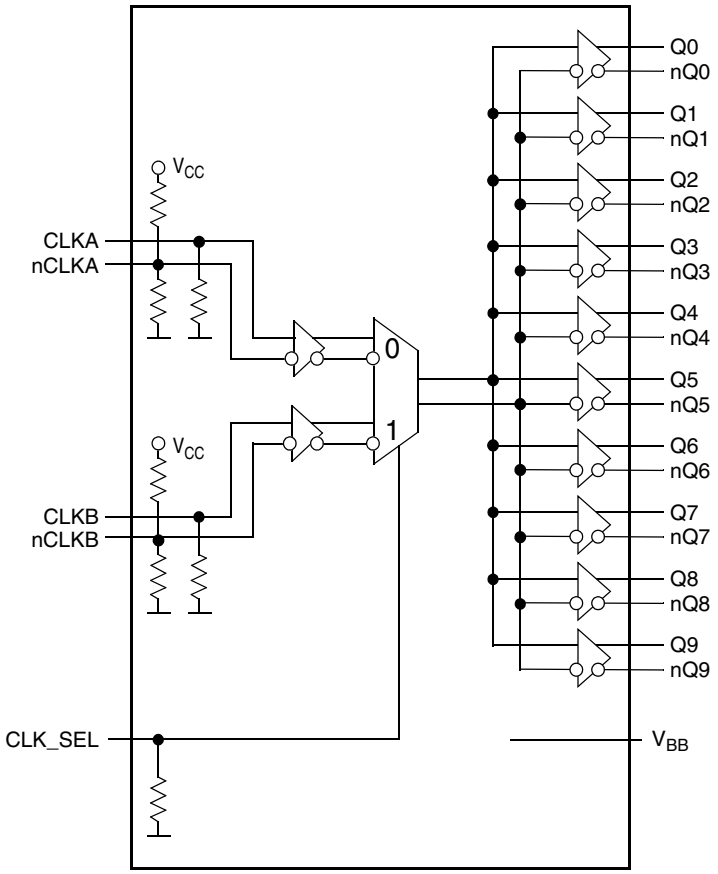
In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The 8T33FS6111 can be operated from a single 3.3V or 2.5V supply.

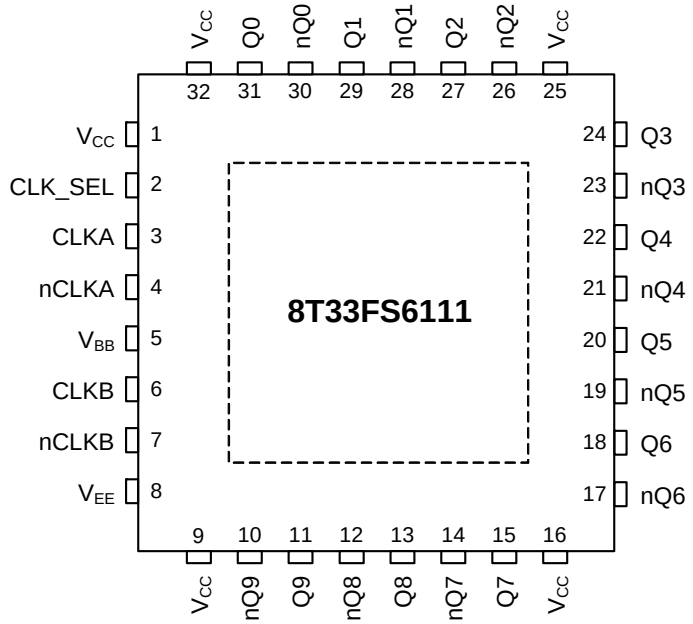
Features

- 1:10 differential clock distribution
- 28ps typical output skew
- Fully differential architecture from input to all outputs
- SiGe:C technology supports near-zero output skew
- Supports DC to 2.7GHz operation of clock or data signals
- LVPECL compatible differential clock outputs
- LVPECL/HSTL compatible differential clock inputs
- Single 3.3V or 2.5V supply
- Standard 32-Lead VFQFN package
- Standard 32-lead LQFP package
- Standard 32-lead TQFP package with EPAD
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



Pin Description and Characteristics

Table 1. Pin Description

Number	Name	Type		Description
1	V_{CC}	Power		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
2	CLK_SEL	Input		Active clock input select.
3	CLKA	Input	LVPECL	Differential reference clock signal input.
4	nCLKA	Input	LVPECL	Differential reference clock signal input.
5	V_{BB}	Output	DC	Reference voltage output for single ended LVPECL operation.
6	CLKB	Input	HSTL/LVPECL	Alternative differential reference clock signal input.
7	nCLKB	Input	HSTL/LVPECL	Alternative differential reference clock signal input.
8	V_{EE}	Power		Negative power supply.
9	V_{CC}	Power		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
10	nQ9	Output	LVPECL	Differential clock outputs.
11	Q9	Output	LVPECL	
12	nQ8	Output	LVPECL	Differential clock outputs.
13	Q8	Output	LVPECL	
14	nQ7	Output	LVPECL	Differential clock outputs.
15	Q7	Output	LVPECL	
16	V_{CC}	Power		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
17	nQ6	Output	LVPECL	Differential clock outputs.
18	Q6	Output	LVPECL	
19	nQ5	Output	LVPECL	Differential clock outputs.
20	Q5	Output	LVPECL	
21	nQ4	Output	LVPECL	Differential clock outputs.
22	Q4	Output	LVPECL	
23	nQ3	Output	LVPECL	Differential clock outputs.
24	Q3	Output	LVPECL	
25	V_{CC}	Power		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
26	nQ2	Output	LVPECL	Differential clock outputs.
27	Q2	Output	LVPECL	
28	nQ1	Output	LVPECL	Differential clock outputs.
29	Q1	Output	LVPECL	
30	nQ0	Output	LVPECL	Differential clock outputs.
31	Q0	Output	LVPECL	
32	V_{CC}	Power		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.

Table 2. Function Table

Control	Default	0	1
CLK_SEL	0	CLKA, nCLKA input pair is active. CLKA can be driven by LVPECL compatible signals.	CLKB, nCLKB input pair is active. CLKB can be driven by HSTL or LVPECL compatible signals.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{CC}	Supply Voltage		–0.3		3.6	V
V_{IN}	DC Input Voltage		–0.3		V_{CC} + 0.3	V
V_{OUT}	DC Output Voltage		–0.3		V_{CC} + 0.3	V
I_{IN}	DC Input Current				±20	mA
I_{OUT}	DC Output Current				±50	mA
T_S	Storage Temperature		–65		125	°C
T_J	Operating Junction Temperature				125	°C

Table 3. General Specifications

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
V_{TT}	Output Termination Voltage[1]			V_{CC} – 2		V
HBM	ESD Protection (Human Body Model)		4000			V
CDM	ESD Protection (Charged Device Model)		2000			V
LU	Latch-up Immunity		200			mA
C_{IN}	Input Capacitance	Inputs		2		pF

NOTE 1: Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase

DC Electrical Characteristics

Table 4. LVPECL/HSTL DC Characteristics, V_{CC} = 2.5V ± 5% or V_{CC} = 3.3V ± 5%, V_{EE} = GND, T_A = -40°C to +85°C

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
Control Input CLK_SEL						
V_{IL}	Input Voltage Low		V_{EE}		V_{CC} – 1.475	V
V_{IH}	Input Voltage High		V_{CC} – 1.165		V_{CC}	V
I_{IN}	Input Current	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			100	µA
Clock Input Pair CLKA, nCLKA (LVPECL differential signals)						
V_{PP}	Differential Input Voltage[1]	Differential operation	0.15		1.3	V
V_{CMR}	Differential Crosspoint Voltage[1,2]	Differential operation	1.0		V_{CC} – (V_{PP}/2)	V
I_{IN}	Input Current	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			150	µA
Clock Input Pair CLKB, nCLKB (HSTL/LVPECL differential signals)						
V_{DIF}	Differential Input Voltage[3]		0.4		1.0	V
V_X	Differential Crosspoint Voltage[3,4]		0.10	0.68 – 0.9	V_{CC} – 1.1	V
I_{IN}	Input Current	$V_{IN} = V_X$ ±0.2V			200	µA
LVPECL Clock Outputs (Q[0:9], nQ[0:9])						
V_{OH}	Output High Voltage	I_{OH} = –30mA[5]	V_{CC} – 1.3		V_{CC} – 0.7	V
V_{OL}	Output Low Voltage	I_{OL} = –5mA[5]	V_{CC} – 1.9		V_{CC} – 1.5	V
Supply Current and V_{BB}						
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current[6]	V_{EE} pin			100	mA
V_{BB}	Output Reference Voltage	I_{BB} = 200µA	V_{CC} – 1.4		V_{CC} – 1.2	V

NOTE 1: V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality. V_{IL} should not be less than -0.3V. V_{IH} should not be greater than V_{CC}.

NOTE 2: V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

NOTE 3: V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality. V_{IL} should not be less than -0.3V. V_{IH} should not be greater than V_{CC}.

NOTE 4: V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{DIF} (DC) specification.

NOTE 5: Equivalent to a termination of 50Ω to V_{TT}.

NOTE 6: I_{CC} calculation: I_{CC} = (number of differential output pairs used) x (I_{OH} + I_{OL}) + I_{EE}
I_{CC} = (number of differential output pairs used) x (V_{OH} – V_{TT})/R_{load} + (V_{OL} – V_{TT})/R_{load} + I_{EE}

AC Electrical Characteristics

Table 5. AC Characteristics, V_{CC} = 3.3V ±5% or V_{CC} = 2.5V ±5%, V_{EE} = GND, T_A = -40°C to +85°C[1]

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
Clock Input Pair CLKA, nCLKA (LVPECL differential signals)						
f_{CLK}	Input Frequency[2]	Differential			2.7	GHz
t_{PD}	Propagation Delay CLKA or CLKB to Q[0:9]	Differential	200	345	530	ps
Clock Input Pair CLKB, nCLKB (HSTL/LVPECL differential signals)						
f_{CLK}	Input Frequency	Differential			2.7	GHz
t_{PD}	Propagation Delay CLKB to Q[0:9]	Differential	200	375	530	ps
LVPECL Clock Outputs (Q[0:9], nQ[0:9])						
$V_{O(P-P)}$	Output Voltage (peak-to-peak) f_O < 300MHz f_O < 1.5GHz f_O < 2.7GHz		 0.45 0.30 0.18		 0.95 0.95 0.95	 V V V
$t_{sk(O)}$	Output-to-Output Skew	Differential		28	50	ps
$t_{sk(PP)}$	Part-to-Part Skew	Differential			250	ps
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	f_{CLK} = 156.25MHz, Integration Range: (12KHz - 20MHz)		74	100	fs
$t_{sk(P)}$	Output Pulse Skew[3]				75	ps
t_r, t_f	Output Rise/Fall Time	20% to 80%		110	300	ps

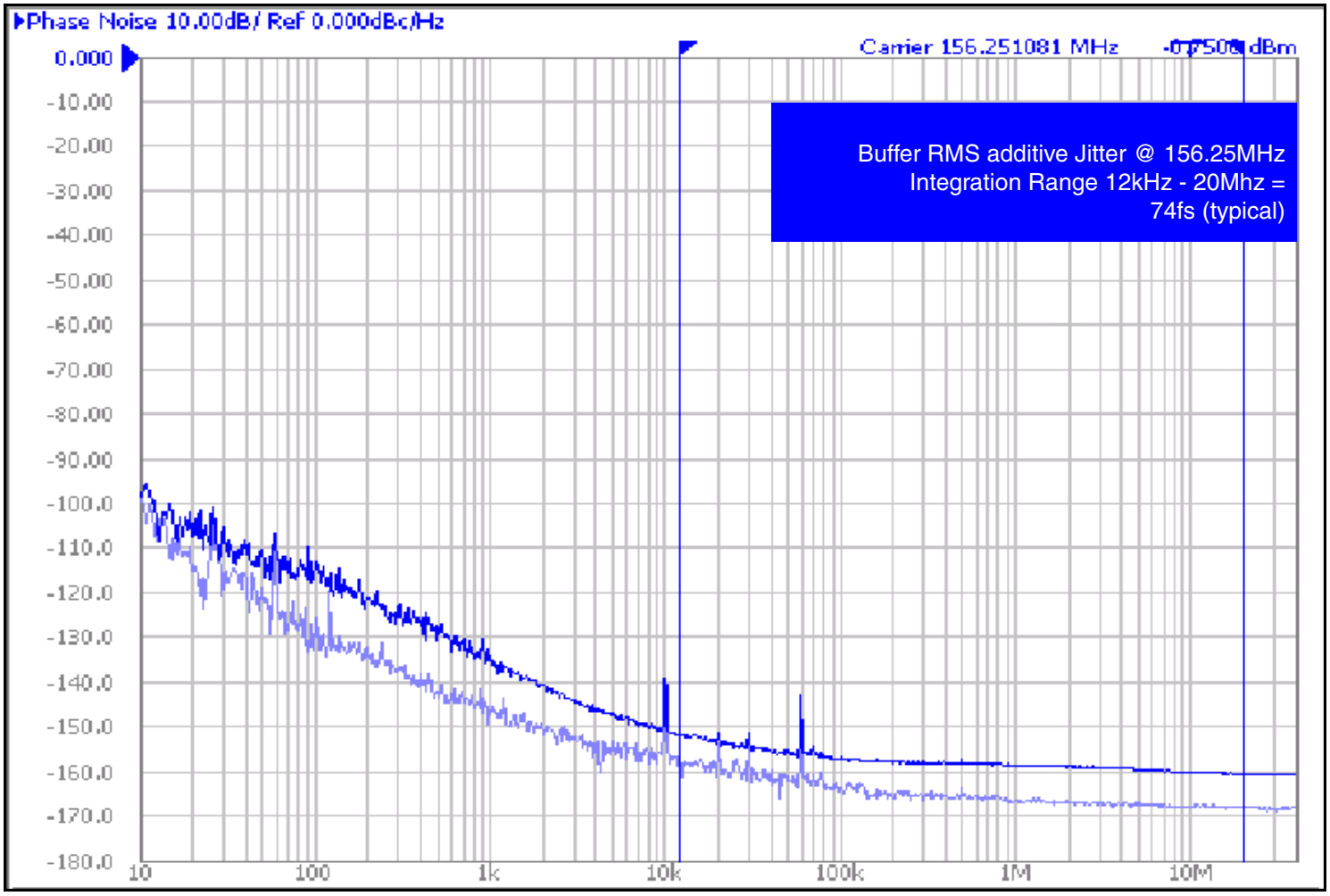
NOTE 1: AC characteristics apply for parallel output termination of 50Ω to V_{TT}.

NOTE 2: The 8T33FS6111I is fully operational up to 3.0GHz and is characterized up to 2.7GHz.

NOTE 3: Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

Additive Phase Jitter

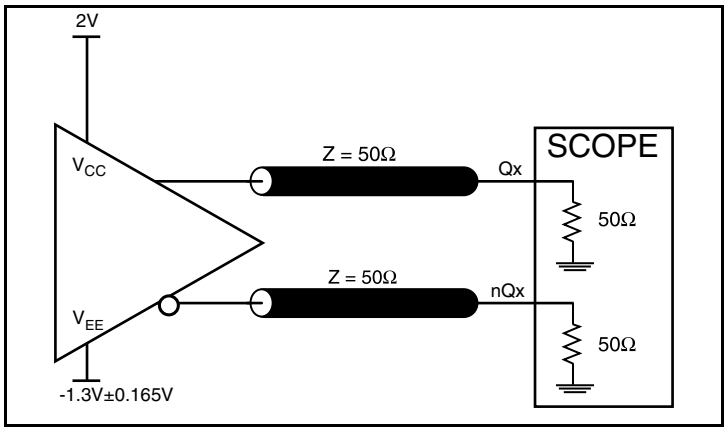
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase Noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



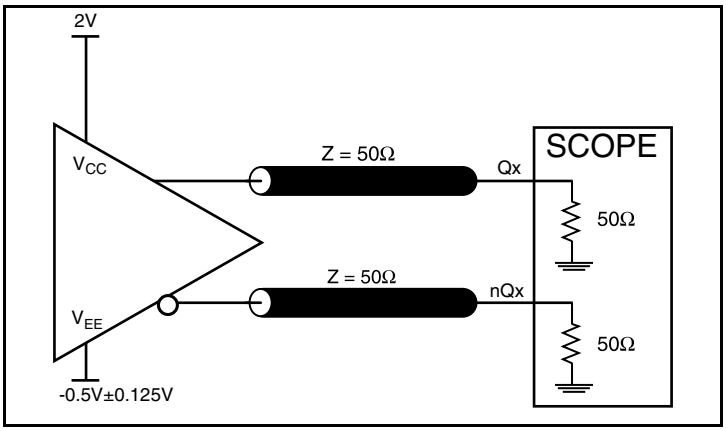
As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Wenzel 156.25MHz Oscillator as the input source.

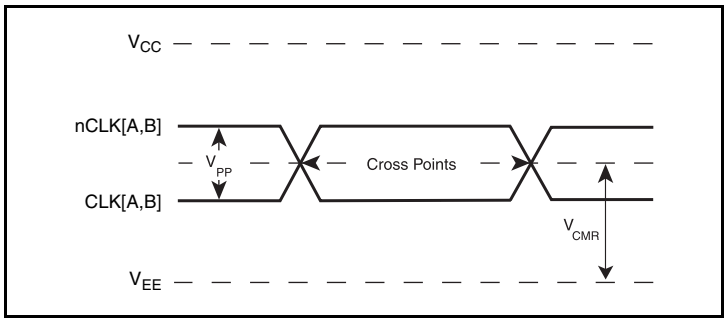
Parameter Measurement Information



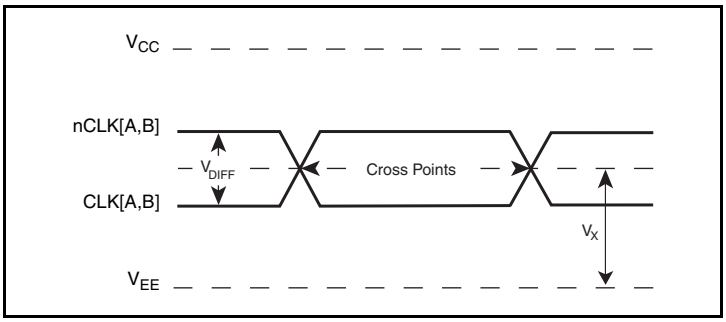
3.3V LVPECL Output Load AC Test Circuit



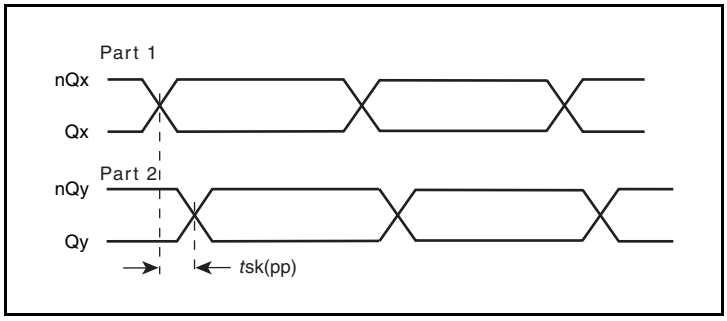
2.5V LVPECL Output Load AC Test Circuit



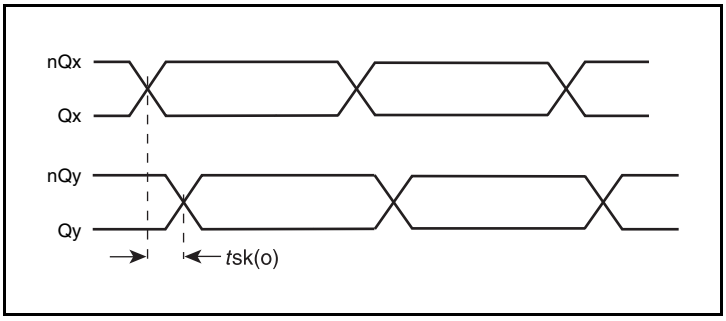
Differential Input Level



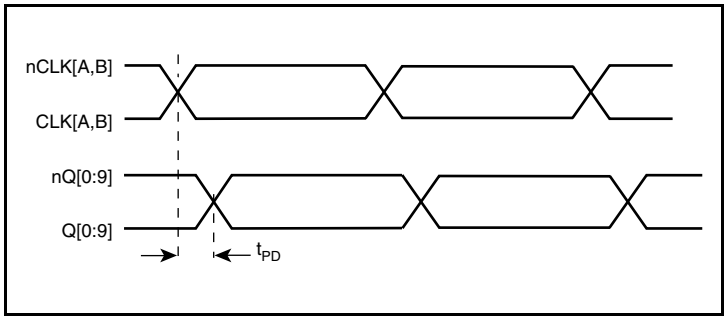
Differential Input Level



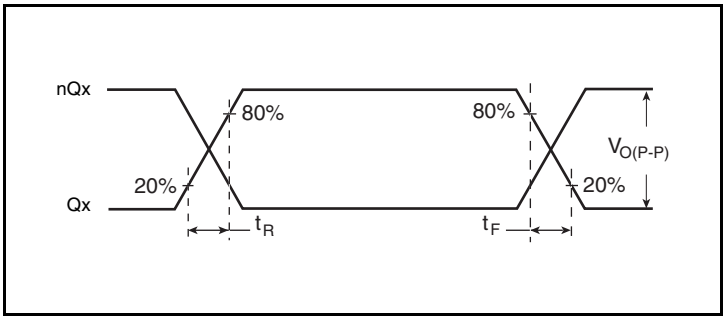
Part-to-Part Skew



Output Skew



Propagation Delay



Output Rise/Fall Time

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

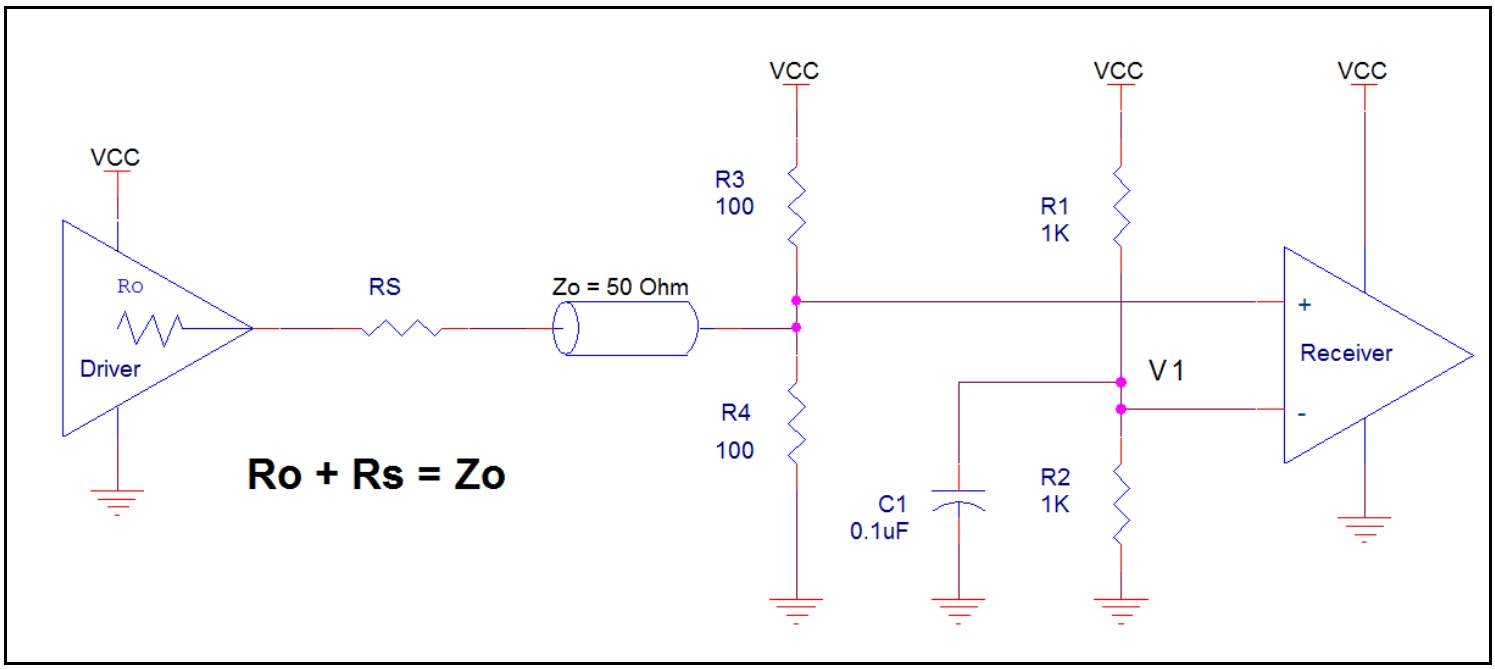


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Recommendations for Unused Input and Output Pins

Inputs:

CLKx/nCLKx Inputs

For applications not requiring the use of a differential input, both the CLKx and nCLKx pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground. For applications

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Maintaining Lowest Device Skew

The 8T33FS6111 guarantees low output-to-output bank skew of 50 ps and a part-to-part skew of max. 250ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The 8T33FS6111 is a mixed analog/digital product. The differential architecture of the 8T33FS6111 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

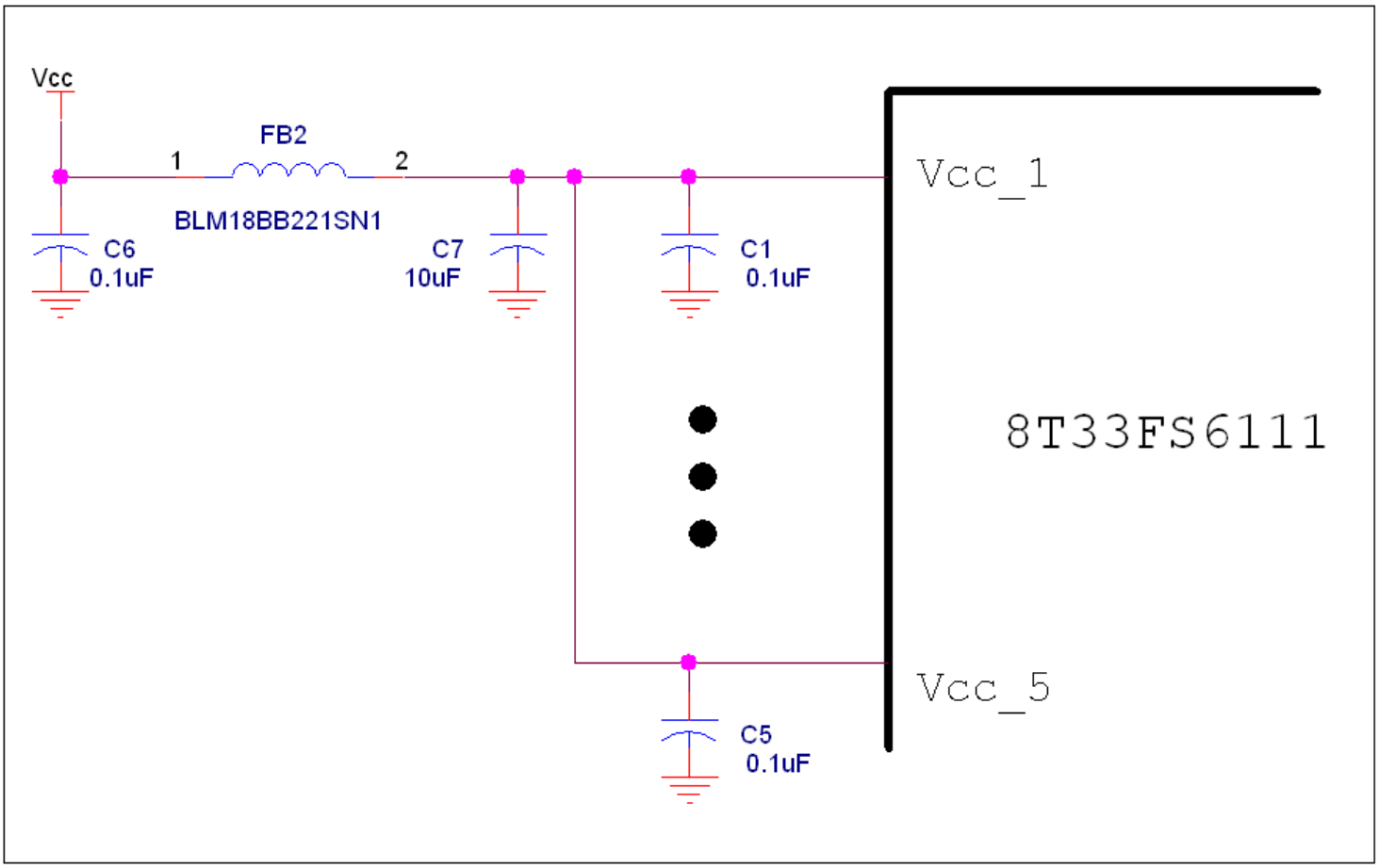


Figure 2. V_{CC} Power Supply Bypass

Use of VBB for single ended LVPECL Clocks

The VBB output pin often provided by LVPECL devices is designed to generate a temperature compensated logic threshold DC voltage for 3.3V LVPECL logic. This voltage is typically used when an upstream source, for whatever reason, has only one LVPECL output available. In this case the implied logic threshold voltage carried in the complementary LVPECL output of the driver is not available and must be generated at the receiver.

In the Application Example below, this option is used to provide functionality of a 1:2 fan out buffer passively. When AC coupling devices from different manufacturers the VBB voltage over temperature does not have to be checked against the logic threshold of the source driver to ensure that there is enough drive level above and below VBB for reliable switching.

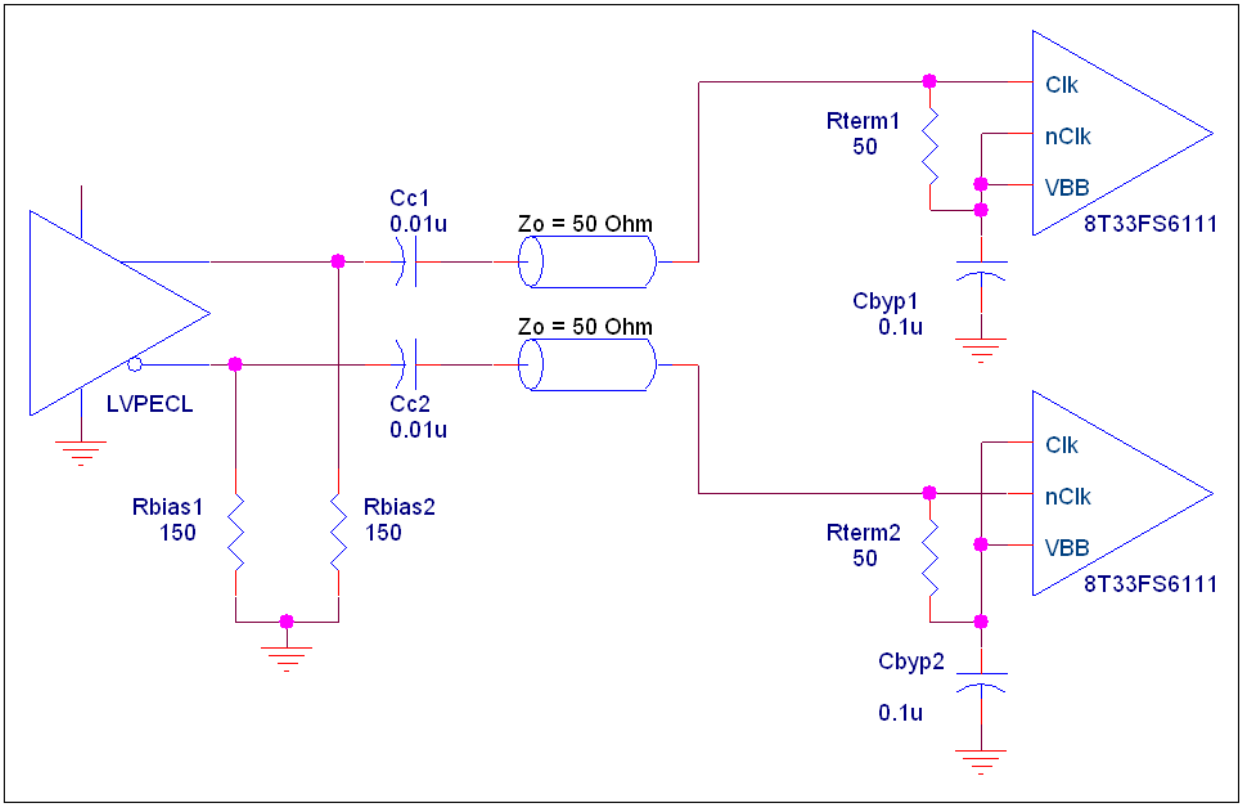


Figure 3. Application Example - Wiring Differential Inputs to Accept a Single Ended LVPECL Level

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Lead frame Base Package, Amkor Technology.

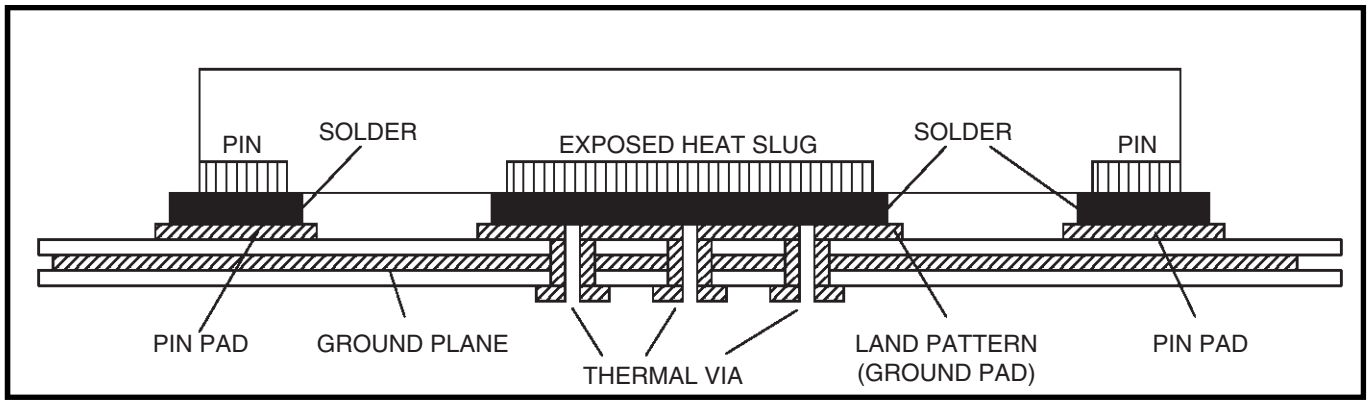


Figure 4. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

3.3V LVPECL Clock Input Interface

The CLK /nCLK accepts LVPECL, LVDS, CML and other differential signals. Both differential outputs must meet the V_{PP} and V_{CMR} input requirements. *Figure 5A* to *Figure 5E* show interface examples for the CLK/ nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

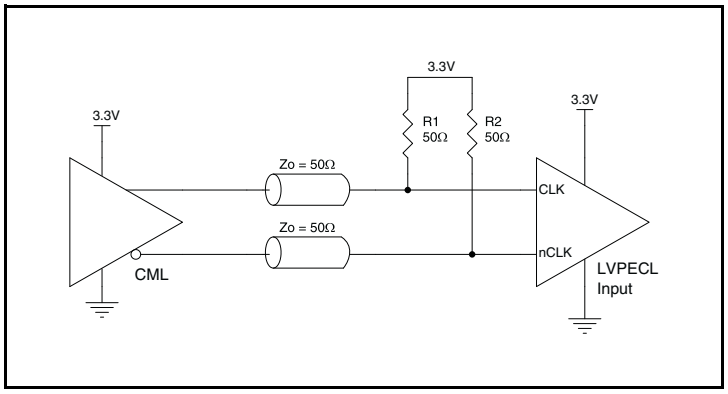


Figure 5A. CLK/nCLK Input Driven by a CML Driver

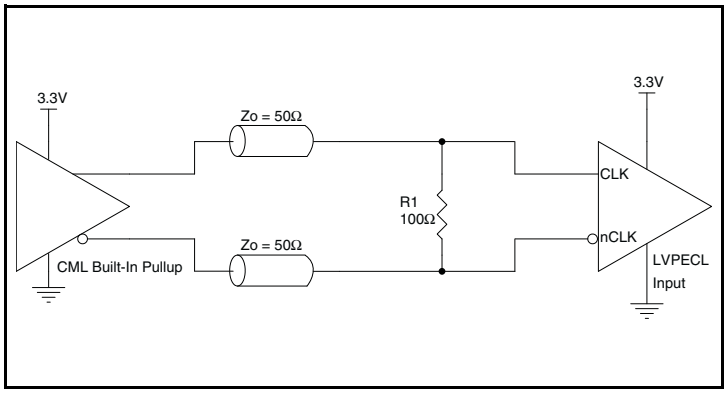


Figure 5B. CLK/nCLK Input Driven by a Built-In Pullup CML Driver

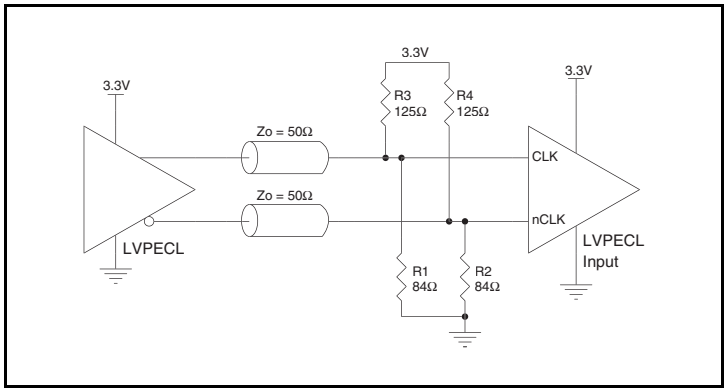


Figure 5C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

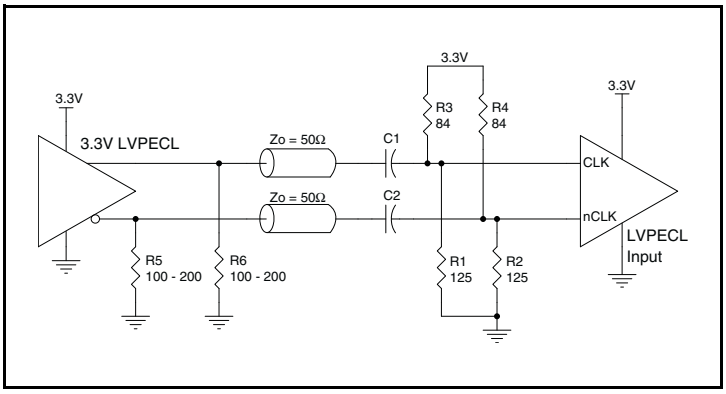


Figure 5D. CLK/nCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

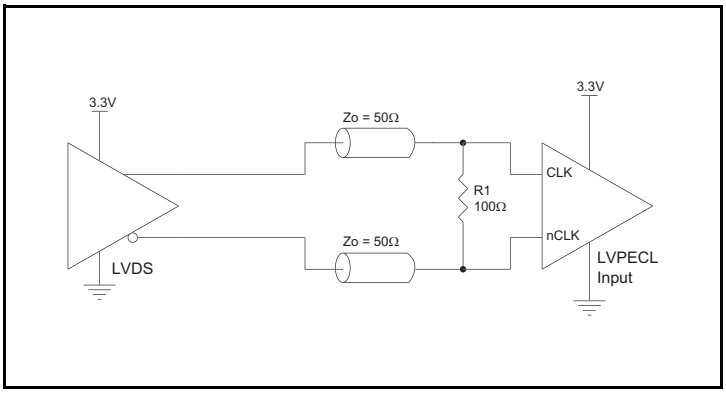


Figure 5E. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V LVPECL Clock Input Interface

The CLK /nCLK accepts LVPECL, LVDS, CML and other differential signals. Both differential outputs must meet the V_{PP} and V_{CMR} input requirements. *Figure 6A* to *Figure 6E* show interface examples for the CLK/ nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

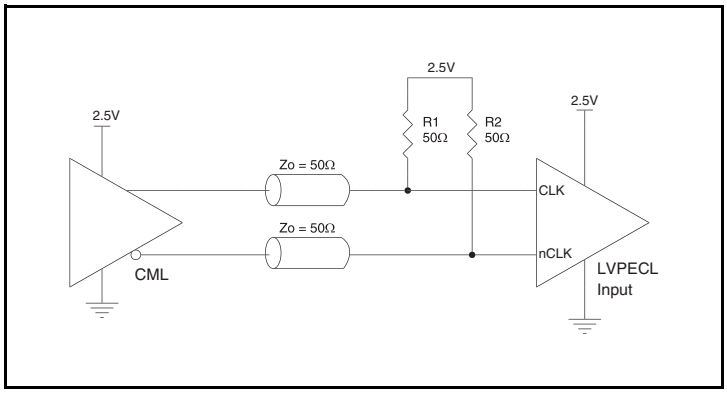


Figure 6A. CLK/nCLK Input Driven by a CML Driver

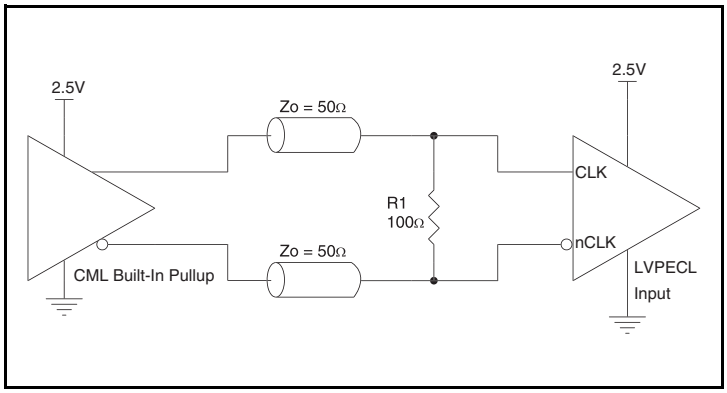


Figure 6B. CLK/nCLK Input Driven by a Built-In Pullup CML Driver

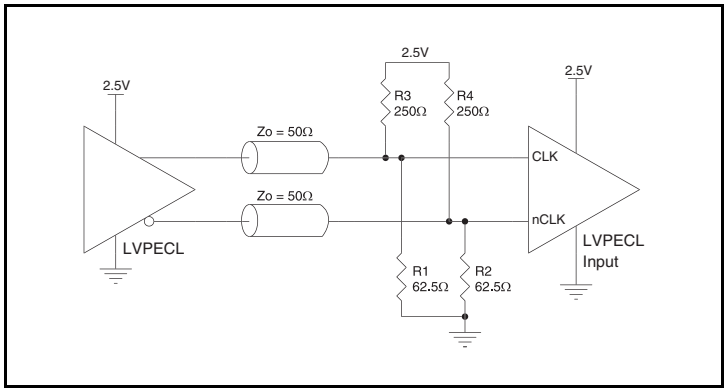


Figure 6C. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

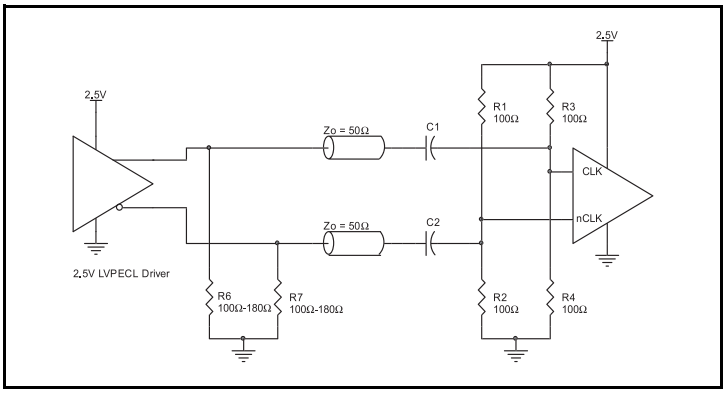


Figure 6D. CLK/nCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

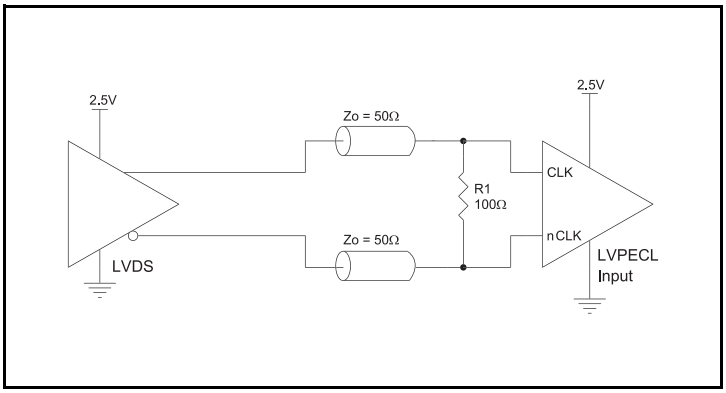


Figure 6E. CLK/nCLK Input Driven by a 2.5V LVDS Driver

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are a low impedance follower output that generate LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figure 7A* and *Figure 7B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

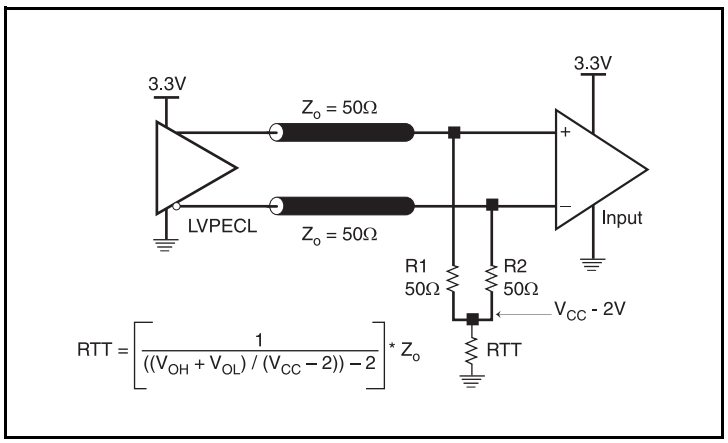


Figure 7A. 3.3V LVPECL Output Termination

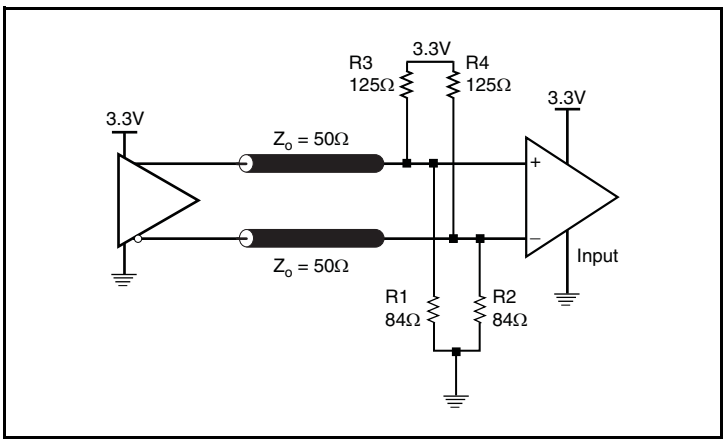


Figure 7B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 8A and *Figure 8B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in *Figure 8B* can be eliminated and the termination is shown in *Figure 8C*.

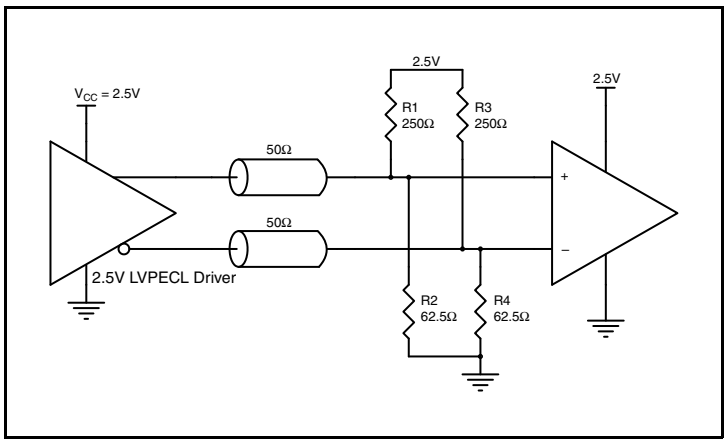


Figure 8A. 2.5V LVPECL Driver Termination Example

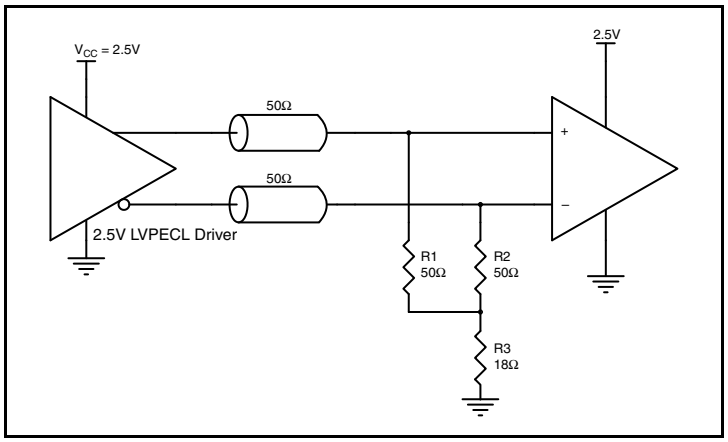


Figure 8B. 2.5V LVPECL Driver Termination Example

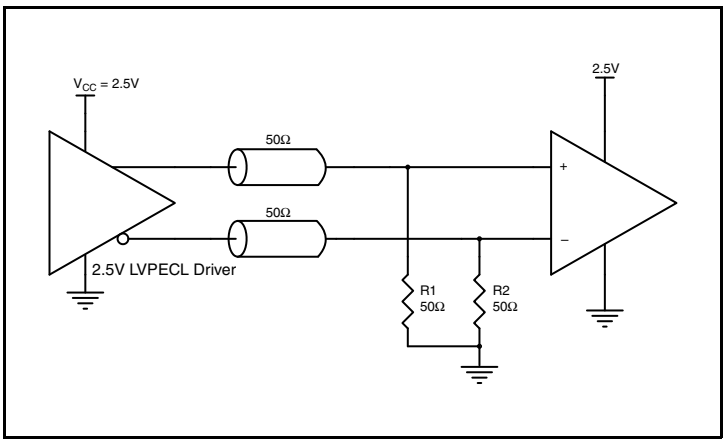


Figure 8C. 2.5V LVPECL Driver Termination Example

Power Considerations (TQFP with EPAD)

This section provides information on power dissipation and junction temperature for the 8T33FS6111.
Equations and example calculations are also provided.

1. Power Dissipation

The total power dissipation for the 8T33FS6111 is the sum of the core power plus the power dissipated due to output switching (load).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The maximum core current at 85°C is as follows:
I_{EE_MAX} = 100mA

Core

- Power(core) = V_{DD_MAX} * (I_{EE_MAX}) = 3.465V * 100mA = **346.5mW**

LVPECL Output

LVPECL driver power dissipation is 33.2mW/Loaded output pair, total power dissipation due to LVPECL outputs switching:

- Power $(outputs)_{MAX}$ = **33.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 10 * 33.2mW = **332mW**

Total Power Dissipation

- **Total Power**
  = Power (core) + Power(outputs)
  = 346.5mW + 332mW
  = 678.5mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 35.3°C/W for TQFP package (with ePAD) per *Table 6* below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.679W * 35.3°C/W = 108.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32-Lead TQFP, EPad

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	35.3	31.8	30.3

Power Considerations (LQFP)

The 8T33FS6111 device was designed and characterized to operate within the ambient industrial temperature range of -40°C to +85°C. The ambient temperature represents the temperature around the device, not the junction temperature. The LQFP package has no EPAD. When using the device in extreme cases, such as high ambient temperature, external air flow or using less number of outputs or lower supply voltage such as 2.5V may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature. The power calculation examples below were generated using a maximum ambient temperature and 2.5V supply voltage. Depending on the applications, the power consumption can be lower or higher. Please contact IDT technical support for any concerns on calculating the power dissipation for your own specific configuration.

This section provides information on power dissipation and junction temperature for the 8T33FS6111.
Equations and example calculations are also provided.

1. Power Dissipation

The total power dissipation for the 8T33FS6111 is the sum of the core power plus the power dissipated due to output switching (load).
The following is the power dissipation for V_{DD} = 2.5V +5% = 2.625V.

The maximum core current at 85°C is as follows:
I_{EE_MAX} = 95mA

Core

- Power(core) = V_{DD_MAX} * (I_{EE}) = 2.625V * 95mA = **249.4mW**

LVPECL Output
LVPECL driver power dissipation is 33.2mW/Loaded output pair, total power dissipation due to LVPECL outputs switching:

- Power $(outputs)_{MAX}$ = **33.2mW/Loaded Output pair**
  If eight outputs are loaded, the total power is 8 * 33.2mW = **265.6mW**

Total Power Dissipation

Total Power
= Power (core) + Power (outputs)
= 249.4mW + 265.6mW
= 515mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 76.1°C/W for LQFP package per *Table 7* below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.515W *76.1°C/W = 124.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32-Lead LQFP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	76.1	72.4	70.2

3A. Calculations and Equations for LVPECL.

The purpose of this section is to calculate power dissipation on the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 9.*

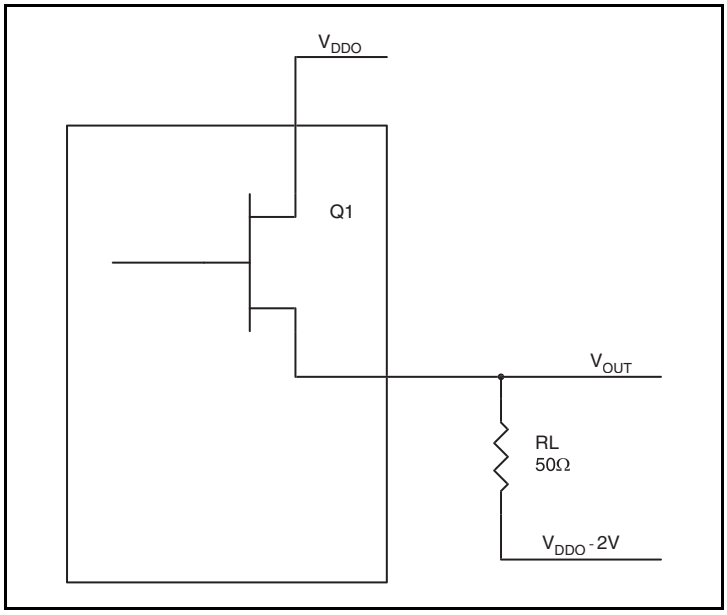


Figure 9. LVPECL Driver Circuit and Termination

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{DDO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{DDO_MAX} – 0.7V**
  ($V_{DD\_MAX} – V_{OH\_MAX}$) = **0.7V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{DDO_MAX} – 1.5V**
  ($V_{DD\_MAX} – V_{OL\_MAX}$) = **1.5V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{DDO\_MAX} – 2V))/R_L] * (V_{DDO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{DDO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{DDO\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.7V)/50Ω] * 0.7V =$ **18.2mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{DDO\_MAX} – 2V))/R_L] * (V_{DDO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{DDO\_MAX} – V_{OL\_MAX}))/R_{L]} * (V_{DDO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.5V)/50Ω] * 1.5V =$ **15mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **33.2mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32-Lead VFQFN, EPad

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	48.9	42.0	39.4

Table 9. θ_{JA} vs. Air Flow Table for a 32-Lead TQFP, EPad

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	35.3	31.8	30.3

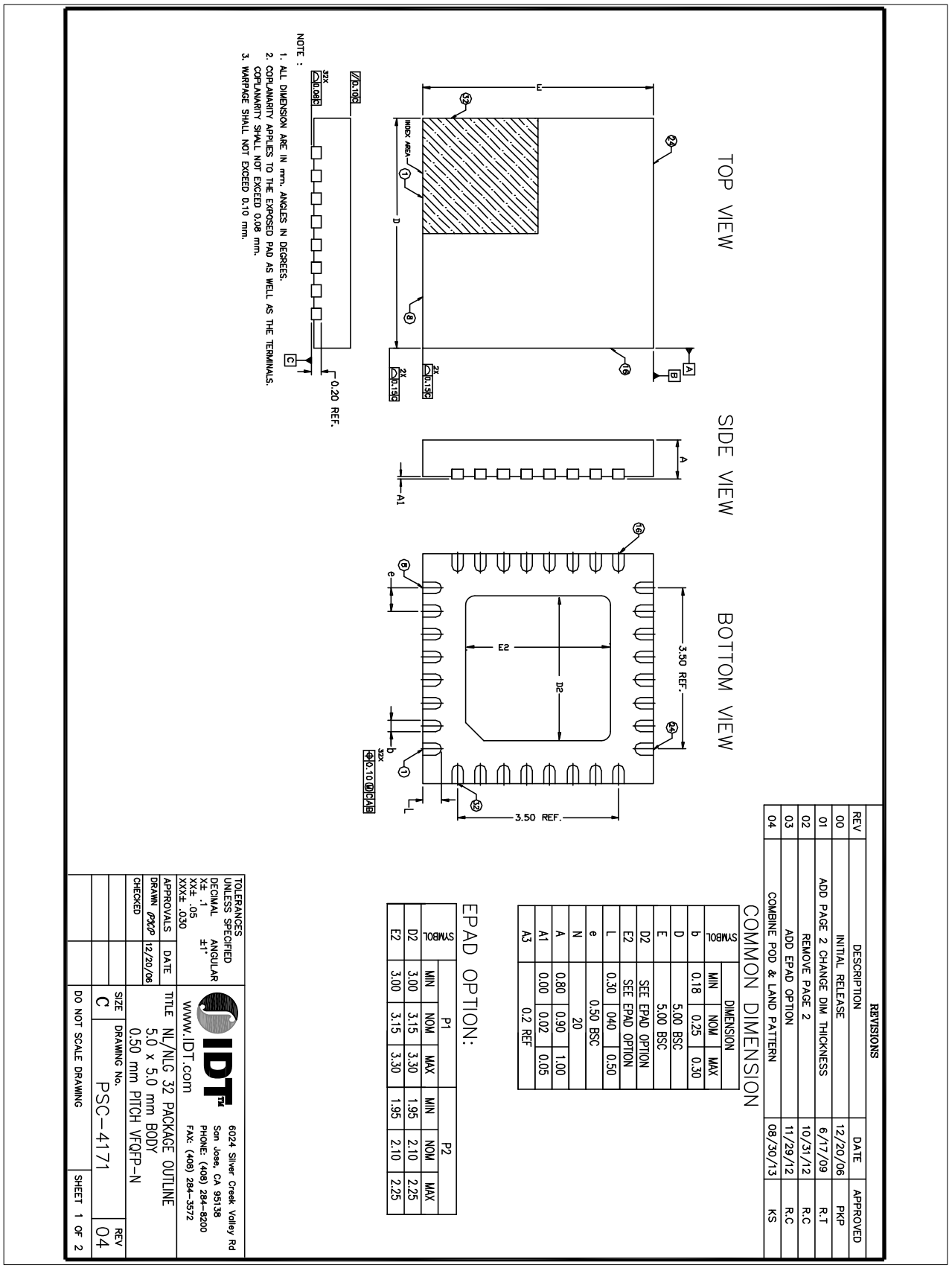
Table 10. θ_{JA} vs. Air Flow Table for a 32-Lead LQFP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	76.1	72.4	70.2

Transistor Count

The transistor count for 8T33FS6111 is: 989

Package Information, VFQFN with ePAD



REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	12/20/06	PKP
01	ADD PAGE 2 CHANGE DIM THICKNESS	6/17/09	R.T
02	REMOVE PAGE 2	10/31/12	R.C
03	ADD EPAD OPTION	11/29/12	R.C
04	COMBINE POD & LAND PATTERN	08/30/13	KS

COMMON DIMENSION

SYMBOL	DIMENSION		
	MIN	NOM	MAX
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
D2	SEE EPAD OPTION		
E2	SEE EPAD OPTION		
L	0.30	040	0.50
e		0.50 BSC	
N		20	
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	

EPAD OPTION:

SYMBOL	P1			P2		
	MIN	NOM	MAX	MIN	NOM	MAX
D2	3.00	3.15	3.30	1.95	2.10	2.25
E2	3.00	3.15	3.30	1.95	2.10	2.25

TOLERANCES
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X± .1 ±1°
XX± .05
XXX± .030

APPROVALS | DATE
DRAWN PKP | 12/20/06
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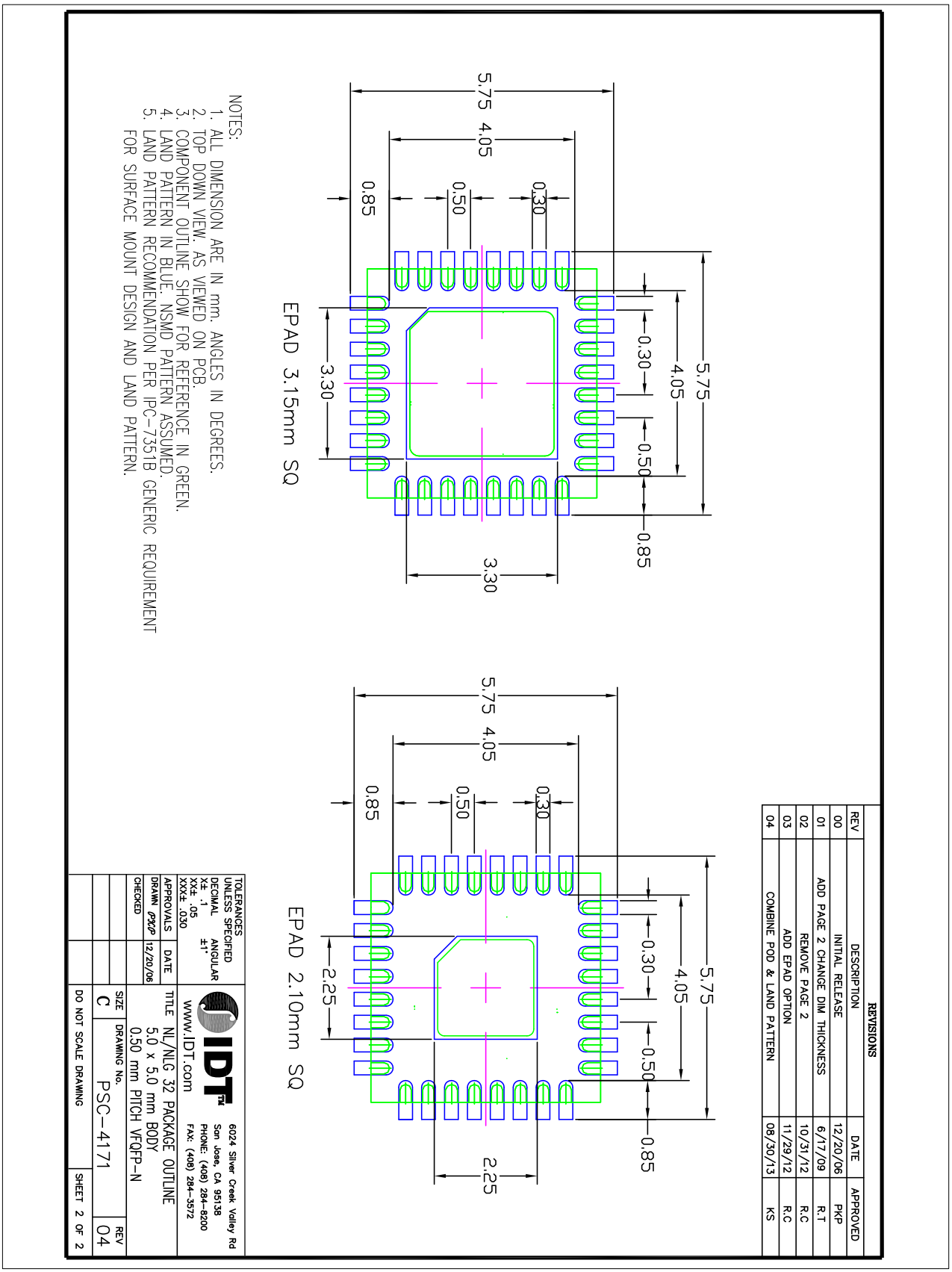
FAX: (408) 284-3572
www.IDT.com

TITLE NL/NLG 32 PACKAGE OUTLINE
5.0 x 5.0 mm BODY
0.50 mm PITCH VFQFP-N

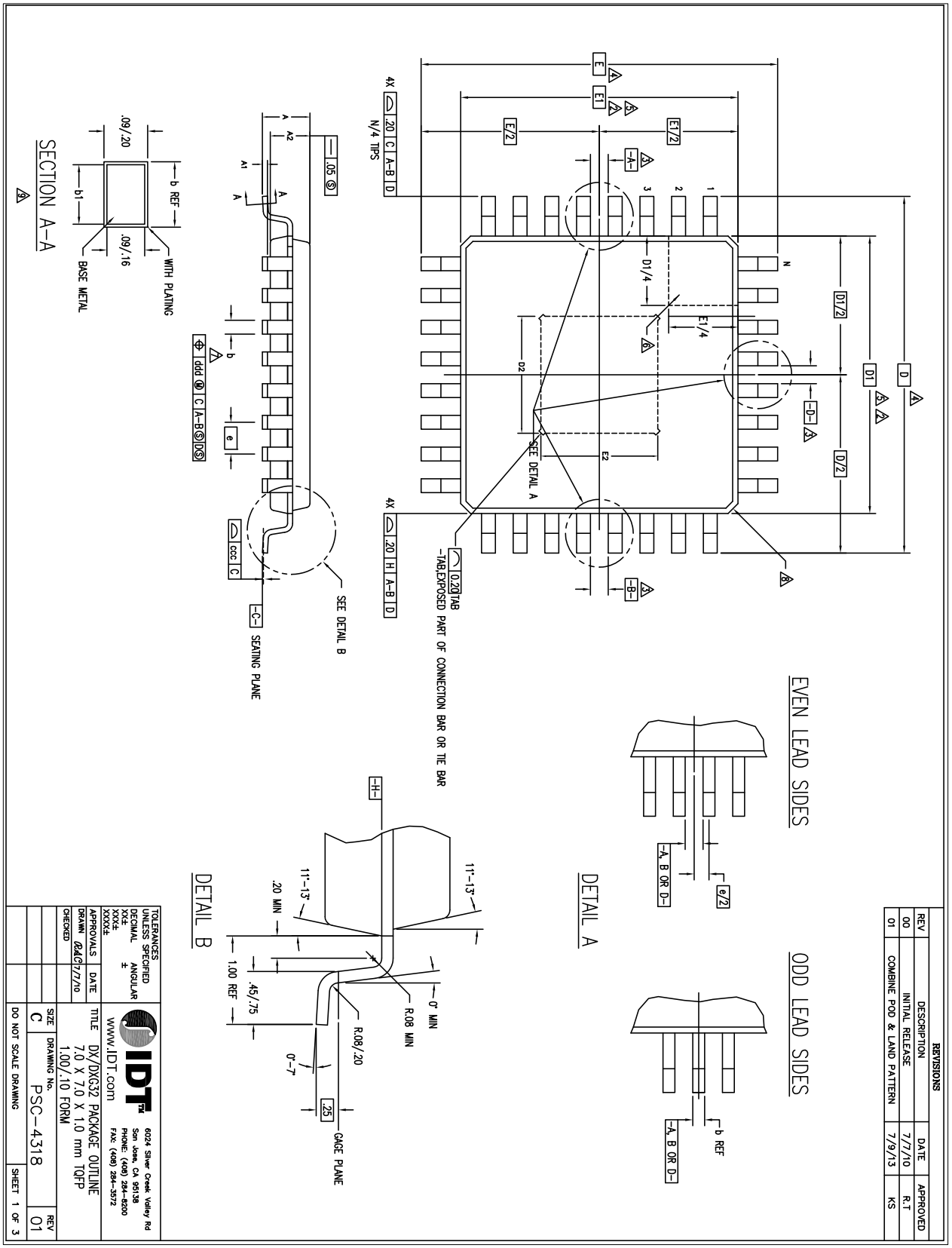
SIZE C | DRAWING No. PSC-4171 | REV 04

DO NOT SCALE DRAWING | SHEET 1 OF 2

Package Information, VFQFN with ePAD, continued



Package Information, TQFP with ePAD



Package Information, TQFP with ePAD, continued

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	7/7/10	R.T
01	COMBINE POD & LAND PATTERN	7/9/13	KS

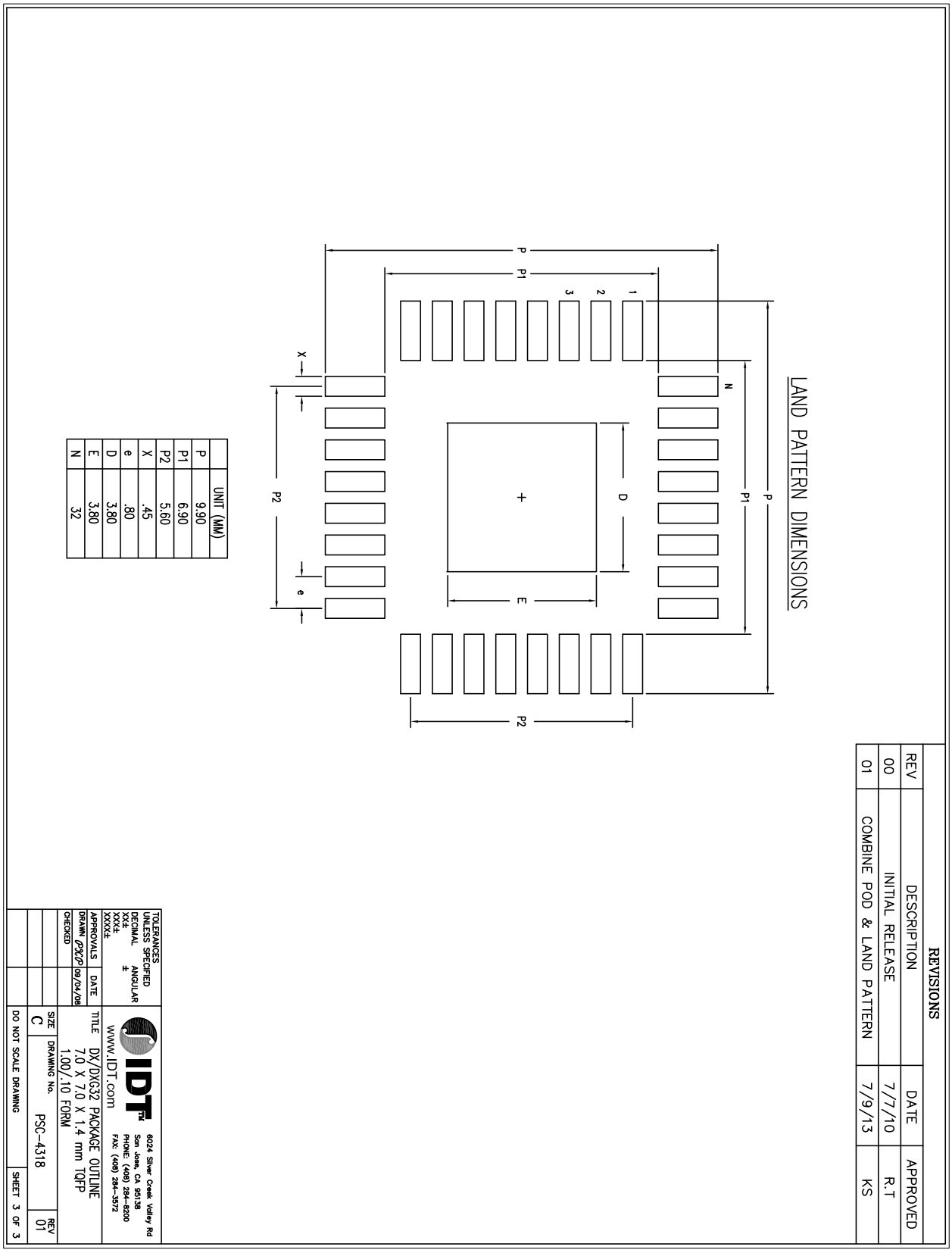
SYMBOL	JEDEC VARIATION BBC			NOTE
	MIN	NOM	MAX	
A	–	–	1.20	
A1	.05	.10	.15	
A2	0.95	1.00	1.05	
D	9.00 BSC			4
D1	7.00 BSC			5,2
E	9.00 BSC			4
E1	7.00 BSC			5,2
N	32			
e	.80 BSC			
E2	3.5			
D2	3.5			
b	.30	.37	.45	7
b1	.30	.35	.40	
ccc	–	–	.10	
ddd	–	–	.20	

NOTES:

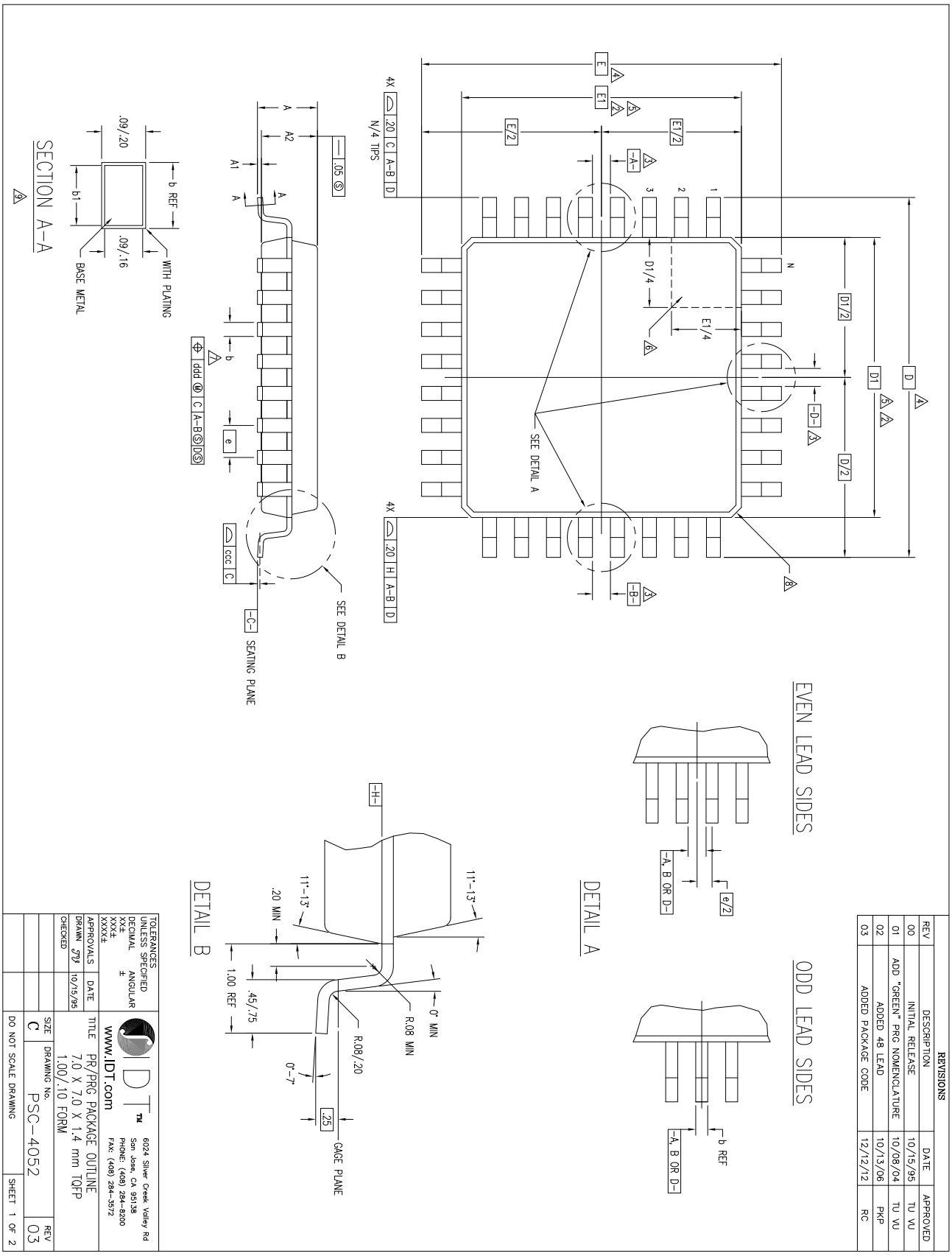
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS [A–B] AND [–D–] TO BE DETERMINED AT DATUM PLANE [–H–]
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [–C–]
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS–026, VARIATIONS BBA & BBC.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	IDT™ www.IDT.com 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 284–8200 FAX: (408) 284–3572
APPROVALS DATE DRAWN RAC 7/7/10 CHECKED	TITLE DX/DXG32 PACKAGE OUTLINE 7.0 X 7.0 X 1.0 mm TQFP 1.00/.10 FORM
	SIZE C · DRAWING No. PSC–4318 · REV 01
	DO NOT SCALE DRAWING · SHEET 2 OF 3

Package Information, TQFP with ePAD, continued



Package Information, LQFP



Package Information, LQFP, continued

PR/PRG32				
SYMBOL	JEDEC VARIATION BBA			NOTE
	MIN	NOM	MAX	
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	9.00 BSC			4
D1	7.00 BSC			5,2
E	9.00 BSC			4
E1	7.00 BSC			5,2
N	32			
e	.80 BSC			
b	.30	.37	.45	7
b1	.30	.35	.40	
ccc	–	–	.10	
ddd	–	–	.20	

PR/PRG48				
SYMBOL	JEDEC VARIATION BBC			NOTE
	MIN	NOM	MAX	
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	9.00 BSC			4
D1	7.00 BSC			5,2
E	9.00 BSC			4
E1	7.00 BSC			5,2
N	48			
e	.50 BSC			
b	.17	.22	.27	7
b1	.17	.20	.23	
ccc	–	–	.08	
ddd	–	–	.08	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE –C–

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

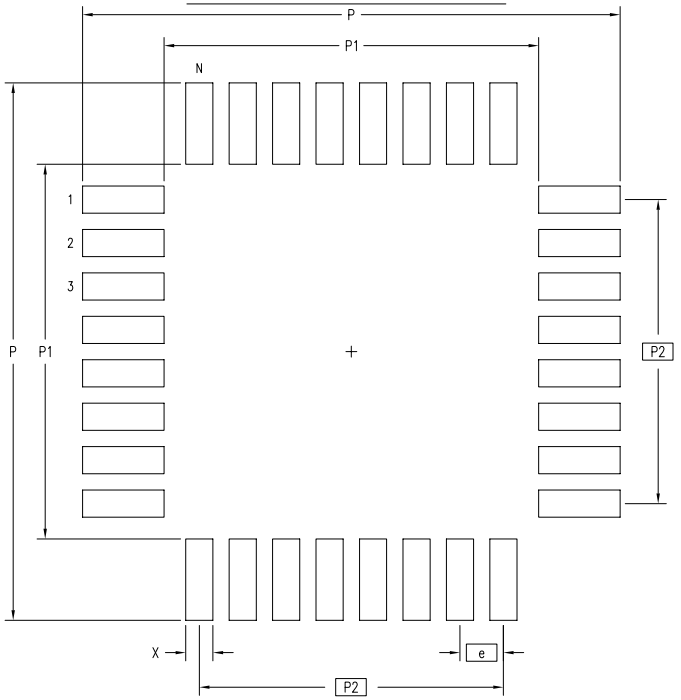
9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS–026, VARIATIONS BBA & BBC.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/15/95	TU VU
01	ADD "GREEN" PRG NOMENCLATURE	10/08/04	TU VU
02	ADDED 48 LEAD	10/13/06	PKP
03	ADDED PACKAGE CODE	12/12/12	RC

LAND PATTERN DIMENSIONS



	MIN	MAX
P	9.80	10.00
P1	6.80	7.00
P2	5.60 BSC	
X	.40	.60
e	.80 BSC	
N	32	

	MIN	MAX
P	9.80	10.00
P1	6.80	7.00
P2	5.50 BSC	
X	.25	.35
e	.50 BSC	
N	48	

TOLERANCES UNLESS SPECIFIED
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7.0 X 7.0 X 1.4 mm TQFP
1.00/.10 FORM

SIZE C | DRAWING No. PSC–4052 | REV 03

DO NOT SCALE DRAWING | SHEET 2 OF 2

Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T33FS6111NLGI	IDT8T33FS6111NLGI	32-Lead VFQFN (EPAD), Lead-Free	Tray	-40°C to 85°C
8T33FS6111NLGI8	IDT8T33FS6111NLGI	32-Lead VFQFN (EPAD), Lead-Free	Tape & Reel	-40°C to 85°C
8T33FS6111DXGI	IDT8T33FS6111DXGI	32-Lead TQFP (EPAD), Lead-Free	Tray	-40°C to 85°C
8T33FS6111DXGI8	IDT8T33FS6111DXGI	32-Lead TQFP (EPAD), Lead-Free	Tape & Reel	-40°C to 85°C
8T33FS6111PFGI	IDT8T33FS6111PFGI	32-Lead LQFP, Lead-Free	Tray	-40°C to 85°C
8T33FS6111PFGI8	IDT8T33FS6111PFGI	32-Lead LQFP, Lead-Free	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
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- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

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(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

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