

N-Channel Power MOSFET

800V, 6A, 0.95Ω

FEATURES

- Super-Junction technology
- High performance due to small figure-of-merit
- High ruggedness performance
- High commutation performance
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

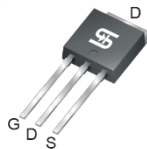
| KEY PERFORMANCE PARAMETERS | | |
|----------------------------|-------|------|
| PARAMETER | VALUE | UNIT |
| V_{DS} | 800 | V |
| $R_{DS(on)}$ (max) | 0.95 | Ω |
| Q_g | 19.6 | nC |

APPLICATION

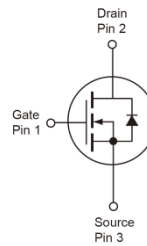
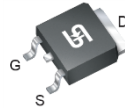
- Power Supply
- Lighting



TO-251 (IPAK)



TO-252 (DPAK)



Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

| ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted) | | | |
|---|----------------|---------------------------|------|
| PARAMETER | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | V_{DS} | 800 | V |
| Gate-Source Voltage | V_{GS} | ±30 | V |
| Continuous Drain Current ^(Note 1) | I_D | $T_C = 25^\circ\text{C}$ | 6 |
| | | $T_C = 100^\circ\text{C}$ | 3.8 |
| Pulsed Drain Current ^(Note 2) | I_{DM} | 18 | A |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$ | P_{DTOT} | 110 | W |
| Single Pulsed Avalanche Energy ^(Note 3) | E_{AS} | 121 | mJ |
| Single Pulsed Avalanche Current ^(Note 3) | I_{AS} | 2.2 | A |
| Operating Junction and Storage Temperature Range | T_J, T_{STG} | - 55 to +150 | °C |

| THERMAL PERFORMANCE | | | |
|--|-----------------|--------------|----------------------|
| PARAMETER | SYMBOL | LIMIT | UNIT |
| Junction to Case Thermal Resistance | $R_{\theta JC}$ | 1.14 | $^{\circ}\text{C/W}$ |
| Junction to Ambient Thermal Resistance | $R_{\theta JA}$ | 62 | $^{\circ}\text{C/W}$ |

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

| ELECTRICAL SPECIFICATIONS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted) | | | | | | |
|---|---|---------------|------------|------------|------------|---------------|
| PARAMETER | CONDITIONS | SYMBOL | MIN | TYP | MAX | UNIT |
| Static (Note 4) | | | | | | |
| Drain-Source Breakdown Voltage | $V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$ | BV_{DSS} | 800 | -- | -- | V |
| Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250\mu\text{A}$ | $V_{GS(TH)}$ | 2 | -- | 4 | V |
| Gate Body Leakage | $V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$ | I_{GSS} | -- | -- | ± 100 | nA |
| Zero Gate Voltage Drain Current | $V_{DS} = 800\text{V}, V_{GS} = 0\text{V}$ | I_{DSS} | -- | -- | 1 | μA |
| Drain-Source On-State Resistance | $V_{GS} = 10\text{V}, I_D = 3\text{A}$ | $R_{DS(on)}$ | -- | 0.8 | 0.95 | Ω |
| Dynamic (Note 5) | | | | | | |
| Total Gate Charge | $V_{DS} = 380\text{V}, I_D = 6\text{A},$ $V_{GS} = 10\text{V}$ | Q_g | -- | 19.6 | -- | nC |
| Gate-Source Charge | | Q_{gs} | -- | 3.5 | -- | |
| Gate-Drain Charge | | Q_{gd} | -- | 9.7 | -- | |
| Input Capacitance | $V_{DS} = 100\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$ | C_{iss} | -- | 691 | -- | pF |
| Output Capacitance | | C_{oss} | -- | 63 | -- | |
| Gate Resistance | $F = 1\text{MHz}, \text{open drain}$ | R_g | -- | 3.4 | -- | Ω |
| Switching (Note 6) | | | | | | |
| Turn-On Delay Time | $V_{DD} = 380\text{V},$ $R_{GEN} = 25\Omega,$ $I_D = 6\text{A}, V_{GS} = 10\text{V},$ | $t_{d(on)}$ | -- | 23 | -- | ns |
| Turn-On Rise Time | | t_r | -- | 12 | -- | |
| Turn-Off Delay Time | | $t_{d(off)}$ | -- | 57 | -- | |
| Turn-Off Fall Time | | t_f | -- | 11 | -- | |
| Source-Drain Diode (Note 4) | | | | | | |
| Forward On Voltage | $I_S = 6\text{A}, V_{GS} = 0\text{V}$ | V_{SD} | -- | -- | 1.4 | V |
| Reverse Recovery Time | $V_R = 100\text{V}, I_S = 6\text{A}$ $di_F/dt = 100\text{A}/\mu\text{s}$ | t_{rr} | -- | 249 | -- | ns |
| Reverse Recovery Charge | | Q_{rr} | -- | 2.6 | -- | μC |

Notes:

- Current limited by package.
- Pulse width limited by the maximum junction temperature.
- $L = 50\text{mH}, I_{AS} = 2.2\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega,$ Starting $T_J = 25^{\circ}\text{C}$
- Pulse test: $PW \leq 300\mu\text{s}, \text{duty cycle} \leq 2\%$.
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

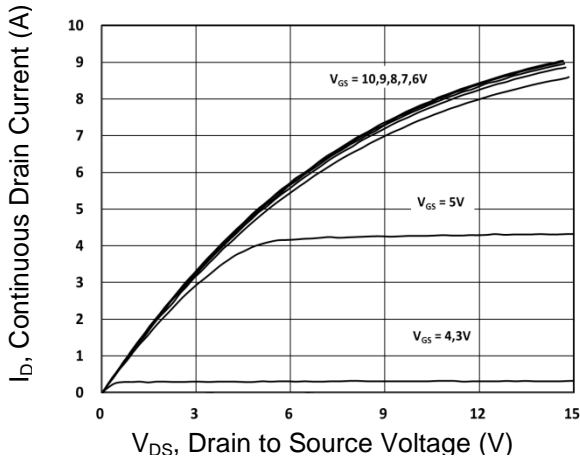
ORDERING INFORMATION

| PART NO. | PACKAGE | PACKING |
|-----------------|----------------|---------------------|
| TSM80N950CH C5G | TO-251 (IPAK) | 75pcs / Tube |
| TSM80N950CP ROG | TO-252 (DPAK) | 2,500pcs / 13" Reel |

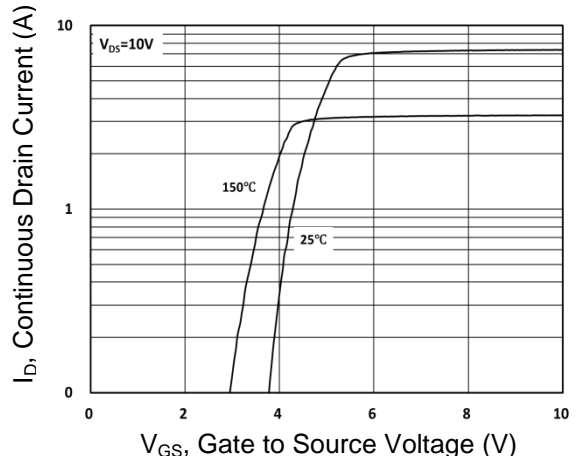
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

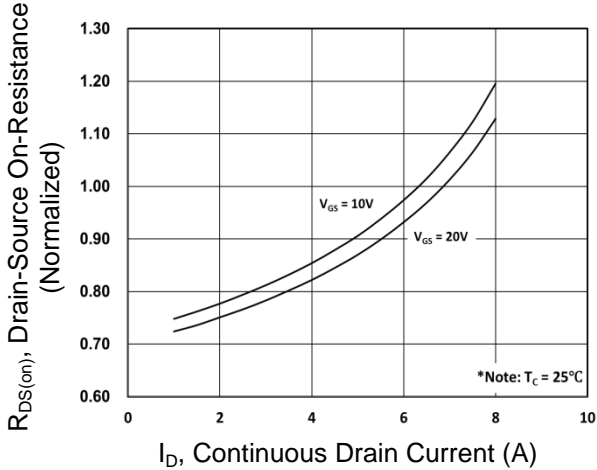
Output Characteristics



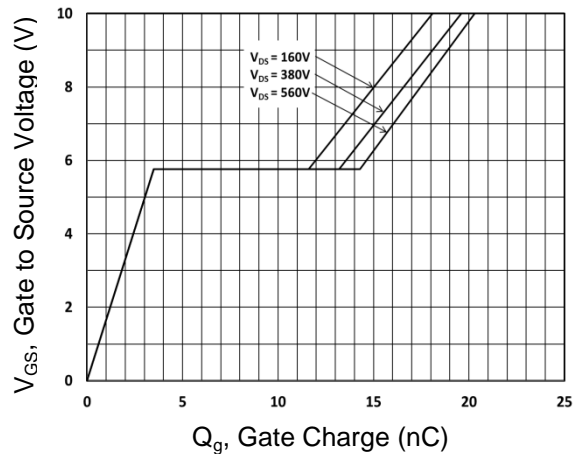
Transfer Characteristics



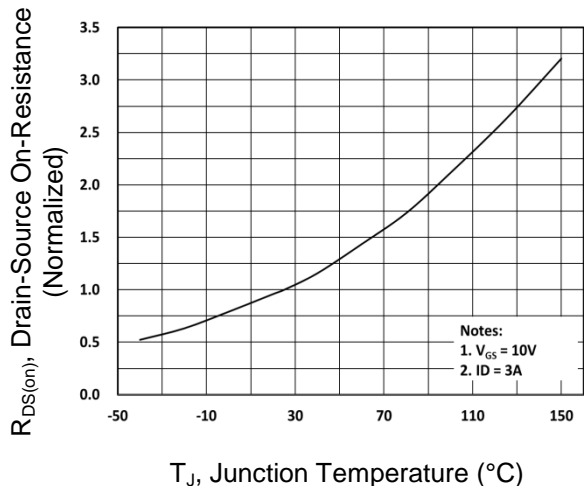
On-Resistance vs. Drain Current



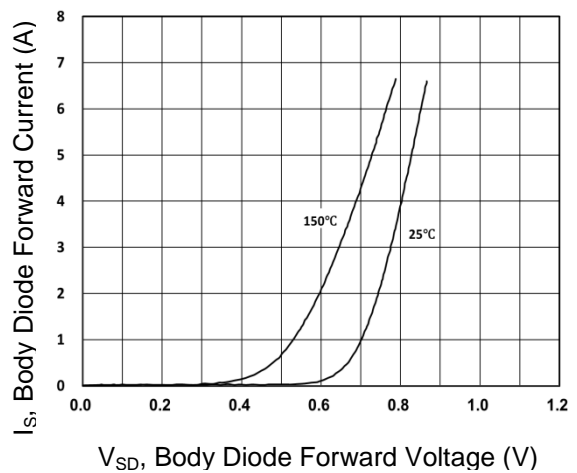
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



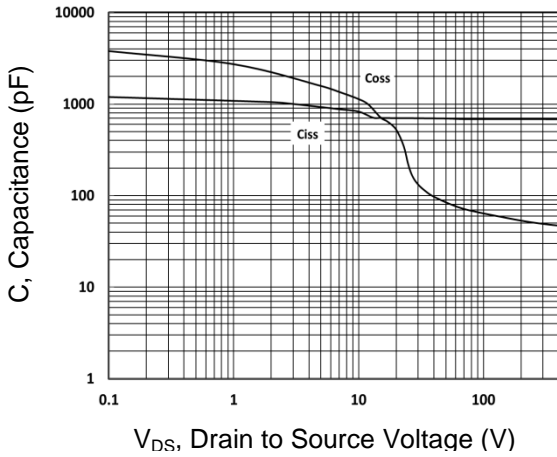
Source-Drain Diode Forward Current vs. Voltage



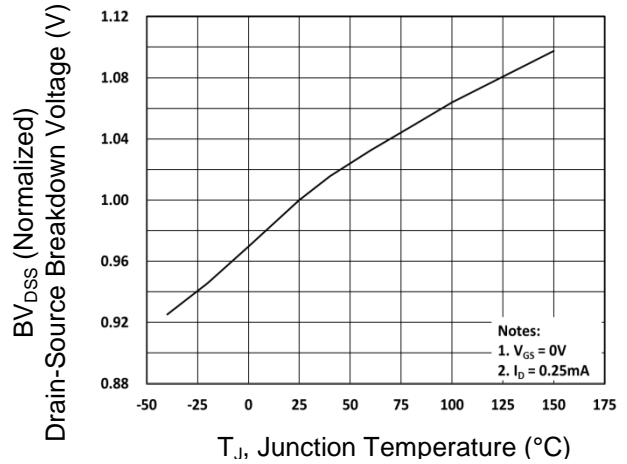
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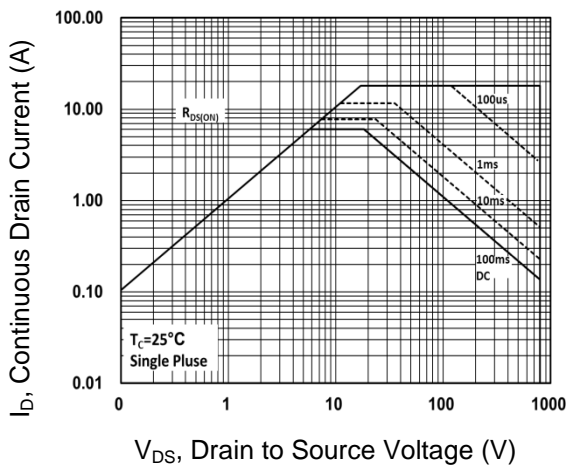
Capacitance vs. Drain-Source Voltage



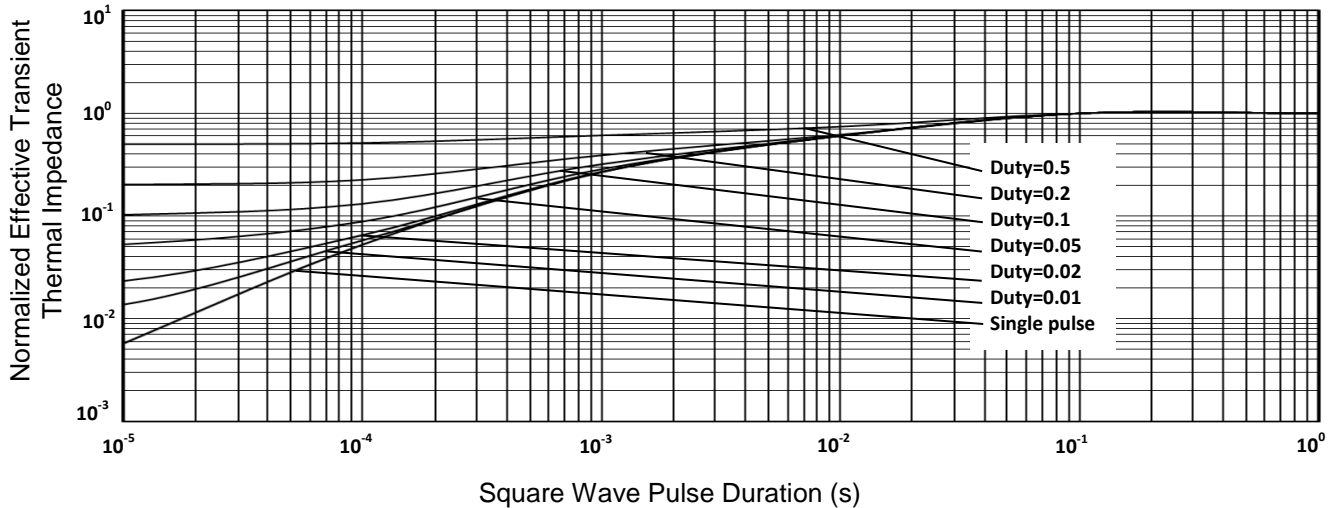
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area

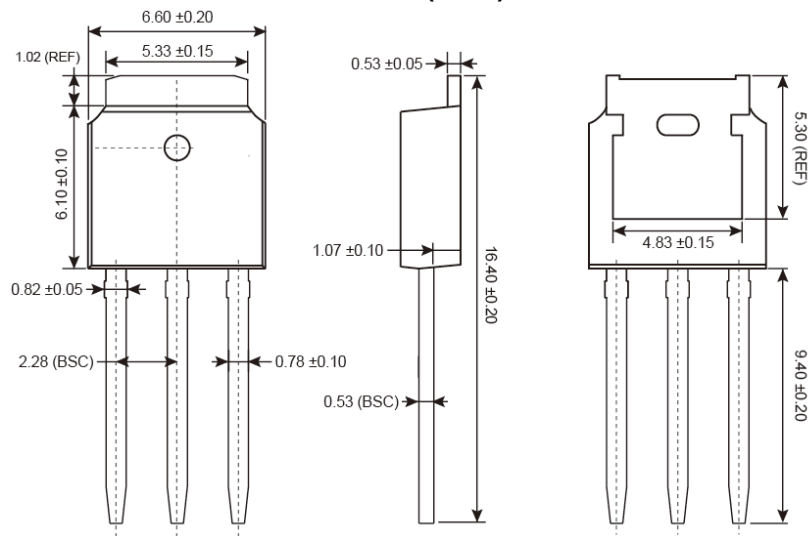


Normalized Thermal Transient Impedance, Junction-to-Case

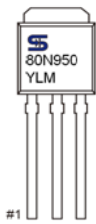


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251 (IPAK)



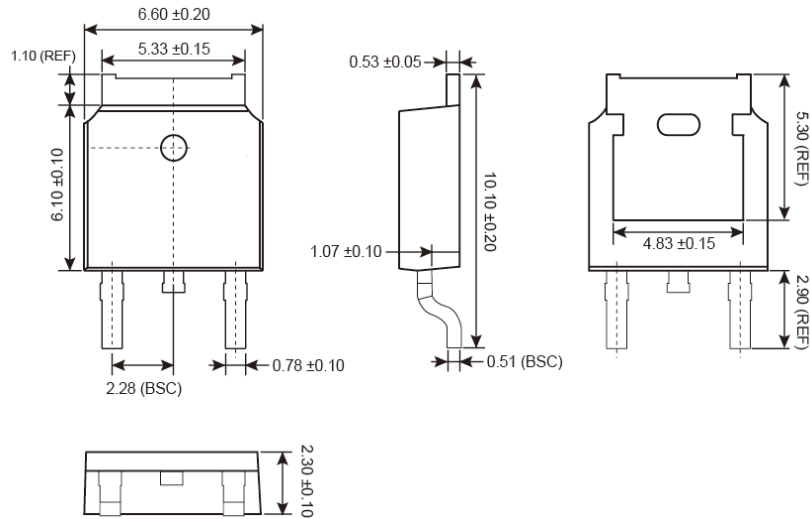
MARKING DIAGRAM



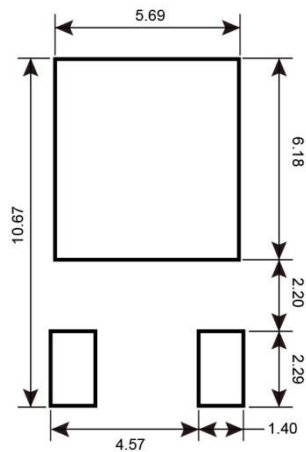
- Y** = Year Code
- M** = Month Code for Halogen Free Product
 - O** =Jan **P** =Feb **Q** =Mar **R** =Apr
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PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

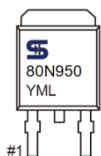
TO-252 (DPAK)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



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