Memory for Plug & Play

DDR/DDR2
(For memory module) SPD Memory

BR34E02FVT-W,BR34E02NUX-W

No.09002EBT03

●Description

BR34E02FVT-W is 256×8 bit Electrically Erasable PROM (Based on Serial Presence Detect)

●Features

1) 256×8 bit architecture serial EEPROM
2) Wide operating voltage range: 1.7V-3.6V
3) Two-wire serial interface
4) High reliability connection using Au pads and Au wires
5) Self-Timed Erase and Write Cycle
6) Page Write Function (16byte)
7) Write Protect Mode
   Settable Reversible Write Protect Function: 00h-7Fh
   Write Protect 1 (Onetime Rom) : 00h-7Fh
   Write Protect 2 (Hardwire WP PIN) : 00h-FFh
8) Low Power consumption
   Write (at 1.7V) : 0.4mA (typ.)
   Read (at 1.7V) : 0.1mA(typ.)
   Standby (at 1.7V) : 0.1μA(typ.)
9) DATA security
   Write protect feature (WP pin)
   Inhibit to WRITE at low Vcc
10) Compact package: TSSOP-B8, VSON008X2030
11) High reliability fine pattern CMOS technology
12) Rewriting possible up to 1,000,000 times
13) Data retention: 40 years
14) Noise reduction Filtered inputs in SCL / SDA
15) Initial data FFh at all addresses

●BR34E02-W Series

Capacity	Bit format	Type	Power Source Voltage	TSSOP-B8	VSON008X2030
2Kbit	256X8	BR34E02-W	1.7V～3.6V	●	●

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.3～+6.5	V
Power Dissipation	Pd	330(BR34E02FVT-W) *1	mW
		300(BR34E02NUX-W) *2	
Storage Temperature	Tstg	-65～+125	℃
Operating Temperature	Topr	-40～+85	℃
Terminal Voltage (A0)	-	-0.3～10.0	V
Terminal Voltage (etcetera)	-	-0.3～Vcc+0.3	V

* Reduce by 3.3mW(*1), 3.0 mW(*2)/°C over 25°C

●Recommended operating conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	1.7～3.6	V
Input Voltage	VIN	0～Vcc	V

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●Memory cell characteristics(Ta=25℃, Vcc=1.7V～3.6V)

Parameter	Specification			Unit
	Min.	Typ.	Max.	
Write / Erase Cycle *1	1,000,000	-	-	Cycles
Data Retention *1	40	-	-	Years

*1:Not 100% TESTED

●Electrical characteristics - DC(Unless otherwise specified Ta=-40℃～+85℃, Vcc=1.7V～3.6V)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max.		
"H" Input Voltage	VIH1	0.7 Vcc	-	Vcc+0.3	V	
"L" Input Voltage	VIL1	-	-	0.3 Vcc	V	
"L" Output Voltage 1	VOL1	-0.3	-	0.4	V	IOL=2.1mA, 2.5V≦Vcc≦3.6V(SDA)
"L" Output Voltage 2	VOL2	-	-	0.2	V	IOL=0.7mA, 1.7V≦Vcc＜2.5V(SDA)
Input Leakage Current 1	ILI1	-1	-	1	μA	VIN=0V～Vcc(A0,A1,A2,SCL)
Input Leakage Current 2	ILI2	-1	-	15	μA	VIN=0V～Vcc(WP)
Input Leakage Current 3	ILI3	-1	-	20	μA	VIN=VHV(A0)
Output Leakage Current	ILO	-1	-	1	μA	VOUT=0V～Vcc
Operating Current	ICC1	-	-	1.0	mA	Vcc=1.7V,fSCL=100kHz, tWR=5ms Byte Write Page Write Write Protect
	ICC2	-	-	3.0	mA	Vcc =3.6V,fSCL=100kHz, tWR=5ms Byte Write Page Write Write Protect
	ICC3	-	-	0.5	mA	Vcc =3.6V,fSCL=100kHz Random Read Current Read Sequential Read
Standby Current	ISB	-	-	2.0	μA	Vcc =3.6V,SDA,SCL= Vcc A0,A1,A2=GND,WP=GND
A0 HV Voltage	VHV	7	-	10	V	VHV-Vcc≧4.8V

○Note: This IC is not designed to be radiation-resistant.

●lectrical characteristics - AC(Unless otherwise specified Ta=-40℃～+85℃, VCC =1.7V～3.6V)

Parameter	Symbol	FAST-MODE 2.5V≦Vcc≦5.5V			STANDARD-MODE 1.7V≦Vcc≦5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fSCL	-	-	400	-	-	100	kHz
Data Clock High Period	tHIGH	0.6	-	-	4.0	-	-	μs
Data Clock Low Period	tLOW	1.2	-	-	4.7	-	-	μs
SDA and SCL Rise Time *1	tR	-	-	0.3	-	-	1.0	μs
SDA and SCL Fall Time *1	tF	-	-	0.3	-	-	0.3	μs
Start Condition Hold Time	tHD:STA	0.6	-	-	4.0	-	-	μs
Start Condition Setup Time	tSU:STA	0.6	-	-	4.7	-	-	μs
Input Data Hold Time	tHD:DAT	0	-	-	0	-	-	ns
Input Data Setup Time	tSU:DAT	100	-	-	250	-	-	ns
Output Data Delay Time	tPD	0.1	-	0.9	0.1	-	3.5	μs
Output Data Hold Time	tDH	0.1	-	-	0.1	-	-	μs
Stop Condition Setup Time	tSU:STO	0.6	-	-	4.0	-	-	μs
Bus Free Time	tBUF	1.2	-	-	4.7	-	-	μs
Write Cycle Time	tWR	-	-	5	-	-	5	ms
Noise Spike Width (SDA and SCL)	tI	-	-	0.1	-	-	0.1	μs
WP Hold Time	tHD：WP	0	-	-	0	-	-	ns
WP Setup Time	tSU：WP	0.1	-	-	0.1	-	-	μs
WP High Period	tHIGH：WP	1.0	-	-	1.0	-	-	μs

*1：Not 100% TESTED

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■Fast / Standard Modes

Fast mode and Standard mode differ only in operation frequency. Operations performed at 100kHz are considered in "Standard-mode", while those conducted at 400kHz are in "Fast-mode".

Please note that these clock frequencies are maximum values. At lower power supply voltage it is difficult to operate at high speeds. The EEPROM can operate at 400kHz, between 2.5V and 3.6V, and at 100kHz from 1.7V-2.5V.

●Synchronous Data Timing

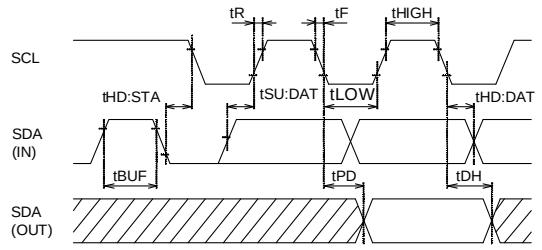

Fig.1-(a) Synchronous Data Timing

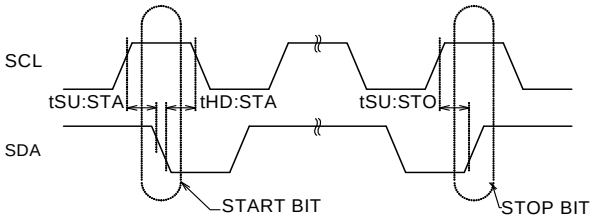

Fig.1-(b) Start/Stop Bit Timing

○SDA data is latched into the chip at the rising edge of SCL clock.

○Output data toggles at the falling edge of SCL clock.

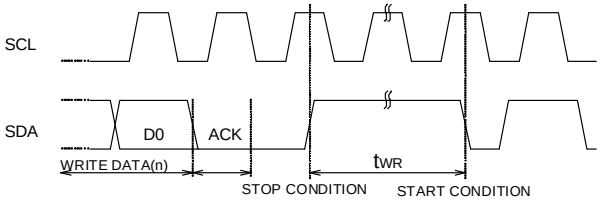

Fig.1-(c) Write Cycle Timing

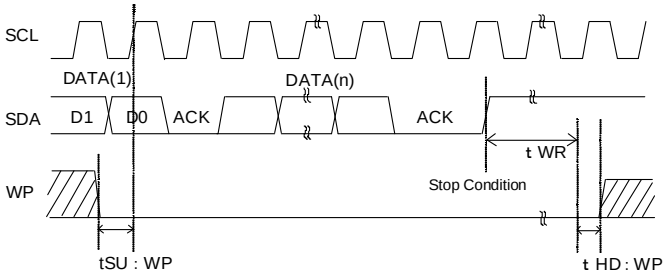

Fig.1-(d) WP Timing Of The Write Operation

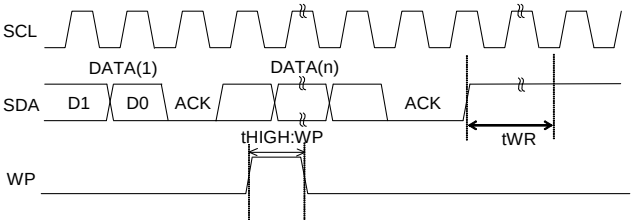

Fig.1-(e) WP Timing Of The Write Cancel Operation

○For WRITE operation, WP must be "Low" from the rising edge of the clock (which takes in D0 of first byte) until the end of tWR. (See Fig.1-(d)) During this period, WRITE operation can be canceled by setting WP "High".（See Fig.1-(e)）

○When WP is set to "High" during tWR, WRITE operation is immediately ceased, making the data unreliable. It must then be re-written.

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●Block diagram

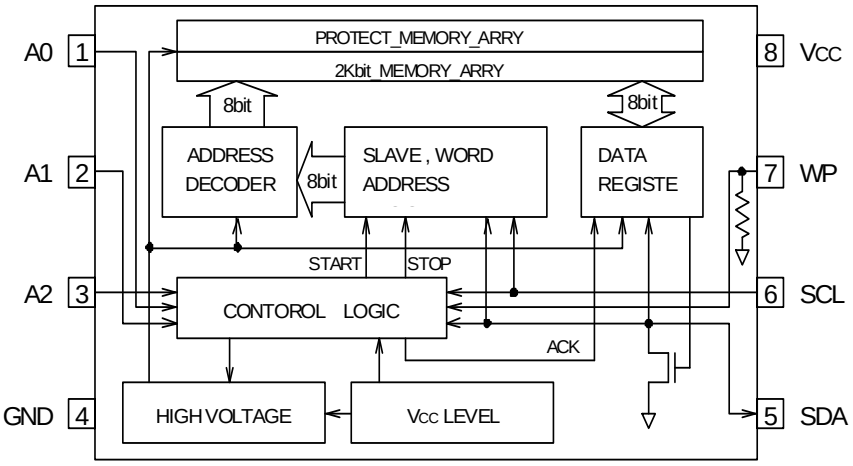

Fig.2 Blo

●Pinout diagram and description

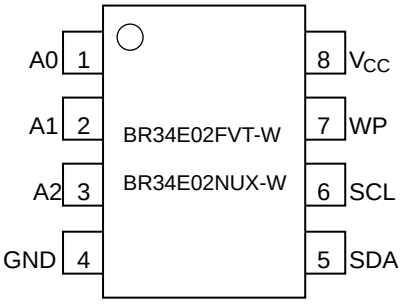

Fig.3 Pin Configuration

Pin Name	Input/Output	Functions
Vcc	-	Power Supply
GND	-	Ground 0V
A0,A1,A2	IN	Slave Address Set.
SCL	IN	Serial Clock Input
SDA	IN / OUT	Slave and Word Address, *1 Serial Data Input, Serial Data Output
WP	IN	Write Protect Input *2

*1 Open drain output requires a pull-up resistor.
*2 WP Pin has a Pull-Down resistor. Please leave unconnected or connect to GND when not in use.

●Electrical characteristics curves

The following characteristic data are typ. value.

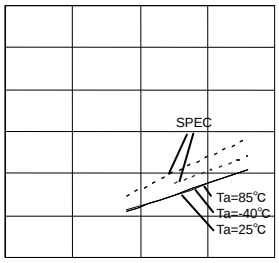

Fig.4 "H" Input Voltage VIH (A0,A1,A2,SCL,SDA,WP)

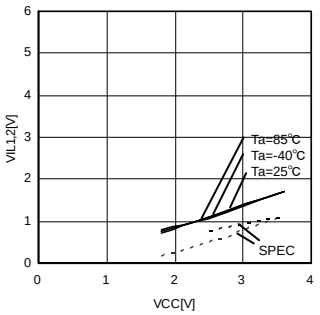

Fig.5 "L" Input Voltage VIL (A0,A1,A2,SCL,SDA,WP)

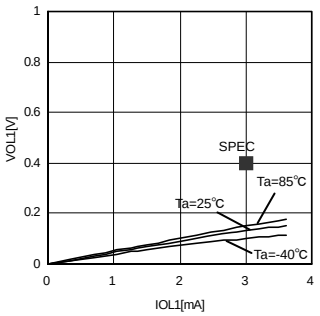

Fig.6 "L" Output Voltage VOL1-IOL1 (Vcc=2.5V)

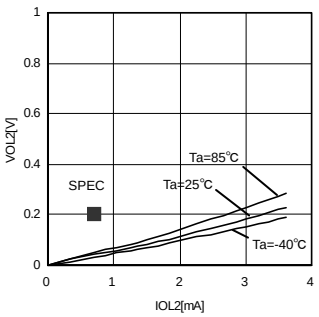

Fig.7 "L" Output Voltage VOL2-IOL2 (Vcc=1.7V)

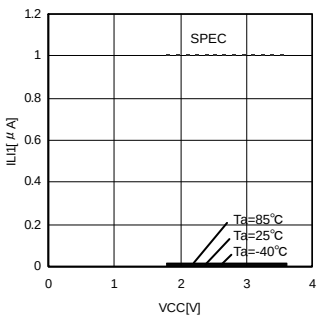

Fig.8 Input Leakage Current ILI1 (A0,A1,A2,SCL,SDA)

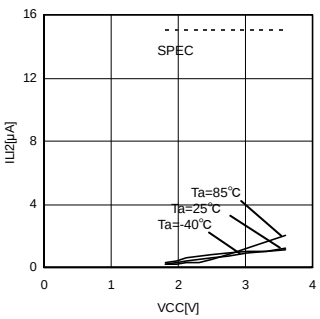

Fig.9 Input Leakage Current ILI2 (WP)

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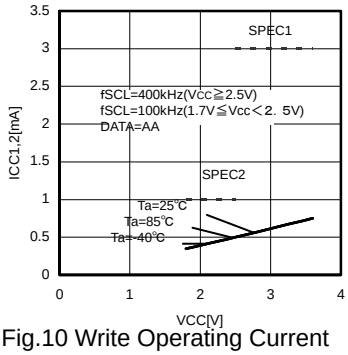


Fig.10 Write Operating Current ICC1,2 (fSCL=100kHz,400kHz)

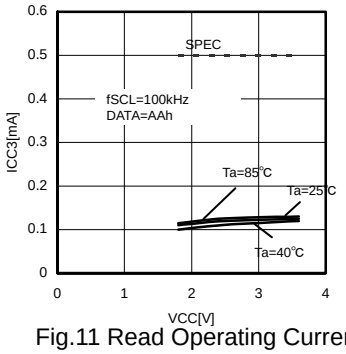


Fig.11 Read Operating Current ICC3 (fSCL=400kHz)

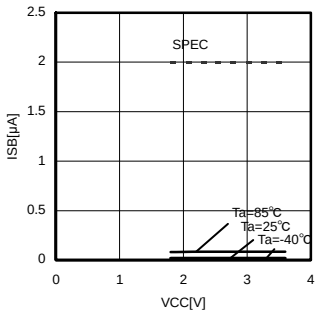


Fig.12 Standby Current ISB

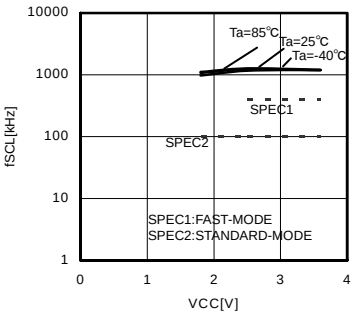


Fig.13 Clock Frequency fSCL

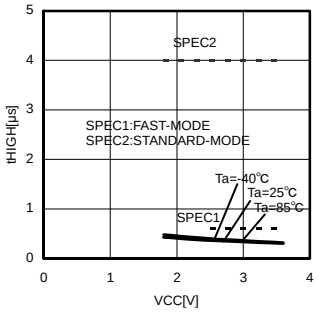


Fig.14 Data Clock High Period tHigh

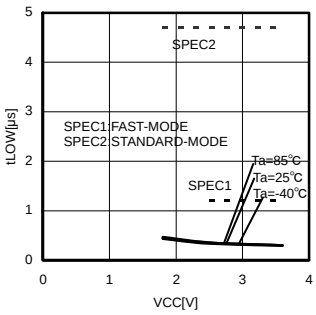


Fig.15 Data Clock Low Period tLow

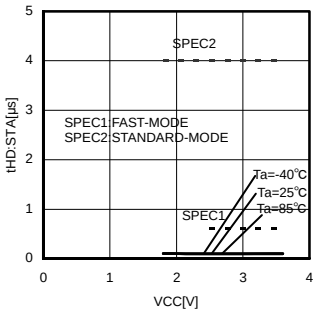


Fig.16 Start Condition Hold Time tHD:STA

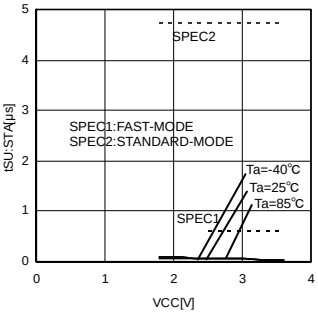
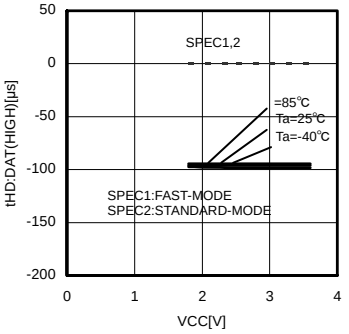


Fig.17 Start Condition Setup Time tSU:STA



FiagmDag.18 ck Di$_{Ta}$rata HoldimtHD:DAT(High)

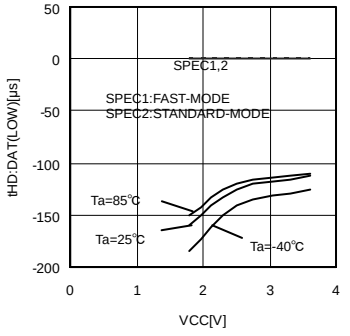


Fig.19 Data Hold Time tHD:DAT(LOW)

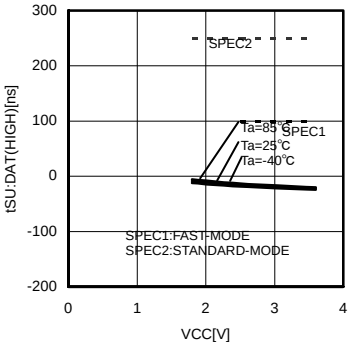


Fig.20 Input Data Setup Time tSU:DAT(HIGH)

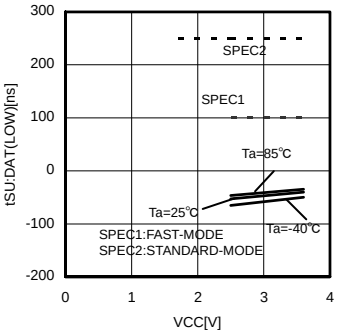


Fig.21 Input Data Setup Time tSU:DAT(LOW)

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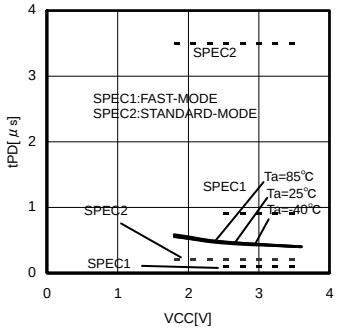

Fig.22 Output Data Delay Time
tPD

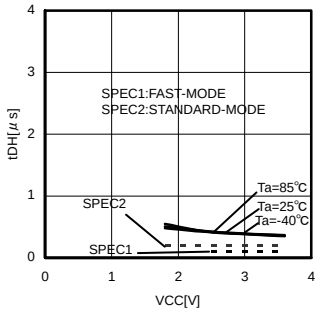

Fig.23 Output Data Hold Time
tDH

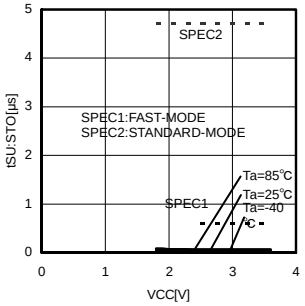

Fig.24 Stop Condition Setup Time
tSU:STO

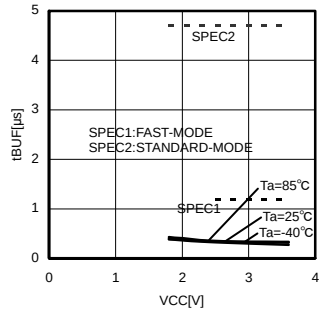

Fig.25 Bus Free Time
tBUF

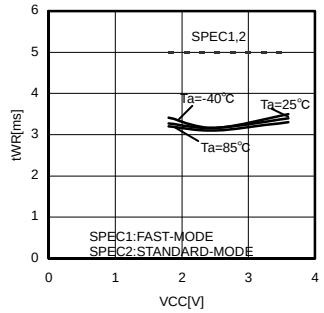

Fig.26 Write Cycle Time
tWR

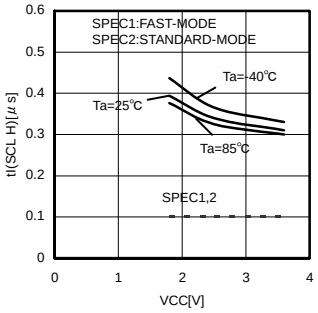

Fig.27 Noise Spike Width
tI(SCL H)

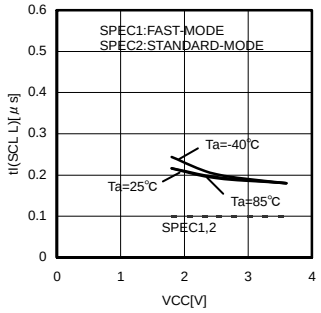

Fig.28 Noise Spike Width
tI(SCL L)

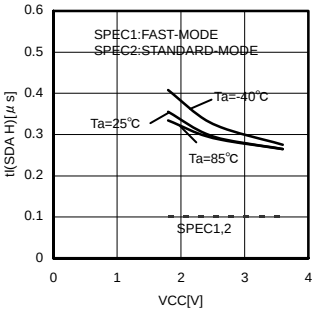

Fig.29 Noise Spike Width
tI(SDA H)

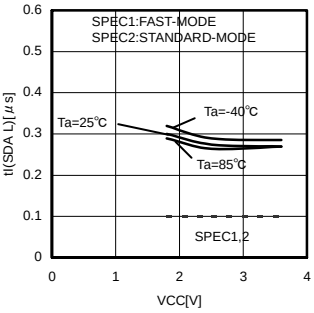

Fig.30 Noise Spike Width
tI(SDA L)

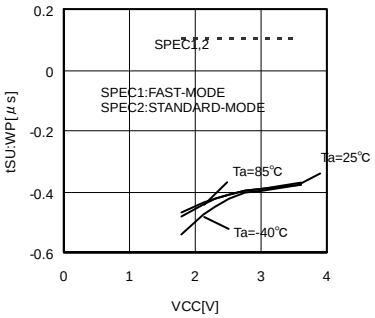

Fig.31 WP Setup Time
tSU:WP

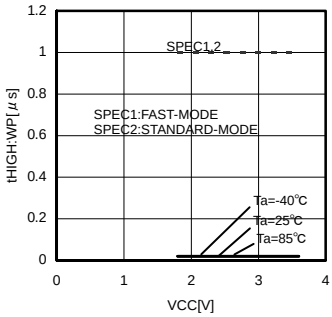

Fig.32 WP High Period
tHigh:WP

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●Data transfer on the I^2C BUS

○Data transfer on the I^2C BUS

The BUS is considered to be busy after the START condition and free a certain time after the STOP condition.
Every SDA byte must be 8-bits long and requires an ACKNOWLEDGE signal after each byte. The devices have Master and Slave configurations. The Master device initiates and ends data transfer on the BUS and generates the clock signals in order to permit transfer.
The EEPROM in a slave configuration is controlled by a unique address. Devices transmitting data are referred to as the Transmitter. The devices receiving the data are called Receiver.

○START Condition (Recognition of the START bit)

- All commands are proceeded by the start condition, which is a High to Low transition of SDA when SCL is High.
- The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. (See Fig.1-(b) START/STOP Bit Timing)

○STOP Condition (Recognition of STOP bit)

- All communications must be terminated by a stop condition, which is a Low to High transition of SDA when SCL is High. (See Fig.1-(b) START/STOP Bit Timing)

○Write Protect By Soft Ware

- Set Write Protect command and permanent set Write Protect command set data of 00h～7Fh in 256 words write protection block. Clear Write Protect command can cancel write protection block which is set by set write Protect command. Cancel of write protection block which is set by permanent set Write Protect command at once is impossibility. When these commands are carried out, WP pin must be OPEN or GND.

○Acknowledge

- Acknowledge is a software used to indicate successful data transfers. The Transmitter device will release the BUS after transmitting eight bits. When inputting the slave address during write or read operation, the Transmitter is the µ-COM. When outputting the data during read operation, the Transmitter is the EEPROM.
- During the ninth clock cycle the Receiver will pull the SDA line Low to verify that the eight bits of data have been received. (When inputting the slave address during write or read operation, EEPROM is the receiver. When outputting the data during read operation the receiver is the µ-COM.)
- The device will respond with an Acknowledge after recognition of a START condition and its slave address (8bit).
- In WRITE mode, the device will respond with an Acknowledge after the receipt of each subsequent 8-bit word (word address and write data).
- In READ mode, the device will transmit eight bits of data, release the SDA line, and monitor the line for an Acknowledge.
- If an Acknowledge is detected and no STOP condition is generated by the Master, the device will continue to transmit the data. If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to standby mode.

○Device Addressing

- Following a START condition, the Master outputs the Slave address to be accessed. The most significant four bits of the slave address are the “device type indentifier.” For this EEPROM it is “1010.
  ” (For WP register access this code is "0110".)
- The next three bits identify the specified device on the BUS (device address).
  The device address is defined by the state of the A0,A1 and A2 input pins. This IC works only when the device address input from the SDA pin corresponds to the status of the A0,A1 and A2 input pins. Using this address scheme allows up to eight devices to be connected to the BUS.
- The last bit of the stream (R/$\overline{W}$…READ/$\overline{WRITE}$) determines the operation to be performed.

R/$\overline{W}$=0 ···· WRITE (including word address input of Random Read)
R/$\overline{W}$=1 ···· READ

Slave Address Set Pin			Device Type	Device Address			Read Write Mode	Access Area
A2	A1	A0	1010	A2	A1	A0	R/$\overline{W}$	2kbit Access to Memory
A2	A1	A0	0110	A2	A1	A0	R/$\overline{W}$	Access to Permanent Set Write Protect Memory
GND	GND	VHV		0	0	1	R/$\overline{W}$	Access to Set Write Protect Memroy
GND	Vcc	VHV		0	1	1	R/$\overline{W}$	Access to Clear Write Protect MEmory

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○WRITE PROTECT PIN(WP)

When WP pin set to Vcc (H level), write protect is set for 256 words (all address). When WP pin set to GND (L level), it is enable to write 256 words (all address).

If permanent protection is done by Write Protect command, lower half area (00～7Fh address) is inhibited writing regardless of WP pin state.

WP pin has a Pull-Down resistor. Please be left unconnected or connect to GND when WP feature is not in use.

○Confirm Write Protect Resistor by ACK

According to state of Write Protect Resistor, ACK is as follows.

State of Write Protect Registor	WP Input	Input Command	ACK	Address	ACK	Data	ACK	Write Cycle(tWR)
In case, protect by PSWP	-	PSWP, SWP, CWP	No ACK	-	No ACK		No ACK	No
		Page or Byte Write (00～7Fh)	ACK	WA7～WA0	ACK	D7～D0	No ACK	No
In case, protect by SWP	0	SWP	No ACK	-	No ACK	-	No ACK	No
		CWP	ACK	-	ACK	-	ACK	Yes
		PSWP	ACK	-	ACK	-	ACK	Yes
		Page or Byte Write (00～7Fh)	ACK	WA7～WA0	ACK	D7～D0	No ACK	No
	1	SWP	No ACK	-	No ACK	-	No ACK	No
		CSP	ACK	-	ACK	-	No ACK	No
		PSWP	ACK	-	ACK	-	No ACK	No
		Page or Byte Write	ACK	WA7～WA0	ACK	D7～D0	No ACK	No
In case, Not protect	0	PSWP, SWP, CWP	ACK	-	ACK	-	ACK	Yes
		Page or Byte Write	ACK	WA7～WA0	ACK	D7～D0	ACK	Yes
	1	PSWP, SWP, CWP	ACK	-	ACK	-	No ACK	No
		Page or Byte Write	ACK	WA7～WA0	ACK	D7～D0	No ACK	No

*- is Don't Care

State of Write Protect Registor	Command	ACK	Address	ACK	Data	ACK
In case, protect by PSWP	PSWP, SWP, CWP	No ACK	-	No ACK	-	No ACK
In case, protect by SWP	SWP	No ACK	-	No ACK	-	No ACK
	CWP	ACK	-	No ACK	-	No ACK
	PSWP	ACK	-	No ACK	-	No ACK
In case, Not protect	PSWP, SWP, CWP	ACK	-	No ACK	-	No ACK

○Write Cycle

During WRITE CYCLE operation data is written in the EEPROM. The Byte Write Cycle is used to write only one byte. In the case of writing continuous data consisting of more than one byte, Page Write is used. The maximum bytes that can be written at one time is 16 bytes.

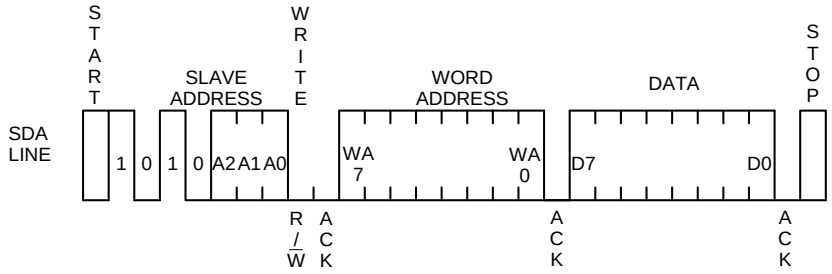

Fig.33 Byte Write Cycle Timing

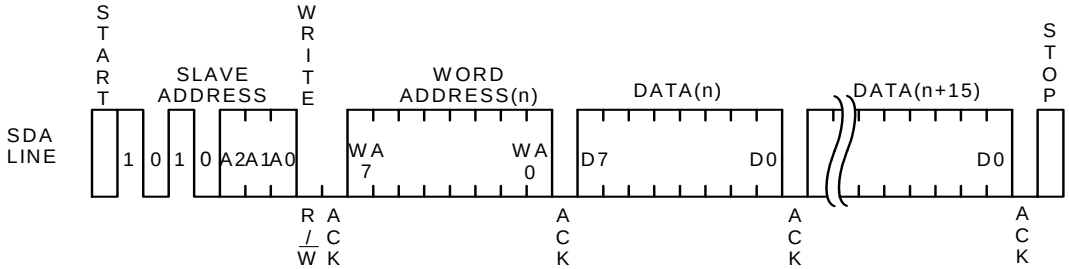

Fig.34 Page Write Cycle Timing

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- With this command the data is programmed into the indicated word address.
- When the Master generates a STOP condition, the device begins the internal write cycle to the nonvolatile memory array.
- Once programming is started no commands are accepted for tWR (5ms max.).
- This device is capable of sixteen-byte Page Write operations.
- If the Master transmits more than sixteen words prior to generating the STOP condition, the address counter will “roll over” and the previously transmitted data will be overwritten.
- When two or more byte of data are input, the four low order address bits are internally incremented by one after the receipt of each word, while the four higher order bits of the address (WA7～WA4) remain constant.

○Read Cycle

During Read Cycle operation data is read from the EEPROM. The Read Cycle is composed of Random Read Cycle and Current Read Cycle. The Random Read Cycle reads the data in the indicated address.
The Current Read Cycle reads the data in the internally indicated address and verifies the data immediately after the Write Operation. The Sequential Read operation can be performed with both Current Read and Random Read. With the Sequential Read Cycle it is possible to continuously read the next data.

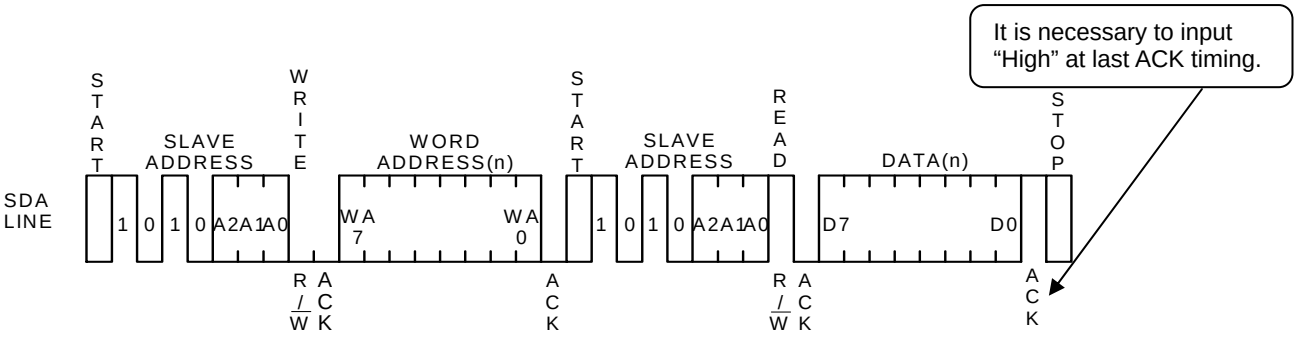

Fig.35 Random Read Cycle Timing

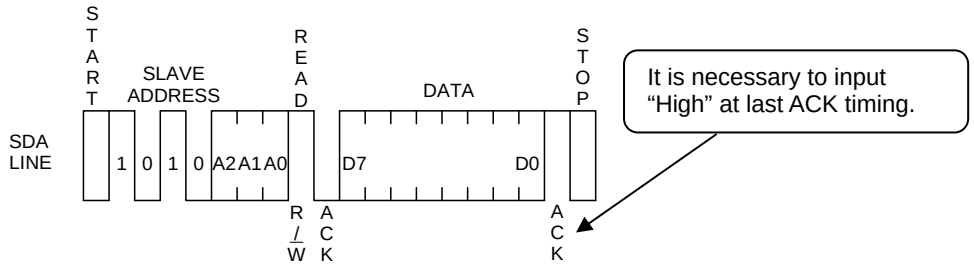

Fig.36 Current Read Cycle Timing

- Random Read operation allows the Master to access any memory location indicated by word address.
- In cases where the previous operation is Random or Current Read (which includes Sequential Read), the internal address counter is increased by one from the last accessed address (n). Thus Current Read outputs the data of the next word address (n+1).
- If an Acknowledge is detected and no STOP condition is generated by the Master (μ-COM), the device will continue to transmit data. (It can transmit all data (2kbit 256word))
- If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to standby mode.
- If an Acknowledge is detected with the "Low" level (not "High" level), the command will become Sequential Read, and the next data will be transmitted. Therefore, the Read command is not terminated. In order to terminate Read input Acknowledge with "High" always, then input a STOP condition.

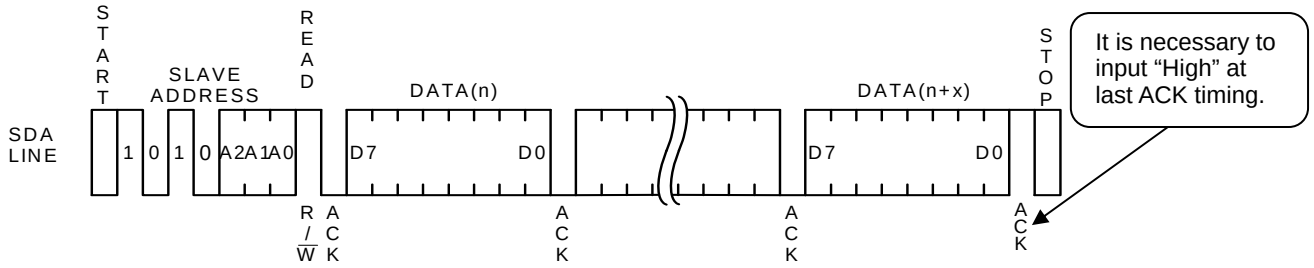

Fig.37 Sequential Read Cycle Timing（With Current Read）

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○Write Protect Cycle

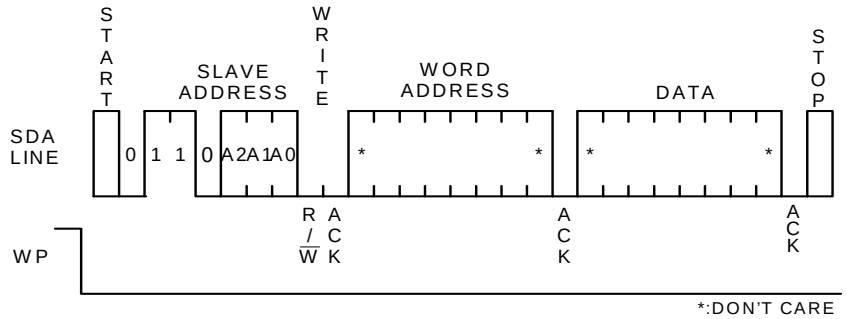

Fig. 38 Permanent Write Protect Cycle

- Permanent set Write Protect command set data of 00h～7Fh in 256 words write protection block. Clear Write Protect command can cancel write protection block which is set by set write Protect command. Cancel of write protection block which is set by permanent set Write Protect command at once is impossibility. When these commands are carried out, WP pin must be OPEN or GND.
- Permanent Set Write Protect command needs tWR from stop condition same as Byete Write and Page Write, During tWR, input command is canceled.
- Refer to P8/19 about reply of ACK in each protect state.

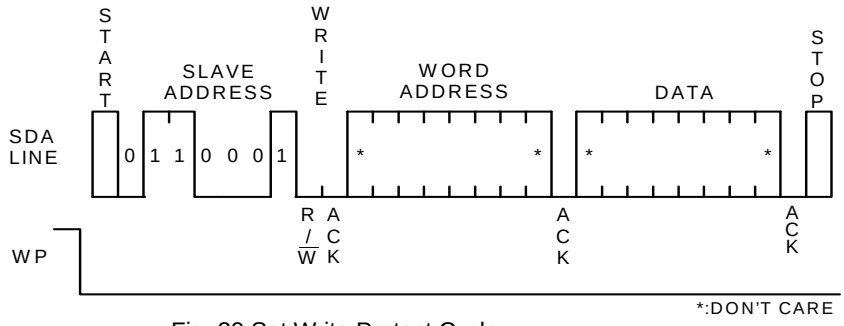

Fig. 39 Set Write Protect Cycle

- Permanent set Write Protect command set data of 00h～7Fh in 256 words write protection block. Clear Write Protect command can cancel write protection block which is set by set write Protect command. Cancel of write protection block which is set by permanent set Write Protect command at once is impossibility. When these commands are carried out, WP pin must be OPEN or GND.
- Permanent Set Protect command needs tWR from stop condition same as Byete Write and Page Write, During tWR, input command is canceled.
- Refer to P8/19 about reply of ACk in each protect state.

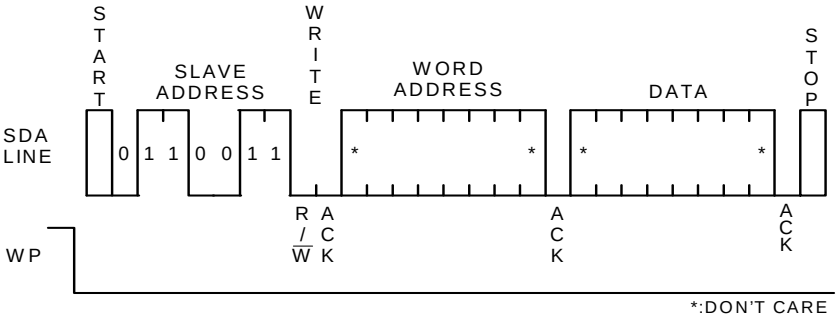

Fig. 40 Clear Write Protect Cycle

- Clear Write Protect command can cancel write protection block which is set by set write Protect command. Cancel of write protection block which is set by permanent set Write Protect command at once is impossibility. When these commands are carried out, WP pin must be OPEN or GND.
- Permanent Clear Write Protect command needs tWR from stop condition same as Byete Write and Page Write, During tWR, input command is canceled.
- Refer to P8/19 about reply of ACk in each protect state.

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●Software Reset

Execute software reset in the event that the device is in an unexpected state after power up and/or the command input needs to be reset. Below are three types(Fig.39 –(a), (b), (c)) of software reset:

During dummy clock, release the SDA BUS (tied to Vcc by a pull-up resistor). During this time the device may pull the SDA line Low for Acknowledge or the outputting of read data.If the Master sets the SDA line to High, it will conflict with the device output Low, which can cause current overload and result in instantaneous power down, which may damage the device.

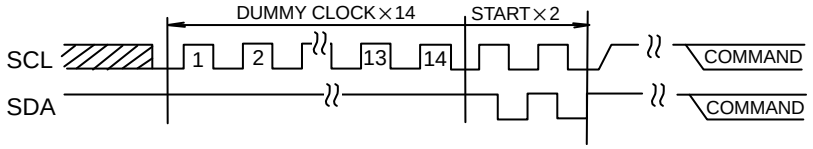

Fig.39-(a) DUMMY CLOCK×14 + START+START

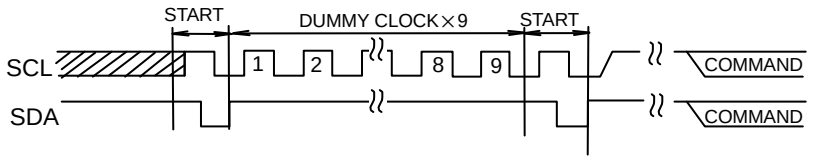

Fig.39-(b) START + DUMMY CLOCK×9 + START

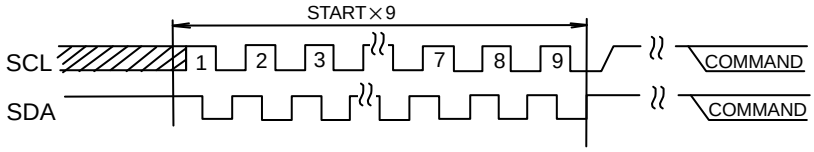

Fig.39-(c) START×9

∗ COMMAND starts with start condition.

●Acknowledge polling

Since the IC ignores all input commands during the internal write cycle, no ACK signal will be returned.

When the Master sends the next command after the Write command, if the device returns an ACK signal it means that the program is completed. No ACK signal indicates that the device is still busy.

Using Acknowledge polling decreases the waiting time by tWR=5ms.

When operating Write or Current Read after Write, first transmit the Slave address (R/$\overline{W}$ is"High" or "Low"). After the device returns the ACK signal continue word address input or data output.

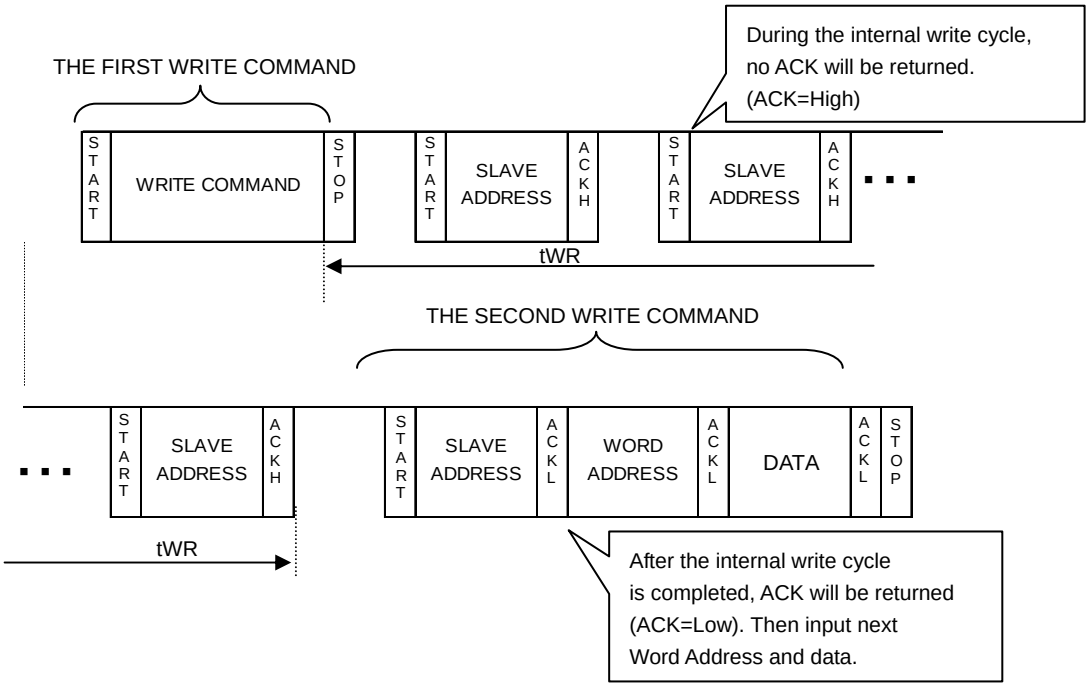

Fig.40 Successive Write Operation By Acknowledge Polling

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●WP effective timing

WP is normally fixed at "H" or "L". However, in case WP needs to be controlled in order to cancel the Write command, pay attention to “WP effective timing” as follows:

The Write command is canceled by setting WP to "H" within the WP cancellation effective period.

The period from the START condition to the rising edge of the clock (which takes in the data DO - the first byte of the Page Write data) is the ‘invalid cancellation period’. WP input is considered inconsequential during this period. The setup time for the rising edge of the SCL, which takes in DO, must be more than 100ns.

The period from the rising edge of SCL (which takes in the data D0) to the end of internal write cycle (tWR) is the ‘effective cancellation period’. When WP is set to "H" during tWR, Write operation is stopped, making it necessary to rewrite the data. It is not necessary to wait for tWR (5ms max.) after stopping the Write command by WP because the device is in standby mode.

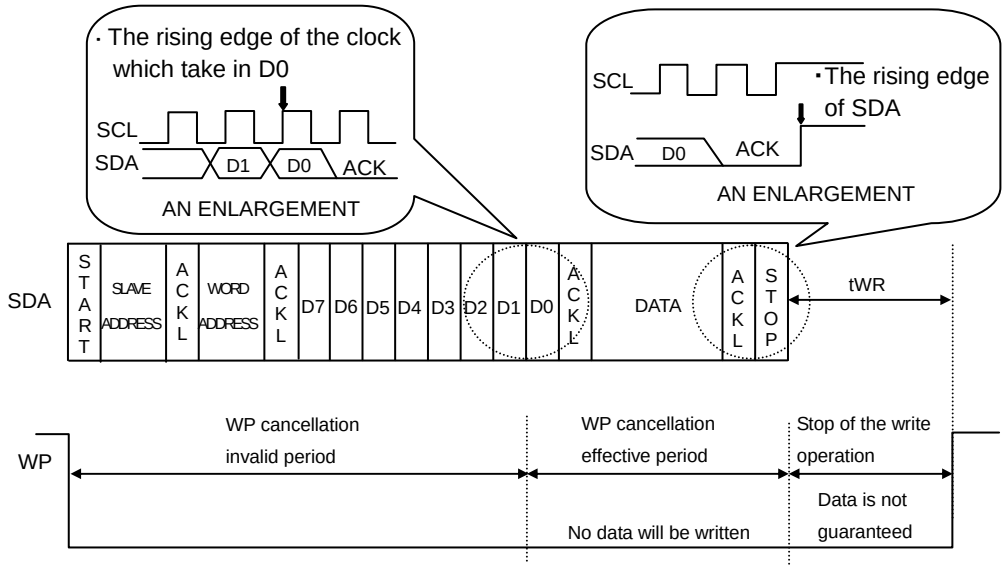

Fig.41 WP effective timing

●Command cancellation from the START and STOP conditions

Command input is canceled by successive inputs of START and STOP conditions. (Refer to Fig.42)

However, during ACK or data output, the device may set the SDA line to Low, making operation of the START and STOP conditions impossible, and thus preventing reset. In this case execute reset by software. (Refer to Fig.39)

The internal address counter will not be determined when operating the Cancel command by the START and STOP conditions during Random, Sequential or Current Read. Operate a Random Read in this case.

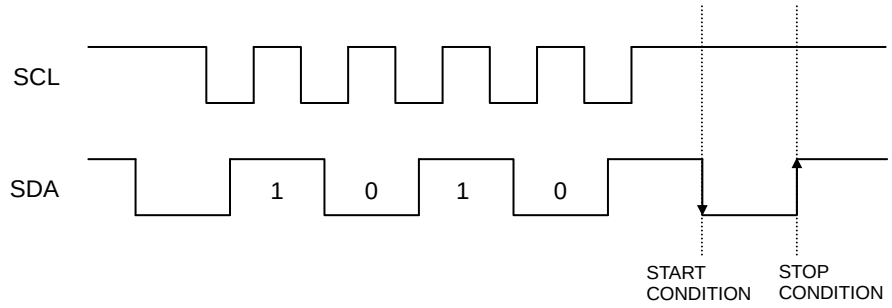

Fig.42 Command cancellation by the START and STOP conditions during input of the Slave Address

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●I/O Circuit

○SDA Pin Pull-up Resistor

A pull-up resistor is required because SDA is an NMOS open drain. Determine the resistor value of (R_{PU}) by considering the VIL and IL, and VOL-IOL characteristics. If a large R_{PU} is chosen, the clock frequency needs to be slow. A smaller R_{PU} will result in a larger operating current.

○Maximum R_{PU}

The maximum of R_{PU} can be determined by the following factors.

①The SDA rise time determined by R_{PU} and the capacitance of the BUS line(CBUS) must be less than tR. In addition, all other timings must be kept within the AC specifications.

②When the SDA BUS is High, the voltage Ⓐ at the SDA BUS is determined from the total input leakage(IL) of all devices connected to the BUS. RPU must be higher than the input High level of the microcontroller and the device, including a noise margin 0.2V_{CC}.

$$V_{CC} - I_L R_{PU} - 0.2\,V_{CC} \geqq V_{IH}$$

$$\therefore \quad R_{PU} \leqq \frac{0.8V_{CC} - V_{IH}}{I_L}$$

Examples: When V_{CC} =3V, IL=10μA, VIH=0.7 V_{CC}

According to ②

$$R_{PU} \leqq \frac{0.8\times3 - 0.7\times3}{10\times10^{-6}}$$

$$\leqq 300\ [k\Omega]$$

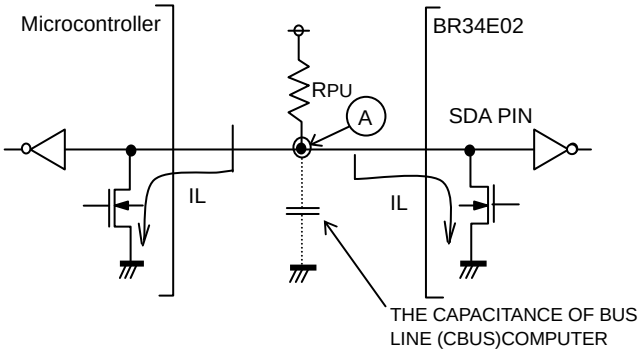

Fig.43 I/O Circuit

○Minimum R_{PU}

The minimum value of R_{PU} is determined by following factors.

①Meets the condition that V_{OLMAX}=0.4V, I_{OLMAX}=3mA when the output is Low.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leqq I_{OL}$$

$$\therefore \quad R_{PU} \geqq \frac{V_{CC} - V_{OL}}{I_{OL}}$$

②V_{OLMAX}=0.4V must be lower than the input Low level of the microcontroller and the EEPROMincluding the recommended noise margin of 0.1V_{CC}.

$V_{OLMAX} \leqq$ VIL-0.1 V_{CC}

Examples: V_{CC}=3V, VOL=0.4V, IOL=3mA, the VIL of the controller and the EEPROM is VIL=0.3V_{CC}, According to ①

$$R_{PU} \geqq \frac{3-0.4}{3\times10^{-3}}$$

$$\geqq 867\ [\Omega]$$

and VOL=0.4 [V]

and VIL=0.3×3

=0.9 [V]

o that condition ② is met

○SCL Pin Pull-up Resistor

When SCL is controlled by the CMOS output the pull-up resistor at SCL is not required.

However, should SCL be set to Hi-Z, connection of a pull-up resistor between SCL and V_{CC} is recommended.

Several kΩ are recommended for the pull-up resistor in order to drive the output port of the microcontroller.

●A0, A1, A2, WP Pin connections

○Device Address Pin (A0, A1, A2) connections

The status of the device address pins is compared with the device address sent by the Master. One of the devices that is connected to the identical BUS is selected. Pull up or down these pins or connect them to V_{CC} or GND. Pins that are not used as device address (N.C.Pins) may be High, Low, or Hi-Z.

○WP Pin connection

The WP input allows or prohibits write operations. When WP is High, only Read is available and Write to all address is prohibited. Both Read and Write are available when WP is Low.

In the event that the device is used as a ROM, it is recommended that the WP input be pulled up or connected to V_{CC}.

When both READ and WRITE are operated, the WP input must be pulled down or connected to GND or controlled.

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●Microcontroller connection

○Concerning Rs

The open drain interface is recommended for the SDA port in the I^2C BUS. However, if the Tri-state CMOS interface is applied to SDA, insert a series resistor (Rs) between the SDA pin of the device and the pull up resistor R_{PU} is recommended, since it will serve to limit the current between the PMOS of the microcontroller, and the NMOS of the EEPROM. Rs also protects the SDA pin from surges. Therefore, Rs is able to be used though open drain inout of the SDA port.

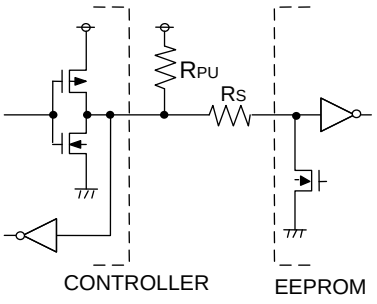


Fig.44 I/O Circuit

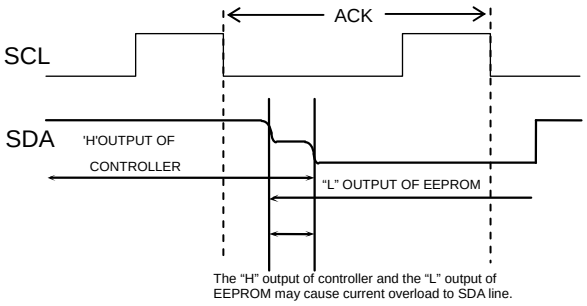


Fig.45 Input/Output Collision Timing

○Rs Maximum

The maximum value of Rs is determined by following factors.

①SDA rise time determined by R_{PU} and the capacitance value of the BUS line (CBUS) of SDA must be less than tR. In addition, the other timings must be within the timing conditions of the AC.

②When the output from SDA is Low, the voltage of the BUS at Ⓐ is determined by R_{PU}, and Rs must be lower than the input Low level of the microcontroller, including recommended noise margin ($0.1V_{CC}$).

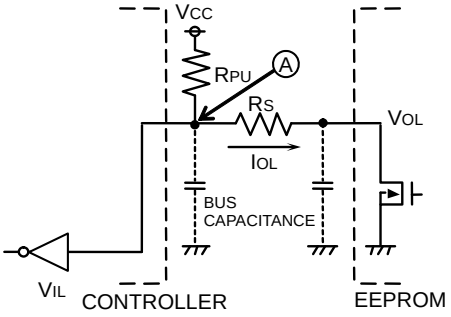


Fig.46 I/O Circuit

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Examples : When V_{CC}=3V V_{IL}=0.3V_{CC} V_{OL}=0.4V R_{PU}=20kΩ

$$\text{According to ②} \quad R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

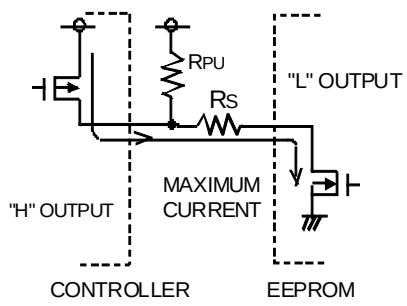
$$\leqq 1.67 \ [k\Omega]$$

○Rs Minimum

The minimum value of Rs is determined by the current overload during BUS conflict.

Current overload may cause noises in the power line and instantaneous power down.

The following conditions must be met, where "I" is the maximum permissible current, which depends on the Vcc line impedance as well as other factors. "I" current must be less than 10mA for EEPROM.



$$\frac{Vcc}{R_S} \leqq I$$

$$\therefore \quad R_S \geqq \frac{Vcc}{I}$$

Examples: When V_{CC}=3V, I=10mA

$$R_S \geqq \frac{3}{10\times10^{-3}}$$

$$\geqq 300 \ [\Omega]$$

Fig.47 I/O Circuit

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●I^2C BUS Input / Output equivalent circuits

○Input (A0,A2,SCL)

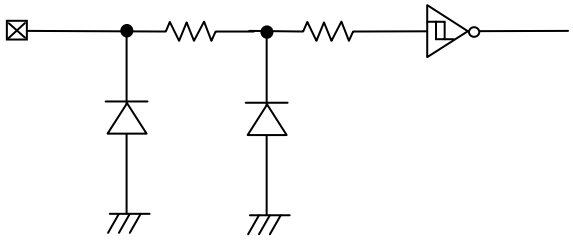

Fig.48 Input Pin Circuit

○Input / Output (SDA)

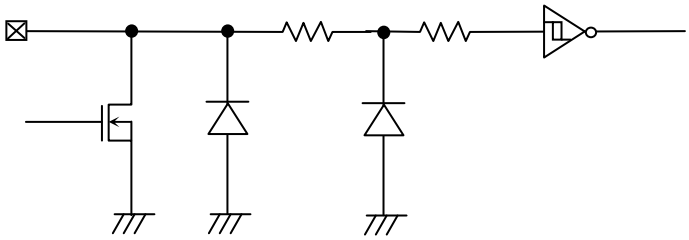

Fig.49 Input / Output Pin Circuit

○Input (A1)

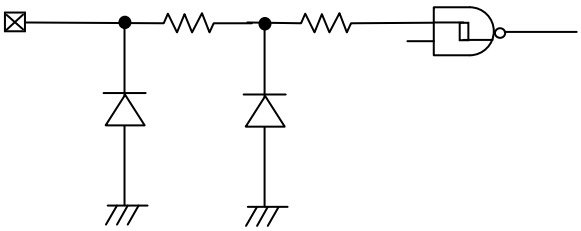

Fig.50 Input Pin Circuit

○Input (WP)

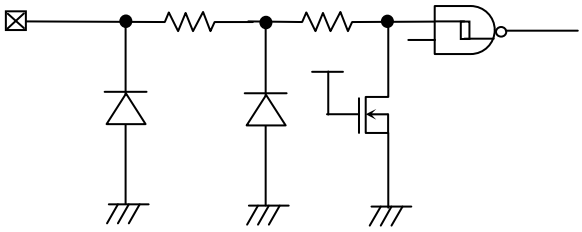

Fig.51 Input Pin Circuit

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●Power Supply Notes

VCC increases through the low voltage region where the internal circuit of IC and the microcontroller are unstable. In order to prevent malfunction, the IC has P.O.R and LVCC functionality. During power up, ensure that the following conditions are met to guaranty P.O.R. and LVCC operability.

1. "SDA='H'" and "SCL='L' or 'H'".
2. Follow the recommended conditions of tR, tOFF, Vbot so that P.O.R. will be activated during power up.

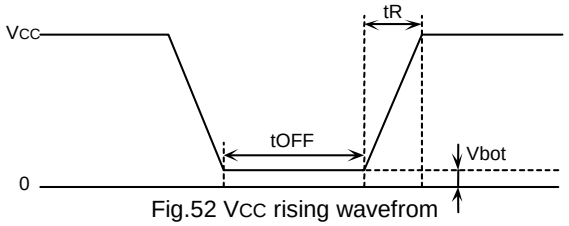

Fig.52 VCC rising wavefrom

Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

3. Prevent SDA and SCL from being "Hi-Z".

In case that condition 1. and/or 2. cannot be met, take following actions.

A) If unable to keep Condition 1 (SDA is "Low" during power up)

→Make sure that SDA and SCL are "High" as in the figure below.

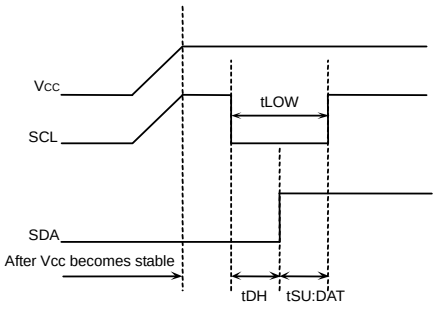

Fig.53 SCL="H" and SDA="L"

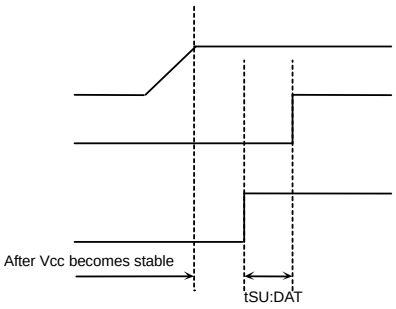

Fig.54 SCL="L" and SDA="L"

B) If unable to keep Condition 2

→After the power stabilizes, execute software reset. (See page 9,10)

C) If unable to keep either Condition 1 or 2

→Follow Instruction A first, then B

●LVCC Circuit

The LVCC circuit prevents Write operation at low voltage and prevents inadvertent writing. A voltage below the LVCC voltage (1.2V typ.) prohibits Write operation.

●VCC Noise

○Bypass Capacitor

Noise and surges on the power line may cause abnormal function. It is recommended that bypass capacitors (0.1µF) be attached between VCC and GND externally.

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●Notes for Use

1) Descrived numeric values and data are design representative values, and the values are not guaranteed.

2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

3) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

5) Heat design
In consideration of permissible dissipation in actual use condition, carry out heat design with sufficient margin.

6) Terminal to terminal short circuit and wrong packaging
When to package LSI on to a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of short circuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

7) Use in a strong electromagnetic field may cause malfunction, therfore, evaluate design sufficiently.

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●Ordering part number

B	R	3	4	E	0	2	F	V	T	-	W	E	2

ROHM type

BUS type
34 : I²C

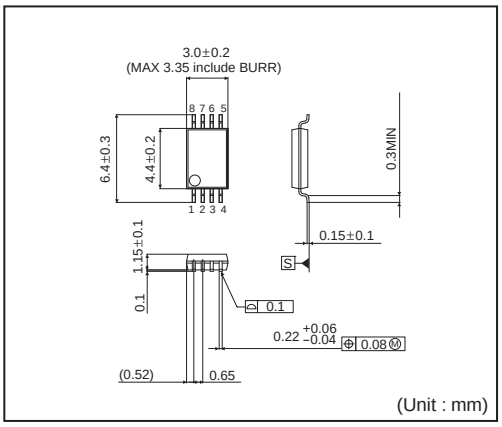
Priduct type

Capacity
02= 2K

Packagr
FVT:TSSOP-B8
NUX:VSON008X2030

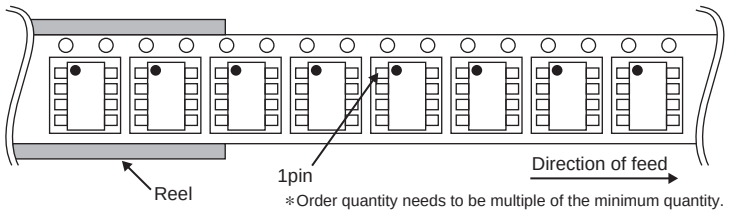
W : Double cell
Packaging and forming specification
E2: Embossed tape and reel
(TSSOP-B8)
TR: Embossed tape and reel
(VSON008X2030)

SSOP-B8



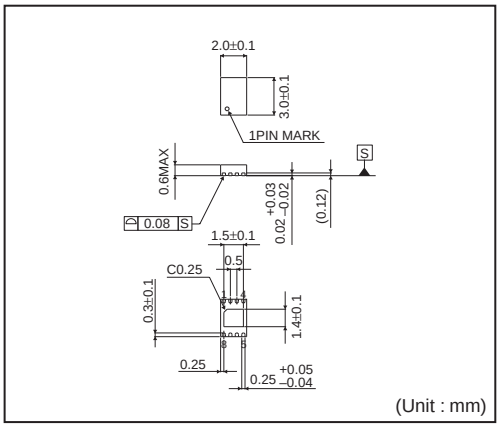
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



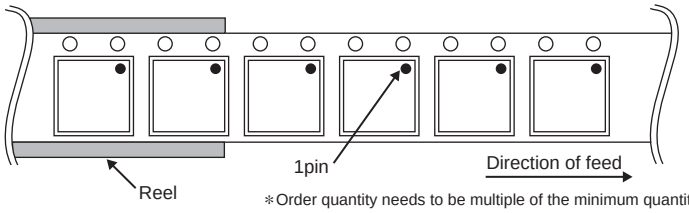
∗Order quantity needs to be multiple of the minimum quantity.

VSON008X2030



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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