WCSN0436V1P

128Kx36 Pipelined SRAM with NoBL™ Architecture

Features

- **Pin compatible and functionally equivalent to ZBT™ devices IDT71V546, MT55L128L36P, and MCM63Z736**
- **Supports 166-MHz bus operations with zero wait states**
  - **Data is transferred on every clock**
- **Internally self-timed output buffer control to eliminate the need to use OE**
- **Fully registered (inputs and outputs) for pipelined operation**
- **Byte Write capability**
- **128K x 36 common I/O architecture**
- **Single 3.3V power supply**
- **Fast clock-to-output times**
  - **3.5 ns (for 166-MHz device)**
  - **3.8 ns (for 150-MHz device)**
  - **4.0 ns (for 143-MHz device)**
  - **4.2 ns (for 133-MHz device)**
  - **5.0 ns (for 100-MHz device)**
  - **7.0 ns (for 80-MHz device)**
- **Clock Enable ($\overline{CEN}$) pin to suspend operation**
- **Synchronous self-timed writes**
- **Asynchronous output enable**
- **JEDEC-standard 100 TQFP package**
- **Burst Capability—linear or interleaved burst order**
- **Low standby power (17.325 mW max.)**

Functional Description

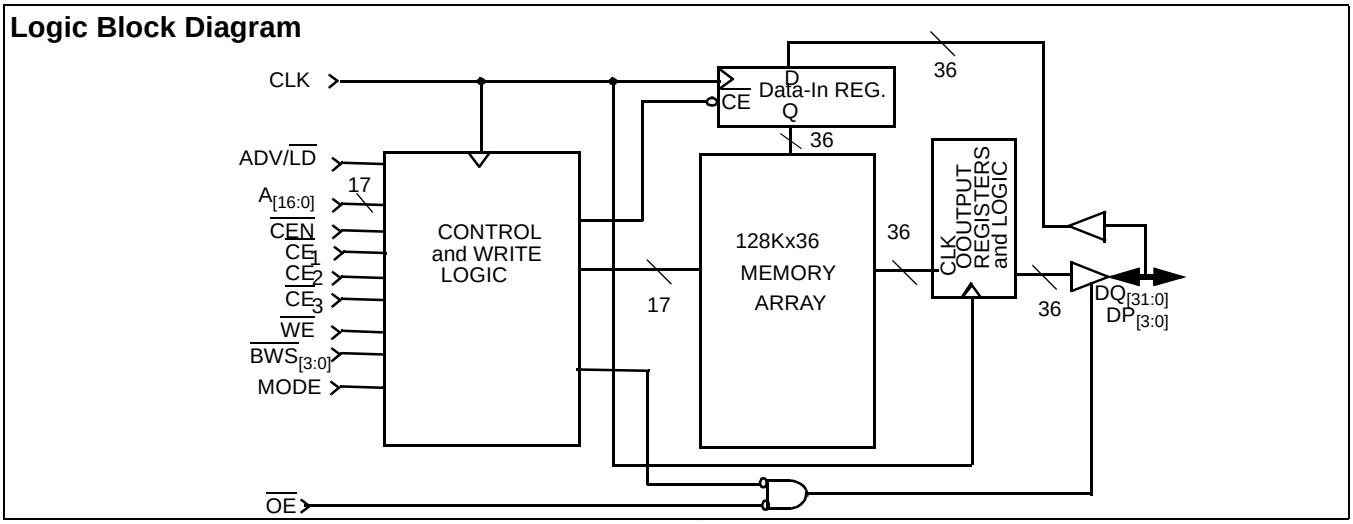
The WCSN0436V1P is a 3.3V, 128K by 36 synchronous-pipelined Burst SRAM designed specifically to support unlimited true back-to-back Read/Write operations without the insertion of wait states. The WCSN0436V1P is equipped with the advanced No Bus Latency™ (NoBL™) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of the SRAM, especially in systems that require frequent Write/Read transitions.The WCSN0436V1P is pin/functionally compatible to ZBT SRAMsIDT71V546, MT55L128L36P, and MCM63Z736.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 3.5 ns (166-MHz device).

Write operations are controlled by the four Byte Write Select ($\overline{BWS}_{[3:0]}$) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. In order to avoid bus contention, the output drivers are synchronously three-stated during the data portion of a write sequence.

Logic Block Diagram

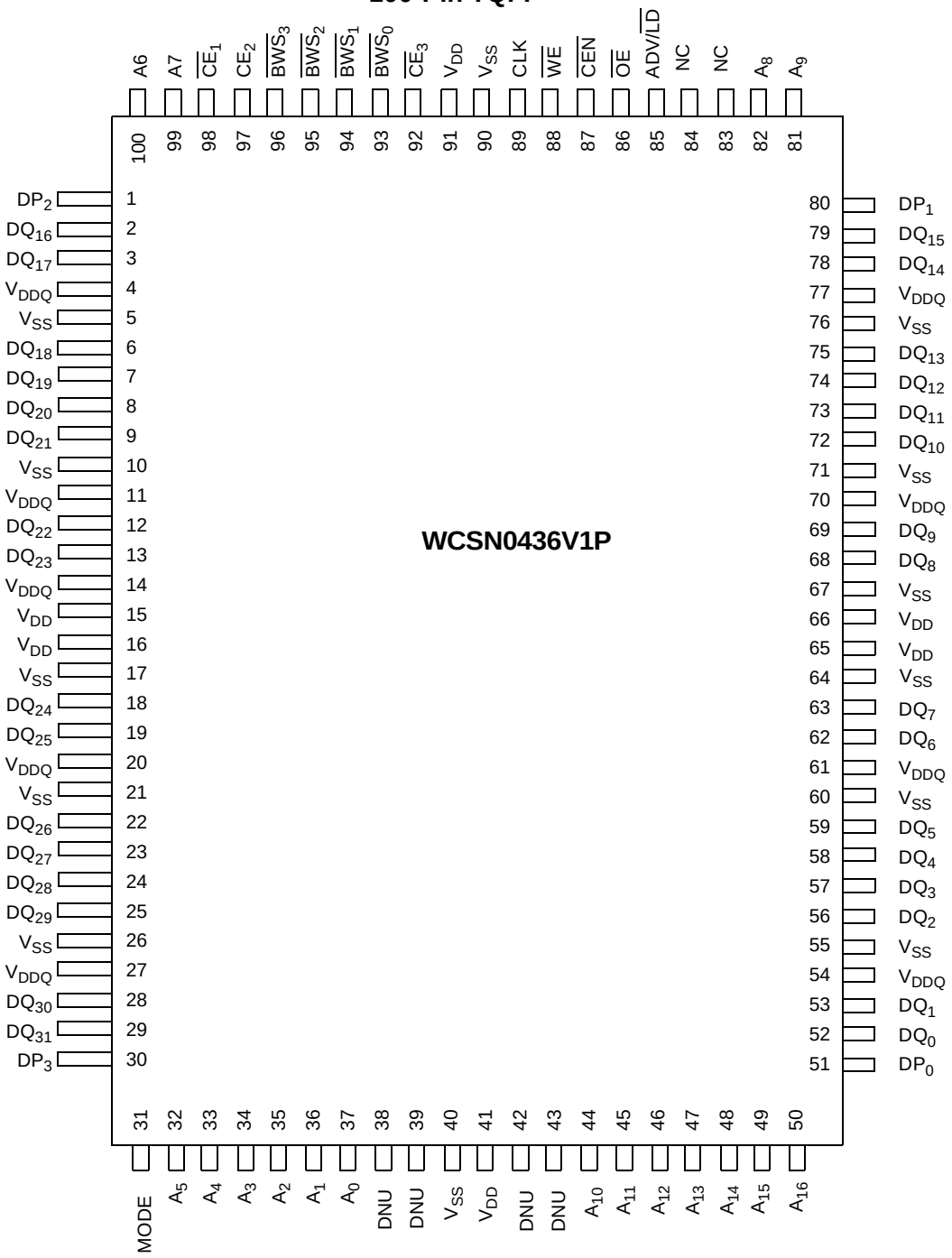


Selection Guide

		-166	-150	-143	-133	-100	-80
Maximum Access Time (ns)		3.5	3.8	4.0	4.2	5.0	7.0
Maximum Operating Current (mA)	Commercial	400	375	350	300	250	200
Maximum CMOS Standby Current (mA)	Commercial	5	5	5	5	5	5

Pin Configuration

100-Pin TQFP



Pin Definitions

Pin Number	Name	I/O	Description
50–44, 81–82, 99, 100, 32–37	$A_{[16:0]}$	Input-Synchronous	Address Inputs used to select one of the 131,072 address locations. Sampled at the rising edge of the CLK.
96–93	$\overline{BWS}_{[3:0]}$	Input-Synchronous	Byte Write Select Inputs, active LOW. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BWS}_0$ controls $DQ_{[7:0]}$ and DP_0, $\overline{BWS}_1$ controls $DQ_{[15:8]}$ and DP_1, BWS_2 controls $DQ_{[23:16]}$ and DP_2, $\overline{BWS}_3$ controls $DQ_{[31:24]}$ and DP_3. See Write Cycle Description table for details.
88	$\overline{WE}$	Input-Synchronous	Write Enable Input, active LOW. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
85	ADV/$\overline{LD}$	Input-Synchronous	Advance/Load Input used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address.
89	CLK	Input-Clock	Clock Input. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
98	$\overline{CE}_1$	Input-Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE_2, and $\overline{CE}_3$ to select/deselect the device.
97	CE_2	Input-Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
92	$\overline{CE}_3$	Input-Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
86	$\overline{OE}$	Input-Asynchronous	Output Enable, active LOW. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device has been deselected.
87	$\overline{CEN}$	Input-Synchronous	Clock Enable Input, active LOW. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the Clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
29–28, 25–22, 19–18, 13–12, 9–6, 3–2, 79–78, 75–72, 69–68, 63–62 59–56, 53–52	$DQ_{[31:0]}$	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[16:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, $DQ_{[31:0]}$ are placed in a three-state condition. The outputs are automatically three-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
30, 1, 80 51	$DP_{[3:0]}$	I/O-Synchronous	Bidirectional Data Parity I/O lines. Functionally, these signals are identical to $DQ_{[31:0]}$. During write sequences, DP_0 is controlled by $\overline{BWS}_0$, DP_1 is controlled by $\overline{BWS}_1$, DP_2 is controlled by $\overline{BWS}_2$, and DP_3 is controlled by $\overline{BWS}_3$.
31	MODE	Input Strap pin	Mode Input. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order.
15, 16, 41, 65, 66, 91	V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to 3.3V power supply.
4, 11, 14, 20, 27, 54, 61, 70, 77	V_{DDQ}	I/O Power Supply	Power supply for the I/O circuitry. Should be connected to a 3.3V power supply.

Pin Definitions (continued)

Pin Number	Name	I/O	Description
5, 10, 17, 21, 26, 40, 55, 60, 64, 67, 71, 76, 90	V_{SS}	Ground	Ground for the device. Should be connected to ground of the system.
83, 84	NC	-	No connects. Reserved for address inputs for depth expansion. Pin 83 and 84 will be used for 256K and 512K depths respectively.
38, 39, 42, 43	DNU	-	Do Not Use pins. These pins should be left floating or tied to V_{SS}.

Introduction

Functional Overview

The WCSN0436V1P is a synchronous-pipelined Burst SRAM designed specifically to eliminate wait states during Write/Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.5 ns (166-MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) active at the rising edge of the clock. If Clock Enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). $\overline{BWS}_{[3:0]}$ can be used to conduct byte write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, (3) the Write Enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs (A_0–A_{16}) is latched into the Address Register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 3.5 ns (166-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (Read/Write/Deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will three-state following the next clock rise.

Burst Read Accesses

The WCSN036V1p has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Access section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap-around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ will increment the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, and (3) the write signal $\overline{WE}$ is asserted LOW. The address presented to A_0–A_{16} is loaded into the Address Register. The write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically three-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on $DQ_{[31:0]}$ and $DP_{[3:0]}$. In addition, the address for the subsequent access (Read/Write/Deselect) is latched into the Address Register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to $DQ_{[31:0]}$ and $DP_{[3:0]}$ (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the Write operation is controlled by $\overline{BWS}_{[3:0]}$ signals. The WCSN0436V1P provides byte write capability that is described in the Write Cycle Description table. Asserting the Write Enable input ($\overline{WE}$) with the selected Byte Write Select ($\overline{BWS}_{[3:0]}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the WCSN0436V1P is a common I/O device, data should not be driven into the device while the outputs are active. The Output Enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the $DQ_{[31:0]}$ and $DP_{[3:0]}$ inputs. Doing so will three-state the output drivers. As a safety precaution, $DQ_{[31:0]}$

and $DP_{[3:0]}$ are automatically three-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The WCSN0436V1p has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four WRITE operations without reasserting the address inputs. ADV/LD must be driven LOW in order to load the initial address, as described in the Single Write Access section above. When ADV/LD is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BWS}_{[3:0]}$ inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
Ax+1, Ax	Ax+1, Ax	Ax+1, Ax	Ax+1, Ax
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
Ax+1, Ax	Ax+1, Ax	Ax+1, Ax	Ax+1, Ax
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Cycle Description Truth Table[1, 2, 3, 4, 5, 6]

Operation	Address Used	$\overline{CE}$	$\overline{CEN}$	ADV/ LD/	$\overline{WE}$	$\overline{BWS_X}$	CLK	Comments
Deselected	External	1	0	L	X	X	L-H	I/Os three-state following next recognized clock.
Suspend	-	X	1	X	X	X	L-H	Clock ignored, all operations suspended.
Begin Read	External	0	0	0	1	X	L-H	Address latched.
Begin Write	External	0	0	0	0	Valid	L-H	Address latched, data presented two valid clocks later.
Burst Read Operation	Internal	X	0	1	X	X	L-H	Burst Read operation. Previous access was a Read operation. Addresses incremented internally in conjunction with the state of MODE.
Burst Write Operation	Internal	X	0	1	X	Valid	L-H	Burst Write operation. Previous access was a Write operation. Addresses incremented internally in conjunction with the state of MODE. Bytes written are determined by $\overline{BWS}_{[3:0]}$.

Notes:

1. X="Don't Care", 1=Logic HIGH, 0=Logic LOW, $\overline{CE}$ stands for ALL Chip Enables active. $\overline{BWS_X}$ = 0 signifies at least one Byte Write Select is active, $\overline{BWS_X}$ = Valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
2. Write is defined by $\overline{WE}$ and $\overline{BWS}_{[3:0]}$. See Write Cycle Description table for details.
3. The DQ and DP pins are controlled by the current cycle and the $\overline{OE}$ signal.
4. CEN=1 inserts wait states.
5. Device will power-up deselected and the I/Os in a three-state condition, regardless of $\overline{OE}$.
6. OE assumed LOW.

Write Cycle Description[7, 8]

Function	$\overline{WE}$	$\overline{BWS_3}$	$\overline{BWS_2}$	$\overline{BWS_1}$	$\overline{BWS_0}$
Read	1	X	X	X	X
Write – No bytes written	0	1	1	1	1
Write Byte 0 – ($DQ_{[7:0]}$ and DP_0)	0	1	1	1	0
Write Byte 1 – ($DQ_{[15:8]}$ and DP_1)	0	1	1	0	1
Write Bytes 1, 0	0	1	1	0	0
Write Byte 2 – ($DQ_{[23:16]}$ and DP_2)	0	1	0	1	1
Write Bytes 2, 0	0	1	0	1	0
Write Bytes 2, 1	0	1	0	0	1
Write Bytes 2, 1, 0	0	1	0	0	0
Write Byte 3 – ($DQ_{[31:24]}$ and DP_3)	0	0	1	1	1
Write Bytes 3, 0	0	0	1	1	0
Write Bytes 3, 1	0	0	1	0	1
Write Bytes 3, 1, 0	0	0	1	0	0
Write Bytes 3, 2	0	0	0	1	1
Write Bytes 3, 2, 0	0	0	0	1	0
Write Bytes 3, 2, 1	0	0	0	0	1
Write All Bytes	0	0	0	0	0

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND.....–0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[9] .....–0.5V to V_{DDQ} + 0.5V

DC Input Voltage[9].....–0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature[10]	V_{DD}/V_{DDQ}
Com'l	0°C to +70°C	3.3V ± 5%
Ind'l	–40°C to +85°C	

Notes:

7. X="Don't Care", 1=Logic HIGH, 0=Logic LOW.
8. Write is initiated by the combination of WE and $\overline{BWS_x}$. Bytes written are determined by $\overline{BWS}_{[3:0]}$. Bytes not selected during byte writes remain unaltered. All I/Os are three-stated during byte writes.
9. Minimum voltage equals –2.0V for pulse duration less than 20 ns.
10. T_A is the case temperature.

Electrical Characteristics Over the Operating Range

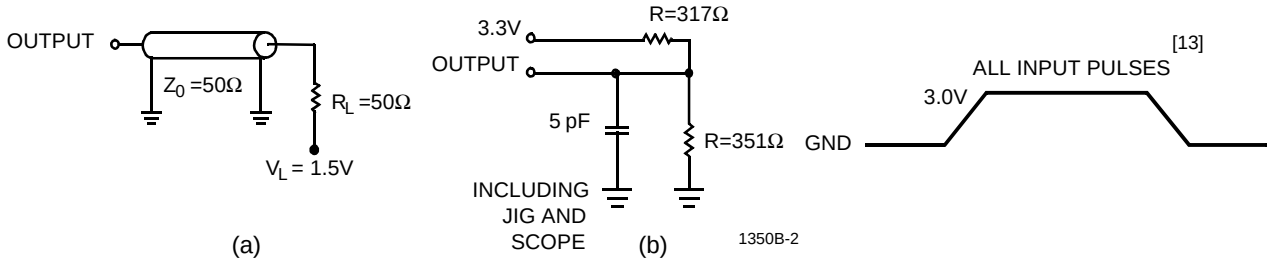
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.465	V
V_{DDQ}	I/O Supply Voltage			3.135	3.465	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA[11]		2.4		V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA[11]			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[9]			–0.3	0.8	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE			–30	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{CC}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	5.0-ns cycle, 166 MHz		400	mA
			6.6-ns cycle, 150 MHz		375	mA
			7.0-ns cycle, 143 MHz		350	mA
			7.5-ns cycle, 133 MHz		300	mA
			10.0-ns cycle, 100 MHz		250	mA
			12.5-ns cycle, 80 MHz		200	mA
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = 1/t_{CYC}	5.0-ns cycle, 166 MHz		80	mA
			6.6-ns cycle, 150 MHz		70	mA
			7.0-ns cycle, 143 MHz		60	mA
			7.5-ns cycle, 133 MHz		50	mA
			10.0-ns cycle, 100 MHz		40	mA
			12.5-ns cycle, 80 MHz		35	mA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	All speed grades		5	mA
I_{SB3}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V f = f_{MAX} = 1/t_{CYC}	5.0-ns cycle, 166 MHz		70	mA
			6.6-ns cycle, 150 MHz		60	mA
			7.0-ns cycle, 143 MHz		50	mA
			7.5-ns cycle, 133 MHz		40	mA
			10.0-ns cycle, 100 MHz		30	mA
			12.5-ns cycle, 80 MHz		25	mA

Note:
11. The load used for V_{OH} and V_{OL} testing is shown in Figure (b) of the AC Test Loads.

Capacitance[12]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V, V_{DDQ} = 3.3V	4	pF
C_{CLK}	Clock Input Capacitance		4	pF
$C_{I/O}$	Input/Output Capacitance		4	pF

AC Test Loads and Waveforms



Thermal Resistance

Description	Test Conditions	Symbol	TQFP Typ.	Units	Notes
Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ_{JA}	28	°C/W	12
Thermal Resistance (Junction to Case)		Θ_{JC}	4	°C/W	12

Notes:

12. Tested initially and after any design or process change that may affect these parameters.
13. A/C test conditions assume signal transition time of 2 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading shown in part (a) of AC Test Loads.

Switching Characteristics Over the Operating Range[13, 14, 15]

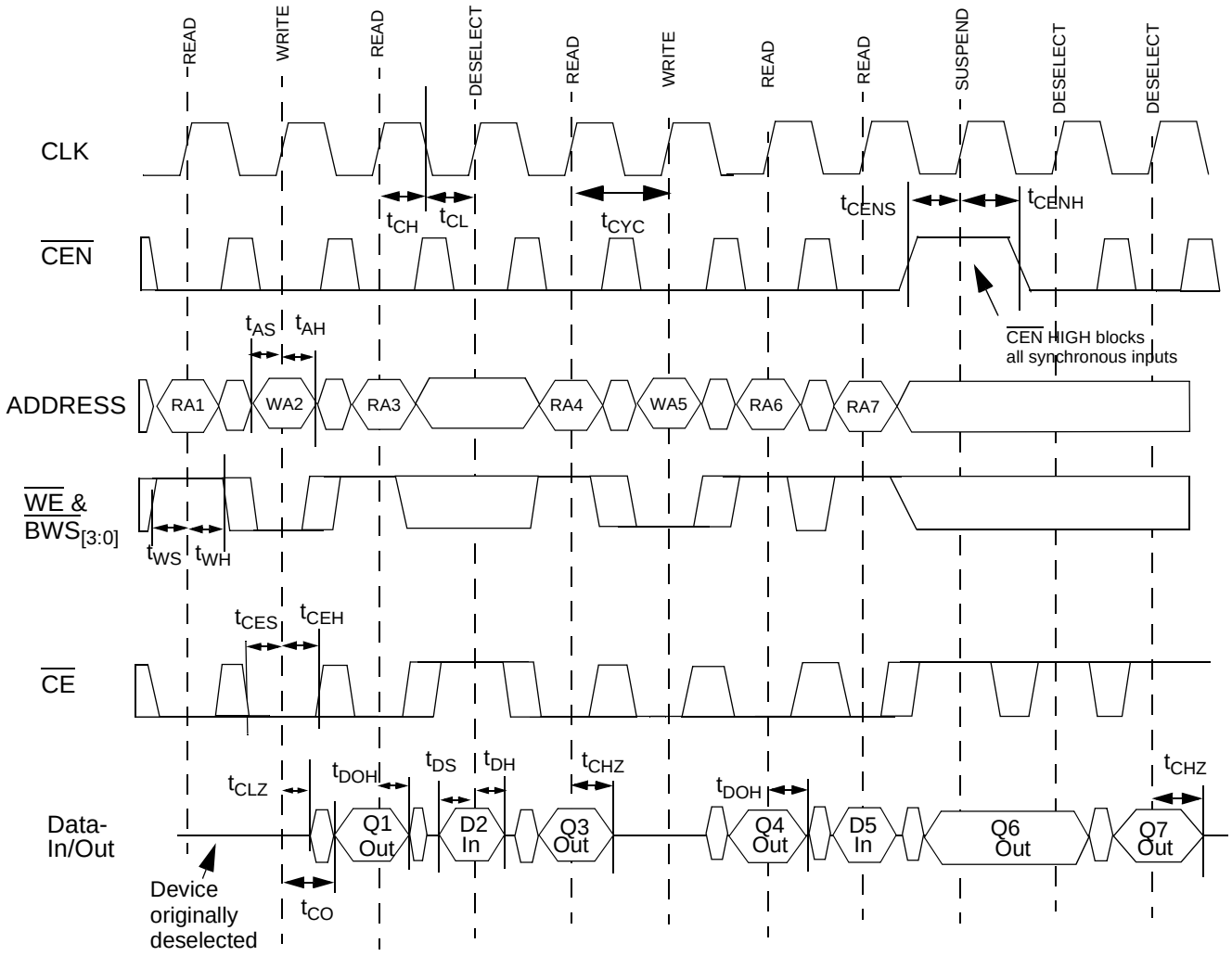
Parameter	Description	-166		-150		-143		-133		-100		-80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	5.0		6.6		7.0		7.5		10		12.5		ns
t_{CH}	Clock HIGH	1.4		2.5		2.8		3.0		4.0		4.0		ns
t_{CL}	Clock LOW	1.4		2.5		2.8		3.0		4.0		4.0		ns
t_{AS}	Address Set-Up Before CLK Rise	1.5		1.5		2.0		2.0		2.2		2.5		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		0.5		0.5		1.0		ns
t_{CO}	Data Output Valid After CLK Rise		3.5		3.8		4.0		4.2		5.0		7.0	ns
t_{DOH}	Data Output Hold After CLK Rise	1.5				1.5		1.5		1.5		1.5		ns
t_{CENS}	$\overline{CEN}$ Set-Up Before CLK Rise	1.5		1.5		2.0		2.0		2.2		2.5		ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.5		0.5		0.5		0.5		0.5		1.0		ns
t_{WES}	$\overline{GW}$, $\overline{BWS}_{[3:0]}$ Set-Up Before CLK Rise	1.5		1.5		2.0		2.0		2.2		2.5		ns
t_{WEH}	$\overline{GW}$, $\overline{BWS}_{[3:0]}$ Hold After CLK Rise	0.5		0.5		0.5		0.5		0.5		1.0		ns
t_{ALS}	ADV/$\overline{LD}$ Set-Up Before CLK Rise	1.5		1.5		2.0		2.0		2.2		2.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.5		0.5		0.5		0.5		0.5		1.0		ns
t_{DS}	Data Input Set-Up Before CLK Rise	1.5		1.5		1.7		1.7		2.0		2.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		0.5		0.5		1.0		ns
t_{CES}	Chip Enable Set-Up Before CLK Rise	1.5		1.5		2.0		2.0		2.2		2.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		0.5		0.5		0.5		1.0		ns
t_{CHZ}	Clock to High-Z[12, 14, 15, 16]	1.5	3.2	1.5	3.2	1.5	3.5	1.5	3.5	1.5	3.5	1.5	5.0	ns
t_{CLZ}	Clock to Low-Z[12, 14, 15, 16]	1.5		1.5		1.5		1.5		1.5		1.5		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[12, 14, 15, 16]		3.0		3.0		4.0		4.2		5.0		7.0	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[12, 14, 15, 16]	0.0		0		0		0		0		0		ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[14]		3.2		3.5		4.0		4.2		5.0		7.0	ns

Notes:

14. t_{CHZ}, t_{CLZ}, t_{OEV}, t_{EOLZ}, and t_{EOHZ} are specified with A/C test conditions shown in part (a) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
15. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
16. This parameter is sampled and not 100% tested.

Switching Waveforms

READ/WRITE/DESELECT Sequence

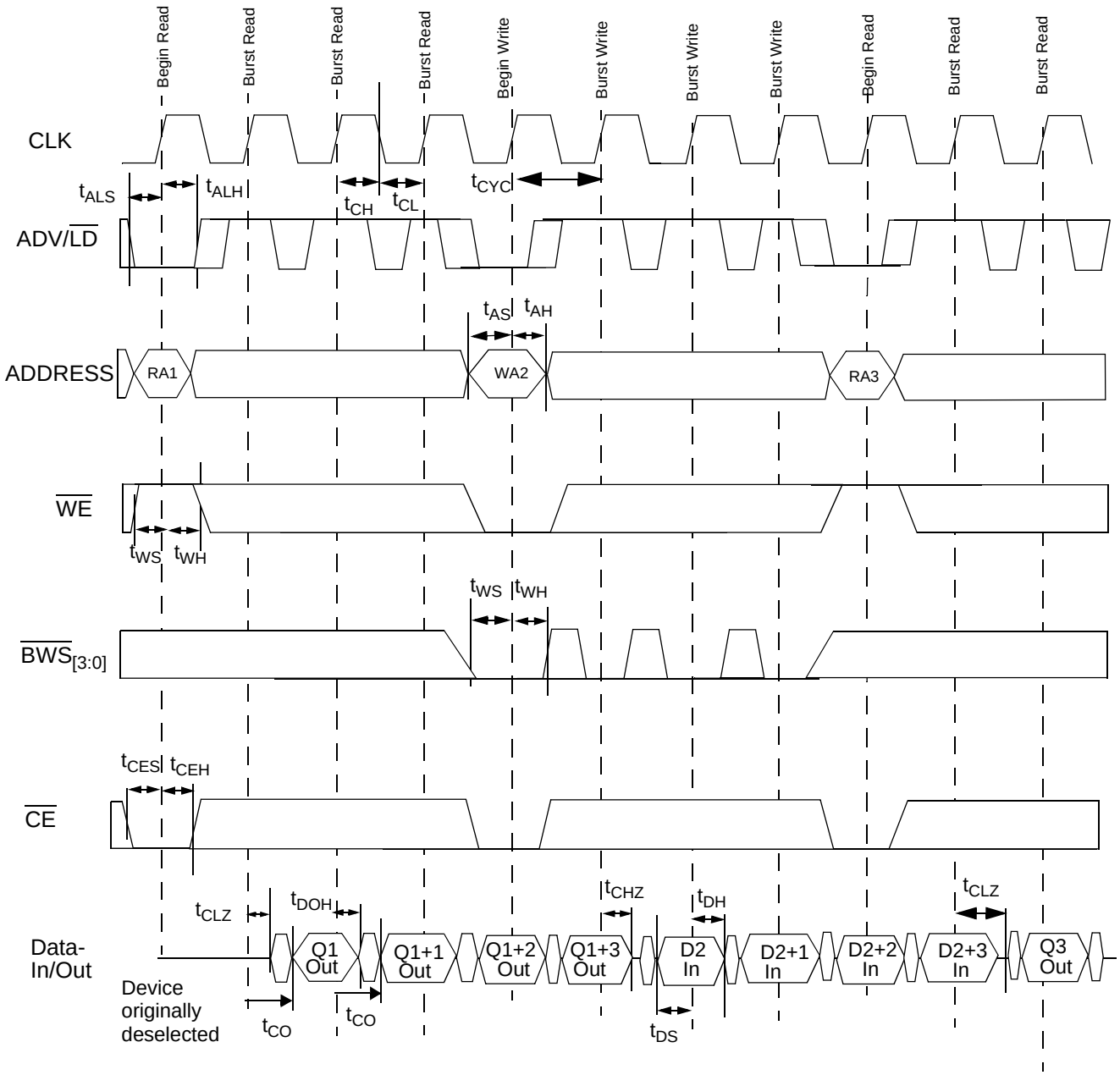


The combination of $\overline{WE}$ & $\overline{BWS}_{[3:0]}$ define a write cycle (see Write Cycle Description table). $\overline{CE}$ is the combination of $\overline{CE}_1$, CE_2, and $\overline{CE}_3$. All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WAx stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. ADV/$\overline{LD}$ held LOW. $\overline{OE}$ held LOW.

= DON'T CARE = UNDEFINED

Switching Waveforms (continued)

Burst Sequences

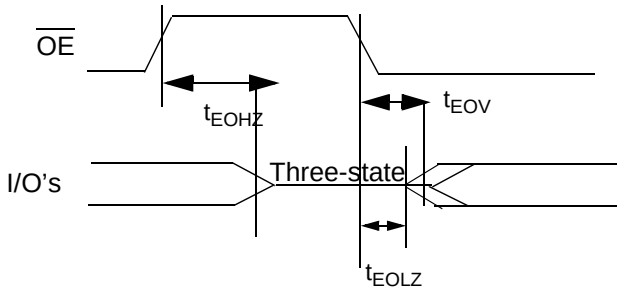


The combination of $\overline{WE}$ & $\overline{BWS}_{[3:0]}$ define a write cycle (see Write Cycle Description table). $\overline{CE}$ is the combination of $\overline{CE}_1$, CE_2, and $\overline{CE}_3$. All chip enables need to be active in order to select the device. Any chip enable can deselect the device. RAx stands for Read Address X, WA stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. $\overline{CEN}$ held LOW. During burst writes, byte writes can be conducted by asserting the appropriate $\overline{BWS}_{[3:0]}$ input signals. Burst order determined by the state of the MODE input. $\overline{CEN}$ held LOW. $\overline{OE}$ held LOW.

☐ = DON'T CARE ☐ = UNDEFINED

Switching Waveforms (continued)

$\overline{OE}$ Timing

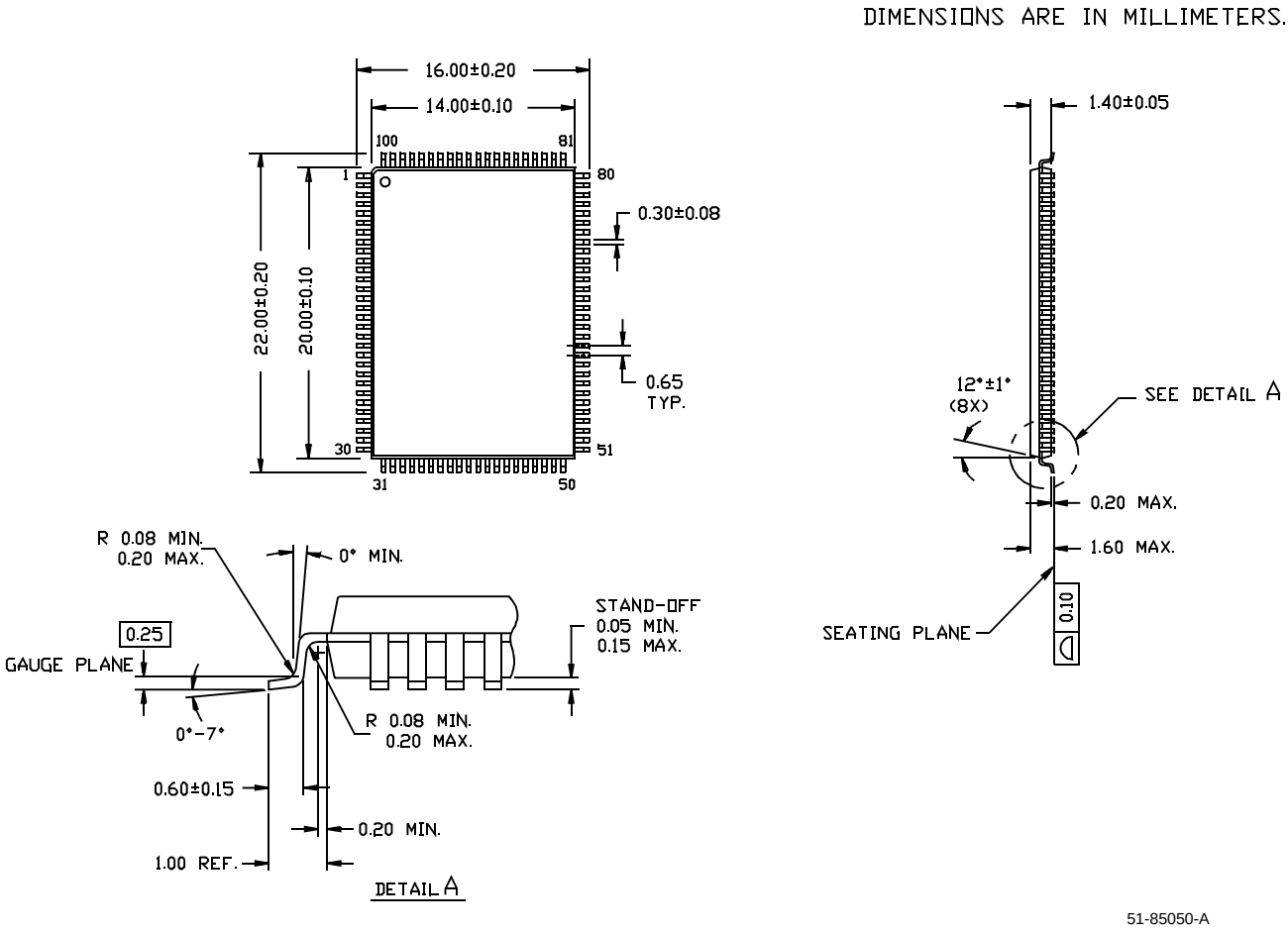


Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
166	WCSN0436V1P-166AC	A101	100-Lead (14 x 20 x 1.4 mm) Thin Quad Flat Pack	Commercial
150	WCSN0436V1P-150AC	A101	100-Lead (14 x 20 x 1.4 mm) Thin Quad Flat Pack	Commercial
143	WCSN0436V1P-143AC	A101	100-Lead (14 x 20 x 1.4 mm) Thin Quad Flat Pack	Commercial
133	WCSN0436V1P-133AC	A101	100-Lead (14 x 20 x 1.4 mm) Thin Quad Flat Pack	Commercial
	WCSN0436V1P-133AI	A101	100-Lead (14 x 20 x 1.4 mm) Thin Quad Flat Pack	Industrial
100	WCSN0436V1P-100AC	A101	100-Lead (14 x 20 x 1.4 mm) Thin Quad Flat Pack	Commercial
	WCSN0436V1P-100AI	A101	100-Lead (14 x 20 x 1.4 mm) Thin Quad Flat Pack	Industrial

Package Diagram

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



Document Title: WCSN0436V1P 128K x 36 Pipelined SRAM with NoBL™ Architecture Document Number: 38-05246				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109953	01/07/02	SZV	Change from Spec number: 38-00910 to 38-05045
New	113259	02/03/02	GLC	Change from Spec number: 38-05045 to 38-05246

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Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А