

NCV8703

300 mA, Ultra-Low Quiescent Current, I_Q 12 μ A, Ultra-Low Noise, LDO Voltage Regulator

The NCV8703 is a low noise, low power consumption and low dropout Linear Voltage Regulator. With its excellent noise and PSRR specifications, the device is ideal for use in products utilizing RF receivers, imaging sensors, audio processors or any component requiring an extremely clean power supply. The NCV8703 uses an innovative Adaptive Ground Current circuit to ensure ultra low ground current during light load conditions.

Features

- Operating Input Voltage Range: 2.0 V to 5.5 V
- Available in Fixed Voltage Options: 0.8 to 3.5 V
Contact Factory for Other Voltage Options
- Ultra-Low Quiescent Current of Typ. 12 μ A
- Ultra-Low Noise: 13 μ V_{RMS} from 100 Hz to 100 kHz
- Very Low Dropout: 180 mV Typical at 300 mA
- $\pm 2\%$ Accuracy Over Load/Line/Temperature
- High PSRR: 68 dB at 1 kHz
- Internal Soft-Start to Limit the Turn-On Inrush Current
- Thermal Shutdown and Current Limit Protections
- Stable with a 1 μ F Ceramic Output Capacitor
- Available in TSOP-5 and XDFN 1.5 x 1.5 mm Package
- Active Output Discharge for Fast Turn-Off
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

Typical Applications

- Satellite Radio Receivers, GPS
- Rear View Camera, Electronic Mirrors, Lane Change Detectors
- Portable Entertainment Systems
- Other Battery Powered Applications

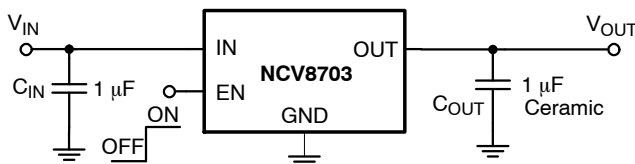
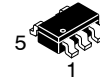


Figure 1. Typical Application Schematic



ON Semiconductor®

<http://onsemi.com>

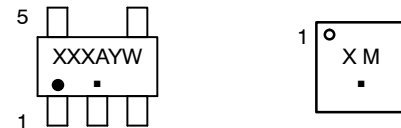


TSOP-5
SN SUFFIX
CASE 483



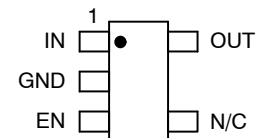
XDFN6
MX SUFFIX
CASE 711AE

MARKING DIAGRAMS

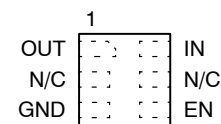


X, XXX = Specific Device Code
M = Date Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

PIN CONNECTIONS



5-Pin TSOP-5
(Top View)



6-Pin XDFN 1.5 x 1.5 mm
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

NCV8703

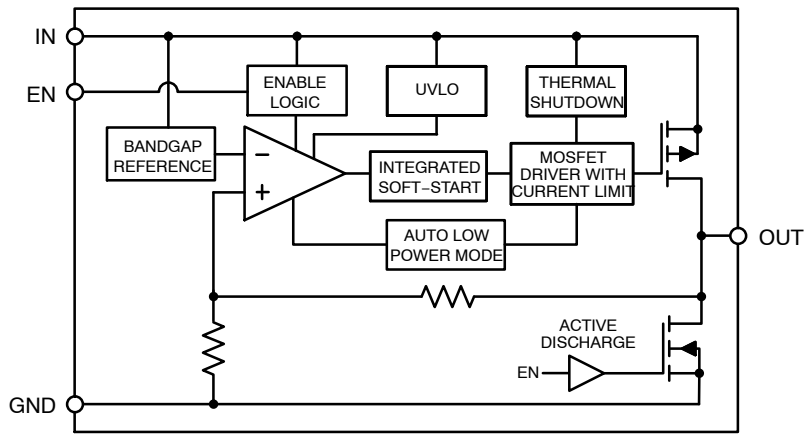


Figure 2. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

| Pin No. XDFN6 | Pin No. TSOP-5 | Pin Name | Description |
|---------------|----------------|----------|---|
| 1 | 5 | OUT | Regulated output voltage pin. A small 1 μ F ceramic capacitor is needed from this pin to ground to assure stability. |
| 2 | 4 | N/C | Not connected. |
| 3 | 2 | GND | Power supply ground. Connected to the die through the lead frame. Soldered to the copper plane allows for effective heat dissipation. |
| 4 | 3 | EN | Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode. |
| 5 | | N/C | Not connected. This pin can be tied to ground to improve thermal dissipation. |
| 6 | 1 | IN | Input pin. A small capacitor is needed from this pin to ground to assure stability. |

Table 2. ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|--------------|----------------------------|--------------|
| Input Voltage (Note 1) | V_{IN} | -0.3 V to 6 V | V |
| Output Voltage | V_{OUT} | -0.3 V to $V_{IN} + 0.3$ V | V |
| Enable Input | V_{EN} | -0.3 V to $V_{IN} + 0.3$ V | V |
| Output Short Circuit Duration | t_{SC} | Indefinite | s |
| Maximum Junction Temperature | $T_{J(MAX)}$ | 125 | $^{\circ}$ C |
| Storage Temperature | T_{STG} | -55 to 150 | $^{\circ}$ C |
| ESD Capability, Human Body Model (Note 2) | ESD_{HBM} | 2000 | V |
| ESD Capability, Machine Model (Note 2) | ESD_{MM} | 200 | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
 ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)
 Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS (Note 3)

| Rating | Symbol | Value | Unit |
|---|------------------------------|------------|-----------------------------|
| Thermal Characteristics, TSOP-5, Thermal Resistance, Junction-to-Air Thermal Characterization Parameter, Junction-to-Lead (Pin 2) | θ_{JA} ψ_{JL} | 241 129 | $^{\circ}\text{C}/\text{W}$ |
| Thermal Characteristics, XDFN6 1.5 x 1.5 mm Thermal Resistance, Junction-to-Air Thermal Characterization Parameter, Junction-to-Board | θ_{JA} ψ_{JB} | 146 77 | $^{\circ}\text{C}/\text{W}$ |

3. Single component mounted on 1 oz, FR4 PCB with 645 mm² Cu area.

Table 4. ELECTRICAL CHARACTERISTICS

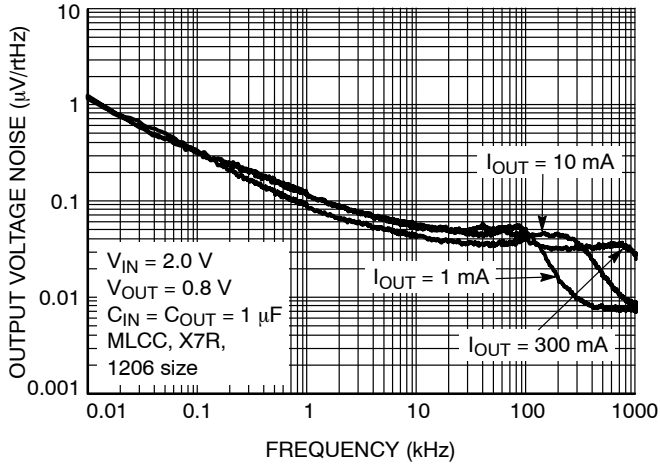
-40°C ≤ T_J ≤ 125°C; V_{IN} = V_{OUT(NOM)} + 0.5 V or 2.0 V, whichever is greater; V_{EN} = 0.9 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 μF unless otherwise noted. Typical values are at T_J = +25°C. (Note 4)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|------------------------------|---|----------------------|------------|---------------|-----|--------------------|
| Operating Input Voltage | | V _{IN} | 2.0 | | 5.5 | V |
| Undervoltage Lock-out | V _{IN} rising | UVLO | 1.2 | 1.6 | 1.9 | V |
| Output Voltage Accuracy | V _{OUT} + 0.5 V ≤ V _{IN} ≤ 5.5 V, I _{OUT} = 0 - 300 mA | V _{OUT} | -2 | | +2 | % |
| Line Regulation | V _{OUT} + 0.5 V ≤ V _{IN} ≤ 4.5 V, I _{OUT} = 10 mA | Reg _{LINE} | | 450 | | μV/V |
| | V _{OUT} + 0.5 V ≤ V _{IN} ≤ 5.5 V, I _{OUT} = 10 mA | Reg _{LINE} | | 600 | | μV/V |
| Load Regulation | I _{OUT} = 0 mA to 300 mA | Reg _{LOAD} | | 20 | | μV/mA |
| Load Transient | I _{OUT} = 1 mA to 300 mA or 300 mA to 1 mA in 1 μs, C _{OUT} = 1 μF | Tran _{LOAD} | | -100/ +150 | | mV |
| Dropout Voltage (Note 5) | I _{OUT} = 300 mA, V _{OUT(nom)} = 2.5 V | V _{DO} | | 180 | 300 | mV |
| Output Current Limit | V _{OUT} = 90% V _{OUT(nom)} | I _{CL} | 310 | 450 | 750 | mA |
| Quiescent Current | I _{OUT} = 0 mA | I _Q | | 12 | 20 | μA |
| Ground Current | I _{OUT} = 300 mA | I _{GND} | | 200 | | μA |
| Shutdown Current | V _{EN} ≤ 0.4 V, T _J = +25°C | I _{DIS} | | 0.12 | | μA |
| | V _{EN} ≤ 0 V, V _{IN} = 2.0 to 4.5 V, T _J = -40 to +85°C | I _{DIS} | | 0.55 | 2 | μA |
| EN Pin Threshold Voltage | | | | | | V |
| High Threshold | V _{EN} Voltage increasing | V _{EN_HI} | 0.9 | | | |
| Low Threshold | V _{EN} Voltage decreasing | V _{EN_LO} | | | 0.4 | |
| EN Pin Input Current | V _{EN} = 5.5 V | I _{EN} | | 100 | 500 | nA |
| Turn-On Time | C _{OUT} = 1.0 μF, from assertion EN pin to 98% V _{OUT(nom)} | t _{ON} | | 200 | | μs |
| Power Supply Rejection Ratio | V _{IN} = 3 V, V _{OUT} = 2.5 V I _{OUT} = 300 mA | PSRR | f = 100 Hz | 70 | | dB |
| | | | f = 1 kHz | 68 | | |
| | | | f = 10 kHz | 53 | | |
| Output Noise Voltage | V _{OUT} = 2.5 V, V _{IN} = 3 V, I _{OUT} = 300 mA f = 100 Hz to 100 kHz | V _N | | 13 | | μV _{rms} |
| Thermal Shutdown Temperature | Temperature increasing from T _J = +25°C | T _{SD} | | 160 | | $^{\circ}\text{C}$ |
| Thermal Shutdown Hysteresis | Temperature falling from T _{SD} | T _{SDH} | - | 20 | - | $^{\circ}\text{C}$ |

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

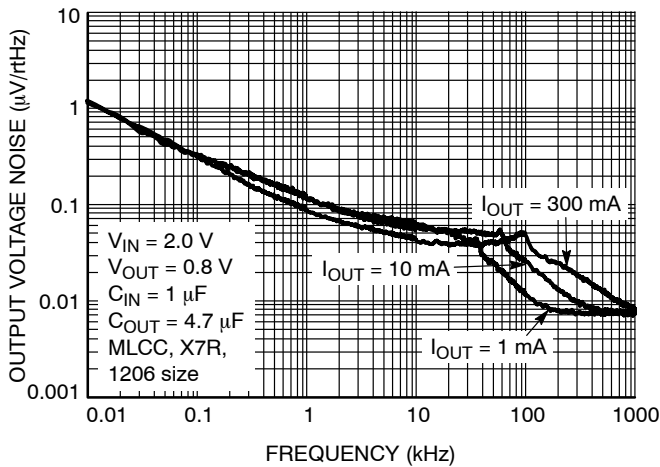
5. Characterized when V_{OUT} falls 100 mV below the regulated voltage at V_{IN} = V_{OUT(NOM)} + 0.5 V.

TYPICAL CHARACTERISTICS



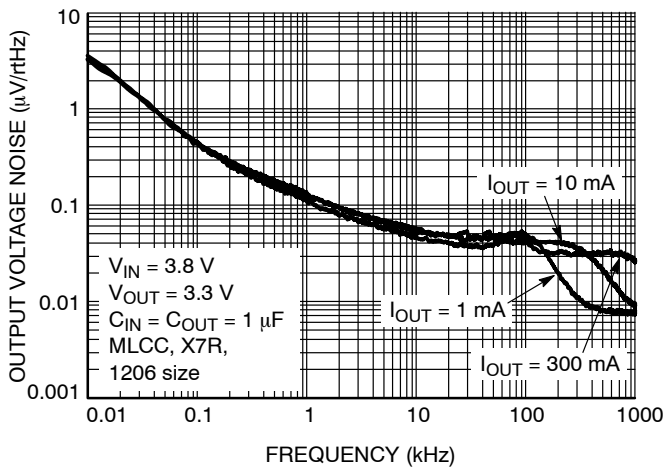
| I _{OUT} | RMS Output Noise (μV _{RMS}) | |
|------------------|---------------------------------------|------------------|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 18.45 | 17.77 |
| 10 mA | 17.18 | 16.43 |
| 300 mA | 14.14 | 13.11 |

Figure 3. Output Voltage Noise Spectral Density for V_{OUT} = 0.8 V, C_{OUT} = 1 μF



| I _{OUT} | RMS Output Noise (μV _{RMS}) | |
|------------------|---------------------------------------|------------------|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 14.07 | 13.14 |
| 10 mA | 16.59 | 15.83 |
| 300 mA | 15.46 | 14.53 |

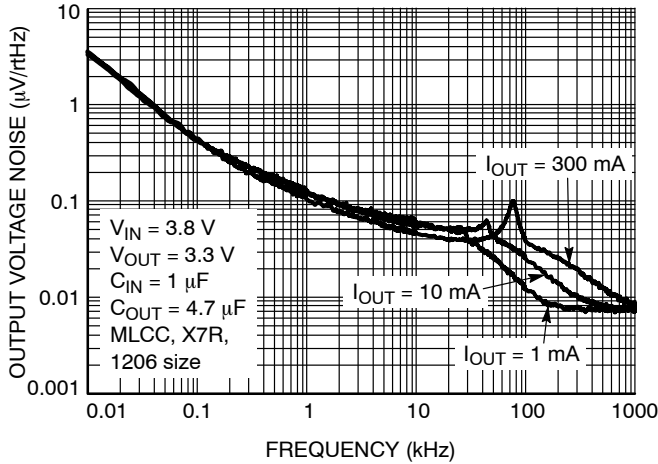
Figure 4. Output Voltage Noise Spectral Density for V_{OUT} = 0.8 V, C_{OUT} = 4.7 μF



| I _{OUT} | RMS Output Noise (μV _{RMS}) | |
|------------------|---------------------------------------|------------------|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 20.29 | 17.06 |
| 10 mA | 19.76 | 16.11 |
| 300 mA | 18.74 | 15.46 |

Figure 5. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 1 μF

TYPICAL CHARACTERISTICS



| I _{OUT} | RMS Output Noise (µV _{RMS}) | |
|------------------|---------------------------------------|------------------|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 17.64 | 13.52 |
| 10 mA | 19.54 | 15.96 |
| 300 mA | 21.50 | 18.71 |

Figure 6. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 4.7 µF

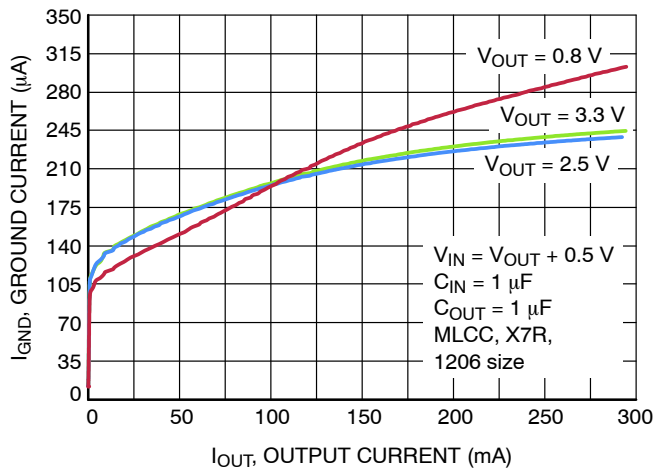


Figure 7. Ground Current vs. Output Current

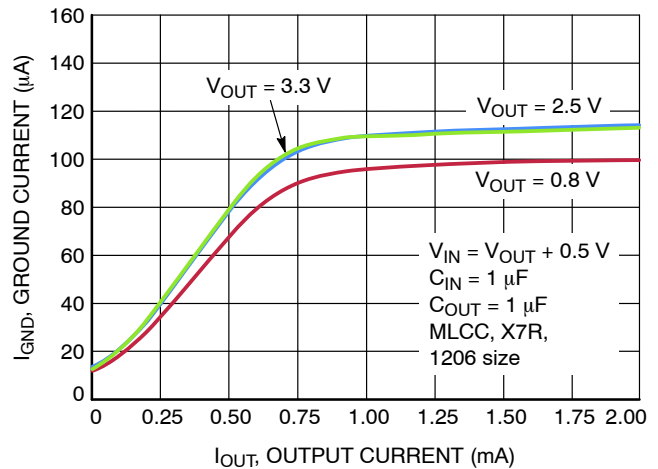


Figure 8. Ground Current vs. Output Current from 0 mA to 2 mA

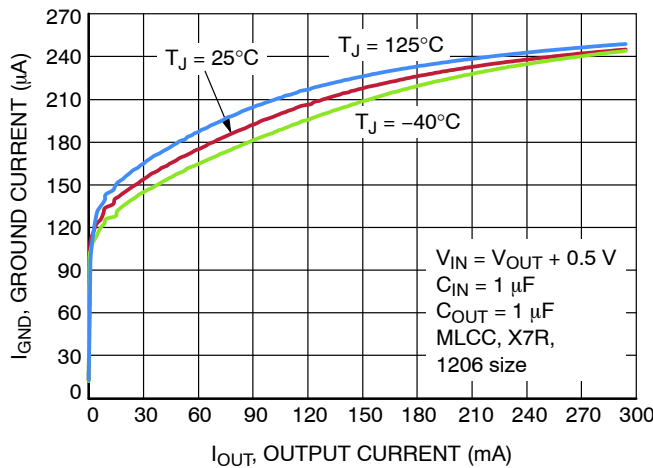


Figure 9. Ground Current vs. Output Current at Temperatures

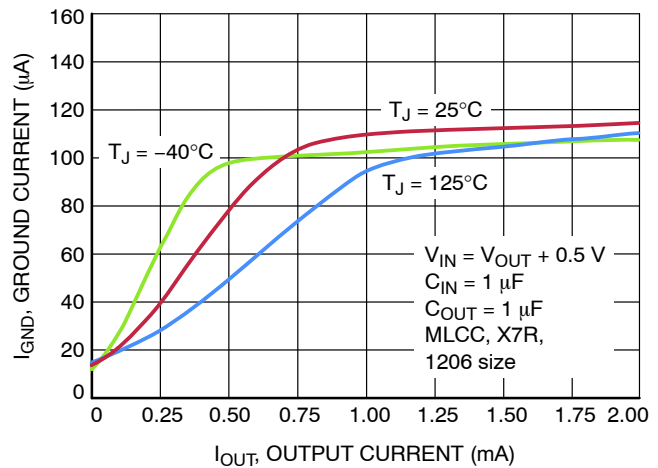


Figure 10. Ground Current vs. Output Current 0 mA to 2 mA at Temperatures

TYPICAL CHARACTERISTICS

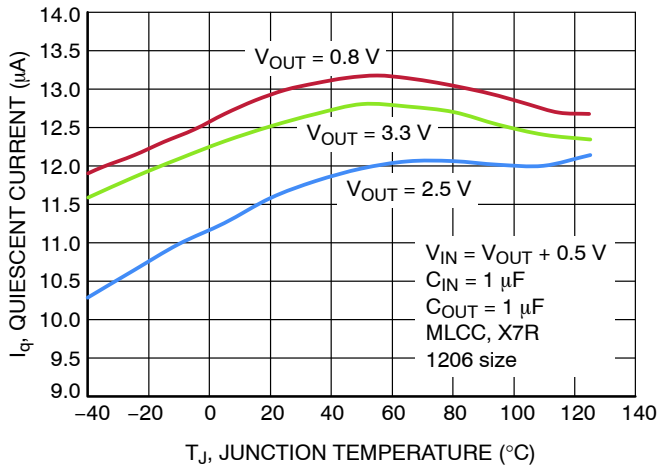


Figure 11. Quiescent Current vs. Temperature

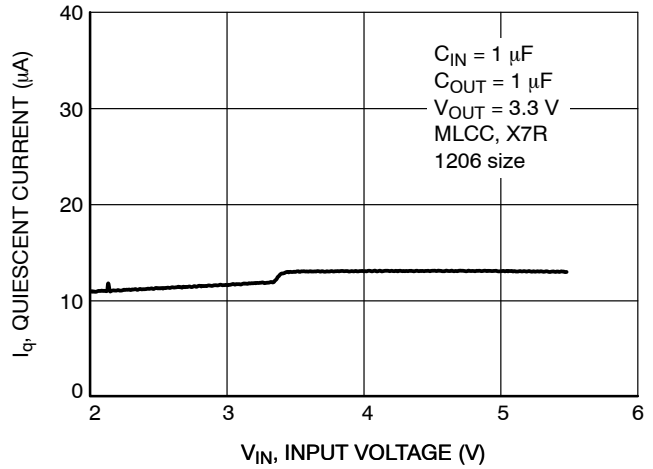


Figure 12. Quiescent Current vs. Input Voltage

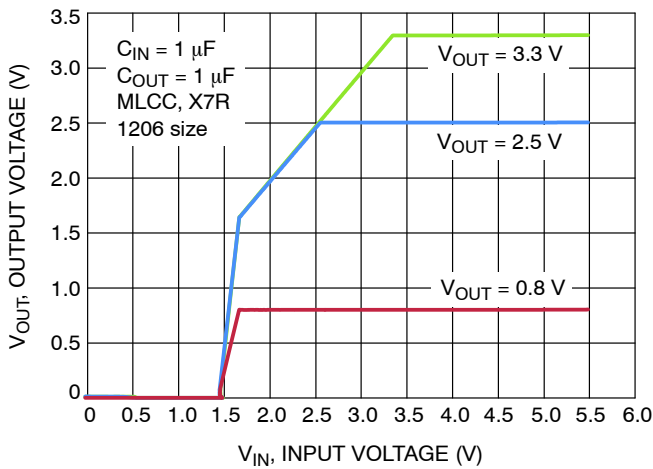


Figure 13. Output Voltage vs. Input Voltage

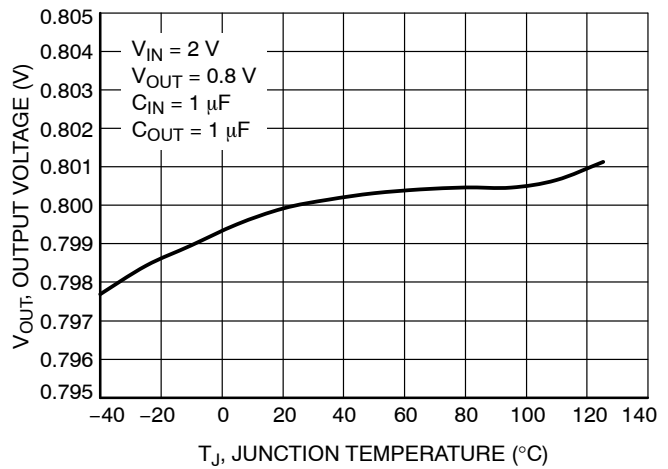


Figure 14. Output Voltage vs. Temperature – 0.8 V

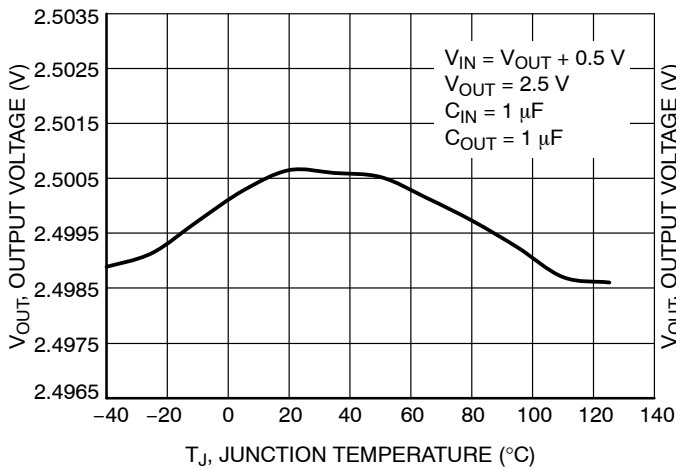


Figure 15. Output Voltage vs. Temperature – 2.5 V

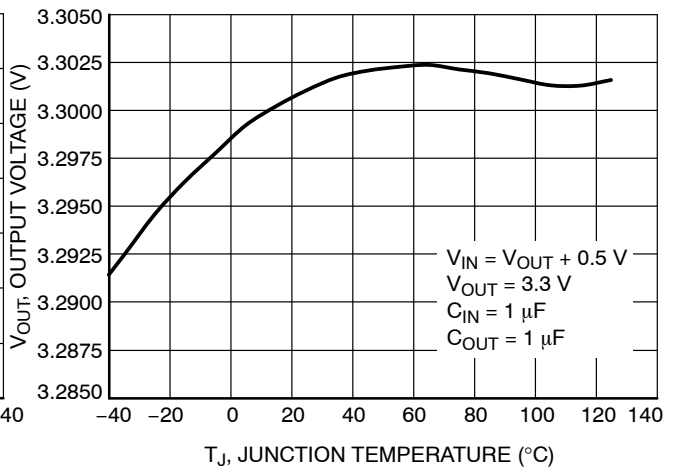


Figure 16. Output Voltage vs. Temperature – 3.3 V

TYPICAL CHARACTERISTICS

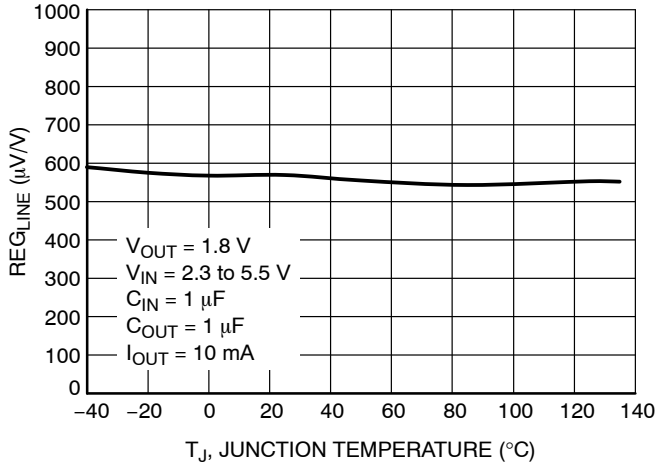


Figure 17. Line Regulation vs. Temperature – 1.8 V

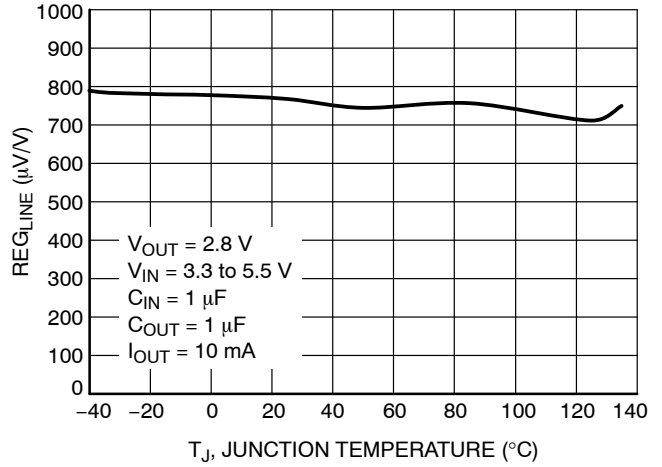


Figure 18. Line Regulation vs. Temperature – 2.8 V

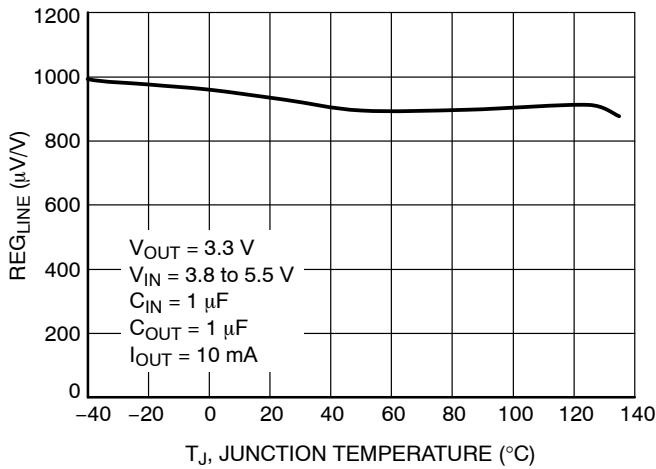


Figure 19. Line Regulation vs. Temperature – 3.3 V

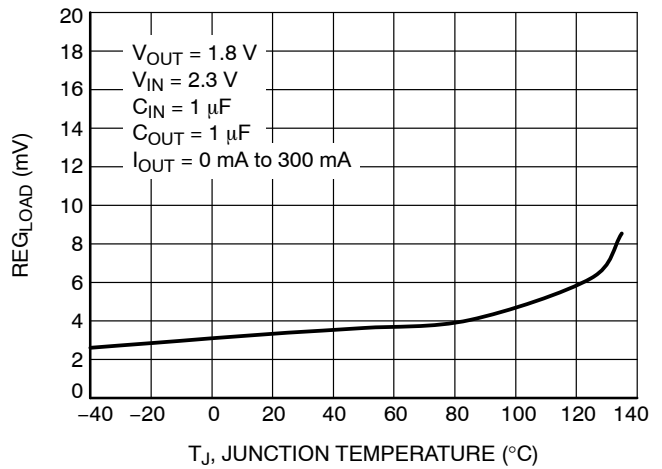


Figure 20. Load Regulation vs. Temperature – 1.8 V

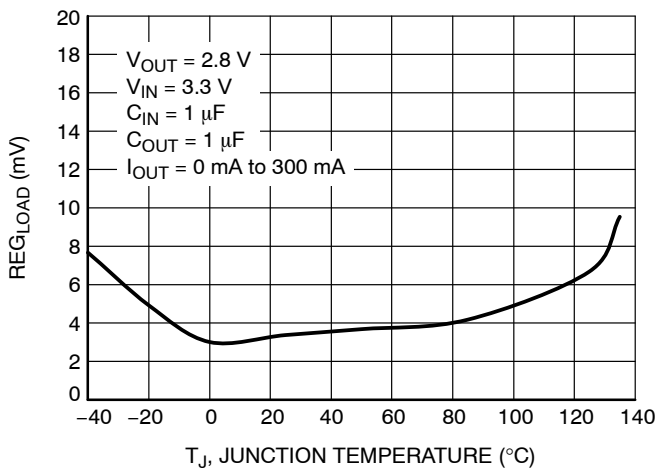


Figure 21. Load Regulation vs. Temperature – 2.8 V

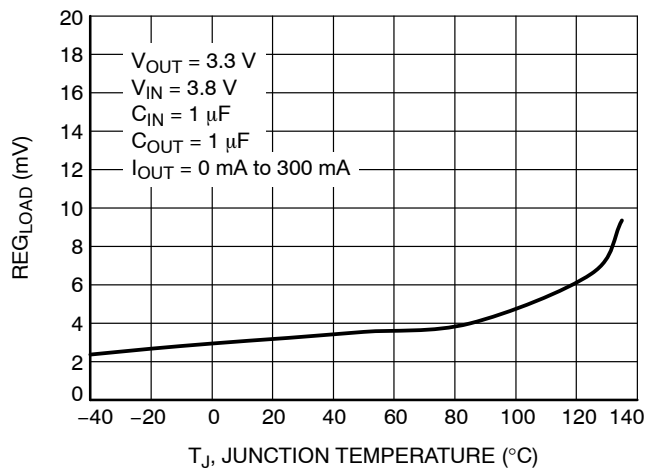


Figure 22. Load Regulation vs. Temperature – 3.3 V

TYPICAL CHARACTERISTICS

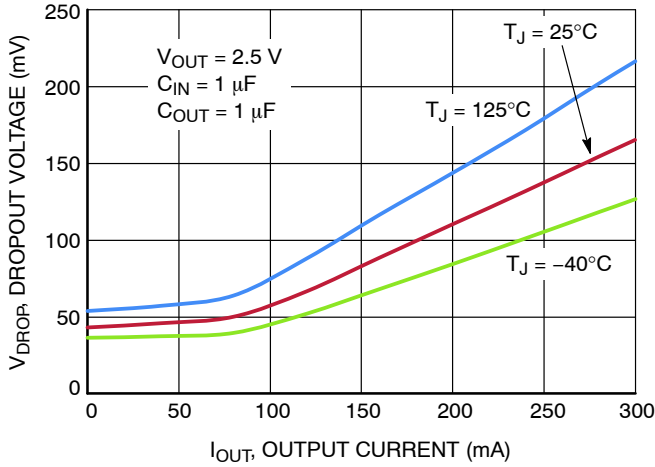


Figure 23. Drop vs. Output Current – 2.5 V

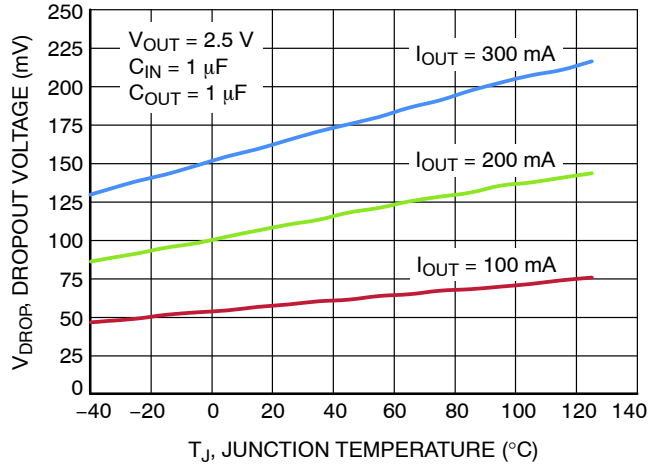


Figure 24. Dropout vs. Temperature – 2.5 V

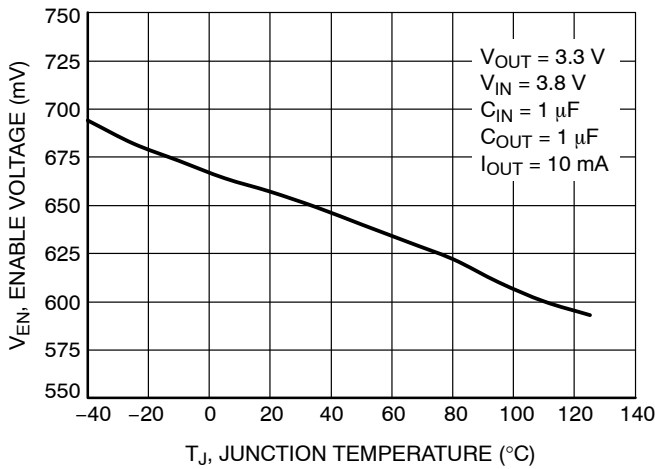


Figure 25. Enable Threshold – High

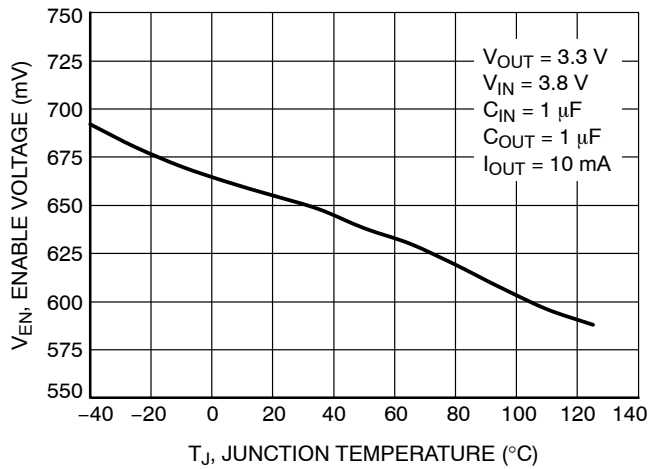


Figure 26. Enable Threshold – Low

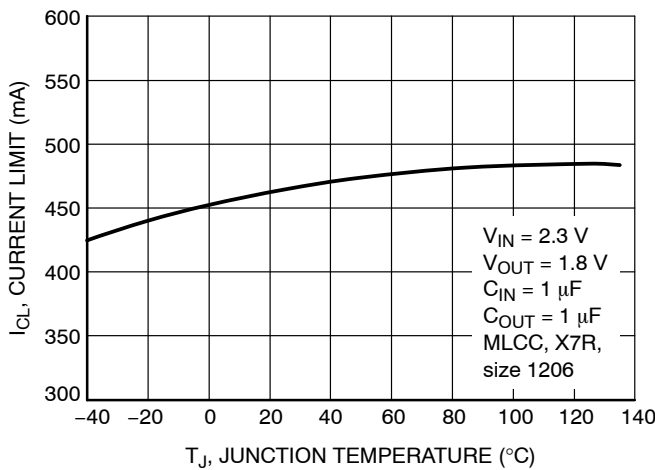


Figure 27. Output Current Limit

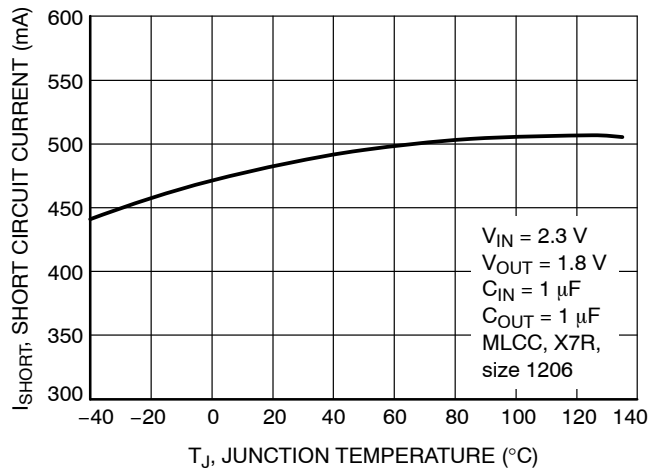


Figure 28. Short Circuit Limit

TYPICAL CHARACTERISTICS

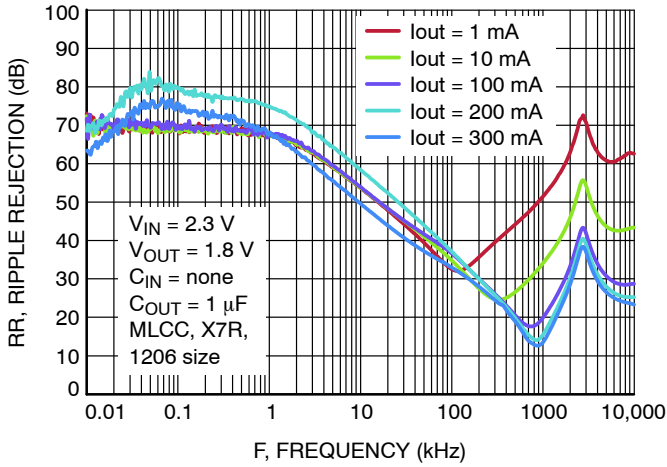


Figure 29. Power Supply Rejection Ratio, $V_{OUT} = 1.8 V$

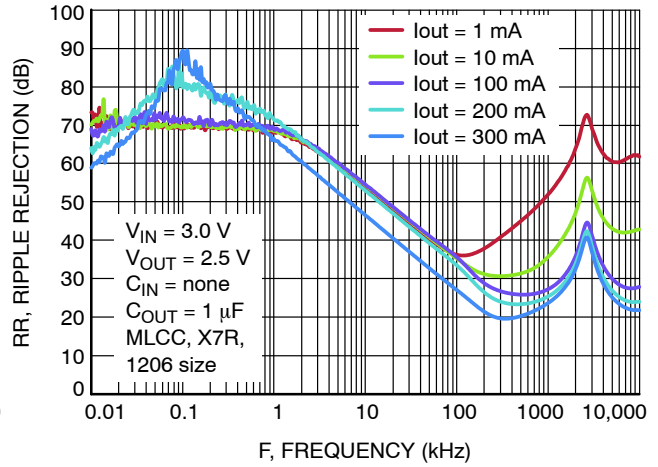


Figure 30. Power Supply Rejection Ratio, $V_{OUT} = 2.5 V$

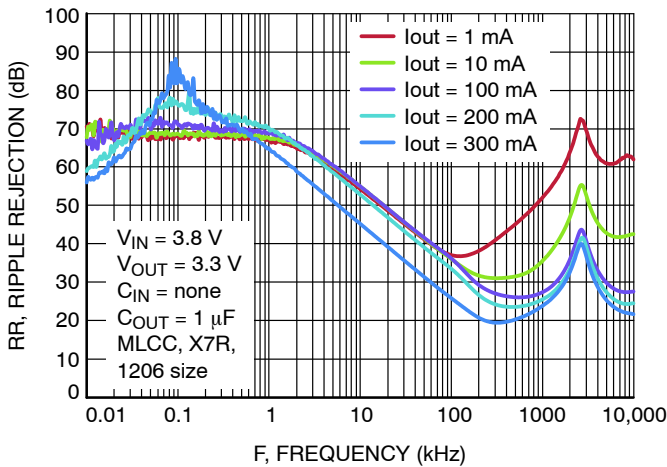


Figure 31. Power Supply Rejection Ratio, $V_{OUT} = 3.3 V$

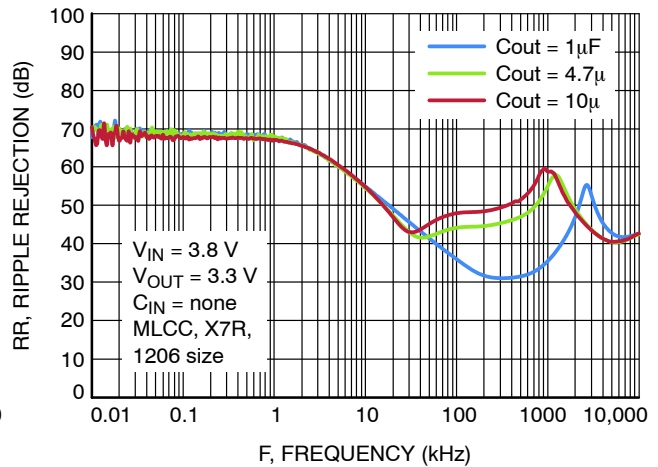


Figure 32. Power Supply Rejection Ratio, $V_{OUT} = 3.3 V, I_{OUT} = 10 mA$

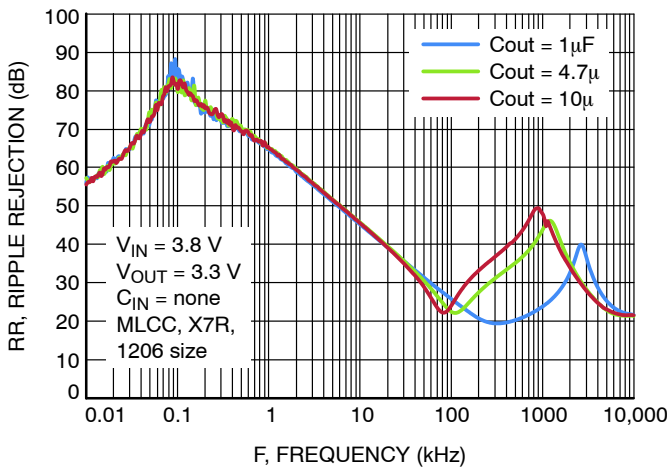


Figure 33. Power Supply Rejection Ratio, $V_{OUT} = 3.3 V, I_{OUT} = 300 mA$

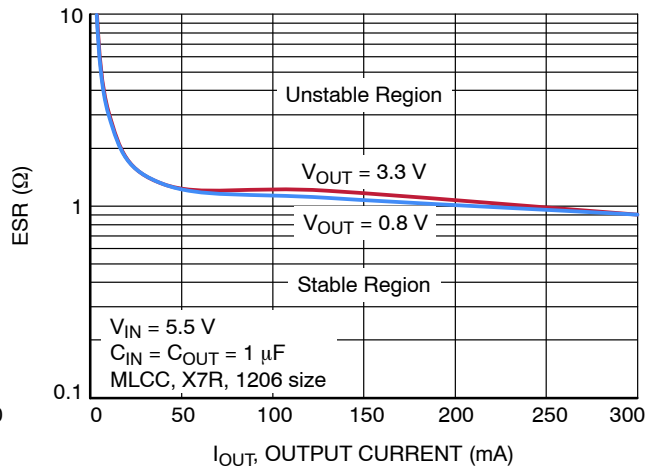


Figure 34. Output Capacitor ESR vs. Output Current

TYPICAL CHARACTERISTICS

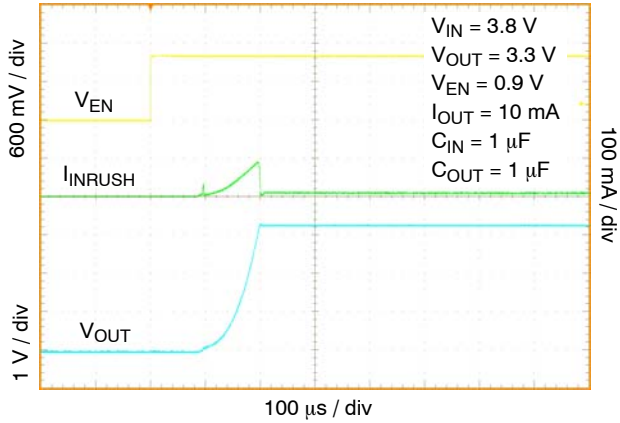


Figure 35. Enable Turn-on Response – $C_{OUT} = 1 \mu F$

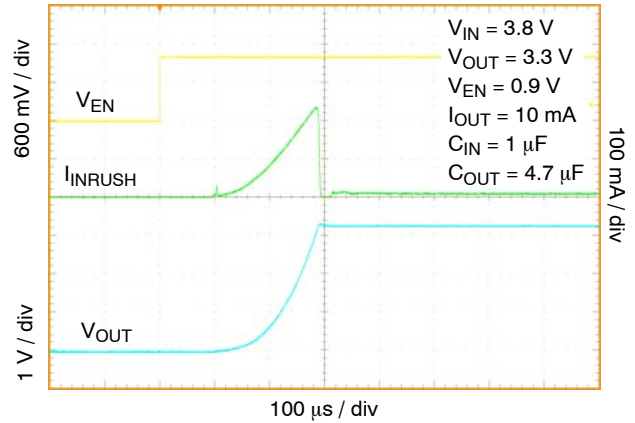


Figure 36. Enable Turn-on Response – $C_{OUT} = 4.7 \mu F$

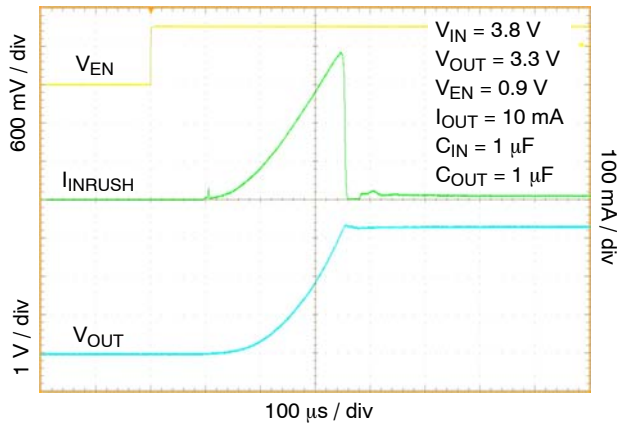


Figure 37. Enable Turn-on Response – $C_{OUT} = 10 \mu F$

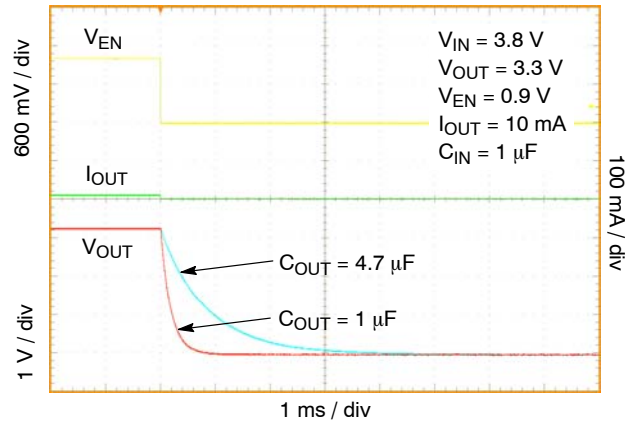


Figure 38. Enable Turn-off Response

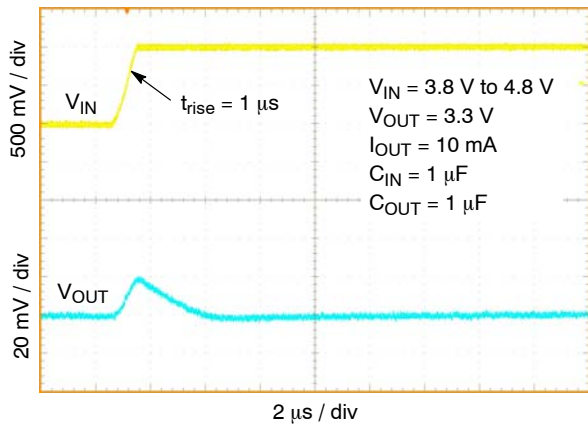


Figure 39. Line Transient Response – Rising Edge, $V_{OUT} = 3.3 V$

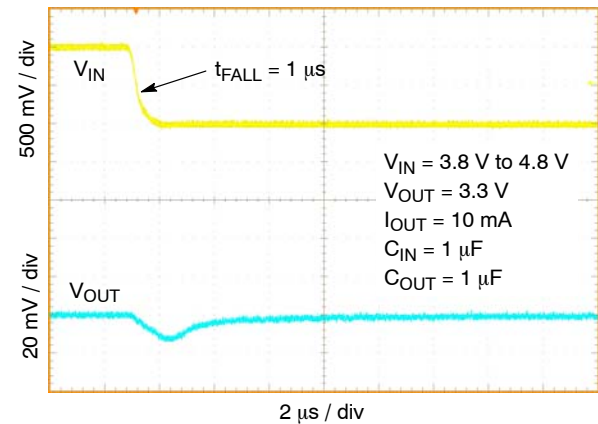


Figure 40. Line Transient Response – Falling Edge, $V_{OUT} = 3.3 V$

TYPICAL CHARACTERISTICS

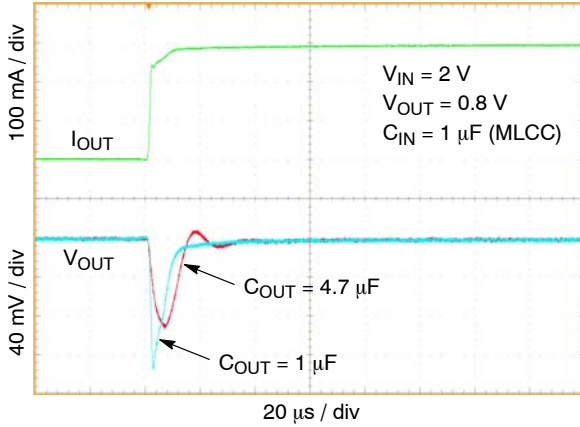


Figure 41. Load Transient Response – Rising Edge, $V_{OUT} = 0.8\text{ V}$, $I_{OUT} = 1\text{ mA}$ to 300 mA , $C_{OUT} = 1\text{ }\mu\text{F}$, $4.7\text{ }\mu\text{F}$

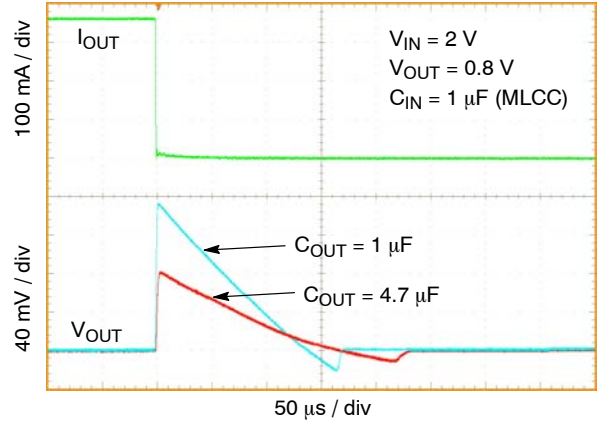


Figure 42. Load Transient Response – Falling Edge, $V_{OUT} = 0.8\text{ V}$, $I_{OUT} = 1\text{ mA}$ to 300 mA , $C_{OUT} = 1\text{ }\mu\text{F}$, $4.7\text{ }\mu\text{F}$

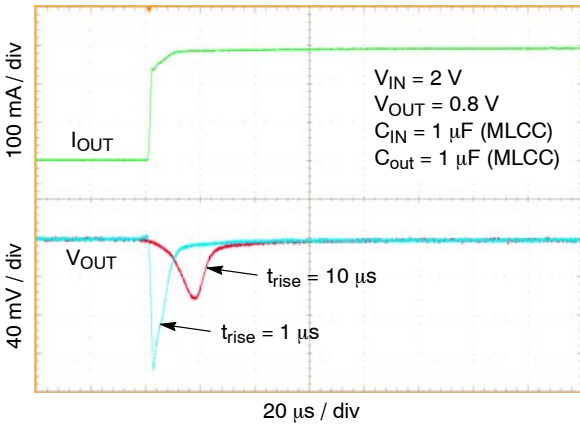


Figure 43. Load Transient Response – Rising Edge, $V_{OUT} = 0.8\text{ V}$, $I_{OUT} = 1\text{ mA}$ to 300 mA , $t_{RISE} = 1\text{ }\mu\text{s}$, $10\text{ }\mu\text{s}$

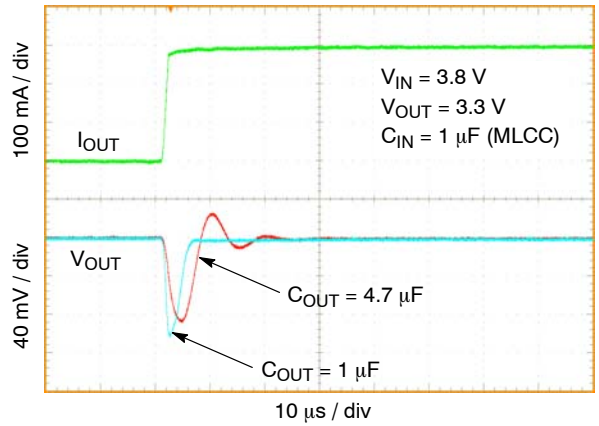


Figure 44. Load Transient Response – Rising Edge, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 1\text{ mA}$ to 300 mA , $C_{OUT} = 1\text{ }\mu\text{F}$, $4.7\text{ }\mu\text{F}$

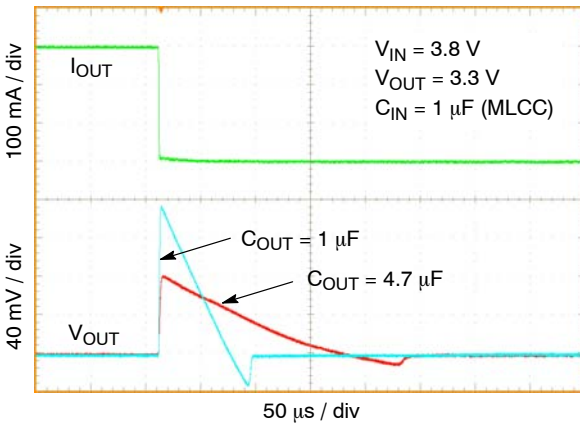


Figure 45. Load Transient Response – Falling Edge, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 1\text{ mA}$ to 300 mA , $C_{OUT} = 1\text{ }\mu\text{F}$, $4.7\text{ }\mu\text{F}$

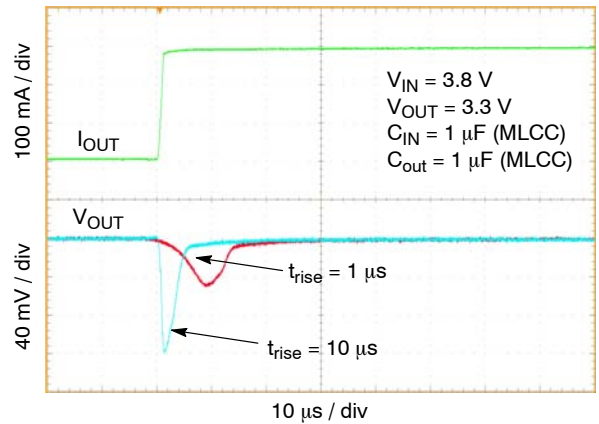


Figure 46. Load Transient Response – Rising Edge, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 1\text{ mA}$ to 300 mA , $t_{RISE} = 1\text{ }\mu\text{s}$, $10\text{ }\mu\text{s}$

TYPICAL CHARACTERISTICS

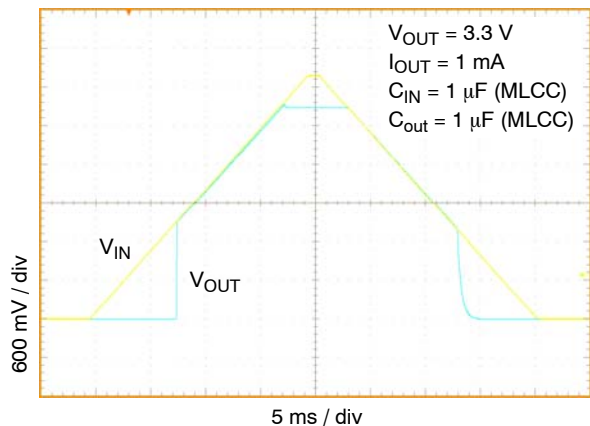


Figure 47. Turn-on/off – Slow Rising V_{IN}

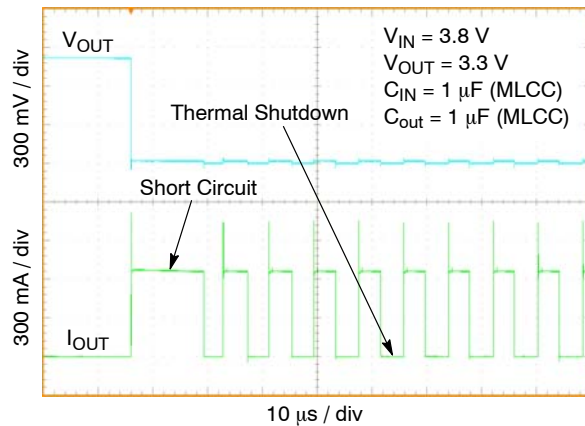


Figure 48. Short Circuit and Thermal Shutdown

APPLICATIONS INFORMATION

General

The NCV8703 is a high performance 300 mA Low Dropout Linear Regulator. This device delivers excellent noise and dynamic performance. Thanks to its adaptive ground current feature the device consumes only 12 μ A of quiescent current at no-load condition. The regulator features ultra-low noise of 13 μ VRMS, PSRR of 68 dB at 1 kHz and very good load/line transient performance. Such excellent dynamic parameters and small package size make the device an ideal choice for powering the precision analog and noise sensitive circuitry in portable applications. The LDO achieves this ultra low noise level output without the need for a noise bypass capacitor. A logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as typ. 120 nA from the IN pin. The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

Input Capacitor Selection (CIN)

It is recommended to connect a minimum of 1 μ F Ceramic X5R or X7R capacitor close to the IN pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the min. /max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes. Larger input capacitor may be necessary if fast and large load transients are encountered in the application.

Output Decoupling (COUT)

The NCV8703 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μ F and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCV8703 is designed to remain stable with minimum effective capacitance of 0.1 μ F to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0402 the effective capacitance drops rapidly with the applied DC bias. Refer to the Figure 49, for the capacitance vs. package size and DC bias voltage dependence.

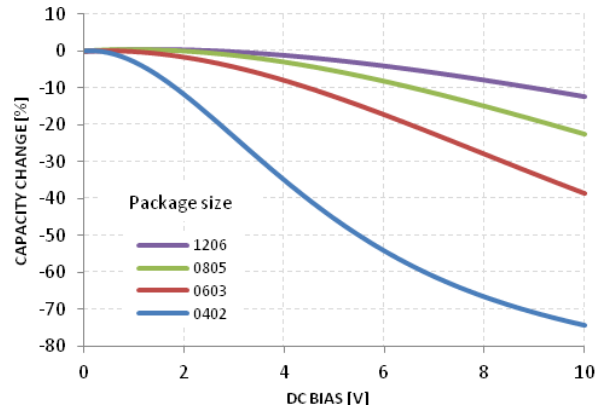


Figure 49. Capacitance Change vs. DC Bias

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 900 m Ω . Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR as shown in typical characteristics. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature. The tantalum capacitors are generally more costly than ceramic capacitors.

No-load Operation

The regulator remains stable and regulates the output voltage properly within the $\pm 2\%$ tolerance limits even with no external load applied to the output.

Enable Operation

The EN pin is used to enable/disable the LDO and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned-off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 320 Ω resistor. In the disable state the device consumes as low as typ. 120 nA from the V_{IN}.

If the EN pin voltage >0.9 V the device is guaranteed to be enabled. The NCV8703 regulates the output voltage and the active discharge transistor is turned-off.

APPLICATIONS INFORMATION

The EN pin has internal pull-down current source with typ. value of 110 nA which assures that the device is turned-off when the EN pin is not connected. Build in 2 mV hysteresis into the EN prevents from periodic on/off oscillations that can occur due to noise.

In the case where the EN function isn't required the EN should be tied directly to IN.

Undervoltage Lockout

The internal UVLO circuitry assures that the device becomes disabled when the V_{IN} falls below typ. 1.5 V. When the V_{IN} voltage ramps-up the NCV8703 becomes enabled, if V_{IN} rises above typ. 1.6 V. The 100 mV hysteresis prevents from on/off oscillations that can occur due to noise on V_{IN} line.

Output Current Limit

Output Current is internally limited within the IC to a typical 490 mA. The NCV8703 will source this amount of current measured when the output voltage drops on the 90% of the nominal V_{OUT} . When the Output Voltage is directly shorted to ground ($V_{OUT} = 0$ V), the short circuit protection will limit the output current to 520 mA (typ). The current limit and short circuit protection will work properly up to $V_{IN} = 5.5$ V at $T_A = 25^\circ\text{C}$. There is no limitation for the short circuit duration.

Internal Soft-Start circuit

NCV8703 contains an internal soft-start circuitry to protect against large inrush currents which could otherwise flow during the start-up of the regulator. Soft-start feature protects against power bus disturbances and assures a controlled and monotonic rise of the output voltage.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold ($T_{SD} - 160^\circ\text{C}$ typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold ($T_{SDU} - 140^\circ\text{C}$ typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCV8703 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCV8703 can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{\theta_{JA}} \quad (\text{eq. 1})$$

The power dissipated by the NCV8703 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{GND}@I_{OUT}) + I_{OUT}(V_{IN} - V_{OUT}) \quad (\text{eq. 2})$$

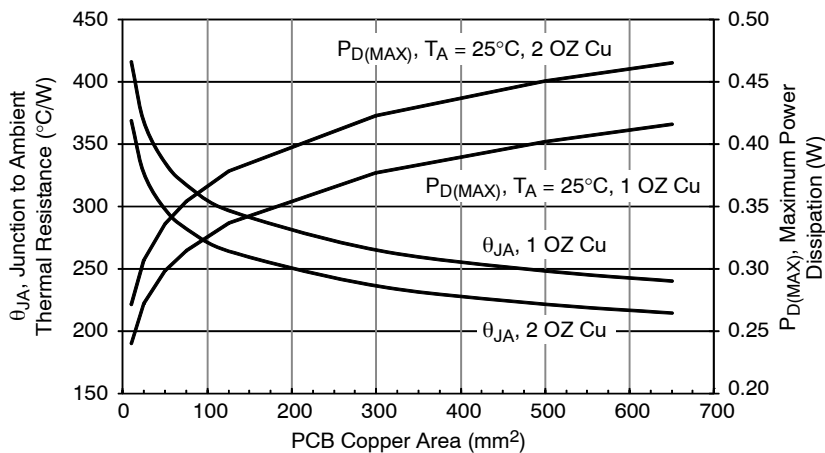


Figure 50. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area (TSOP-5)

APPLICATIONS INFORMATION

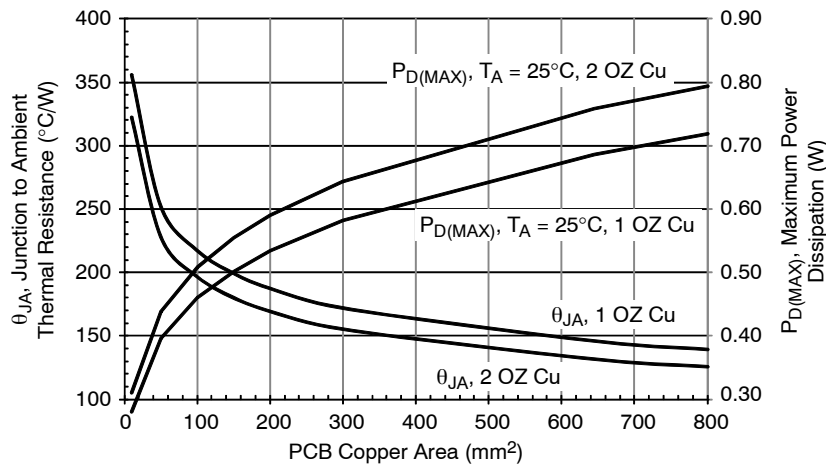


Figure 51. θ_{JA} vs. Copper Area (XDFN6)

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Load Regulation

The NCV8703 features very good load regulation of typically 6 mV in 0 mA to 300 mA range. In order to achieve this very good load regulation a special attention to PCB design is necessary. The trace resistance from the OUT pin to the point of load can easily approach 100 mΩ which will cause 30 mV voltage drop at full load current, deteriorating the excellent load regulation.

Line Regulation

The IC features very good line regulation of 0.6 mV/V measured from $V_{IN} = V_{OUT} + 0.5$ V to 5.5 V. For battery operated applications it may be important that the line regulation from $V_{IN} = V_{OUT} + 0.5$ V up to 4.5 V is only 0.45 mV/V.

Power Supply Rejection Ratio

The NCV8703 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Output Noise

The IC is designed for ultra-low noise output voltage without external noise filter capacitor (C_{nr}). Figures 3 – 6 shows NCV8703 noise performance. Generally the noise performance in the indicated frequency range improves with increasing output current.

Although even at $I_{OUT} = 1$ mA the noise levels are below 20 μV_{RMS} .

Turn-On Time

The turn-on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT} , T_A .

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from Equation 2.

NCV8703

ORDERING INFORMATION

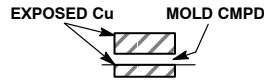
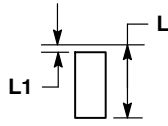
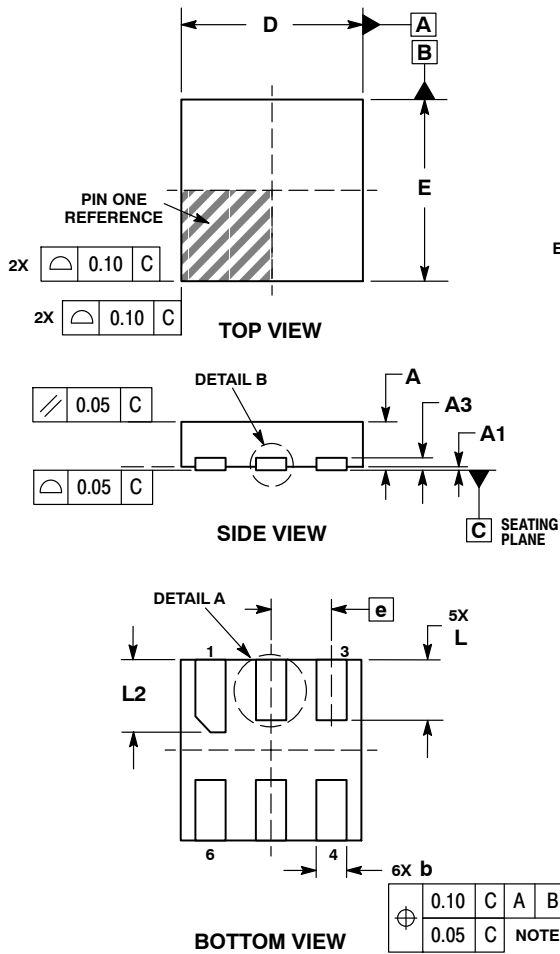
| Device | Voltage Option | Marking | Package | Shipping † |
|----------------|----------------|---------|---------|--------------------|
| NCV8703MX18TCG | 1.8 V | J | XDFN6 | 3000 / Tape & Reel |
| NCV8703MX28TCG | 2.8 V | K | | |
| NCV8703MX30TCG | 3.0 V | L | | |
| NCV8703MX33TCG | 3.3 V | P | | |
| NCV8703SN18T1G | 1.8 V | VEC | TSOP5 | 3000 / Tape & Reel |
| NCV8703SN28T1G | 2.8 V | VED | | |
| NCV8703SN30T1G | 3.0 V | VEE | | |
| NCV8703SN33T1G | 3.3 V | VEF | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCV8703

PACKAGE DIMENSIONS

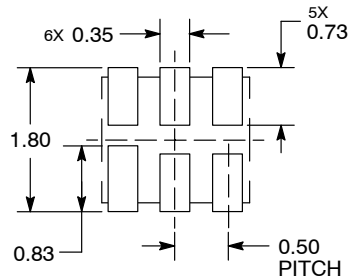
XDFN6 1.5x1.5, 0.5P
CASE 711AE
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20mm FROM TERMINAL TIP.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.35 | 0.45 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 REF | |
| b | 0.20 | 0.30 |
| D | 1.50 BSC | |
| E | 1.50 BSC | |
| e | 0.50 BSC | |
| L | 0.40 | 0.60 |
| L1 | --- | 0.15 |
| L2 | 0.50 | 0.70 |

RECOMMENDED MOUNTING FOOTPRINT*



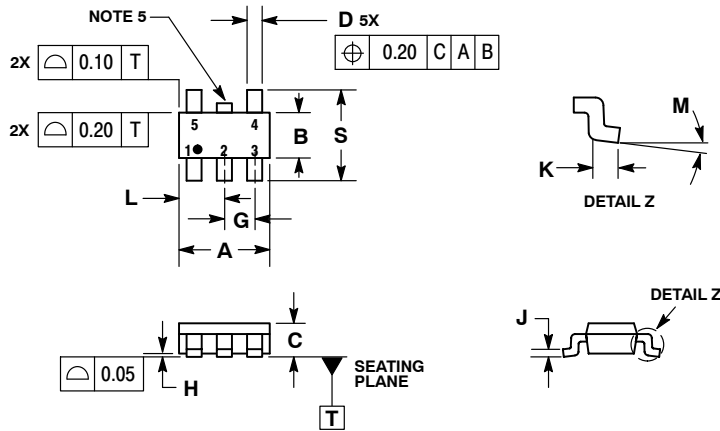
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCV8703

PACKAGE DIMENSIONS

TSOP-5 CASE 483-02 ISSUE H

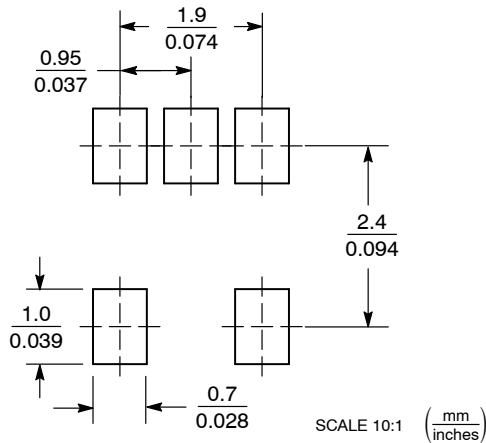


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 3.00 BSC | |
| B | 1.50 BSC | |
| C | 0.90 | 1.10 |
| D | 0.25 | 0.50 |
| G | 0.95 BSC | |
| H | 0.01 | 0.10 |
| J | 0.10 | 0.26 |
| K | 0.20 | 0.60 |
| L | 1.25 | 1.55 |
| M | 0° 10° | |
| S | 2.50 | 3.00 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Телефон: 8 (812) 309-75-97 (многоканальный)

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Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А