

74AHC3GU04-Q100

Triple unbuffered inverter

Rev. 2 — 27 February 2019

Product data sheet

1. General description

The 74AHC3GU04-Q100 is a high-speed Si-gate CMOS device. This device provides three inverter gates with unbuffered outputs.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pf, R = 0 Ω)

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC3GU04DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74AHC3GU04DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

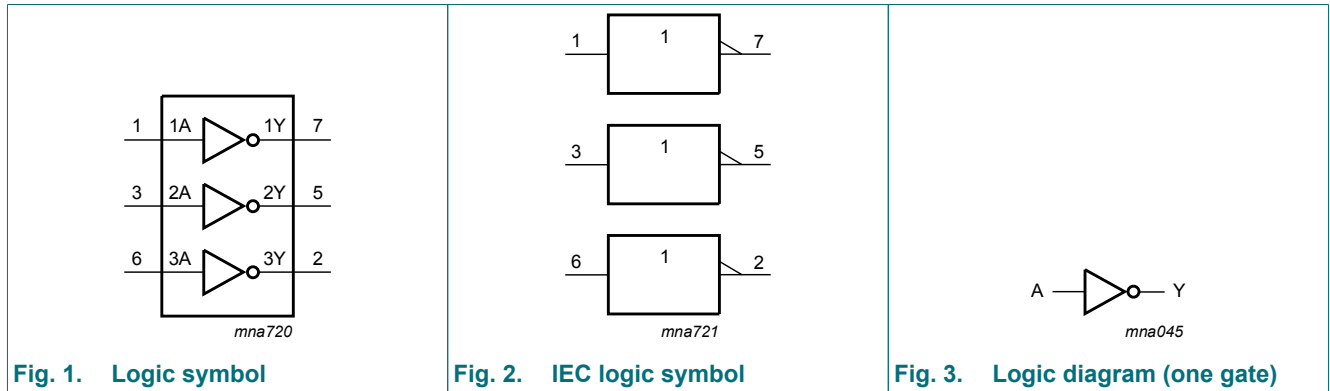
4. Marking

Table 2. Marking codes

Type number	Marking code [1]
74AHC3GU04DP-Q100	AU4
74AHC3GU04DC-Q100	AU4

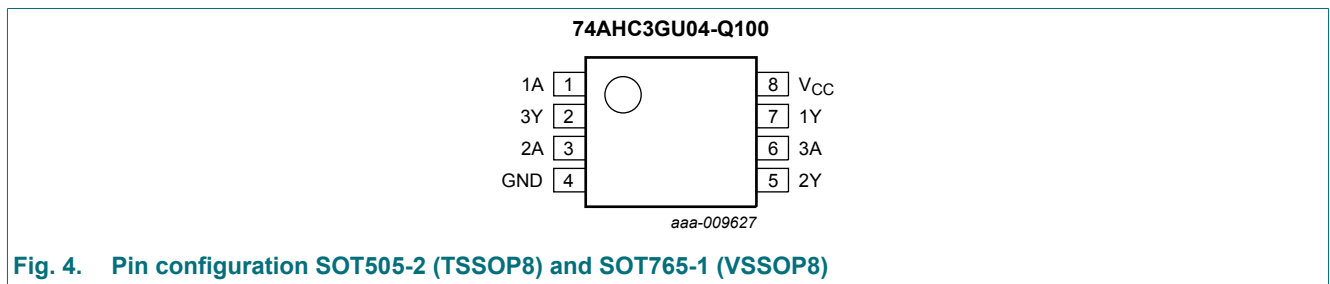
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
A	Y
L	H
H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V [1]	-20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	± 20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	± 25	mA
I_{CC}	supply current		-	75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V ± 0.3 V	-	-	100	ns/V
		$V_{CC} = 5.0$ V ± 0.5 V	-	-	20	ns/V

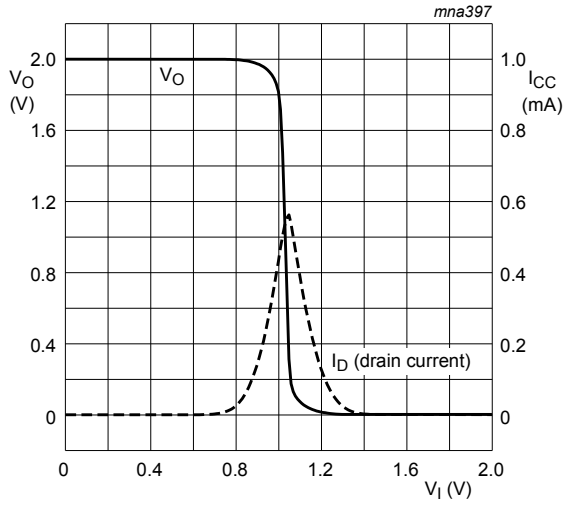
10. Static characteristics

Table 7. Static characteristics

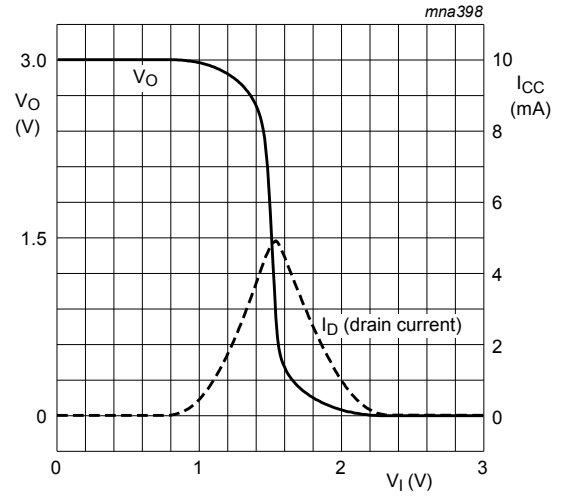
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.7	-	-	1.7	-	1.7	-	V
		V _{CC} = 3.0 V	2.4	-	-	2.4	-	2.4	-	V
		V _{CC} = 5.5 V	4.4	-	-	4.4	-	4.4	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.3	-	0.3	-	0.3	V
		V _{CC} = 3.0 V	-	-	0.6	-	0.6	-	0.6	V
		V _{CC} = 5.5 V	-	-	1.1	-	1.1	-	1.1	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 µA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
C _I	input capacitance		-	3.0	10	-	10	-	10	pF

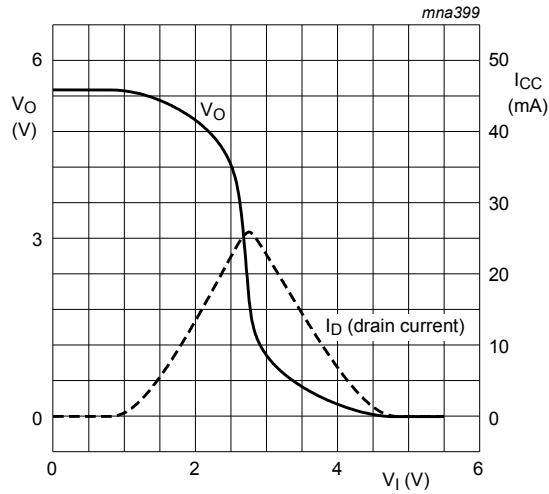
10.1. Typical transfer characteristics



a. $V_{CC} = 2.0\text{ V}; I_O = 0\text{ A}$



b. $V_{CC} = 3.0\text{ V}; I_O = 0\text{ A}$



c. $V_{CC} = 5.5\text{ V}; I_O = 0\text{ A}$

Fig. 5. Typical transfer characteristic

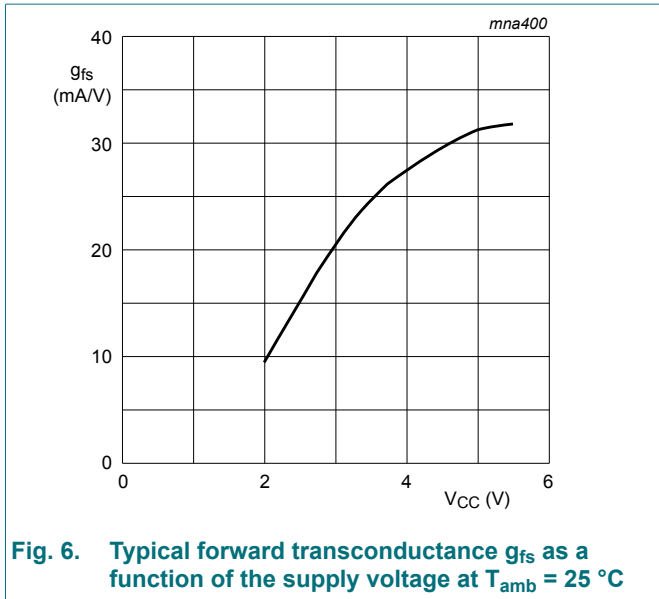


Fig. 6. Typical forward transconductance g_{fs} as a function of the supply voltage at $T_{amb} = 25\text{ }^{\circ}\text{C}$

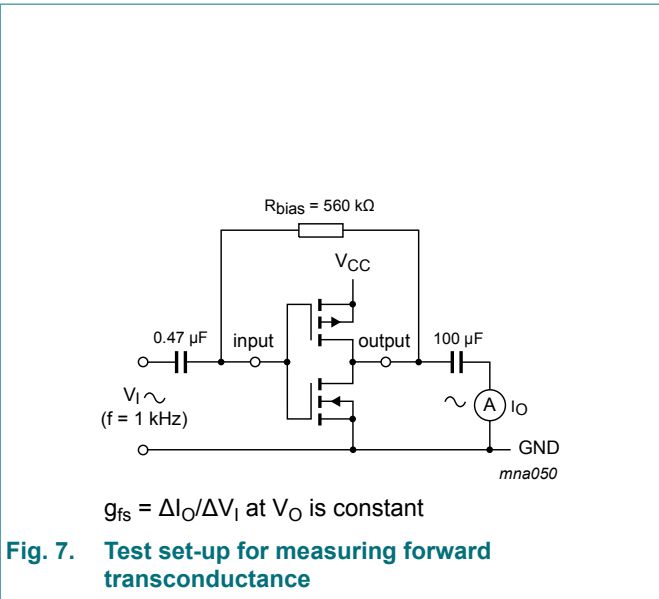


Fig. 7. Test set-up for measuring forward transconductance

11. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0\text{ V}$; For test circuit see Fig. 9.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Fig. 8 [1]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$; $C_L = 15\text{ pF}$ [2]	-	3.0	7.1	1.0	8.5	1.0	10.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$; $C_L = 50\text{ pF}$ [2]	-	4.3	10.6	1.0	12.0	1.0	13.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$; $C_L = 15\text{ pF}$ [3]	-	2.5	5.5	1.0	6.0	1.0	7.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$; $C_L = 50\text{ pF}$ [3]	-	3.5	7.0	1.0	8.0	1.0	9.0	ns
C_{PD}	power dissipation capacitance	per buffer; $V_I = GND$ to V_{CC} [4]	-	4	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] Typical values are measured at $V_{CC} = 3.3\text{ V}$.
- [3] Typical values are measured at $V_{CC} = 5.0\text{ V}$.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1. Waveforms and test circuit

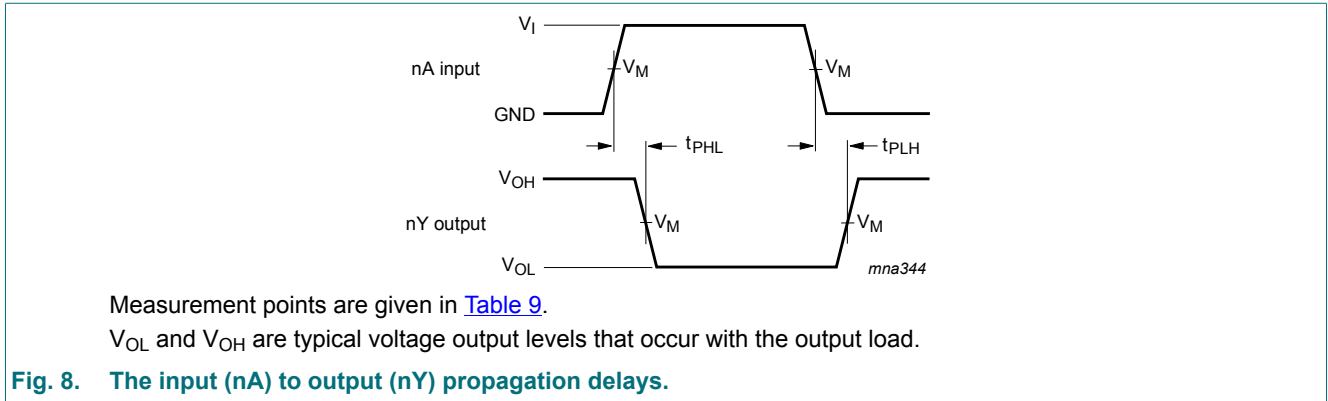


Table 9. Measurement points

Input	Output
V_M	V_M
$0.5V_{CC}$	$0.5V_{CC}$

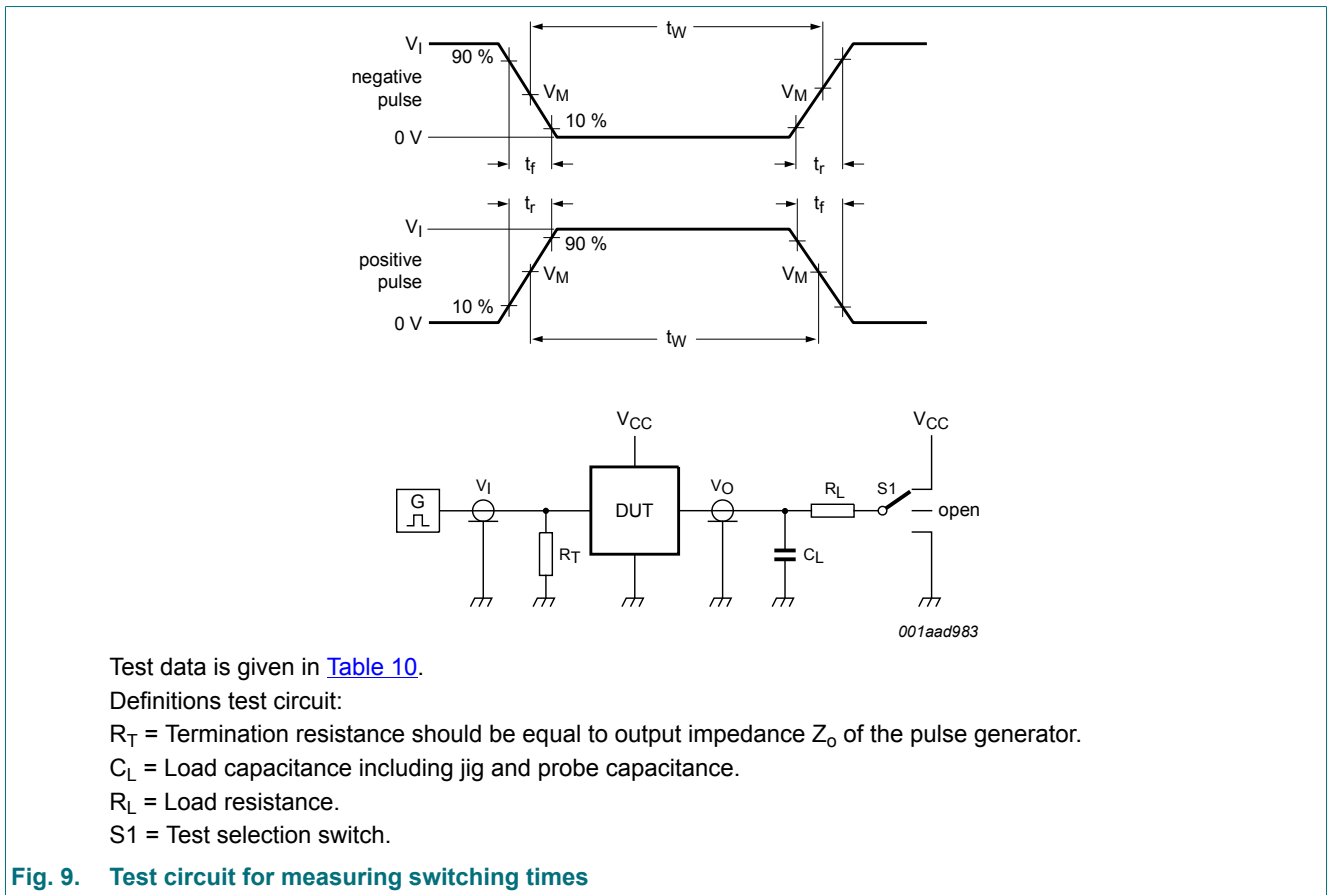


Table 10. Test data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
V_{CC}	≤ 3 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Application information

Some applications are:

- Linear amplifier (see Fig. 10)
- In crystal oscillator design (see Fig. 11)

Remark: All values given are typical unless otherwise specified.

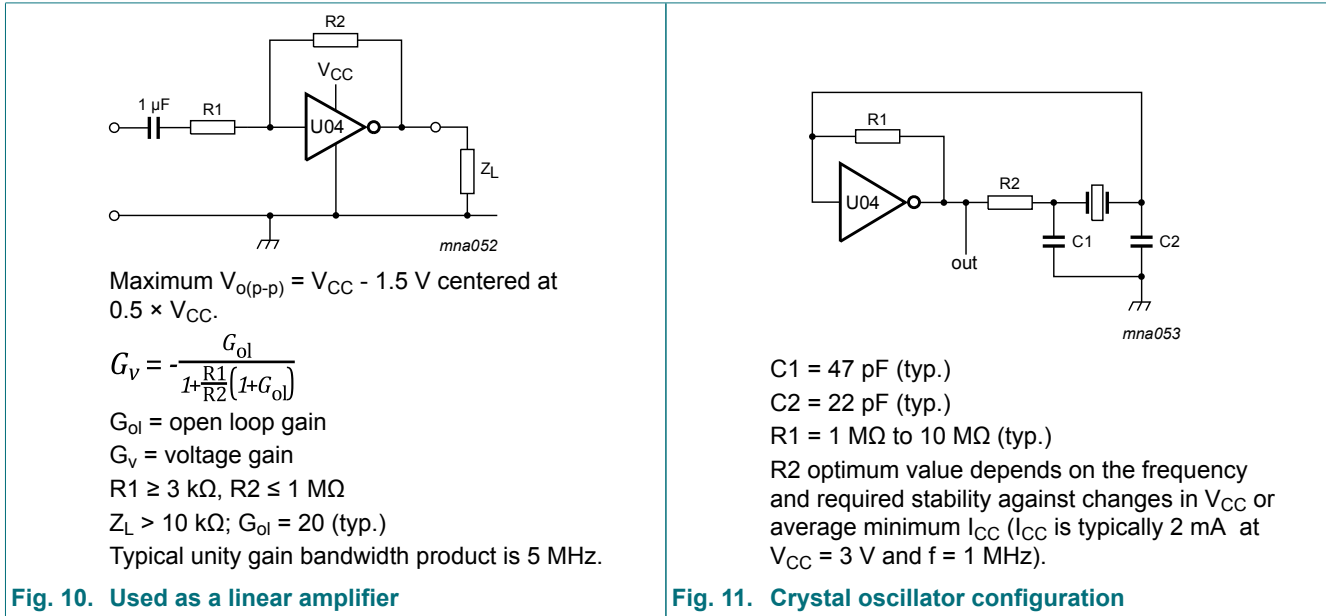


Table 11. External components for resonator (f < 1 MHz)

All values given are typical and must be used as an initial set-up.

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 MΩ	220 kΩ	56 pF	20 pF
16 kHz to 24.9 kHz	22 MΩ	220 kΩ	56 pF	10 pF
25 kHz to 54.9 kHz	22 MΩ	100 kΩ	56 pF	10 pF
55 kHz to 129.9 kHz	22 MΩ	100 kΩ	47 pF	5 pF
130 kHz to 199.9 kHz	22 MΩ	47 kΩ	47 pF	5 pF
200 kHz to 349.9 kHz	22 MΩ	47 kΩ	47 pF	5 pF
350 kHz to 600 kHz	22 MΩ	47 kΩ	47 pF	5 pF

Table 12. Optimum value for R2

Frequency	R2	Optimum for
3 kHz	2.0 kΩ	minimum required I_{CC}
	8.0 kΩ	minimum influence due to change in V_{CC}
6 kHz	1.0 kΩ	minimum required I_{CC}
	4.7 kΩ	minimum influence by V_{CC}
10 kHz	0.5 kΩ	minimum required I_{CC}
	2.0 kΩ	minimum influence by V_{CC}
14 kHz	0.5 kΩ	minimum required I_{CC}
	1.0 kΩ	minimum influence by V_{CC}
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

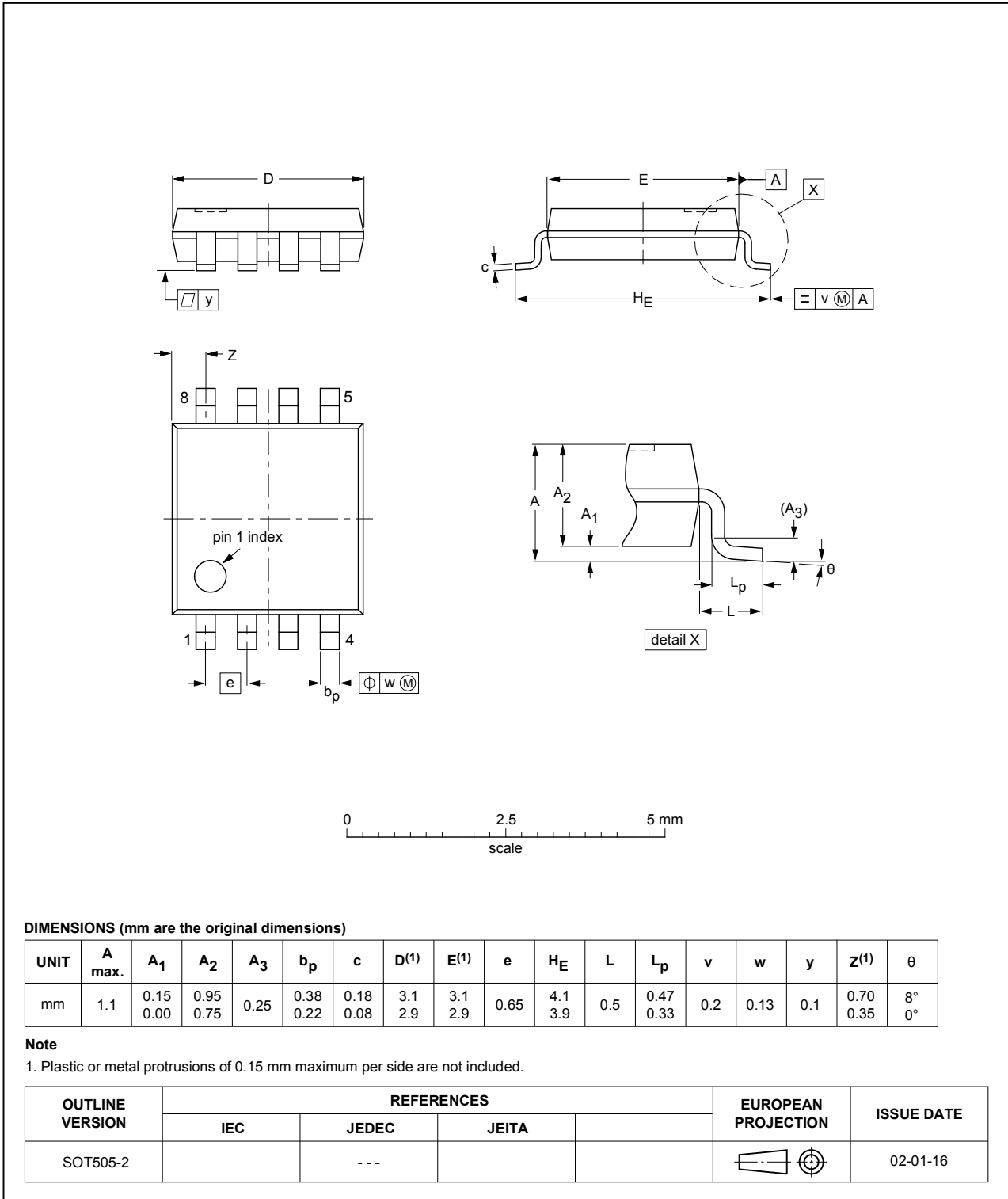


Fig. 12. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

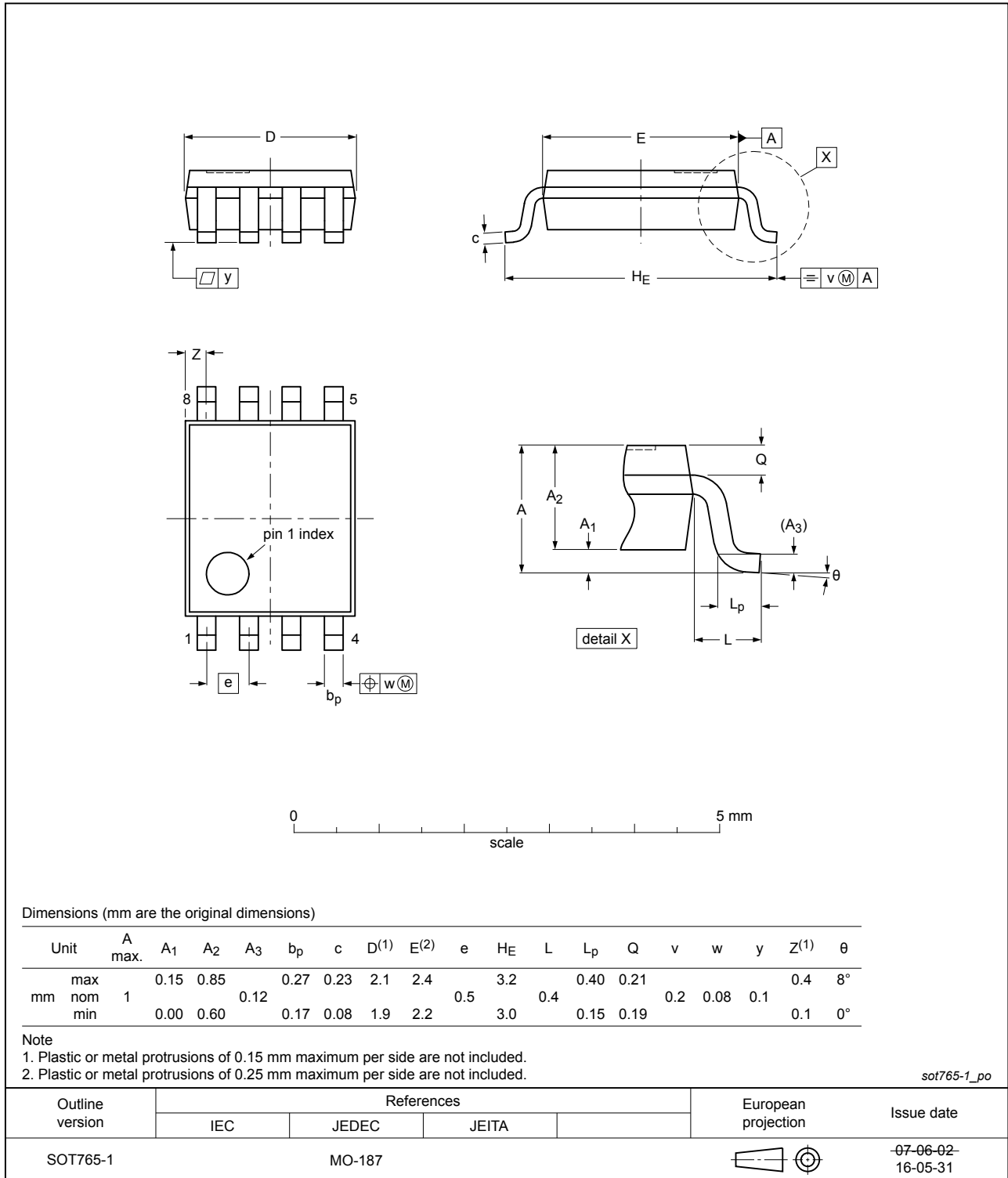


Fig. 13. Package outline SOT765-1 (VSSOP8)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC3GU04_Q100 v.2	20190227	Product data sheet	-	74AHC3GU04_Q100 v.1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Package outline drawing SOT765-1 (VSSOP8) updated 			
74AHC3GU04_Q100 v.1	20131118	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Телефон: 8 (812) 309-75-97 (многоканальный)

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