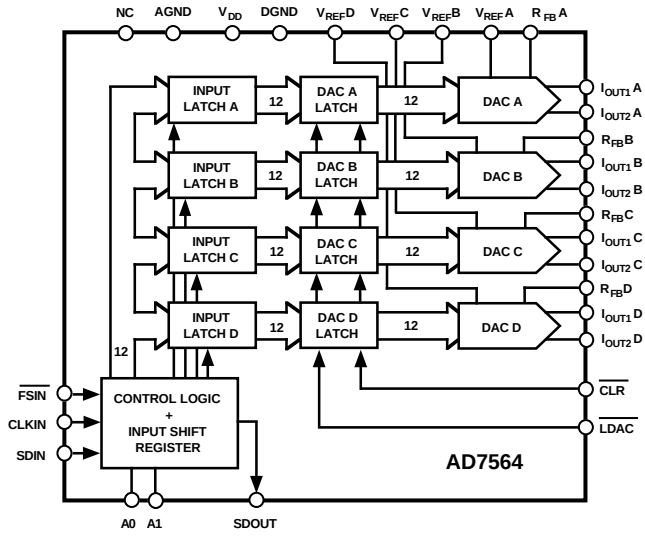
LC²MOS
+3.3 V/+5 V, Low Power, Quad 12-Bit DAC

AD7564

FEATURES
Four 12-Bit DACs in One Package
4-Quadrant Multiplication
Separate References
Single Supply Operation
Guaranteed Specifications with +3.3 V/+5 V Supply
Low Power
Versatile Serial Interface
Simultaneous Update Capability
Reset Function
28-Pin SOIC, SSOP and DIP Packages

APPLICATIONS
Process Control
Portable Instrumentation
General Purpose Test Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7564 contains four 12-bit DACs in one monolithic device. The DACs are standard current output with separate V_{REF}, I_{OUT1}, I_{OUT2} and R_{FB} terminals. These DACs operate from a single +3.3 V to +5 V supply.

The AD7564 is a serial input device. Data is loaded using $\overline{FSIN}$, CLKIN and SDIN. Two address pins A0 and A1 set up a device address, and this feature may be used to simplify device loading in a multi-DAC environment. Alternatively, A0 and A1 can be ignored and the serial out capability used to configure a daisy-chained system.

All DACs can be simultaneously updated using the asynchronous $\overline{LDAC}$ input, and they can be cleared by asserting the asynchronous $\overline{CLR}$ input.

The device is packaged in 28-pin SOIC, SSOP and DIP packages.

PRODUCT HIGHLIGHTS

1. The AD7564 contains four 12-bit current output DACs with separate V_{REF} inputs.
2. The AD7564 can be operated from a single +3.3 V to +5 V supply.
3. Simultaneous update capability and reset function are available.
4. The AD7564 features a fast, versatile serial interface compatible with modern 3 V and 5 V microprocessors and microcomputers.
5. Low power, 50 μW at 5 V and 33 μW at 3.3 V.

REV. B

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AD7564–SPECIFICATIONS

Normal Mode

(V_{DD} = +4.75 V to +5.25 V; $I_{OUT1}A$ to $I_{OUT1}D$ = $I_{OUT2}A$ = $I_{OUT2}D$ = AGND = 0 V; V_{REF} = +10 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	B Grade[1]	Units	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	1 LSB = $V_{REF}/2^{12}$ = 2.44 mV when V_{REF} = 10 V
Relative Accuracy	±0.5	LSB max	
Differential Nonlinearity	±0.5	LSB max	All Grades Guaranteed Monotonic Over Temperature
Gain Error			
+25°C	±4	LSBs max	
T_{MIN} to T_{MAX}	±5	LSBs max	
Gain Temperature Coefficient[2]	2	ppm FSR/°C typ	
	5	ppm FSR/°C max	
Output Leakage Current			
I_{OUT1}			
@ +25°C	10	nA max	
T_{MIN} to T_{MAX}	50	nA max	
REFERENCE INPUT			
Input Resistance	6	kΩ min	Typical Input Resistance = 9.5 kΩ
	13	kΩ max	
Ladder Resistance Mismatch	2	% max	Typically 0.6%
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±1	µA max	
C_{IN}, Input Capacitance[2]	10	pF max	
DIGITAL OUTPUT (SDOUT)			
Output Low Voltage (V_{OL})	0.4	V max	Load Circuit as in Figure 2.
Output High Voltage (V_{OH})	4.0	V min	
POWER REQUIREMENTS			
V_{DD} Range	4.75/5.25	V min/V max	Part Functions from 3.3 V to 5.25 V
Power Supply Rejection[2]			
$\Delta Gain/\Delta V_{DD}$	–75	dB typ	
I_{DD}	10	µA max	V_{INH} = V_{DD}, V_{INL} = 0 V At Input Levels of 0.8 V and 2.4 V, I_{DD} is Typically 2 mA.

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Not production tested. Guaranteed by characterization at initial product release.

Specifications subject to change without notice.

Biased Mode[1] (V_{DD} = +3 V to +5.5 V; V_{IOUT1} = V_{IOUT2} = 1.23 V; AGND = 0 V; V_{REF} = 0 V to 2.45 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	A Grade[2]	Units	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	1 LSB = $(V_{IOUT2} - V_{REF})/2^{12}$ = 300 μV when V_{IOUT2} = 1.23 V and V_{REF} = 0 V
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±0.9	LSB max	All Grades Guaranteed Monotonic Over Temperature
Gain Error			
+25°C	±4	LSBs max	
T_{MIN} to T_{MAX}	±5	LSBs max	
Gain Temperature Coefficient[3]	2	ppm FSR/°C typ	
	5	ppm FSR/°C max	
Output Leakage Current			See Terminology Section
I_{OUT1}			
@ +25°C	10	nA max	
T_{MIN} to T_{MAX}	50	nA max	
Input Resistance			
@ I_{OUT2} Pins	6	kΩ min	This Varies with DAC Input Code
DIGITAL INPUTS			
V_{INH}, Input High Voltage @ V_{DD} = +5 V	2.4	V min	
V_{INH}, Input High Voltage @ V_{DD} = +3.3 V	2.1	V min	
V_{INL}, Input Low Voltage @ V_{DD} = +5 V	0.8	V max	
V_{INL}, Input Low Voltage @ V_{DD} = +3.3 V	0.6	V max	
I_{INH}, Input Current	±1	μA max	
C_{IN}, Input Capacitance[3]	10	pF max	
DIGITAL OUTPUT (SDOUT)			Load Circuit as in Figure 2.
Output Low Voltage (V_{OL})	0.4	V max	V_{DD} = +5 V
Output Low Voltage (V_{OL})	0.2	V max	V_{DD} = +3.3 V
Output High Voltage (V_{OH})	4.0	V min	V_{DD} = +5 V
Output High Voltage (V_{OH})	V_{DD} – 0.2	V min	V_{DD} = +3.3 V
POWER REQUIREMENTS			
V_{DD} Range	3/5.5	V min/V max	
Power Supply Sensitivity[3]			
$\Delta Gain/\Delta V_{DD}$	–75	dB typ	
I_{DD}	10	μA max	V_{INH} = V_{DD} – 0.1 V min, V_{INL} = 0.1 V max; SDOUT Open Circuit
			I_{DD} is typically 2 mA with V_{DD} = +5 V, V_{INH} = 2.4 V min, V_{INL} = 0.8 V max; SDOUT Open Circuit

NOTES

[1]These specifications apply with the devices biased up at 1.23 V for single supply applications. The model numbering reflects this by means of a "-B" suffix (for example: AD7564AR-B). Figure 19 is an example of Biased Mode Operation.

[2]Temperature ranges is as follows: A Version: –40°C to +85°C.

[3]Not production tested. Guaranteed by characterization at initial product release.

Specifications subject to change without notice.

AC Performance Characteristics

Normal Mode

(V_{DD} = +4.75 V to +5.25 V; V_{IOUT1} = V_{IOUT2} = AGND = 0 V. V_{REF} = 6 V rms, 1 kHz sine wave; DAC output op amp is AD843; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. These characteristics are included for Design Guidance and are not subject to test.)

Parameter	B Grade	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	550	ns typ	To 0.01% of Full-Scale Range. DAC Latch Alternately Loaded with All 0s and All 1s
Digital-to-Analog Glitch Impulse	35	nV-s typ	Measured with V_{REF} = 0 V. DAC Register Alternately Loaded with All 0s and All 1s
Multiplying Feedthrough Error	–70	dB max	V_{REF} = 20 V p-p, 10 kHz Sine Wave. DAC Latch Loaded with All 0s
Output Capacitance	60	pF max	All 1s Loaded to DAC
	30	pF max	All 0s Loaded to DAC
Channel-to-Channel Isolation	–76	dB typ	Feedthrough from Any One Reference to the Others with 20 V p-p, 10 kHz Sine Wave Applied
Digital Crosstalk	5	nV-s typ	Effect of All 0s to All 1s Code Transition on Nonselected DACs
Digital Feedthrough	5	nV-s typ	Feedthrough to Any DAC Output with $\overline{FSIN}$ High and Square Wave Applied to SDIN and SCLK
Total Harmonic Distortion	–83	dB typ	V_{REF} = 6 V rms, 1 kHz Sine Wave
Output Noise Spectral Density @ 1 kHz	30	nV/$\sqrt{Hz}$ typ	All 1s Loaded to the DAC. V_{REF} = 0 V. Output Op Amp Is ADOP07

AC Performance Characteristics

Biased Mode

(V_{DD} = +3 V to +5.5 V; V_{IOUT1} = V_{IOUT2} = 1.23 V; AGND = 0 V. V_{REF} = 1 kHz, 2.45 V p-p, sine wave biased at 1.23 V; DAC output op amp is AD820; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. These characteristics are included for Design Guidance and are not subject to test.)

Parameter	A Grade	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	3.5	µs typ	To 0.01% of Full-Scale Range. V_{REF} = 0 V. DAC Latch Alternately Loaded with all 0s and all 1s.
Digital to Analog Glitch Impulse	35	nV-s typ	Measured with V_{IOUT2} = 0 V and V_{REF} = 0 V. DAC Register Alternately Loaded with all 0s and all 1s.
Multiplying Feedthrough Error	–70	dB max	DAC Latch Loaded with all 0s.
Output Capacitance	100	pF max	All 1s Loaded to DAC
	40	pF max	All 0s Loaded to DAC
Digital Feedthrough	5	nV-s typ	Feedthrough to Any DAC Output with FSIN HIGH and a Square Wave Applied to SDIN and CLKIN
Total Harmonic Distortion	–76	dB typ	
Output Noise Spectral Density @ 1 kHz	20	nV/$\sqrt{Hz}$ typ	All 1s Loaded to DAC. V_{IOUT2} = 0 V; V_{REF} = 0 V

Timing Specifications[1] ($T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	Limit at V_{DD} = +3 V to +3.6 V	Limit at V_{DD} = +4.75 V to +5.25 V	Units	Description
t_1	180	100	ns min	CLKIN Cycle Time
t_2	80	40	ns min	CLKIN High Time
t_3	80	40	ns min	CLKIN Low Time
t_4	50	30	ns min	$\overline{FSIN}$ Setup Time
t_5	50	30	ns min	Data Setup Time
t_6	10	5	ns min	Data Hold Time
t_7	125	90	ns min	$\overline{FSIN}$ Hold Time
t_8[2]	100	70	ns max	SDOUT Valid After CLKIN Falling Edge
t_9	80	40	ns min	$\overline{LDAC}$, $\overline{CLR}$ Pulse Width

NOTES

[1]Not production tested. Guaranteed by characterization at initial product release. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V for a V_{DD} of 5 V and from a voltage level 1.35 V for a V_{DD} of 3.3 V.

[2]t_8 is measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V with a V_{DD} of 5 V and 0.6 V or 2.1 V for a V_{DD} of 3.3 V.

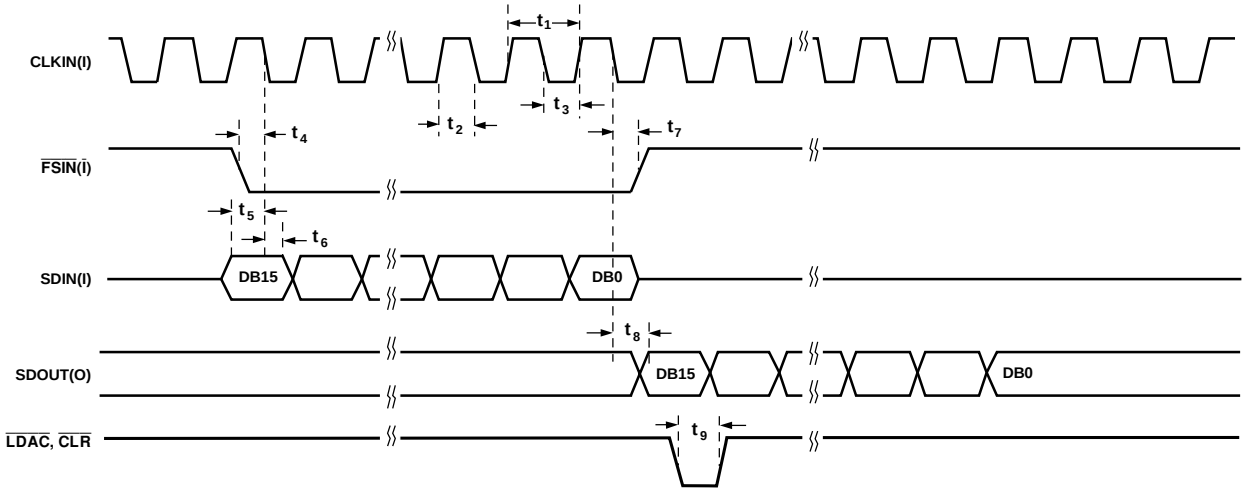


Figure 1. Timing Diagram

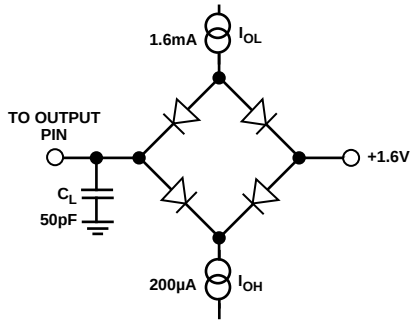


Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS[1]

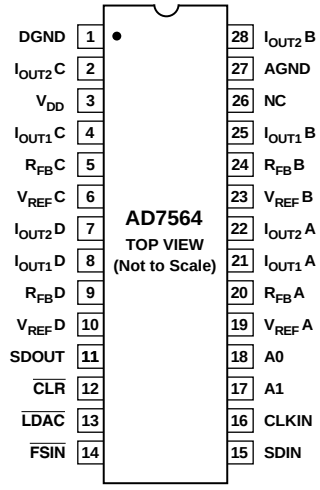
(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . –0.3 V to +6 V
I_{OUT1} to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
I_{OUT2} to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
AGND to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
V_{RFB}, V_{REF} to DGND . . . . . ±15 V
Input Current to Any Pin Except Supplies[2] . . . . . ±10 mA
Operating Temperature Range
Commercial Plastic (A, B Versions). . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
DIP Package, Power Dissipation . . . . . 875 mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering (10 sec) . . . . . 260°C
SOIC Package, Power Dissipation . . . . . 875 mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering (10 sec) . . . . . 260°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
SSOP Package, Power Dissipation . . . . . 900 mW
θ_{JA} Thermal Impedance . . . . . 100°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

PIN CONFIGURATION

DIP, SOIC and SSOP Packages



NC = NO CONNECT

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7564 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTIONS

Pin Number	Mnemonic	Description
1	DGND	Digital Ground.
2	$I_{OUT2}C$	I_{OUT2} terminal for DAC C. This should normally connect to the signal ground of the system.
3	V_{DD}	Positive power supply. This is +5 V ± 5%.
4	$I_{OUT1}C$	I_{OUT1} terminal for DAC C.
5	$R_{FB}C$	Feedback resistor for DAC C.
6	$V_{REF}C$	DAC C reference input.
7	$I_{OUT2}D$	I_{OUT2} terminal for DAC D. This should normally connect to the signal ground of the system.
8	$I_{OUT1}D$	I_{OUT1} terminal for DAC D.
9	$R_{FB}D$	Feedback resistor for DAC D.
10	$V_{REF}D$	DAC D reference input.
11	SDOUT	This shift register output allows multiple devices to be connected in a daisy chain configuration.
12	$\overline{CLR}$	Asynchronous $\overline{CLR}$ input. When this input is taken low, all DAC latches are loaded with all 0s.
13	$\overline{LDAC}$	Asynchronous LDAC input. When this input is taken low, all DAC latches are simultaneously updated with the contents of the input latches.
14	$\overline{FSIN}$	Level-triggered control input (active low). This is the frame synchronization signal for the input data. When $\overline{FSIN}$ goes low, it enables the input shift register, and data is transferred on the falling edges of CLKIN. If the address bits are valid, the 12-bit DAC data is transferred to the appropriate input latch on the sixteenth falling edge after $\overline{FSIN}$ goes low.
15	SDIN	Serial data input. The device accepts a 16-bit word. DB0 and DB1 are DAC select bits. DB2 and DB3 are device address bits. DB4 to DB15 contain the 12-bit data to be loaded to the selected DAC.
16	CLKIN	Clock Input. Data is clocked into the input shift register on the falling edges of CLKIN. Add a pull-down resistor on the clock line to avoid timing issues.
17	A1	Device address pin. This input in association with A0 gives the device an address. If DB2 and DB3 of the serial input stream do not correspond to this address, the data which follows is ignored and not loaded to any input latch. However, it will appear at SDOUT irrespective of this.
18	A0	Device address pin. This input in association with A1 gives the device an address.
19	$V_{REF}A$	DAC A reference input.
20	$R_{FB}A$	Feedback resistor for DAC A.
21	$I_{OUT1}A$	I_{OUT1} terminal for DAC A.
22	$I_{OUT2}A$	I_{OUT2} terminal for DAC A. This should normally connect to the signal ground of the system.
23	V_{REFB}	DAC B reference input.
24	$R_{FB}B$	Feedback resistor for DAC B.
25	$I_{OUT1}B$	I_{OUT1} terminal for DAC B.
26	N/C	No Connect pin.
27	AGND	This pin connects to the back gates of the current steering switches. It should be connected to the signal ground of the system.
28	$I_{OUT2}B$	I_{OUT2} terminal for DAC B. This should normally connect to the signal ground of the system.

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Gain Error
Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustable to zero with an external potentiometer.

Output Leakage Current
Output leakage current is current which flows in the DAC ladder switches when these are turned off. For the I_{OUT1} terminal, it can be measured by loading all 0s to the DAC and be measured by loading all 0s to the DAC and measuring the I_{OUT1} current. Minimum current will flow in the I_{OUT2} line when the DAC is loaded with all 1s. This is a combination of the switch leakage current and the ladder termination resistor current. The I_{OUT2} leakage current is typically equal to that in I_{OUT1}.

Output Capacitance
This is the capacitance from the I_{OUT1} pin to AGND.

Output Voltage Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For the AD7564, it is specified with the AD843 as the output op amp.

Digital to Analog Glitch Impulse
This is the amount of charge injected into the analog output when the inputs change state. It is normally specified as the area of the glitch in either pA-secs or nV-secs, depending upon whether the glitch is measured as a current or voltage signal. It is measured with the reference input connected to AGND and the digital inputs toggled between all 1s and all 0s.

AC Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC I_{OUT} terminal, when all 0s are loaded in the DAC.

Channel-to-Channel Isolation
Channel-to-channel isolation refers to the proportion of input signal from one DAC's reference input which appears at the output of any other DAC in the device and is expressed in dBs.

Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as the Digital Crosstalk and is specified in nV-secs.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up at on the I_{OUT} pin and subsequently on the op amp output. This noise is digital feedthrough.

Table I. AD7564 Loading Sequence

DB15											DB0				
DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	A1	A0	DS1	DS0

Table II. DAC Selection

DS1	DS0	Function
0	0	DAC A Selected
0	1	DAC B Selected
1	0	DAC C Selected
1	1	DAC D Selected

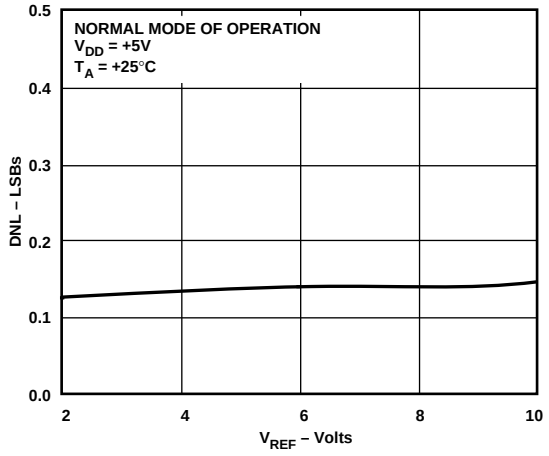


Figure 3. Differential Nonlinearity Error vs. V_{REF} (Normal Mode)

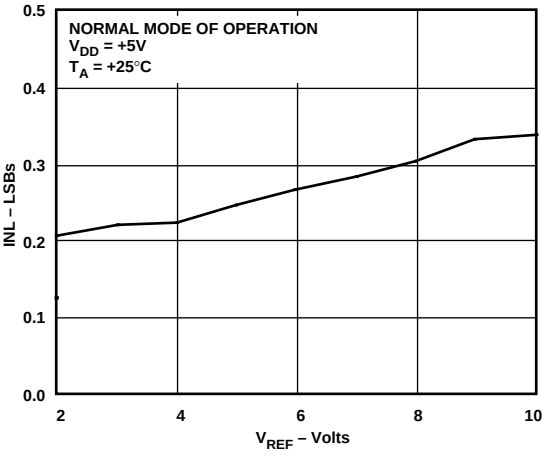


Figure 6. Integral Nonlinearity Error vs. V_{REF} (Normal Mode)

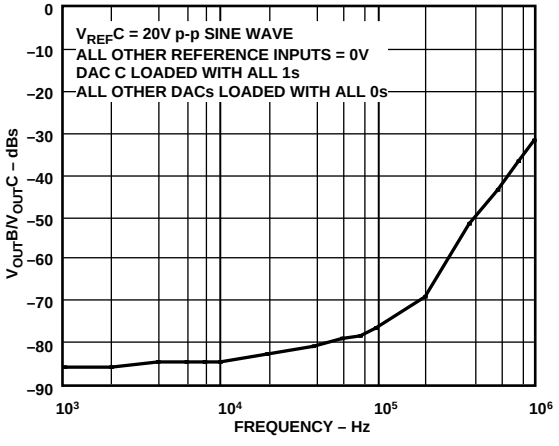


Figure 4. Channel-to-Channel Isolation (1 DAC to 1 DAC)

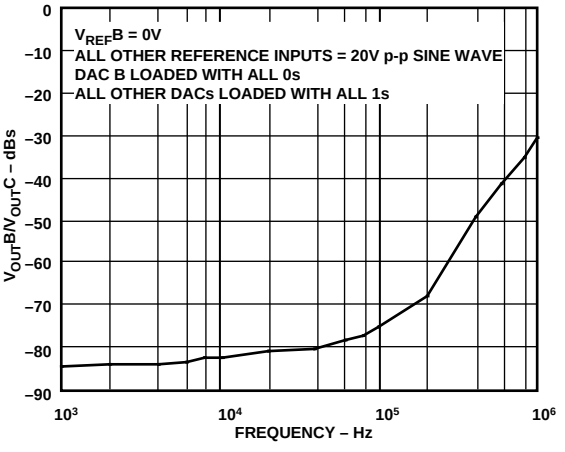


Figure 7. Channel-to-Channel Isolation (1 DAC to All Other DACs)

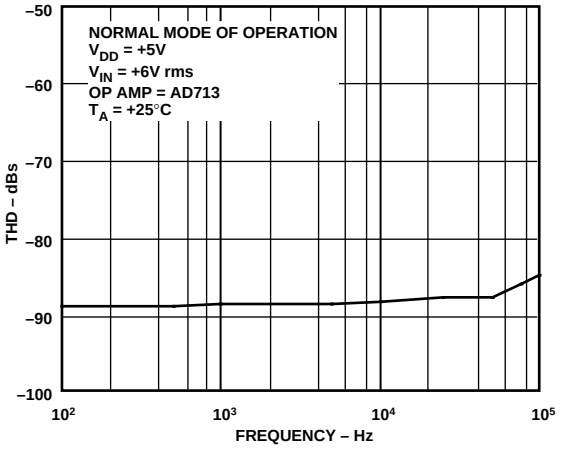


Figure 5. Total Harmonic Distortion vs. Frequency (Normal Mode)

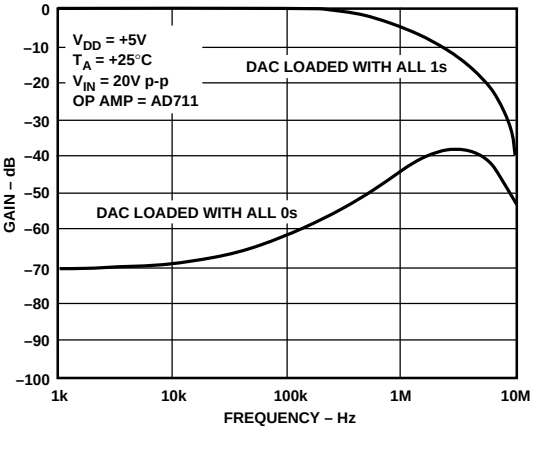


Figure 8. Multiplying Frequency Response vs. Digital Code (Normal Mode)

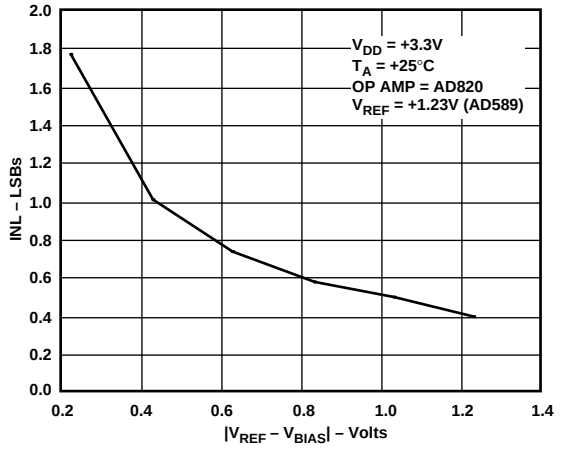


Figure 9. Integral Nonlinearity Error vs. V_{REF} (Biased Mode)

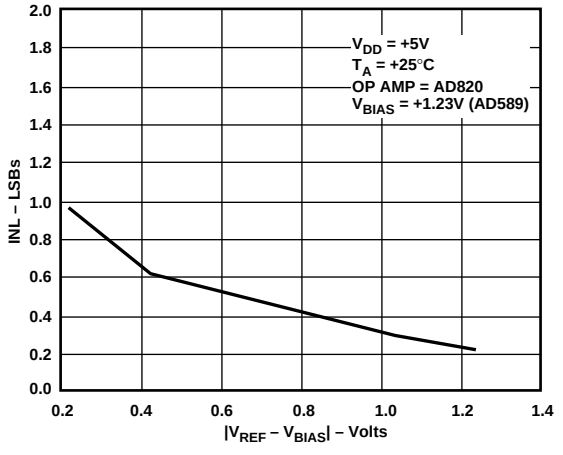


Figure 10. Integral Nonlinearity Error vs. V_{REF} (Biased Mode)

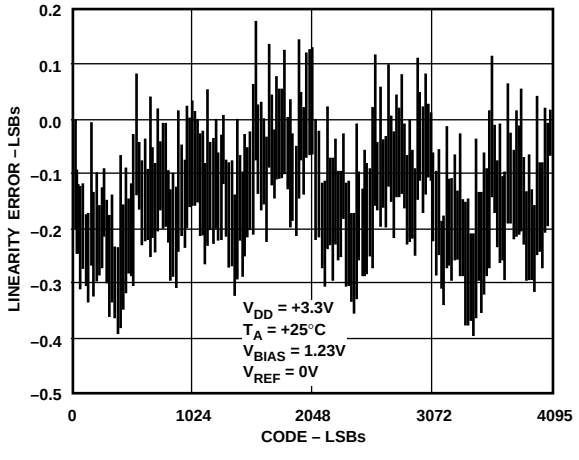


Figure 11. All Codes Linearity Plot (Biased Mode)

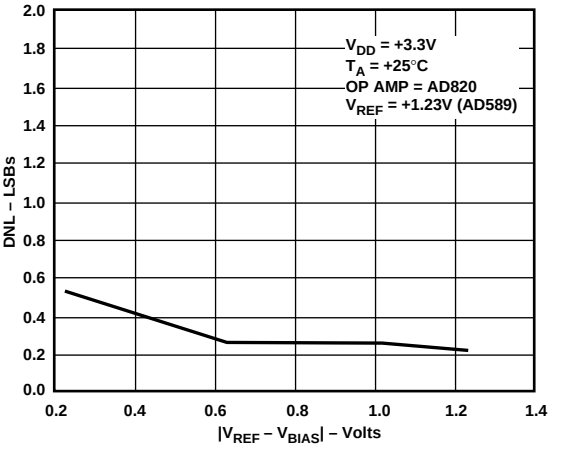


Figure 12. Differential Nonlinearity Error vs. V_{REF} (Biased Mode)

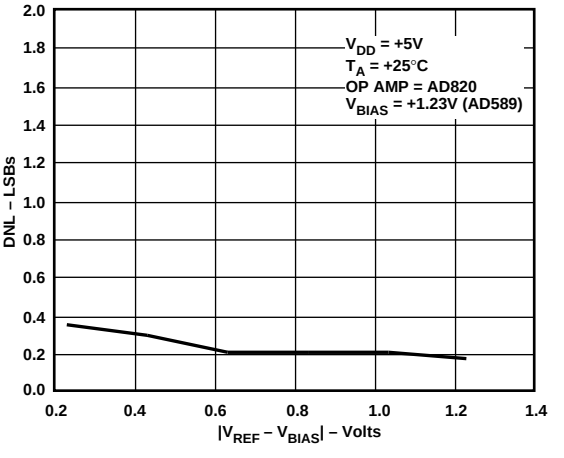


Figure 13. Differential Nonlinearity Error vs. V_{REF} (Biased Mode)

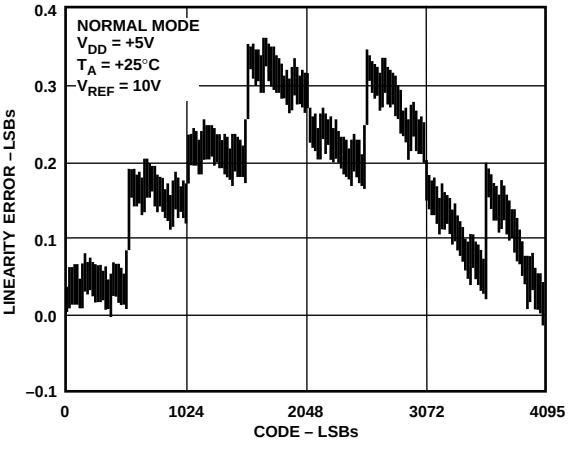


Figure 14. All Codes Linearity Plot (Normal Mode)

GENERAL DESCRIPTION

D/A Section

The AD7564 contains four 12-bit current output D/A converters. A simplified circuit diagram for one of the D/A converters is shown in Figure 15.

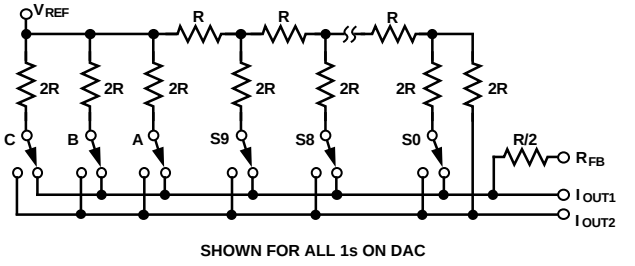


Figure 15. Simplified D/A Circuit Diagram

A segmented scheme is used whereby the 2 MSBs of the 12-bit data word are decoded to drive the three switches A, B and C. The remaining 10 bits of the data word drive the switches S0 to S9 in a standard R-2R ladder configuration.

Each of the switches A to C steers 1/4 of the total reference current with the remaining current passing through the R-2R section.

All DACs have separate V_{REF}, I_{OUT1}, I_{OUT2} and R_{FB} pins.

When an output amplifier is connected in the standard configuration of Figure 17, the output voltage is given by:

$$V_{OUT} = D \times V_{REF}$$

where D is the fractional representation of the digital word loaded to the DAC. Thus, in the AD7564, D can be set from 0 to 4095/4096.

Interface Section

The AD7564 is a serial input device. Three input signals control the serial interface. These are $\overline{FSIN}$, CLKIN and SDIN. The timing diagram is shown in Figure 1.

Data applied to the SDIN pin is clocked into the input shift register on each falling edge of CLKIN. SDOUT is the shift register output. It allows multiple devices to be connected in a daisy chain fashion with the SDOUT pin of one device connected to the SDIN of the next device. $\overline{FSIN}$ is the frame synchronization for the device.

When the sixteen bits have been received in the input shift register, DB2 and DB3 (A0 and A1) are checked to see if they correspond to the state on pins A0 and A1. If it does, then the word is accepted. Otherwise, it is disregarded. This allows the user to address a number of AD7564s in a very simple fashion. DB1 and DB0 of the 16-bit word determine which of the four DAC input latches is to be loaded. When the $\overline{LDAC}$ line goes low, all four DAC latches in the device are simultaneously loaded with the contents of their respective input latches and the outputs change accordingly.

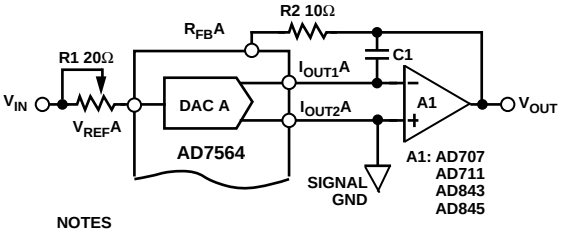
Bringing the $\overline{CLR}$ line low resets the DAC latches to all 0s. The input latches are not affected so that the user can revert to the previous analog output if desired.

Figure 16. Input Logic

UNIPOLAR BINARY OPERATION

(2-Quadrant Multiplication)

Figure 17 shows the standard unipolar binary connection diagram for one of the DACs in the AD7564. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication. Resistors R1 and R2 allow the user to adjust the DAC gain error. Offset can be removed by adjusting the output amplifier offset voltage.



NOTES
1. ONLY ONE DAC IS SHOWN FOR CLARITY.
2. DIGITAL INPUT CONNECTIONS ARE OMITTED.
3. C1 PHASE COMPENSATION (5–15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

Figure 17. Unipolar Binary Operation

A1 should be chosen to suit the application. For example, the AD707 is ideal for very low bandwidth applications while the AD843 and AD845 offer very fast settling time in wide bandwidth applications. Appropriate multiple versions of these amplifiers can be used with the AD7564 to reduce board space requirements.

The code table for Figure 17 is shown in Table III.

Table III. Unipolar Binary Code Table

Digital Input MSB . . . LSB	Analog Output (V_{OUT} as Shown in Figure 17)
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0001	$-V_{REF}$ (2049/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096)
0111 1111 1111	$-V_{REF}$ (2047/4096)
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	$-V_{REF}$ (0/4096) = 0

NOTE
Nominal LSB size for the circuit of Figure 17 is given by: V_{REF} (1/4096).

BIPOLAR OPERATION

4-Quadrant Multiplication)

Figure 18 shows the standard connection diagram for bipolar operation of any one of the DACs in the AD7564. The coding is offset binary as shown in Table IV. When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication. To maintain the gain error specifications, resistors R3, R4 and R5 should be ratio matched to 0.01%.

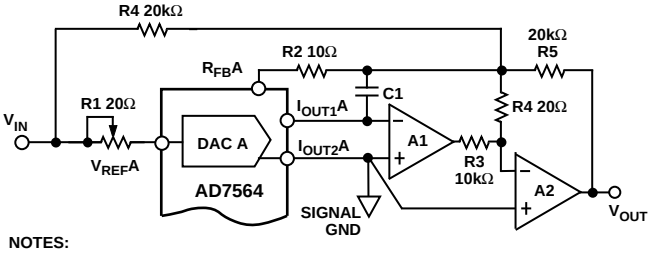


Figure 18. Bipolar Operation (4-Quadrant Multiplication)

Table IV. Bipolar (Offset Binary) Code Table

Digital Input MSB . . . LSB	Analog Output (V_{OUT} as Shown in Figure 18)
1111 1111 1111	$-V_{REF}$ (2047/2048)
1000 0000 0001	$-V_{REF}$ (1/2048)
1000 0000 0000	$-V_{REF}$ (0/2048 = 0)
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0001	$-V_{REF}$ (2047/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048) = $-V_{REF}$

NOTE

Nominal LSB size for the circuit of Figure 18 is given by: V_{REF} (1/2048).

SINGLE SUPPLY APPLICATIONS

The "–B" versions of the AD7564 are specified and tested for single supply applications. Figure 19 shows a typical circuit for operation with a single +3.3 V to +5 V supply.

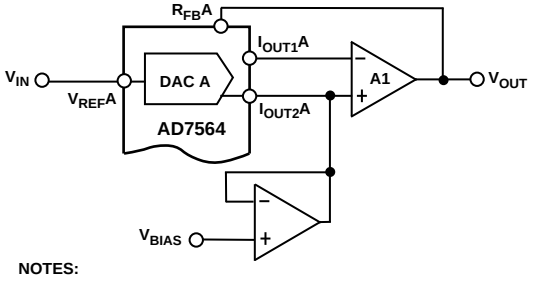


Figure 19. Single Supply Current Mode Operation

In the current mode circuit of Figure 19, I_{OUT2} and hence I_{OUT1}, is biased positive by an amount V_{BIAS}. For the circuit to operate correctly, the DAC ladder termination resistor must be connected internally to I_{OUT2}. This is the case with the AD7564. The output voltage is given by:

$$V_{OUT} = \left\{ D \times \frac{R_{FB}}{R_{DAC}} \times (V_{BIAS} - V_{IN}) \right\} + V_{BIAS}$$

As D varies from 0 to 4095/4096, the output voltage varies from $V_{OUT} = V_{BIAS}$ to $V_{OUT} = 2\ V_{BIAS} - V_{IN}$. V_{BIAS} should be a low impedance source capable of sinking and sourcing all possible variations in current at the I_{OUT2} terminal without any problems.

Voltage Mode Circuit

Figure 20 shows DAC A of the AD7564 operating in the voltage-switching mode. The reference voltage, V_{IN} is applied to the I_{OUT1} pin, I_{OUT2} is connected to AGND and the output voltage is available at the V_{REF} terminal. In this configuration, a positive reference voltage results in a positive output voltage; making single supply operation possible. The output from the DAC is a voltage at a constant impedance (the DAC ladder resistance). Thus, an op amp is necessary to buffer the output voltage. The reference voltage input no longer sees a constant input impedance, but one which varies with code. So, the voltage input should be driven from a low impedance source.

It is important to note that V_{IN} is limited to low voltages because the switches in the DAC no longer have the same source-drain voltage. As a result, their on-resistance differs and this degrades the integral linearity of the DAC. Also, V_{IN} must not go negative by more than 0.3 volts or an internal diode will turn on, causing possible damage to the device. This means that the full-range multiplying capability of the DAC is lost.

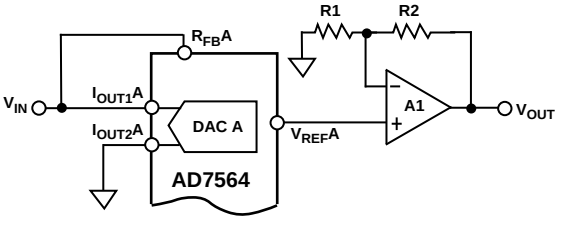


Figure 20. Single Supply Voltage Switching Mode Operation

MICROPROCESSOR INTERFACING

AD7564 to 80C51 Interface

A serial interface between the AD7564 and the 80C51 microcontroller is shown in Figure 21. TXD of the 80C51 drives SCLK of the AD7564 while RXD drives the serial data line of the part. The FSIN signal is derived from the port line P3.3.

The 80C51 provides the LSB of its SBUF register as the first bit in the serial data stream. Therefore, the user will have to ensure that the data in the SBUF register is arranged correctly so that the data word transmitted to the AD7564 corresponds to the loading sequence shown in Table I. When data is to be transmitted to the part, P3.3 is taken low. Data on RXD is valid on the falling edge of TXD. The 80C51 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7564, P3.3 is left low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7564. When the second serial transfer is complete, the P3.3 line is taken high. Note that the 80C51 outputs the serial data byte in a format which has the LSB first. The AD7564 expects the MSB first. The 80C51 transmit routine should take this into account.

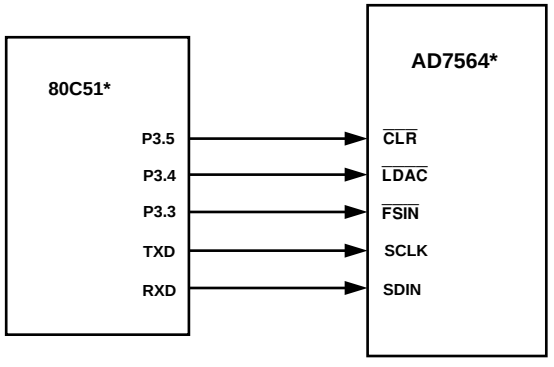


Figure 21. AD7564 to 80C51 Interface

$\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ on the AD7564 are also controlled by 80C51 port outputs. The user can bring $\overline{\text{LDAC}}$ low after every two bytes have been transmitted to update the DAC which has been programmed. Alternatively, it is possible to wait until all the input registers have been loaded (sixteen byte transmits) and then update the DAC outputs.

AD7564 to 68HC11 Interface

Figure 22 shows a serial interface between the AD7564 and the 68HC11 microcontroller. SCK of the 68HC11 drives SCLK of the AD7564 while the MOSI output drives the serial data line of the AD7564. The FSIN signal is derived from a port line (PC7 shown).

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 0 and its CPHA bit is a 1. When data is to be transmitted to the part, PC7 is taken low. When the 68HC11 is configured like this, data on MOSI is valid on the falling edge of SCK. The 68HC11 transmits its serial data in 8-bit bytes (MSB first), with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7564 , PC7 is left low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7564. When the second serial transfer is complete, the PC7 line is taken high.

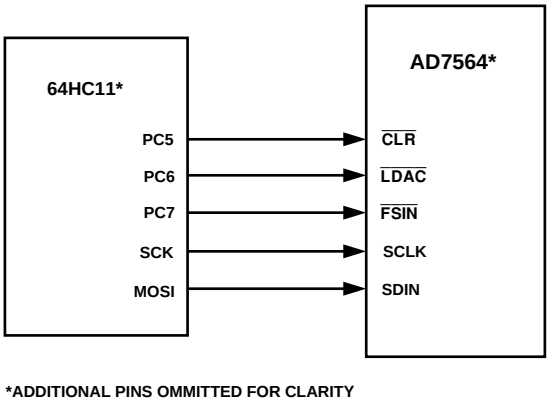


Figure 22. AD7564 to 64HC11 Interface

In Figure 22, $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ are controlled by the PC6 and PC5 port outputs. As with the 80C51, each DAC of the AD7564 can be updated after each two-byte transfer, or else all DACs can be simultaneously updated. This interface is suitable for both 3 V and 5 V versions of the 68HC11 microcontroller.

AD7564 to ADSP-2101/ADSP-2103 Interface

Figure 23 shows a serial interface between the AD7564 and the ADSP-2101/ADSP-2103 digital signal processors. The ADSP-2101 operates from 5 V while the ADSP-2103 operates from 3 V supplies. These processors are set up to operate in the SPORT Transmit Alternate Framing Mode.

The following DSP conditions are recommended: Internal SCLK; Active low Framing Signal; 16-bit word length. Transmission is initiated by writing a word to the TX register after the SPORT has been enabled. The data is then clocked out on every rising edge of SCLK after TFS goes low. TFS stays low until the next data transfer.

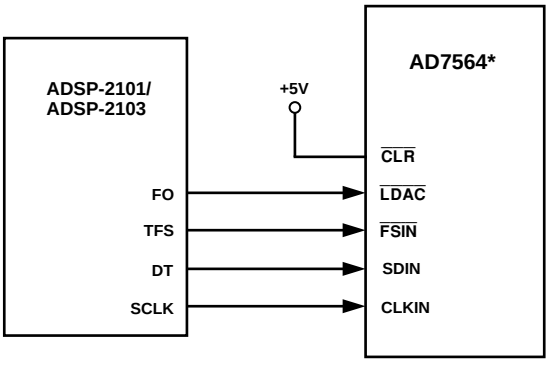


Figure 23. AD7564 to ADSP-2101/ADSP-2103 Interface

AD7564 to TMS320C25 Interface

Figure 24 shows an interface circuit for the TMS320C25 digital signal processor. The data on the DX pin is clocked out of the processor's Transmit Shift Register by the CLKX signal. Sixteen-bit transmit format should be chosen by setting the FO bit in the ST1 register to 0. The transmit operation begins when data is written into the data transmit register of the TMS320C25. This data will be transmitted when the FSX line goes low while CLKX is high or going high. The data, starting with the MSB, is then shifted out to the DX pin on the rising edge of CLKX. When all bits have been transmitted, the user can update the DAC outputs by bringing the XF output flag low.

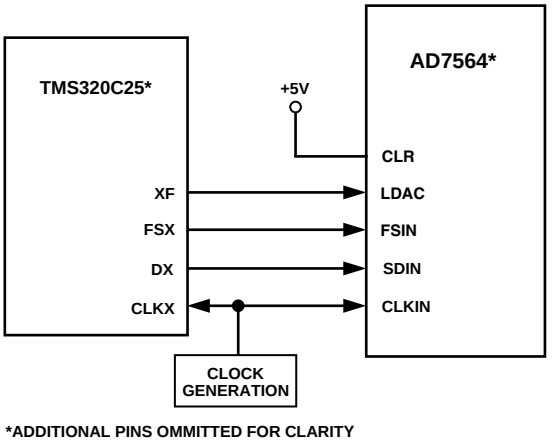


Figure 24. AD7564 to TMS320C25 Interface

APPLICATION HINTS

Output Offset

CMOS D/A converters in circuits such as Figures 17, 18 and 19 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. For the AD7564 to maintain specified accuracy with V_{REF} at 10 V, it is recommended that V_{OS} be no greater than 500 μV, or $(50 \times 10^{-6}) \times (V_{REF})$, over the temperature range of operation. Suitable amplifiers include the ADOP-07, ADOP-27, AD711, AD845 or multiple versions of these.

Temperature Coefficients

The gain temperature coefficient of the AD7564 has a maximum value of 5 ppm/°C and a typical value of 2 ppm/°C. This corresponds to gain shifts of 2 LSBs and 0.8 LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale in Figures 17 and 18, their temperature coefficients should be taken into account. For further information see "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs," Application Note, Publication Number E630c-5-3/86, available from Analog Devices.

High Frequency Considerations

The output capacitances of the AD7564 DACs work in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor. This is shown as C1 in Figures 17 and 18.

APPLICATIONS

Programmable State Variable Filter

The AD7564 with its multiplying capability and fast settling time is ideal for many types of signal conditioning applications. The circuit of Figure 25 shows its use in a state variable filter design. This type of filter has three outputs: low pass, high pass and bandpass. The particular version shown in Figure 25 uses the AD7564 to control the critical parameters f_O, Q and A_O. Instead of several fixed resistors, the circuit uses the DAC equivalent resistances as circuit elements.

Thus, R1 in Figure 25 is controlled by the 12-bit digital word loaded to DAC A of the AD7564. This is also the case with R2, R3 and R4. The fixed resistor R5 is the feedback resistor, $R_{FB}B$.

$$\textit{DAC Equivalent Resistance, } R_{EQ} = (R_{LADDER} \times 4096)/N$$

where: R_{LADDER} is the DAC ladder resistance

N is the DAC Digital Code in Decimal ($0 < N < 4096$)

In the circuit of Figure 25:

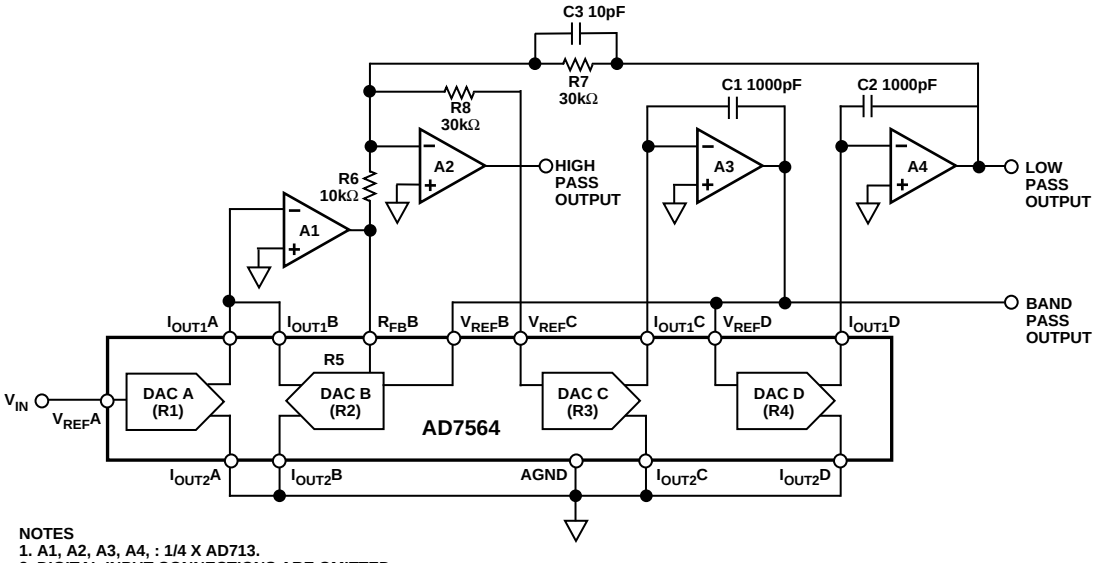
C1 = C2, R7 = R8, R3 = R4 (i.e., the same code is loaded to each DAC).

$$\textit{Resonant Frequency, } f_O = 1/(2\,\pi\, R3C1)$$

$$\textit{Quality Factor, } Q = (R6/R8) \times (R2/R5)$$

$$\textit{Bandpass Gain, } A_O = -R2/R1$$

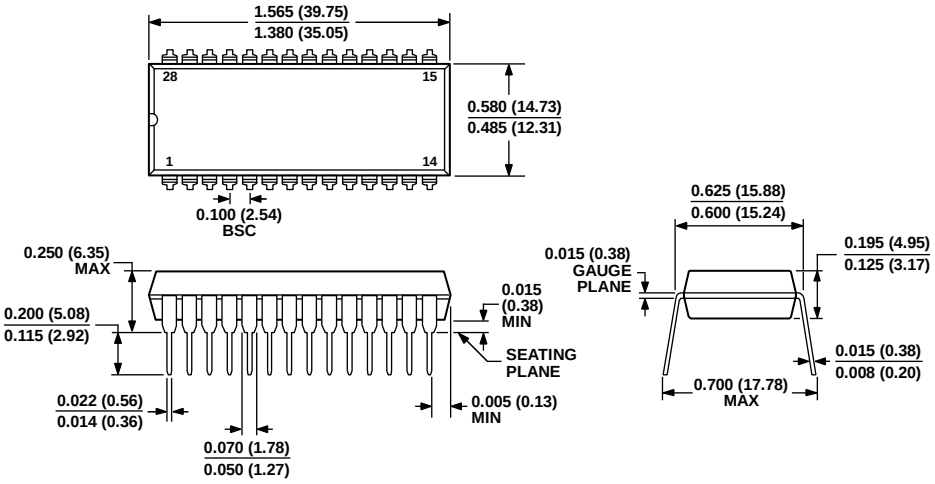
Using the values shown in Figure 25, the Q range is 0.3 to 5 and the f_O range is 0 to 12 kHz.



NOTES
1. A1, A2, A3, A4, : 1/4 X AD713.
2. DIGITAL INPUT CONNECTIONS ARE OMITTED.
3. C3 IS A COMPENSATION CAPACITOR TO ELIMINATE Q AND GAIN VARIATIONS CAUSED BY AMPLIFIER GAIN AND BANDWIDTH LIMITATIONS.

Figure 25. Programmable 2nd Order State Variable Filter

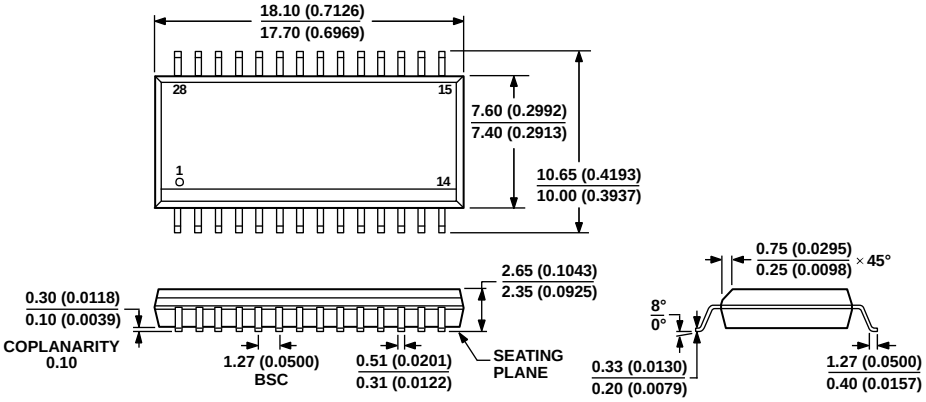
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-011
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE LEADS.

071006-A

Figure 26. 28-Lead Plastic Dual In-Line Package [PDIP]
Wide Body
(N-28-2)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

06-07-2006-A

Figure 27. 28-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-28)
Dimensions shown in millimeters and (inches)

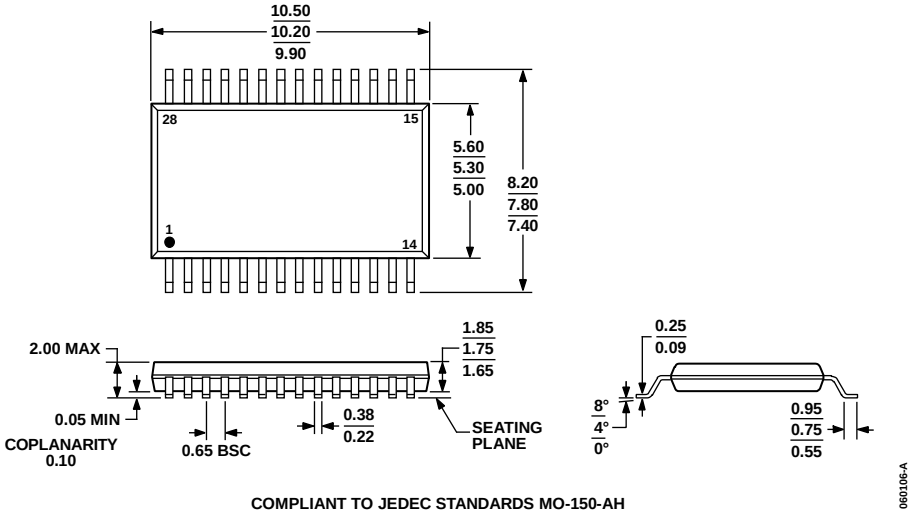


Figure 28. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7564AR-B	−40°C to +85°C	28-Lead SOIC_W	RW-28
AD7564ARS-B	−40°C to +85°C	28-Lead SSOP	RS-28
AD7564ARS-BREEL	−40°C to +85°C	28-Lead SSOP	RS-28
AD7564ARSZ-B	−40°C to +85°C	28-Lead SSOP	RS-28
AD7564ARSZ-BREEL	−40°C to +85°C	28-Lead SSOP	RS-28
AD7564ARZ-B	−40°C to +85°C	28-Lead SOIC_W	RW-28
AD7564ARZ-BREEL	−40°C to +85°C	28-Lead SOIC_W	RW-28
AD7564BN	−40°C to +85°C	28-Lead PDIP	N-28-2
AD7564BNZ	−40°C to +85°C	28-Lead PDIP	N-28-2
AD7564BR	−40°C to +85°C	28-Lead SOIC_W	RW-28
AD7564BR-REEL	−40°C to +85°C	28-Lead SOIC_W	RW-28
AD7564BRS	−40°C to +85°C	28-Lead SSOP	RS-28
AD7564BRS-REEL	−40°C to +85°C	28-Lead SSOP	RS-28
AD7564BRSZ	−40°C to +85°C	28-Lead SSOP	RS-28
AD7564BRSZ-REEL	−40°C to +85°C	28-Lead SSOP	RS-28
AD7564BRZ	−40°C to +85°C	28-Lead SOIC_W	RW-28
AD7564BRZ-REEL	−40°C to +85°C	28-Lead SOIC_W	RW-28

REVISION HISTORY

2/12—Rev. A to Rev. B

Changes to Pin 16 Description 7
Updated Outline Dimensions 17
Changes to Ordering Guide 17

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D10540-0-2/12(B)

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