

NCP51200, NCV51200

3 Amp V_{TT} Termination Regulator DDR1, DDR2, DDR3, LPDDR3, DDR4

The NCP51200 is a source/sink Double Data Rate (DDR) termination regulator specifically designed for low input voltage and low-noise systems where space is a key consideration.

The NCP51200 maintains a fast transient response and only requires a minimum output capacitance of 20 μ F. The NCP51200 supports a remote sensing function and all power requirements for DDR V_{TT} bus termination. The NCP51200 can also be used in low-power chipsets and graphics processor cores that require dynamically adjustable output voltages.

The NCP51200 is available in the thermally-efficient DFN10 Exposed Pad package, and is rated both Green and Pb-free.

Features

- For Automotive Applications
- Input Voltage Rails: Supports 2.5 V, 3.3 V and 5 V Rails
- PV_{CC} Voltage Range: 1.1 to 3.5 V
- Integrated Power MOSFETs
- Fast Load-Transient Response
- P_{GOOD} – Logic output pin to Monitor V_{TT} Regulation
- EN – Logic input pin for Shutdown mode
- V_{RI} – Reference Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider
- Remote Sensing (V_{TTS})
- Built-in Soft Start, Under Voltage Lockout and Over Current Limit
- Thermal Shutdown
- Small, Low-Profile 10-pin, 3x3 DFN Package
- NCV51200MWTXG – Wettable Flank Option for Enhanced Optical Inspection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable*
- These Devices are Pb-Free and are RoHS Compliant

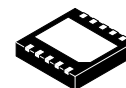
Applications

- DDR Memory Termination
- Desktop PC's, Notebooks, and Workstations
- Servers and Networking equipment
- Telecom/Datacom, GSM Base Station
- Graphics Processor Core Supplies
- Set Top Boxes, LCD-TV/PDP-TV, Copier/Printers
- Chipset/RAM Supplies as Low as 0.5 V
- Active Bus Termination



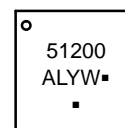
ON Semiconductor®

<http://onsemi.com>



DFN10, 3x3, 0.5P
CASE 485C

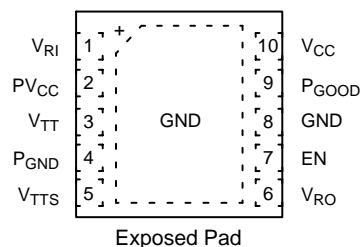
MARKING DIAGRAM



51200 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTION



ORDERING INFORMATION

Device	Package	Shipping†
NCP51200MNTXG	DFN10 (Pb-Free)	3000 / Tape & Reel
NCV51200MNTXG*	DFN10 (Pb-Free)	3000 / Tape & Reel
NCV51200MWTXG*	DFN10 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP51200, NCV51200

PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Pin Function
1	V _{RI}	V _{TT} External Reference Input (set to V _{DDQ} / 2 thru resistor network).
2	PV _{CC}	Power input. Internally connected to the output source MOSFET.
3	V _{TT}	Power Output of the Linear Regulator.
4	P _{GND}	Power Ground. Internally connected to the output sink MOSFET.
5	V _{TTS}	V _{TT} Sense Input. The V _{TTS} pin provides accurate remote feedback sensing of V _{TT} . Connect V _{TTS} to the remote DDR termination bypass capacitors.
6	V _{RO}	Independent Buffered V _{TT} Reference Output. Sources and sinks over 5 mA. Connect to GND thru 0.1 μF ceramic capacitor.
7	EN	Shutdown Control Input. CMOS compatible input. Logic high = enable, logic low = shutdown. Connect to V _{DDQ} for normal operation.
8	GND	Common Ground.
9	P _{GOOD}	Power Good (Open Drain output).
10	V _{CC}	Analog power supply input. Connect to GND thru a 1 – 4.7 μF ceramic capacitor.
	THERMAL PAD	Pad for thermal connection. The exposed pad must be connected to the ground plane using multiple vias for maximum power dissipation performance.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V _{CC} , PV _{CC} , V _{TT} , V _{TTS} , V _{RI} , V _{RO} (Note 1)		-0.3 to 6.0	V
EN, P _{GOOD} (Note 1)		-0.3 to 6.0	V
P _{GND} to GND (Note 1)		-0.3 to +0.3	V
Storage Temperature	T _{STG}	-55 to 150	°C
Operating Junction Temperature Range	T _J	150	°C
ESD Capability, Human Body Model (Note 2)	ESD _{HBM}	2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

2. This device series incorporates ESD protection and is tested by the following method:

ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)

ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)

Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

DISSIPATION RATINGS

Package	T _A = 25°C Power Rating	Derating Factor above T _A = 25°C	T _A = +85°C Power Rating
10-Pin DFN	1.92 W	19 mW/°C	0.79 W

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	2.375 to 5.5	V
Voltage Range	V _{RO}	-0.1 to 1.8	V
	V _{RI}	0.5 to 1.8	
	PV _{CC} , V _{TT} , V _{TTS} , EN, P _{GOOD}	-0.1 to 3.5	
	P _{GND}	-0.1 to +0.1	
Operating Free-Air Temperature	T _A	-40 to +125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NCP51200, NCV51200

ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$; $V_{CC} = 3.3\text{ V}$; $PV_{CC} = 1.8\text{ V}$; $V_{RI} = V_{TTS} = 0.9\text{ V}$; $EN = V_{CC}$; $C_{OUT} = 3 \times 10\ \mu\text{F}$ (Ceramic); unless otherwise noted.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
-----------	------------	--------	-----	-----	-----	-------

Supply Current

V_{CC} Supply Current	$T_A = +25^{\circ}\text{C}$, $EN = 3.3\text{ V}$, No Load	I_{VCC}		0.7	1	mA
V_{CC} Shutdown Current	$T_A = +25^{\circ}\text{C}$, $EN = 0\text{ V}$, $V_{RI} = 0\text{ V}$, No Load	$I_{VCC\ SHD}$		65	80	μA
	$T_A = +25^{\circ}\text{C}$, $EN = 0\text{ V}$, $V_{RI} > 0.4\text{ V}$, No Load			200	400	
V_{CC} UVLO Threshold	Wake-up, $T_A = +25^{\circ}\text{C}$	V_{UVLO}	2.2	2.3	2.375	V
	Hysteresis		50			
PV_{CC} Supply Current	$T_A = +25^{\circ}\text{C}$, $EN = 3.3\text{ V}$, No Load	I_{PVCC}		1	50	μA
PV_{CC} Shutdown Current	$T_A = +25^{\circ}\text{C}$, $EN = 0\text{ V}$, No Load	$I_{PVCC\ SHD}$		0.1	50	μA

V_{TT} Output

V_{TT} Output Offset Voltage	$V_{RO} = 1.25\text{ V}$ (DDR1), $I_{TT} = 0\text{ A}$	V_{OS}	-15		+15	mV
	$V_{RO} = 0.9\text{ V}$ (DDR2), $I_{TT} = 0\text{ A}$		-15		+15	
	$PV_{CC} = 1.5\text{ V}$, $V_{RO} = 0.75\text{ V}$ (DDR3), $I_{TT} = 0\text{ A}$		-15		+15	
V_{TT} Voltage Tolerance to V_{RO}	$-2\text{ A} \leq I_{TT} \leq +2\text{ A}$		-25		+25	mV
Source Current Limit	$V_{TTS} = 90\% * V_{RO}$		3		4.5	A
Sink Current Limit	$V_{TTS} = 110\% * V_{RO}$		3.5		5.5	A
Soft-start Current Limit Timeout		T_{SS}		200		μs
Discharge MOSFET On-resistance	$V_{RI} = 0\text{ V}$, $V_{TT} = 0.3\text{ V}$, $EN = 0\text{ V}$, $T_A = +25^{\circ}\text{C}$	R_{DIS}		18	25	Ω

V_{RI} - Input Reference

V_{RI} Voltage Range		V_{RI}	0.5		1.8	V
V_{RI} Input-bias Current	$EN = 3.3\text{ V}$	I_{RI}			+1	μA
V_{RI} UVLO Voltage	V_{RI} rising	$V_{RI\ UVLO}$	360	390	435	mV
	Hysteresis	$V_{RI\ HYS}$	60			

V_{RO} - Output Reference

V_{RO} Voltage			V_{RI}			V
V_{RO} Voltage Tolerance to V_{RI}	$I_{RO} = \pm 10\text{ mA}$, $0.6\text{ V} \leq V_{RI} \leq 1.25\text{ V}$		-15		+15	mV
V_{RO} Source Current Limit	$V_{RO} = 0\text{ V}$		10	40		mA
V_{RO} Sink Current Limit	$V_{RO} = 0\text{ V}$		10	40		mA

P_{GOOD} - Powergood Comparator

P_{GOOD} Lower Threshold	(with respect to V_{RO})		-23.5%	-20%	-17.5%	V/V
P_{GOOD} Upper Threshold	(with respect to V_{RO})		17.5%	20%	23.5%	
P_{GOOD} Hysteresis			5%			
P_{GOOD} Start-up Delay	Start-up rising edge, V_{TTS} within 15% of V_{RO}		2			ms
P_{GOOD} Leakage Current	$V_{TTS} = V_{RI}$ ($P_{GOOD} = \text{True}$) $P_{GOOD} = V_{CC} + 0.2\text{ V}$				1	μA
$P_{GOOD} = \text{False}$ Delay	V_{TTS} is beyond $\pm 20\%$ P_{GOOD} trip thresholds		10			μs
P_{GOOD} Output Low Voltage	$I_{GOOD} = 4\text{ mA}$				0.4	V

NCP51200, NCV51200

ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$; $V_{CC} = 3.3\text{ V}$; $PV_{CC} = 1.8\text{ V}$; $V_{RI} = V_{TTS} = 0.9\text{ V}$; $EN = V_{CC}$; $C_{OUT} = 3 \times 10\ \mu\text{F}$ (Ceramic); unless otherwise noted.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Logic Input Threshold	EN Logic high	V_{IH}	1.7			V
	EN Logic low	V_{IL}			0.3	V
Hysteresis Voltage	EN pin	V_{ENHYS}	0.5			V
Logic Leakage Current	EN pin, $T_A = +25^{\circ}\text{C}$	I_{LEAK}	-1		+1	μA

Thermal Shutdown

Thermal Shutdown Temperature		T_{SD}		150		$^{\circ}\text{C}$
Thermal Shutdown Hysteresis		T_{SH}		25		$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

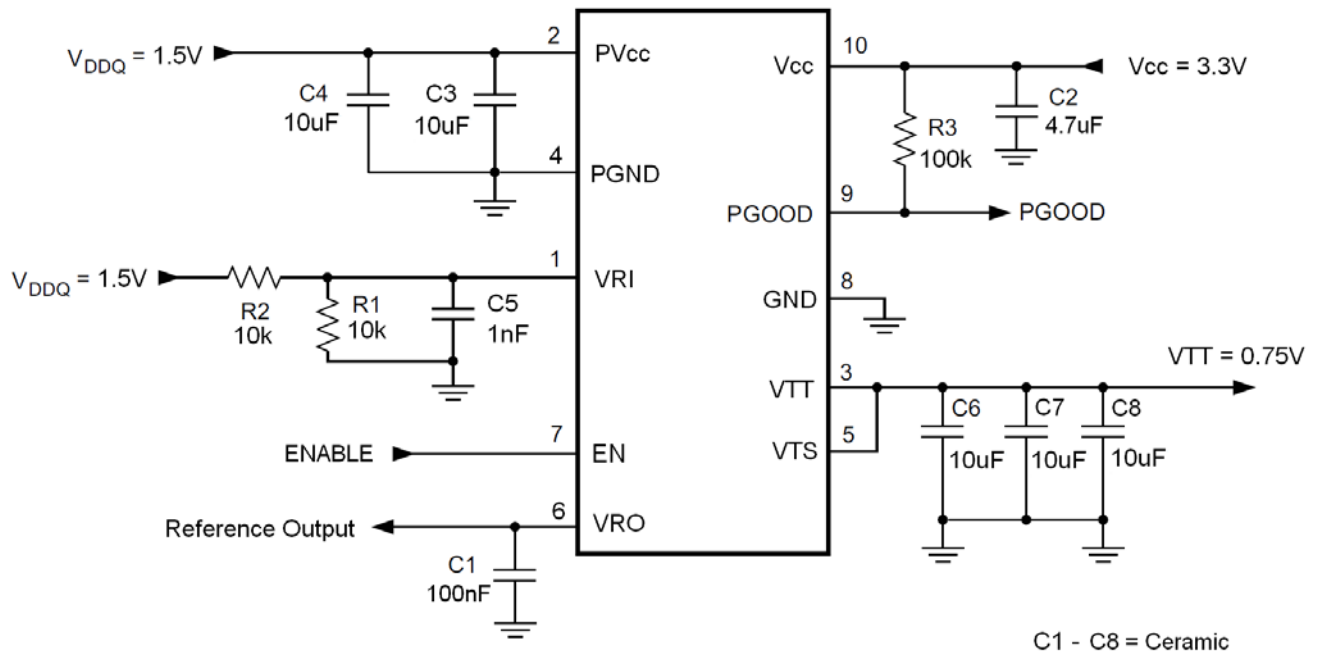


Figure 1. Typical DDR-3 Application Schematic

General

The NCP51200 is a sink/source tracking termination regulator specifically designed for low input voltage and low external component count systems where space is a key application parameter. The NCP51200 integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, V_{TTS} , should be connected to the positive terminal of the output capacitors as a separate trace from the high current path from V_{TT} .

V_{RI} – Generation of Internal Voltage Reference

The output voltage, V_{TT} , is regulated to V_{RO} . When V_{RI} is configured for standard DDR termination applications, V_{RI} can be set by an external equivalent ratio voltage divider connected to the memory supply bus (V_{DDQ}). The NCP51200 supports V_{RI} voltage from 0.5 V to 1.8 V, making it versatile and ideal for many types of low-power LDO applications.

V_{RO} – Reference Output

When it is configured for DDR termination applications, V_{RO} generates the DDR V_{TT} reference voltage for the memory application. It is capable of supporting both a sourcing and sinking load of 10 mA. V_{RO} becomes active when V_{RI} voltage rises to 435 mV and V_{CC} is above the UVLO threshold. When V_{RO} is less than 360 mV, it is disabled and subsequently discharges to GND through an internal 10 k Ω MOSFET. V_{RO} is independent of the EN pin state.

Soft Start

The soft-start function of the V_{TT} pin is achieved via a current clamp. The current clamp allows the output capacitors to be charged with low and constant current, providing a linear ramp-up of the output voltage. When

V_{TT} is outside of the power good window, the current clamp level is one-half of the full over-current limit (OCL) level. When V_{TT} rises or falls within the P_{GOOD} window, the current clamp level switches to the full OCL level.

The soft-start function is completely symmetrical; it works not only from GND to the V_{RO} voltage but also from PV_{CC} to the V_{RO} voltage.

EN – Enable Control

When EN is driven high, the NCP51200 V_{TT} regulator begins normal operation. When EN is driven low, V_{TT} is discharged to GND through an internal 18- Ω MOSFET. V_{REF} remains on when EN is driven low.

P_{GOOD} – PowerGood

The NCP51200 provides an open-drain P_{GOOD} output that goes high when the V_{TT} output is within $\pm 20\%$ of V_{RO} . P_{GOOD} de-asserts within 10 μ s after the output exceeds the limits of the PowerGood window. During initial V_{TT} startup, P_{GOOD} asserts high 2 ms after the V_{TT} enters power good window. Because P_{GOOD} is an open-drain output, a 100 k Ω , pull-up resistor between P_{GOOD} and a stable active supply voltage rail is required.

The LDO has a constant over-current limit (OCL). Note that the OCL level reduces by one-half when the output voltage is not within the power good window. This reduction is non-latch protection. For V_{CC} under-voltage lockout (UVLO) protection, the NCP51200 monitors V_{CC} voltage. When the V_{CC} voltage is lower than the UVLO threshold voltage, both the V_{TT} and V_{RO} regulators are powered off. This shutdown is also non-latch protection.

Thermal Shutdown with Hysteresis

If the NCP51200 is to operate in elevated temperatures for long durations, care should be taken to ensure that the maximum operating junction temperature is not exceeded. To guarantee safe operation, the NCP51200 provides on-chip thermal shutdown protection. When the chip junction temperature exceeds 150°C, the part will shutdown. When the junction temperature falls back to 125°C, the device resumes normal operation. If the junction temperature exceeds the thermal shutdown threshold then the V_{TT} and V_{RO} regulators are both shut off, discharged by the internal discharge MOSFETs. The shutdown is a non-latch protection.

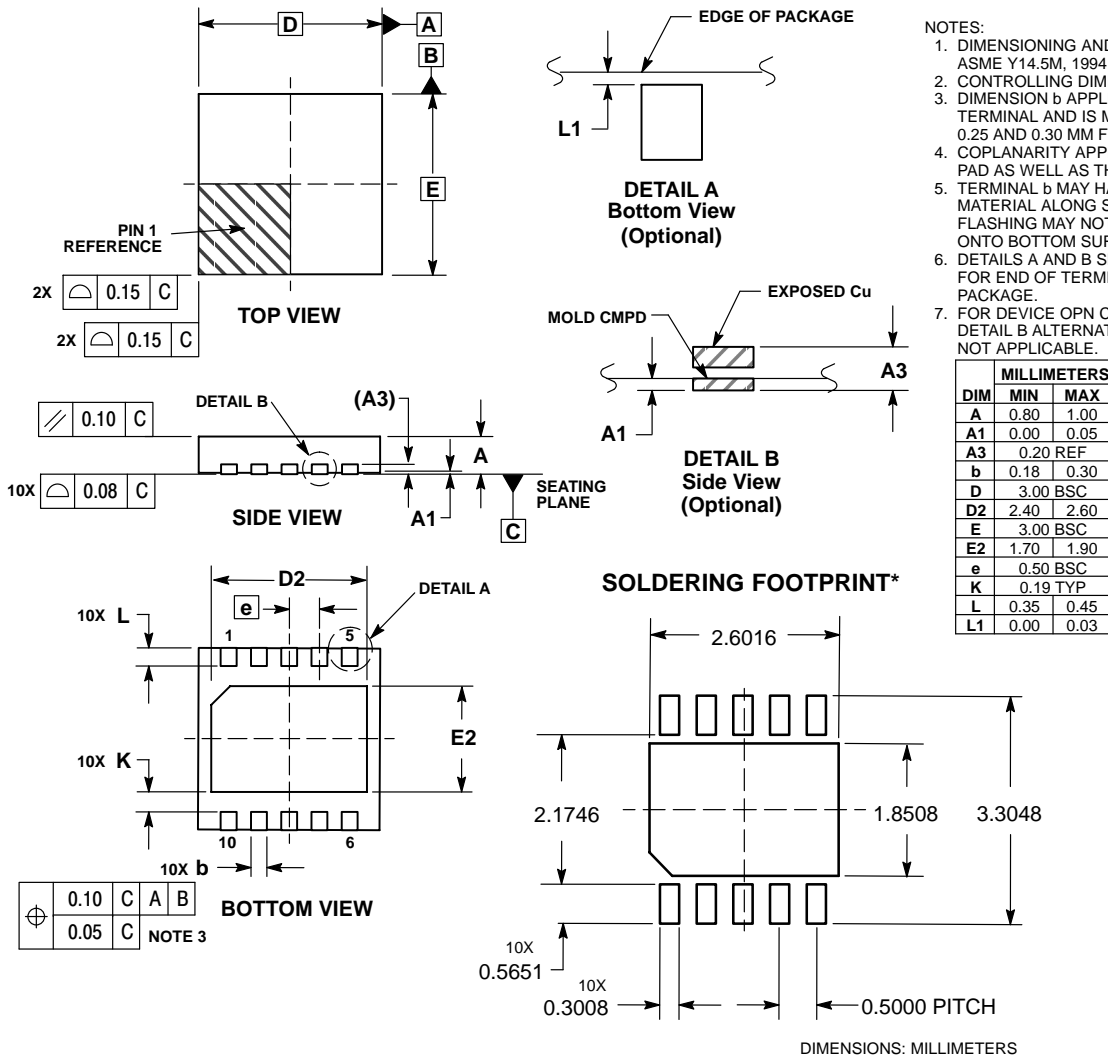
Tracking Startup and Shutdown

The NCP51200 also supports tracking startup and shutdown when EN is tied directly to the system bus and not used to turn on or turn off the device. During tracking startup, V_{TT} follows V_{RO} once V_{RI} voltage is greater than 435 mV. V_{RI} follows the rise of V_{DDQ} memory supply rail via a voltage divider. The typical soft-start time for the V_{DDQ} memory supply rail is approximately 3 ms, however it may vary depending on the system configuration. The SS time of the V_{TT} output no longer depends on the OCL setting, but it is a function of the SS time of the V_{DDQ} memory supply rail. P_{GOOD} is asserted 2 ms after V_{TT} is within $\pm 20\%$ of V_{RO} . During tracking shutdown, V_{TT} falls following V_{RO} until V_{RO} reaches 360 mV. Once V_{RO} falls below 360 mV, the internal discharge MOSFETs are turned on and quickly discharge both V_{RO} and V_{TT} to GND. P_{GOOD} is de-asserted once V_{TT} is beyond the $\pm 20\%$ range of V_{RO} .

NCP51200, NCV51200

PACKAGE DIMENSIONS

DFN10, 3x3, 0.5P
CASE 485C
ISSUE C



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А