TSOP, FP-BGA
Commercial Temp
Industrial Temp

64K x 16
1Mb Asynchronous SRAM

7, 8, 10, 12 ns
3.3 V V_{DD}
Center V_{DD} and V_{SS}

Features

- Fast access time: 7, 8, 10, 12 ns
- CMOS low power operation: 145/125/100/85 mA at minimum cycle time
- Single 3.3 V power supply
- All inputs and outputs are TTL-compatible
- Byte control
- Fully static operation
- Industrial Temperature Option: –40° to 85°C
- Package line up
  - GP: RoHS-compliant 400 mil, 44-pin TSOP Type II package
  - U: 6 mm x 8 mm Fine Pitch Ball Grid Array package
  - GU: RoHS-compliant 6 mm x 8 mm Fine Pitch Ball Grid Array package

Description

The GS71116A is a high speed CMOS static RAM organized as 65,536-words by 16-bits. Static design eliminates the need for external clocks or timing strobes. Operating on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS71116A is available in the 6 mm x 8 mm Fine Pitch BGA and 400 mil TSOP Type-II packages.

Pin Descriptions

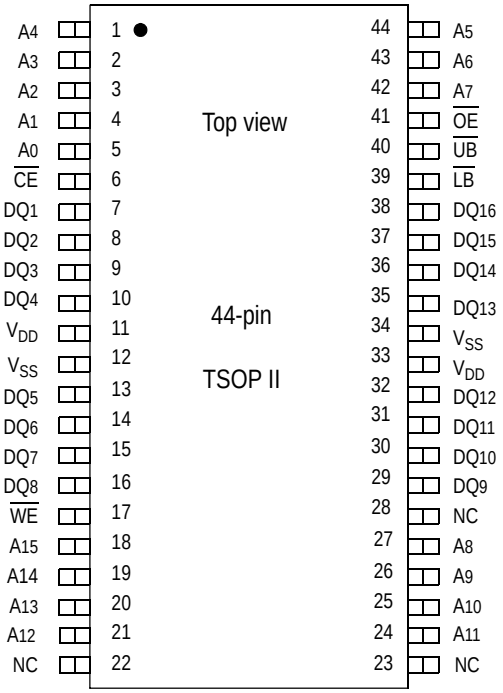
Symbol	Description
A_0–A_{15}	Address input
DQ_1–DQ_{16}	Data input/output
$\overline{CE}$	Chip enable input
$\overline{LB}$	Lower byte enable input (DQ1 to DQ8)
$\overline{UB}$	Upper byte enable input (DQ9 to DQ16)
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{DD}	+3.3 V power supply
V_{SS}	Ground
NC	No connect

Fine Pitch BGA 64K x 16-Bump Configuration

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	DQ16	$\overline{UB}$	A3	A4	$\overline{CE}$	DQ1
C	DQ14	DQ15	A5	A6	DQ2	DQ3
D	V_{SS}	DQ13	NC	A7	DQ4	V_{DD}
E	V_{DD}	DQ12	NC	NC	DQ5	V_{SS}
F	DQ11	DQ10	A8	A9	DQ7	DQ6
G	DQ9	NC	A10	A11	$\overline{WE}$	DQ8
H	NC	A12	A13	A14	A15	NC

6 mm x 8 mm, 0.75 mm Bump Pitch (Package U)
Top View

TSOP-II 64K x 16-Pin Configuration



Package TP

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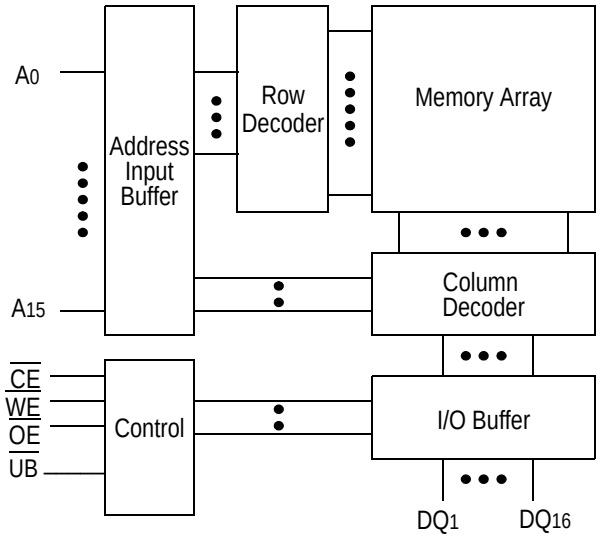
Block Diagram



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ1 to DQ8	DQ9 to DQ16	V_{DD} Current
H	X	X	X	X	Not Selected	Not Selected	I_{SB1}, I_{SB2}
L	L	H	L	L	Read	Read	I_{DD}
			L	H	Read	High Z	
			H	L	High Z	Read	
L	X	L	L	L	Write	Write	
			L	H	Write	Not Write, High Z	
			H	L	Not Write, High Z	Write	
L	H	H	X	X	High Z	High Z	
L	X	X	H	H	High Z	High Z	

Note:
X: “H” or “L”

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	–0.5 to +4.6	V
Input Voltage	V_{IN}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Output Voltage	V_{OUT}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	T_{STG}	–55 to 150	^{0}C

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -7/-8/-10/-12	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} +0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	—	70	^{0}C
Ambient Temperature, Industrial Range	T_{AI}	–40	—	85	^{0}C

Notes:
1. Input overshoot voltage should be less than V_{DD} +2 V and not exceed 20 ns.
2. Input undershoot voltage should be greater than –2 V and not exceed 20 ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	7	pF

Notes:
1. Tested at T_A = 25°C, f = 1 MHz
2. These parameters are sampled and are not 100% tested.

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DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1uA
Output Leakage Current	I_{LO}	Output High Z V_{OUT} = 0 to V_{DD}	–1 uA	1uA
Output High Voltage	V_{OH}	I_{OH} = –4 mA	2.4	
Output Low Voltage	V_{OL}	I_{LO} = +4 mA		0.4V

Power Supply Currents

Parameter	Symbol	Test Conditions	0 to 70°C				–40 to 85°C			
			7 ns	8 ns	10 ns	12 ns	7 ns	8 ns	10 ns	12 ns
Operating Supply Current	I_{DD}	$\overline{CE} \le V_{IL}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time I_{OUT} = 0 mA	145 mA	125 mA	100 mA	85 mA	150 mA	130 mA	105 mA	90 mA
Standby Current	I_{SB1}	$\overline{CE} \ge V_{IH}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time	25 mA	20 mA	20 mA	15 mA	30 mA	25 mA	25 mA	20 mA
Standby Current	I_{SB2}	$\overline{CE} \ge V_{DD} - 0.2$ V All other inputs $\ge V_{DD} - 0.2$ V or ≤ 0.2 V	2 mA				5 mA			

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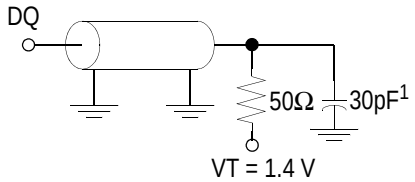
AC Test Conditions

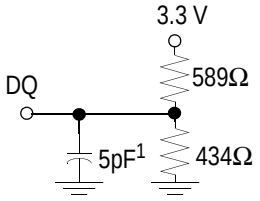
Parameter	Conditions
Input high level	V_{IH} = 2.4 V
Input low level	V_{IL}= 0.4 V
Input rise time	tr = 1V/ns
Input fall time	tf = 1 V/ns
Input reference level	1.4 V
Output reference level	1.4 V
Output load	Fig. 1& 2

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}

Output Load 1



Output Load 2



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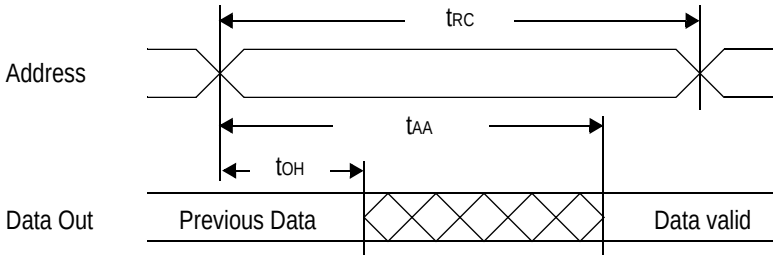
AC Characteristics

Read Cycle

Parameter	Symbol	-7		-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	7	—	8	—	10	—	12	—	ns
Address access time	t_{AA}	—	7	—	8	—	10	—	12	ns
Chip enable access time ($\overline{CE}$)	t_{AC}	—	7	—	8	—	10	—	12	ns
Byte enable access time ($\overline{UB}$, $\overline{LB}$)	t_{AB}	—	3	—	3.5	—	4	—	5	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	—	3	—	3.5	—	4	—	5	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	—	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	0	—	ns
Byte enable to output in low Z ($\overline{UB}$, $\overline{LB}$)	t_{BLZ}*	0	—	0	—	0	—	0	—	ns
Chip disable to output in High Z ($\overline{CE}$)	t_{HZ}*	—	3.5	—	4	—	5	—	6	ns
Output disable to output in High Z ($\overline{OE}$)	t_{OHZ}*	—	3	—	3.5	—	4	—	5	ns
Byte disable to output in High Z ($\overline{UB}$, $\overline{LB}$)	t_{BHZ}*	—	3	—	3.5	—	3.5	—	3.5	—

* These parameters are sampled and are not 100% tested.

Read Cycle 1: $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, $\overline{UB}$ and, or $\overline{LB} = V_{IL}$



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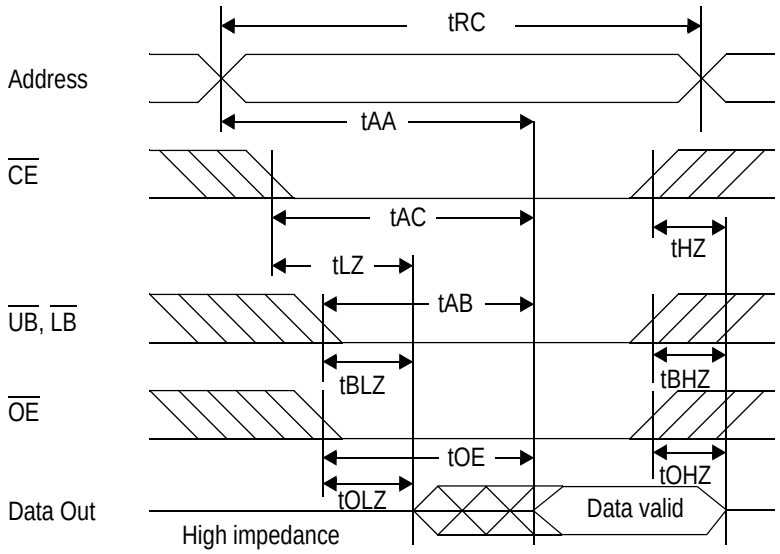
Read Cycle 2: $\overline{WE} = V_{IH}$



Write Cycle

Parameter	Symbol	-7		-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write cycle time	tWC	7	—	8	—	10	—	12	—	ns
Address valid to end of write	tAW	5	—	5.5	—	7	—	8	—	ns
Chip enable to end of write	tCW	5	—	5.5	—	7	—	8	—	ns
Byte enable to end of write	tBW	5	—	5.5	—	7	—	8	—	ns
Data set up time	tDW	3.5	—	4	—	5	—	6	—	ns
Data hold time	tDH	0	—	0	—	0	—	0	—	ns
Write pulse width	tWP	5	—	5.5	—	7	—	8	—	ns
Address set up time	tAS	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	tWR	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	tWR1	0	—	0	—	0	—	0	—	ns
Output Low Z from end of write	tWLZ*	3	—	3	—	3	—	3	—	ns
Write to output in High Z	tWHZ*	—	3	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested.

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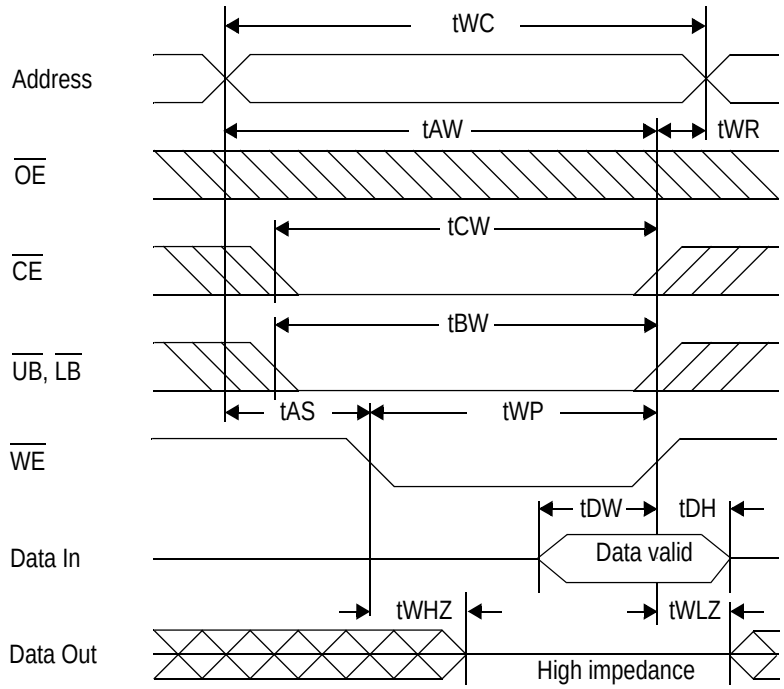
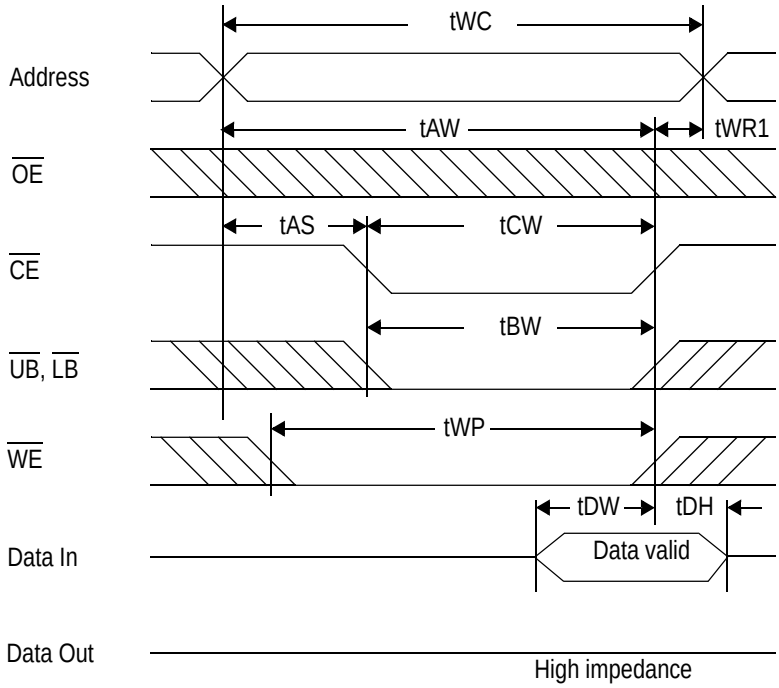
Write Cycle 1: $\overline{WE}$ control



Write Cycle 2: $\overline{CE}$ control



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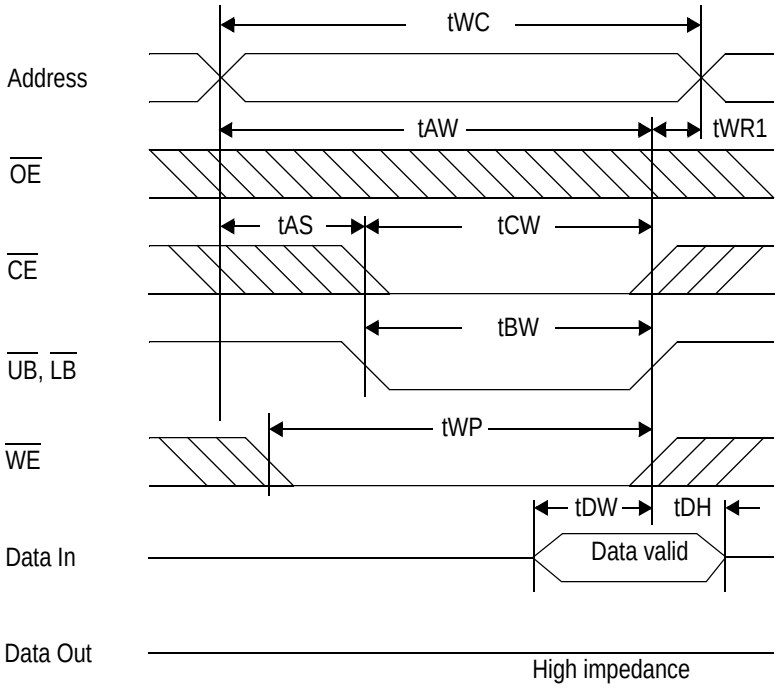
Write Cycle 3: $\overline{UB}$, $\overline{LB}$ control



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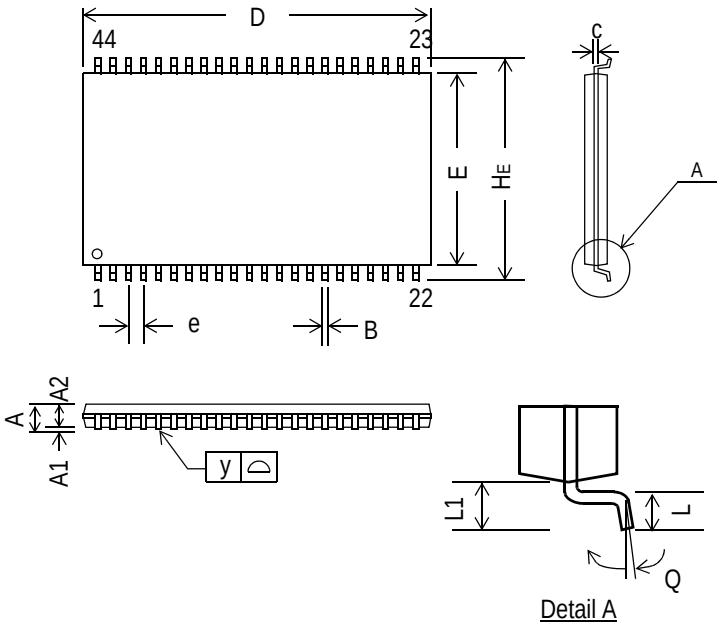
44 Pin, 400 mil TSOP-II



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	—	—	0.047	—	—	1.20
A1	0.002	—	—	0.05	—	—
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.01	0.014	0.018	0.25	0.35	0.45
c	—	0.006	—	—	0.15	—
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
e	—	0.031	—	—	0.80	—
H_E	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	—	0.031	—	—	0.80	—
y	—	—	0.004	—	—	0.10
Q	0°	—	5°	0°	—	5°

Notes:

1. Dimension D& E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Controlling dimension: mm

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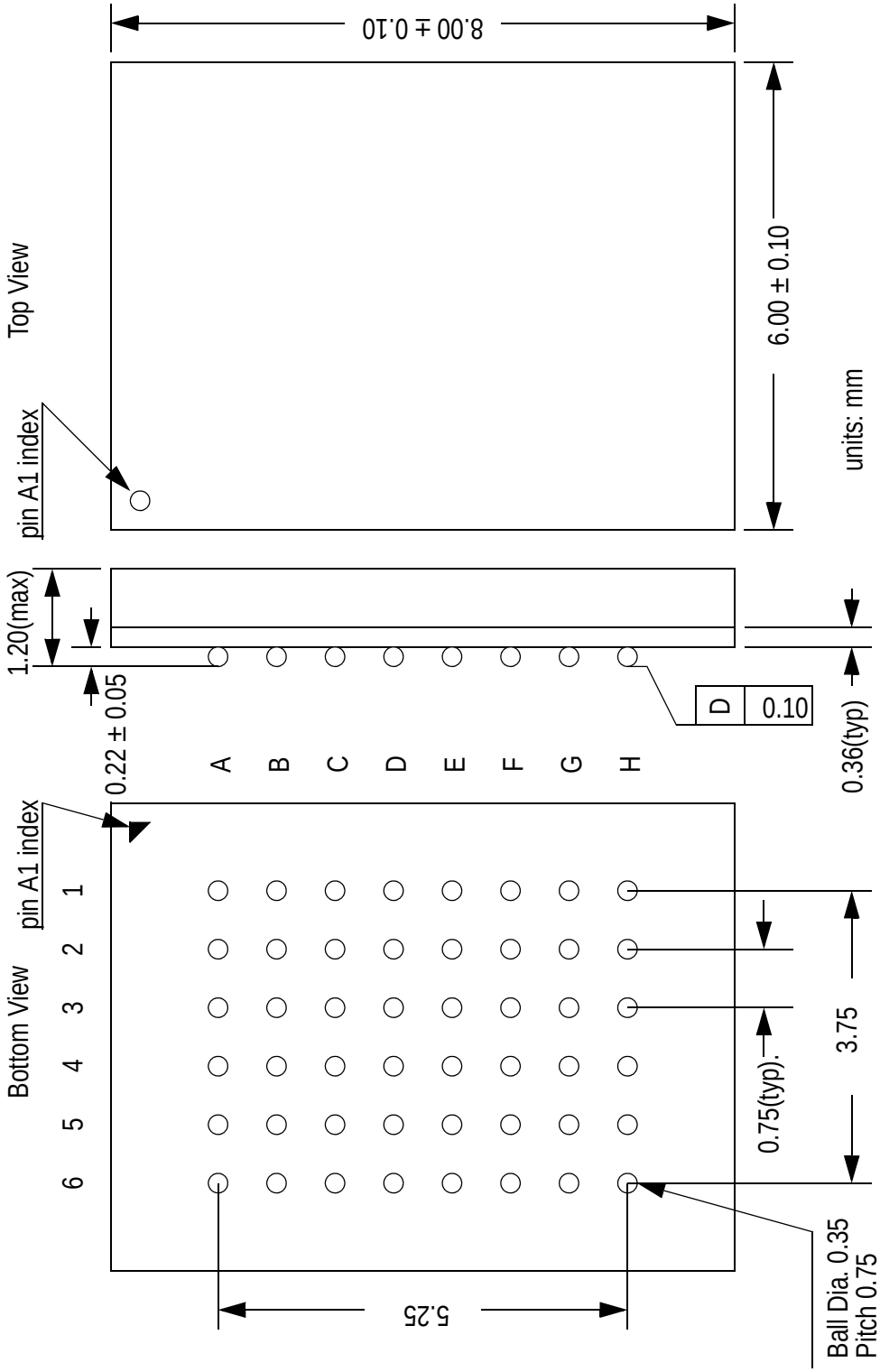
6 mm x 8 mm Fine Pitch BGA



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Ordering Information

Part Number*	Package	Access Time	Temp. Range
GS71116AGP-7	RoHS-compliant 400 mil TSOP-II	7 ns	Commercial
GS71116AGP-8	RoHS-compliant 400 mil TSOP-II	8 ns	Commercial
GS71116AGP-10	RoHS-compliant 400 mil TSOP-II	10 ns	Commercial
GS71116AGP-12	RoHS-compliant 400 mil TSOP-II	12 ns	Commercial
GS71116AGP-7I	RoHS-compliant 400 mil TSOP-II	7 ns	Industrial
GS71116AGP-8I	RoHS-compliant 400 mil TSOP-II	8 ns	Industrial
GS71116AGP-10I	RoHS-compliant 400 mil TSOP-II	10 ns	Industrial
GS71116AGP-12I	RoHS-compliant 400 mil TSOP-II	12 ns	Industrial
GS71116AU-7	6 mm x 8 mm Fine Pitch BGA	7 ns	Commercial
GS71116AU-8	6 mm x 8 mm Fine Pitch BGA	8 ns	Commercial
GS71116AU-10	6 mm x 8 mm Fine Pitch BGA	10 ns	Commercial
GS71116AU-12	6 mm x 8 mm Fine Pitch BGA	12 ns	Commercial
GS71116AU-7I	6 mm x 8 mm Fine Pitch BGA	7 ns	Industrial
GS71116AU-8I	6 mm x 8 mm Fine Pitch BGA	8 ns	Industrial
GS71116AU-10I	6 mm x 8 mm Fine Pitch BGA	10 ns	Industrial
GS71116AU-12I	6 mm x 8 mm Fine Pitch BGA	12 ns	Industrial
GS71116AGU-7	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	7 ns	Commercial
GS71116AGU-8	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	8 ns	Commercial
GS71116AGU-10	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	10 ns	Commercial
GS71116AGU-12	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	12 ns	Commercial
GS71116AGU-7I	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	7 ns	Industrial
GS71116AGU-8I	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	8 ns	Industrial
GS71116AGU-10I	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	10 ns	Industrial
GS71116AGU-12I	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	12 ns	Industrial

Note:
Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. For example: GS71116AGP-8T.

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1Mb Asynchronous Datasheet Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Revision
71116A_r1		• Creation of new datasheet
71116A_r1; 71116_r1_01	Content	• Added 6 ns speed bin to entire document
71116A_r1_01; 71116A _r1_02	Content	• Updated all power numbers • Changed 6 mm x 10 mm FPBGA package designator from U to X
71116A_r1_02; 71116A _r1_03	Content	• Updated Recommended Operating Conditions table on page 4 • Changed FPBGA package from 6 x 10 to 6 x 8 (package U) • Updated Read Cycle AC Characteristics table
71116A_r1_03; 71116A _r1_04	Content	• Removed 6 ns speed bin from entire document • Added 7 ns speed bin to entire document
71116A_r1_04; 71116A _r1_05	Content	• Updated timings for tBHZ (Read Cycle) for 10 ns and 12 ns
71116A_r1_05; 71116A_r1_06	Content/Format	• Updated format • Added RoHS-compliant information for TSOP-II package
71116A_r1_06; 71116A_r1_07	Content/Format	• Added RoHS-compliant information for FP-BGA package
71116A_r1_07; 71116A_r1_08	Content	• Added RoHS-compliant 400 mil SOJ
71116A_r1_08; 71116A_r1_09	Content	• Updated to MP in ordering information table • Rev.1.09a Removed Status column from Ordering Information table. • Removed reference to 400 mil, 44–pin SOJ package from entire document
71116A_r1_09; 71116A_r1_10	Content	• Removed 5/6-RoHS TSOP-II references due to EOL

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Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А